# FEATURES OVERVIEW

- Triple ADC with 12 - 140 MHz Sampling Rate
- Integrated line locked PLL generates pixel clock from HSYNC
- Integrated 5-bit pixel clock phase adjustment for precise sample timing control
- Integrated clamp with timing generator
- Integrated Brightness & Contrast controls
- Integrated precision voltage reference
- Compatible with VGA through SXGA RGB graphics signals
- Pin Compatible with AD9883A
- Serial port programming interface
- Mid-Scale Clamping
- Fully Sync Processing
- 4:2:2 Output Format Mode

# BLOCK DIAGRAM
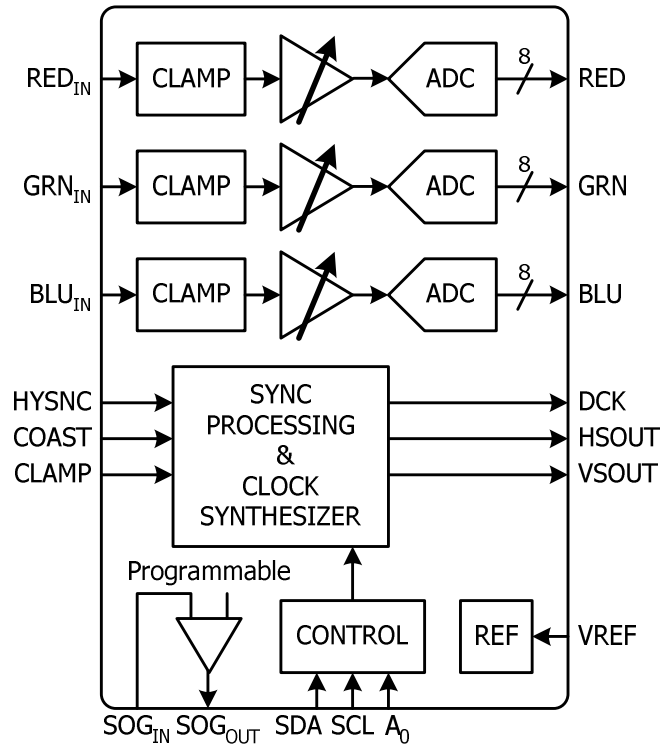


# DESCRIPTION

Most flat-panel monitors and projectors require a digital graphics input in order to accurately scale and display graphics.  The huge installed base of computers with analog video graphics interfaces necessitates the use of a graphics digitizer to re-digitize the analog RGB signal before further processing.

- The MST9883 is a fully integrated analog interface for digitizing high-resolution RGB graphics signals from PC's and workstations.  With a sampling rate capability of up to 140 MHz, it can accurately support display resolutions up to 1280x1024 (SXGA) at 75 Hz.  The clamped input circuits provide sufficient bandwidth to accurately digitize each pixel.

- The MST9883 provides a high performance highly integrated solution to support the digitization process, including the ADC's, a voltage reference, a PLL to generate the pixel sampling clock from HSYNC, clamping circuits, and programmable offset and gain circuits to provide brightness and contrast controls.

- When the COAST signal is asserted, the PLL will maintain its output frequency when HSYNC pulses are absent, such as during the VSYNC period in some systems.

- A 32-step programmable phase adjustment control (0-360 deg) is provided for the pixel sampling clock to adjust for the difference between the HSYNC edge and RGB pixel edge timing.

- The MST9883 can send output data through one 24-bit port at the pixel clock rate.

## REGISTER SET

### Register Map

| Function Name | ADDR | Bit Definition | | | | | | | | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | | LSB | |
| REVID | 00H | -- | -- | -- | -- | -- | -- | -- | 0 | 00xh |
| PLLDIVM | 01H | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | 69xh |
| PLLDIVL | 02H | N3 | N2 | N1 | N0 | -- | -- | -- | -- | D0xh |
| PLLGAIN | 03H | VCO1 | VCO0 | CP2 | CP1 | CP0 | -- | -- | -- | 48xh |
| PHASE | 04H | PA4 | PA3 | PA2 | PA1 | PA0 | -- | -- | -- | 40xh |
| CLPDLY | 05H | CP7 | CP6 | CP5 | CP4 | CP3 | CP2 | CP1 | CP0 | 05xh |
| CLPDUR | 06H | CD7 | CD6 | CD5 | CD4 | CD3 | CD2 | CD1 | CD0 | 05xh |
| HOP | 07H | HOP7 | HOP6 | HOP5 | HOP4 | HOP3 | HOP2 | HOP1 | HOP0 | 20xh |
| REDGAIN | 08H | RG7 | RG6 | RG5 | RG4 | RG3 | RG2 | RG1 | RG0 | 80xh |
| GRNGAIN | 09H | GG7 | GG6 | GG5 | GG4 | GG3 | GG2 | GG1 | GG0 | 80xh |
| BLUGAIN | 0AH | BG7 | BG6 | BG5 | BG4 | BG3 | BG2 | BG1 | BG0 | 80xh |
| REDOFFST | 0BH | RO7 | RO6 | RO5 | RO4 | RO3 | RO2 | RO1 | RO0 | 80xh |
| GRNOFFST | 0CH | GO7 | GO6 | GO5 | GO4 | GO3 | GO2 | GO1 | GO0 | 80xh |
| BLUOFFST | 0DH | BO7 | BO6 | BO5 | BO4 | BO3 | BO2 | BO1 | BO0 | 80xh |
| SYNCTRL | 0EH | HPO | HSPOL | HSOUTPOL | AHO | AHS | VOI | AVO | AVS | 40xh |
| GENCTRL | 0FH | EXTCLMP | CLAMPOL | COSEL | CPOLOV | CSTPOL | SEEK | PWRN | -- | 4Exh |
| SOGMIDC | 10H | SOG4 | SOG3 | SOG2 | SOG1 | SOG0 | R_SEL | G_SEL | B_SEL | B8xh |
| SYNSEPT | 11H | SST7 | SST6 | SST5 | SST4 | SST3 | SST2 | SST1 | SST0 | 20xh |
| PRECO | 12H | PRC7 | PRC6 | PRC5 | PRC4 | PRC3 | PRC2 | PRC1 | PRC0 | 00xh |
| POSTCO | 13H | POC7 | POC6 | POC5 | POC4 | POC3 | POC2 | POC1 | POC0 | 00xh |
| SYNCD(RO) | 14H | HSD | AHS | IHSPD | VSD | AVS | OVPD | SOGD | ICPD | -- |
| DOUTF | 15H | -- | -- | -- | -- | UVI | -- | V422 | -- | 02xh |
| RESERVED | 16H | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| STATUS(RO) | 17H | LOCK | STAT6 | STAT5 | STAT4 | STAT3 | STAT2 | STAT1 | STAT0 | -- |
| RESERVED | 18H | -- | -- | -- | -- | -- | -- | -- | -- | -- |

## Register Definitions

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| REVID | 00H (RO) |

MST9883 Revision ID code.  Read only.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| PLLDIVM | 01H (R/W) |
| PLLDIVL | 02H (R/W) |

N[11:0] - PLL divider ratio  sets the number of pixels per line.  When PLL is locked, it will generate N[11:0]+1 output clocks per input HSYNC cycle.

The MST9883 derives its internal master clock with a PLL using HSYNC as the input timing reference.  This master clock is commonly referred to in this specification as the pixel rate clock, as it goes through one cycle for every pixel (plus blanking overhead) on a horizontal line.  Normally N will be 20-30% higher than the number of active pixels in the display due to blanking and horizontal retrace overhead.

The VESA association has established some standard timing specifications which will help to determine the approximate value of N[11:0] for each horizontal and vertical resolution and frame rate.  However, since many systems do not follow the standards exactly, the display system designer needs to provide automatic or manual means to find and set the correct value of N[11:0].  If N[11:0] is set incorrectly vertical noise bars will usually appear on the display.  These bars normally increase in number as the magnitude error in the value of N[11:0] increases.

| REGISTER NAME | | | SUB-ADDRESS | |
|---|---|---|---|---|
| PLLGAIN | | | 03H (R/W) | |
| Register Bit | Alias- | Value- | Function | |
| 7:6 | VCO[1:0]/ RNG[1:0] | | VCO Range (equivalent) | |
| | | 0 | 12-36 MHz | |
| | | 1 | 36-72 MHz (default power-up value) | |
| | | 2 | 72-110 MHz | |
| | | 3 | 110-140 MHz | |
| 5:3 | CP[2:0] | | Charge Pump current (equivalent) | |
| | | 0 | 50 µA | |
| | | 1 | 100 µA | |
| | | 2 | 150 µA | |
| | | 3 | 250 µA | |
| | | 4 | 350 µA | |
| | | 5 | 500 µA | |
| | | 6 | 750 µA | |
| | | 7 | 1500 µA | |
| 2:0 | - | - | Reserved | |

| REGISTER NAME | | | SUB-ADDRESS |
|---|---|---|---|
| PHASE | | | 04H (R/W) |
| Register Bit | Alias- | Value- | Function |
| 7:3 | PA[4:0] | 0-31 | ADC sampling clock phase adjust.  Can adjust the sampling clock phase in 11.25 degree increments over one pixel clock period.  ADC Sampling clock edge will trail PLL clock edge by PA[4:0]*11.25 degrees. |
| 2:0 | - | - | Reserved. |

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| CLPDLY | 05H (R/W) |

CP[7:0] − Internally generated clamp start time. When EXTCLMP is set to 0, the MST9883 uses an internally generated clamp timer to set the start time and duration of the clamp signal. The timer reference is 1 pixel clock for each count. The starting point for the timer is the trailing edge of the HSYNC input. Clamping will start CP[7:0] pixel clock cycles after the trailing edge of HSYNC and continue for CD[7:0] pixel clock cycles.

Insufficient clamping time may lead to uneven brightness, and slow recovery from large changes in the brightness. Typical settings of 08h / 10h are suggested for CP[7:0] / CD[7:0] as a starting point that will work for most common video formats.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| CLPDUR | 06H (R/W) |

CD[7:0] − Internally generated clamp duration. The timer reference is 1 pixel clock for each count.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| HOP | 07H (R/W) |

HOP[7:0] − HSYNC Output Pulse-Width. Set the duration of the HSYNC output pulse.

The leading edge of the HSYNC output is triggered by the internally generated, phase-adjusted PLL feedback clock. The MST9883 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the HSYNC output, which is also phase adjusted.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| REDGAIN | 08H (R/W) |

RG[7:0] − Red input gain setting. The MST9883 can support input signals ranging from 1 Vpp to 0.5 Vpp. A register value of 00h will set the input voltage full scale range to 0.5 Vpp. Higher register values support larger input voltages. The highest setting, FFh will support an input voltage of 1 Vpp.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| GRNGAIN | 09H (R/W) |

GG[7:0] − Green input gain setting. See REDGAIN register description.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| BLUGAIN | 0AH (R/W) |

BG[7:0] − Blue input gain setting. See REDGAIN register description.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| REDOFFST | 0BH (R/W) |

RO[7:0] − Red channel offset. See GRNOFFST register.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| GRNOFFST | 0CH (R/W) |

GO[7:0] − Green channel offset. Control the green brightness level. Higher values decrease the brightness, lower values increase the brightness. The green channel will clamp the black level to an output code of 0 when GO[7:0]=80h. For example, GO[7:0] = 00h will result in a green-channel digital output code of 77 during the black level. GO[7:0] = FFh will result in a green-channel digital output code of -78 (below the bottom of the range) during the black level. Since the digital outputs cannot support negative integers, the digital output code during black level would be clipped at 0 in this case.

1 LSB offset = 0.615 LSB ADC (Note: this ratio is independent of the gain setting)

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| BLUOFFST | 0DH (R/W) |

BO[7:0] − Blue channel offset. See GRNOFFST register.

| REGISTER NAME | | | SUB-ADDRESS |
|---|---|---|---|
| SYNCTRL | | | 0EH (R/W) |
| Register Bit | Alias | Value | Function |
| 7 | HPO | 0 | HSYNC polarity determined by chip (default) |
| | | 1 | HSYNC polarity determined by user |
| 6 | HSPOL | 0 | HSYNC treated as active low.  PLL will synchronize to falling (leading) edge of HSYNC input, and clamp will synchronize to rising (trailing) edge of HSYNC. |
| | | 1 | HSYNC treated as active high.  PLL will synchronize to rising (leading) edge of HSYNC input, and clamp will synchronize to falling (trailing) edge of HSYNC.  (default) |
| 5 | HSOUTPOL | 0 | Positive output signal polarity for HSOUT & SOGOUT (default) |
| | | 1 | Negative output signal polarity for HSOUT & SOGOUT |
| 4 | AHO | 0 | Auto determines the Active Interface (default) |
| | | 1 | Override, AHS (Bit 3) determines the Active Interface |
| 3 | AHS | 0 | HSYNC Input (default) |
| | | 1 | Sync-On-Green Input |
| 2 | VOI | 0 | Inverts the output polarity of VSYNC |
| | | 1 | Not inverts the output polarity of VSYNC (default) |
| 1 | AVO | 0 | Auto determines the Active VSYNC (default) |
| | | 1 | Override, AVS (Bit 0) determines the Active VSYNC |
| 0 | AVS | 0 | VSYNC Input (default) |
| | | 1 | Sync Separator Output |

| REGISTER NAME | | | SUB-ADDRESS |
|---|---|---|---|
| GENCTRL | | | 0FH (R/W) |
| Register Bit | Alias | Value | Function |
| 7 | EXTCLMP | 0 | Use internal clamp timer to generate clamp signal. Registers CLPLCAE and CLPDUR will set the delay and duration of the clamp signal from the leading edge of HSYNC. (default) |
| | | 1 | Use CLAMP pin to indicate to clamp. |
| 6 | CLAMPOL | 0 | CLAMP pin polarity treated as active high.  When EXTCLMP is high and CLAMP pin is high then clamp will occur. |
| | | 1 | CLAMP pin treated as active low.  When EXTCLMP is high and CLAMP is low, then clamp will occur.  (default) |
| 5 | COSEL | 0 | COAST Input Pin. |
| | | 1 | VSYNC is selected, and the additional decision of using the VSYNC as input pin or as Sync Separator output need to be made.  (Ref.  Bit 1 & 0 of SYNCTRP) |
| 4 | CPOLOV | 0 | COAST polarity determined by chip.  (default) |
| | | 1 | COAST polarity determined by user. |
| 3 | CSTPOL | 0 | COAST input is treated as active low.  When COAST pin is low, PLL will maintain a fixed frequency, and will not attempt to track the input HSYNC during this time. |
| | | 1 | COAST input treated as active high.  When COAST pin is high, PLL will maintain a fixed frequency.  (default) |
| 2 | SEEK | 0 | Disallow Seek Mode (low-power mode).  (default) |
| | | 1 | Allow Seek Mode (low-power mode).  The low-power mode occurs when there are no signals on any of the Sync inputs. |
| 1 | PWRN | 0 | When inactive, the chip is in full power-down. |
| | | 1 | When active, the chip is in normal power operation.  (default) |
| 0 | -- | - | Reserved. |

| REGISTER NAME | | | SUB-ADDRESS |
|---|---|---|---|
| SOGMIDC | | | 10H (R/W) |
| Register Bit | Alias- | Value- | Function |
| 7:3 | SOG[4:0] | 0-31 | This register adjusts the comparator threshold of the Sync-on-Green slicer.  The adjustment increments in steps of 10mV, with the minimum setting of 10mV (11111) and the maximum setting of 330mV (00000). |
| 2 | R_SEL | 0 | When in-active, the RED channel is clamped to ground.  (default) |
| | | 1 | When active, the RED channel is clamped to mid-scale.  (Pin 37) |
| 1 | G_SEL | 0 | When in-active, the Green channel is clamped to ground.  (default) |
| | | 1 | When active, the Green channel is clamped to mid-scale.  (Pin 37) |
| 0 | B_SEL | 0 | When in-active, the Blue channel is clamped to ground.  (default) |
| | | 1 | When active, the Blue channel is clamped to mid-scale.  (Pin 37) |

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| SYNSEPT | 11H (R/W) |

SYNSEPT sets the sync separator threshold count value. The sync separator counting increment is fixed internally at 200 ns intervals (5MHz). This register is to be programmed to a value greater than the maximum hsync pulse width. When the composite hsync pulse width becomes larger than the SYNSEPT value, the sync separator will interpret it as a VSYNC pulse.

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| PRECO | 12H (R/W) |
| POSTCO | 13H (R/W) |

PRECOAST[7:0] − Pre-COAST. Sets the number of HSYNC periods that the COAST becomes active before VSYNC.

POSTCOAST[7:0] − Post-COAST. Sets the number of HSYNC periods that the COAST will remain active after VSYNC.

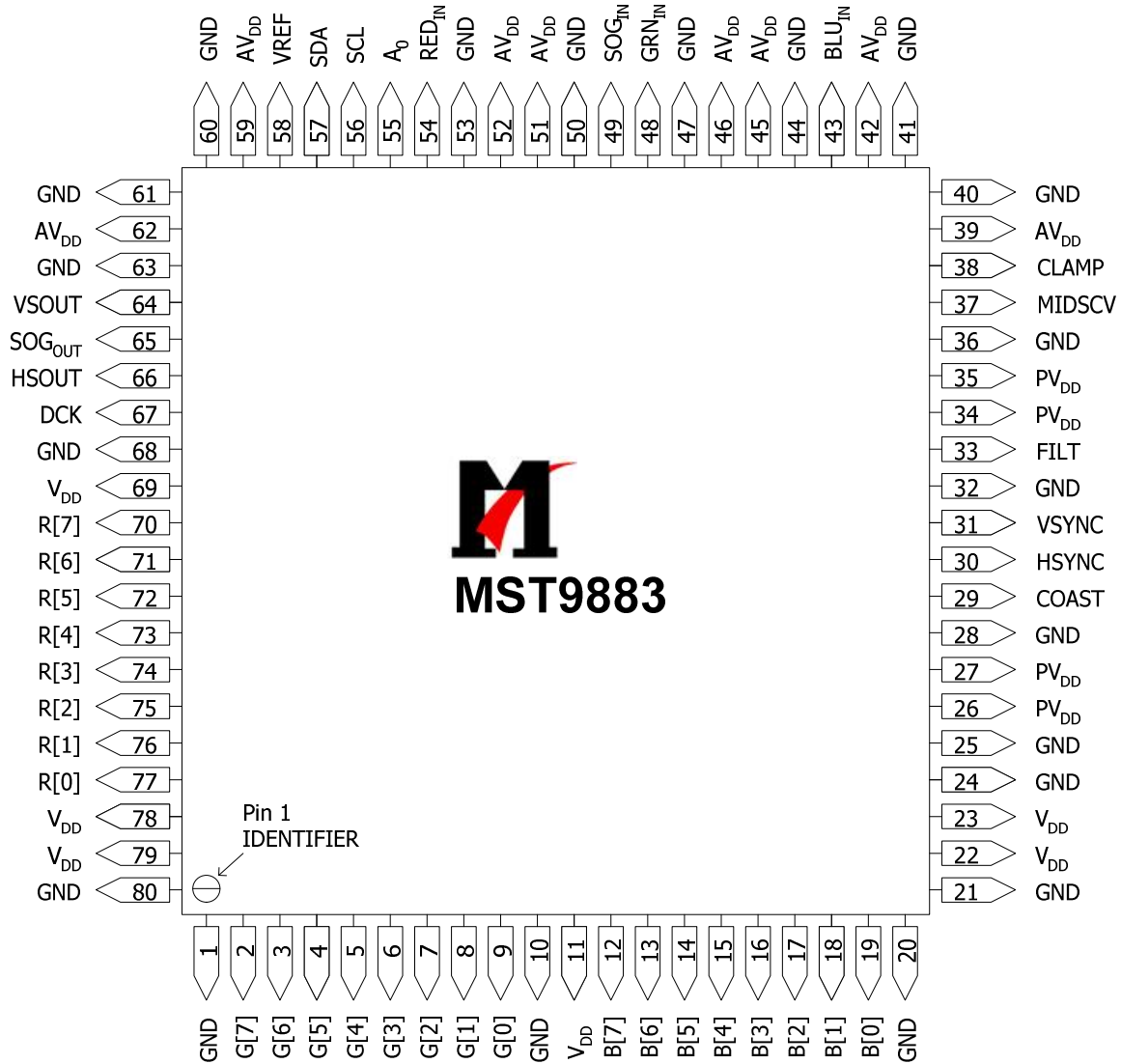| REGISTER NAME | | | SUB-ADDRESS | |
|---|---|---|---|---|
| SYNCD | | | 14H (RO) | |
| Register Bit | Alias | Value | Function | |
| 7 | HSD | 0 | It is set to low (Logic 0) if no activity detected on HSYNC. (default) | |
| | | 1 | It is set to high (Logic 1) if HSYNC is present on the analog interface. | |
| 6 | AHS | 0 | When in-active (Logic 0), use the HSYNC pin input for HSYNC. | |
| | | 1 | When active, use the SOG pin input for HSYNC. | |
| 5 | IHSPD | 0 | It is set to low (Logic 0) if HSYNC input polarity is detected as negative. | |
| | | 1 | It is set to high (Logic 1) if HSYNC input polarity is detected as positive. | |
| 4 | VSD | 0 | It is set to low (Logic 0) if no activity detected on VSYNC. | |
| | | 1 | It is set to high (Logic 1) if VSYNC is present on the analog interface. | |
| 3 | AVS | 0 | When in-active (Logic 0), use the VSYNC pin input for VSYNC. | |
| | | 1 | When active (Logic 1), use the Sync separator for VSYNC. | |
| 2 | OVPD | 0 | VSYNC polarity is active low. | |
| | | 1 | VSYNC polarity is active high. | |
| 1 | SOGD | 0 | It is set to low (Logic 0) if no activity detected on the Sync-on-Green input pin. | |
| | | 1 | It is set to high (Logic 1) if sync activity is detected on the Sync-on-Green input pin. | |
| 0 | ICPD | 0 | COAST polarity is negative. | |
| | | 1 | COAST polarity is positive. | |

| REGISTER NAME | SUB-ADDRESS |
|---|---|
| DOUTF | 15H (R/W) |

UVI − When set to high, the R/B sequence of "4-2-2" will be reversed.

V422 − "4-2-2" Output Formatting Mode (Bit 1). When set to low, the output will be in 4-2-2 format; otherwise, the output will be in 4-4-4 format.

| Channel | Input Connection | Output Format |
|---|---|---|
| Red | V | U/V |
| Green | Y | Y |
| Blue | U | High Impedance |

## PIN CONFIGURATION



Top pins (left to right, 60–41): GND, $AV_{DD}$, VREF, SDA, SCL, $A_0$, $RED_{IN}$, GND, $AV_{DD}$, $AV_{DD}$, GND, $SOG_{IN}$, $GRN_{IN}$, GND, $AV_{DD}$, $AV_{DD}$, GND, $BLU_{IN}$, $AV_{DD}$, GND

Left pins (61–80):
| Pin | Signal |
|---|---|
| 61 | GND |
| 62 | $AV_{DD}$ |
| 63 | GND |
| 64 | VSOUT |
| 65 | $SOG_{OUT}$ |
| 66 | HSOUT |
| 67 | DCK |
| 68 | GND |
| 69 | $V_{DD}$ |
| 70 | R[7] |
| 71 | R[6] |
| 72 | R[5] |
| 73 | R[4] |
| 74 | R[3] |
| 75 | R[2] |
| 76 | R[1] |
| 77 | R[0] |
| 78 | $V_{DD}$ |
| 79 | $V_{DD}$ |
| 80 | GND |

Pin 1 IDENTIFIER

Right pins (40–21):
| Pin | Signal |
|---|---|
| 40 | GND |
| 39 | $AV_{DD}$ |
| 38 | CLAMP |
| 37 | MIDSCV |
| 36 | GND |
| 35 | $PV_{DD}$ |
| 34 | $PV_{DD}$ |
| 33 | FILT |
| 32 | GND |
| 31 | VSYNC |
| 30 | HSYNC |
| 29 | COAST |
| 28 | GND |
| 27 | $PV_{DD}$ |
| 26 | $PV_{DD}$ |
| 25 | GND |
| 24 | GND |
| 23 | $V_{DD}$ |
| 22 | $V_{DD}$ |
| 21 | GND |

Bottom pins (left to right, 1–20): GND, G[7], G[6], G[5], G[4], G[3], G[2], G[1], G[0], GND, $V_{DD}$, B[7], B[6], B[5], B[4], B[3], B[2], B[1], B[0], GND

## PIN DESCRIPTIONS

| Pin Name | Pin Type | Function | Pin Number(s) |
|---|---|---|---|
| $RED_{IN}$ | Analog Input | Red analog input | 54 |
| $GRN_{IN}$ | Analog Input | Green analog input | 48 |
| $BLU_{IN}$ | Analog Input | Blue analog input | 43 |
| $SOG_{IN}$ | Analog Input | Sync on Green analog input | 49 |
| | | | |
| CLAMP | Digital CMOS Input | External Clamp Input | 38 |
| HSYNC | Digital CMOS Input | Horizontal SYNC Input | 30 |
| VSYNC | Digital CMOS Input | Vertical SYNC Input | 31 |
| COAST | Digital CMOS Input | Hold PLL Frequency, do not track HSYNC | 29 |
| | | | |
| SCL | Digital CMOS Input | Serial Interface clock | 56 |
| SDA | Digital CMOS Input/Output | Serial Interface data pin | 57 |
| $A_0$ | Digital CMOS Input | Serial interface address pin | 55 |
| | | | |
| R [7:0] | Digital CMOS 3-state Output | Red output data | 70-77 |
| G [7:0] | Digital CMOS 3-state Output | Green output data | 2-9 |
| B [7:0] | Digital CMOS 3-state Output | Blue output data | 12-19 |
| DCK | Digital CMOS 3-state Output | Output data clock | 67 |
| HSOUT | Digital CMOS 3-state Output | HSYNC output | 66 |
| VSOUT | Digital CMOS 3-state Output | VSYNC output | 64 |
| $SOG_{OUT}$ | Digital CMOS 3-state Output | SYNC on Green Slicer Output | 65 |
| | | | |
| FILT | | No Connection | 33 |
| | | | |
| VREF | Reference | Internal Reference Bypass | 58 |
| MIDSCV | Reference | Internal Mid-Scale Voltage Bypass | 37 |
| | | | |
| $AV_{DD}$ | 3.3v Power | Analog Power | 39,42,45,46,51,52,59,62 |
| $PV_{DD}$ | 3.3v Power | PLL Power | 26,27,34,35 |
| $V_{DD}$ | 3.3v Power | Digital Output Power | 11,22, 23, 69,78,79 |
| GND | System Ground | System Ground | 1,10,20,21,24,25,28,32,36, 40,41,44,47,50,53,60,61,63, 68,80 |

## ELECTRICAL SPECIFICATIONS ($AV_{DD} = PV_{DD} = V_{DD} = 3.3V$)

| Parameter | Temp | Test Level | MST9883-110 Min | Typ | Max | MST9883-140 Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 8 | | | 8 | | Bits |
| DC ACCURACY | | | | | | | | | |
| Differential Nonlinearity | 25°C | 1 | | ±0.5 | 1.25/-1.0 | | ±0.5 | 1.35/-1.0 | LSB |
| | Full | 4 | | | 1.35/-1.0 | | | 1.45/-1.0 | LSB |
| Integral Nonlinearity | 25°C | 1 | | ±0.5 | ±1.85 | | ±0.5 | ±2.00 | LSB |
| | Full | 4 | | | ±2.00 | | | ±2.30 | |
| No Missing Codes | Full | 4 | | Guaranteed | | | Guaranteed | | |
| ANALOG INPUT | | | | | | | | | |
| Input Voltage Range | | | | | | | | | |
| Minimum | Full | 4 | | | 0.5 | | | 0.5 | V p-p |
| Maximum | Full | 4 | 1.0 | | | 1.0 | | | V p-p |
| Input Bias Current | Full | 2 | | | 1 | | | 1 | µA |
| Input Offset Voltage | Full | 4 | | 2 | 5 | | 2 | 5 | LSB |
| Input Full-Scale Matching | Full | 4 | | 1.0 | 3.0 | | 1.0 | 3.0 | %FS |
| Offset Adjustment Range | Full | 4 | 54 | 62 | 70 | 54 | 62 | 70 | %FS |
| SWITCHING PERFORMANCE | | | | | | | | | |
| Maximum Conversion Rate | Full | 4 | 110 | | | 140 | | | MSPS |
| Minimum Conversion Rate | Full | 2 | | | 10 | | | 10 | MSPS |
| Data to Clock Skew, $t_{sk1}$ | Full | 2 | 0.3 | | 0.5 | 0.3 | | 0.5 | ns |
| Data to Clock Skew, $t_{sk2}$ | Full | 2 | 0.8 | | 1.8 | 0.8 | | 1.8 | ns |
| HSYNC Input Frequency | Full | 2 | 15 | | 110 | 15 | | 110 | kHz |
| Maximum PLL Clock Rate | Full | 4 | 110 | | | 140 | | | MHz |
| Minimum PLL Clock Rate | Full | 2 | | | 10 | | | 10 | MHz |
| PLL Jitter | Full | 2 | | | 300[1] | | | 300[1] | ps p-p |
| Sampling Phase Tempco | Full | 2 | | 15 | | | 15 | | ps/°C |
| DIGITAL INPUTS | | | | | | | | | |
| Input Voltage, High ($V_{IH}$) | Full | 4 | 2.5 | | | 2.5 | | | V |
| Input Voltage, Low ($V_{IL}$) | Full | 4 | | | 0.8 | | | 0.8 | V |
| Input Current, High ($I_{IH}$) | Full | 2 | | | -1.0 | | | -1.0 | µA |
| Input Current, Low ($I_{IL}$) | Full | 2 | | | 1.0 | | | 1.0 | µA |
| Input Capacitance | 25°C | 3 | | 5 | | | 5 | | pF |
| DIGITAL OUTPUTS | | | | | | | | | |
| Output Voltage, High ($V_{OH}$) | Full | 4 | $V_{DD}$ - 0.1 | | | $V_{DD}$ - 0.1 | | | V |
| Output Voltage, Low ($V_{OL}$) | Full | 4 | | | 0.1 | | | 0.1 | V |
| Duty Cycle | | | | | | | | | |
| DCK | Full | 2 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| Output Coding | | | | Binary | | | Binary | | |
| POWER SUPPLY | | | | | | | | | |
| $AV_{DD}$ Supply Voltage | Full | 2 | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| $PV_{DD}$ Supply Voltage | Full | 2 | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| $V_{DD}$ Supply Voltage | Full | 2 | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| Total Power Dissipation | Full | 4 | | 590[2] | 720[2] | | 730 | 880 | mW |
| Power-Down Supply Current | Full | 4 | | 3 | 10 | | 3 | 10 | mA |
| Power-Down Dissipation | Full | 4 | | 10 | 33 | | 10 | 33 | mW |
| DYNAMIC PERFORMANCE | | | | | | | | | |
| Analog Bandwidth, Full Power | 25°C | 3 | | 300 | | | 300 | | MHz |
| Signal-to-Noise Ratio (SNR) (Without Harmonics) | 25°C | 3 | | 46 | | | 43 | | dB |
| THERMAL CHARACTERISTICS | | | | | | | | | |
| $\theta_{JC}$-Junction-to-Case Thermal Resistance | | 3 | | 17 | | | 17 | | °C/W |
| $\theta_{JC}$-Junction-to-Ambient Thermal Resistance | | 3 | | 39.7 | | | 39.7 | | °C/W |

**Notes**

**1 With Timing Interval Analyzer (TIA) measurement**

**2 With firmware control**

**Specifications are subjected to change without notice.**

## Explanation of Test Levels

Test Level

1. 100% production tested

2. Parameter is guaranteed by design and characterization testing

3. Parameter is a typical value only

4. 100% production tested at 25°C; guaranteed by design and characterization testing

## 2-WIRE SERIAL BUS SPECIFICATION

| Parameter | Symbol | STANDARD-MODE | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | 4.0 | - | μs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | - | μs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4.0 | - | μs |
| Set-up time for a repeated START condition | $t_{SU;STA}$ | 4.7 | - | μs |
| Data hold time: | $t_{HD;DAT}$ | 0 | 3.45 | μs |
| Data set-up time | $t_{SU;DAT}$ | 250 | - | ns |
| Rise time of both SDA and SCL signals | $t_r$ | - | 1000 | ns |
| Fall time of both SDA and SCL signals | $t_f$ | - | 300 | ns |
| Set-up time for STOP condition | $t_{SU;STO}$ | 4.0 | - | μs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 4.7 | - | μs |

## ABSOLUTE MAXIMUM RATINGS♣

| Parameter | Rating | Units |
|---|---|---|
| AVDD, PVDD | -0.5 ~ +3.6 | V |
| VDD | -0.5 ~ +3.6 | V |
| Analog Inputs | -0.5 ~ $AV_{DD}$ | V |
| VREF | 0.0 ~ $AV_{DD}$ | V |
| Digital Inputs | 0.0 ~ 5.0 | V |
| Digital Output Current | 20 | mA |
| Operating Temperature | -20 ~ +80 | ºC |
| Storage Temperature | -65 ~ +150 | ºC |
| Maximum Junction Temperature | +150 | ºC |
| Maximum Case Temperature | +150 | ºC |

♣ **Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of the limits indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| MST9883-110 | 0°C to +70°C | LQFP | 80 |
| MST9883-140 | 0°C to +70°C | LQFP | 80 |

## MARKING INFORMATION

MST9883
□□□□□□□□□□□□
Operation Code B
Date Code (YYWW)
Lot Number
Operation Code A

## DISCLAIMER

MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST9883 comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

# APPLICATION GUIDE

## Serial Port

Registers are accessed through a 2-wire serial port interface. The MST9883 is a slave device and the 7-bit slave address is selected by the A0 pin according to the following able:

| A0 | MST9883 Slave Address |
|----|------------------------|
| 0  | 1001100h               |
| 1  | 1001101h               |

The pins SDA and SCL interface to the host, 2-wire serial port master controller. The SDA and SCL pins are designed to interface with 3.3v inputs. If the SDA and SCL inputs are driven from 5v logic, then they should be protected by series connected resistors to avoid large currents flowing through the MST9883 protection diodes.

During data transfer, the SDA input is allowed to transition only when SCL is low. SDA transitions while SCL is high will be interpreted as 2-wire serial port START / STOP control signals. When the serial interface is inactive, both SCL and SDA should be high.

All data transfers are 1-byte MSB-first.

For basic data transfer, each 2-wire serial port access cycle uses a 5-step process:

- START signal
- Slave Address byte
- Register Address byte
- Data byte
- STOP signal

A data transfer is initiated by sending a START control signal (figure 1) comprising of a HIGH-LOW transition on SDA while SCL is held HIGH.

The first 8-bits of data after the START signal comprise a 7-bit slave address signal followed by a 1-bit READ (HIGH) or WRITE (LOW) signal. If the transmitted address matches the MST9883 slave address, the MST9883 will acknowledge by pulling SDA low on the 9th SCL cycle (figure 2). If the addresses do not match, the MST9883 will not acknowledge.
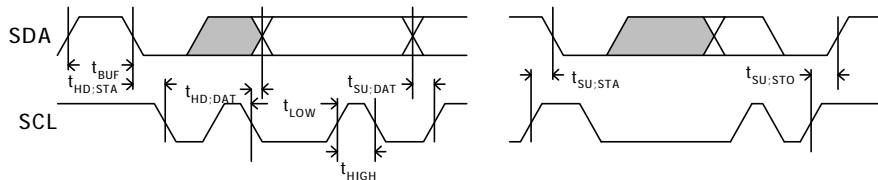


Figure 1. Serial Port Read/Write Timing
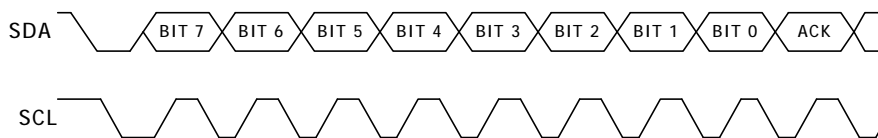


Figure 2. Serial Interface - Typical Byte Transfer
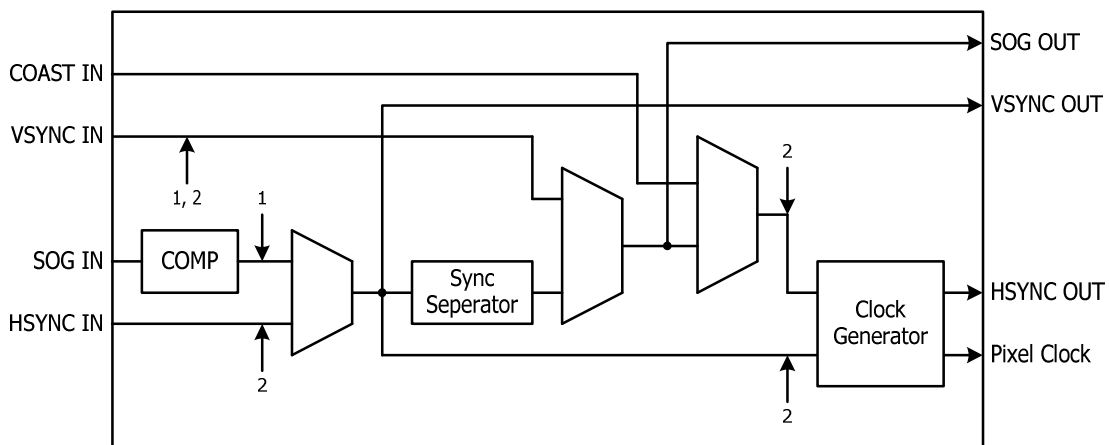


Figure 3. SYNC Processing Block Diagram

## Writing to Registers

To write data to a MST9883 control register, 3 bytes must be sent:

- Write the slave address byte with bit R/W=L
- Write the register address byte
- Write the desired register value

After each register value is written the register address auto-increments to allow multiple registers to be written within 1 write cycle.

## Reading from Registers

To read data from a MST9883 control register, a similar sequence must be followed except that it requires 2 separate but linked transfer cycles:

- Write the slave address byte with bit R/W=L
- Write the register address byte
- Write the slave address byte with bit R/W=H
- Read the desired register value

After each register value is read the register address auto-increments to allow multiple registers to be read within 1 read cycle.

When reading, there should be a STOP signal (optional) following the register address byte transfer, followed by a START signal.

The master device signaling to the MST9883 can generate a REPEATED START signal by generating a START signal without first generating a STOP signal to end the current transfer sequence. This may be used to change the mode of communications (read, write) between the master and slave without releasing the serial interface lines. This is only necessary when multiple master devices access the same serial interface lines.

## Serial Interface Examples

Multiple bus cycles can be linked together for multiple register read and write accesses. Each ACK handshake prepares the master and the MST9883 to transfer the next data byte.

- Write to one register

Start signal

Slave address byte

Register address byte

Data byte

Stop signal

- Write to N registers

Start signal

Slave address byte

Register address byte =ADDR

Data byte to address ADDR

Data byte to ADDR+1

Data byte to ADDR+2

....

Data byte to ADDR+N

Stop signal

- Read from one register

Start signal

Slave address byte (R/W bit = W)

Register address byte

Start signal

Slave address byte (R/W bit = R)

Data byte from register address

Stop signal

- Read from N sequential registers

Start signal

Slave address byte (R/W bit = W)

Register base address byte

Start signal

Slave address byte (R/W bit = R)

Data byte from base address + 1

Data byte from base address + 2

...

Data byte from base address + N

Stop signal.

# DESIGN GUIDE OVERVIEW

## General Description

The MST9883 is a highly-integrated analog interface for digitizing high-resolution RGB signals for PC's and workstations, and provides many innovative solutions to support the digitization process.  MST9883 can accurately support display resolutions up to 1280x1024 (SXGA) at 75Hz.

- The MST9883 provides a serial port programmable interface over the following input controls:

- Brightness & Contrast adjustment

- Clamping

- Pixel clock generation

- Clock phase adjustment (sampling)

## Input Signal Handling

### Analog Inputs

The MST9883 has three high impedance analog input pins for the red, green, and blue channels.  They will accommodate signals ranging from 0.5V to 1.0V p-p.  Clamping is provided to allow RGB inputs to be AC-coupled.
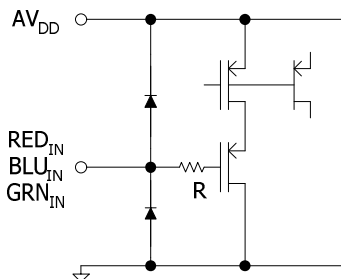


Figure 4. Equivalent Analog Input Circuit
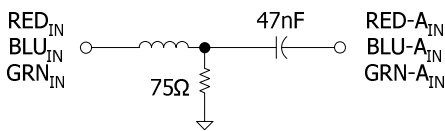


Figure 5. Analog Input Interface Circuit

### HSYNC, VSYNC Inputs

The MST9883 requires only a horizontal sync signal to generate the pixel clock and clamp timing.  No external loop filter is required for PLL.
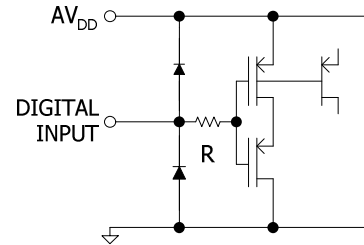


Figure 6. Equivalent Digital Input Circuit

### Serial Control Port

The serial control port (SDA, SCL) is designed for 3.3V logic.  If driven by 5V supplies, the SDA and SCL should be protected using 150-Ohms series resistors.
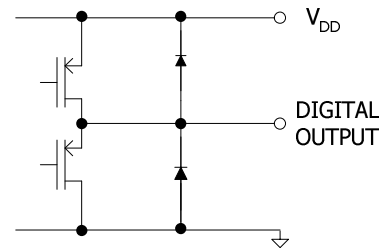


Figure 7. Equivalent Digital Output Circuit

## Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3V power supply ($V_{DD}$).
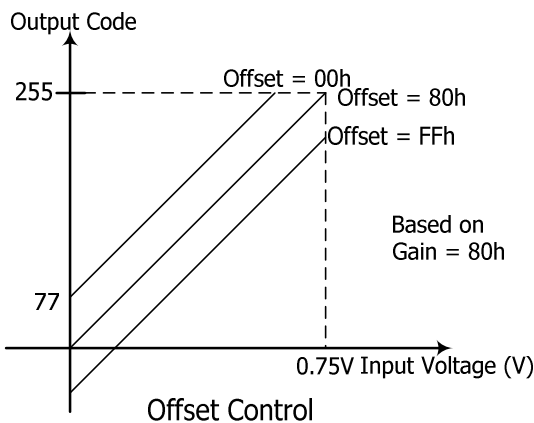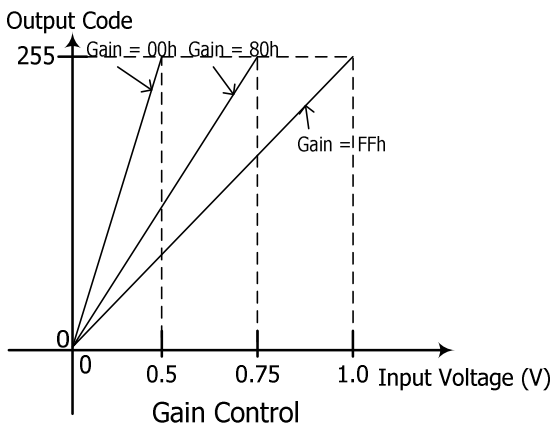
## Clamping

To properly digitize the incoming signal, the dc offset of the input signal must be adjusted to fit the range of the on-board A/D converters.  Clamping forces the ac-coupling capacitor to maintain a dc offset voltage between the external input and the internal signal to satisfy the condition.  The MST9883 provides 2 clamp-timing options:

- The first recommended method uses the external CLAMP pin which directly generates the clamping action.  This model is entered by setting EXTCLMP=1 and CLAMPOL to the desired polarity.

- The second recommended method uses an internal counter to generate the clamp signals.  The register CLPLACE sets the number of ADC clock periods between the trailing edge of HSYNC and the start of the clamping.  The CLPDUR register sets the duration of the clamp.  Recommended values for the CLPLACE and CLPDUR registers are 08h and 0Ah, respectively.

## Gain and Offset Control

The MST9883 can accommodate input signals ranging from 0.5V to 1.0V full scale.  To accommodate input signals in this range, gain and offset registers are provided, with independent control for all 3 analog inputs. The gain register is an 8-bit control which sets the full-scale input voltage between 0.5v (GAIN=00h) and 1.0v (GAIN=FFh) in 256 increments.  Note that increasing the value in the gain register reduces the contrast.

The offset register provides a ±127 LSB adjustment to the image brightness for the red, green, and blue channel inputs, where 1 LSB offset = 0.615 LSB ADC (Note: this ratio is independent with the gain setting).

controls are used to optimize the PLL performance for each specific video format. Table I (next page) shows the recommended settings for the most common video formats.  A phase adjustment register is provided which allows the sampling of the ADC input to occur  at 1 of 32 discrete time-points evenly spaced over each pixel clock period.  This phase adjustment provides a way to find the optimal pixel sampling time.



Figure 8.  Pixel Sampling Times



Gain Control



Offset Control

## Clock Generation

A Phase Locked Loop (PLL) is employed to generate the pixel clock.  Using an innovative approach, the external loop filter has been eliminated from the PLL. The MST9883 uses advanced CMOS signal processing techniques to reduce the effects of manufacturing variations and board level noise on the PLL performance. The jitter compliance of the MST9883 PLL has been carefully designed to avoid degrading the performance of the MST9883 ADC function when digitizing typical video signals, an example of which is shown in Fig. 8.  The VCORNGE and CURRENT register
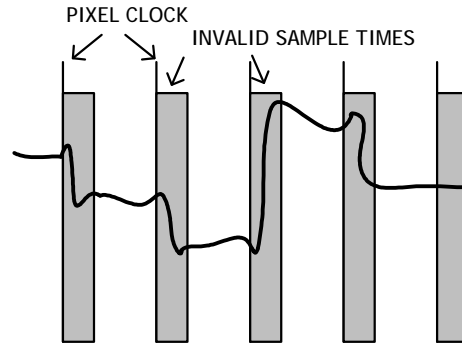
## DIGITAL TIMING

### Horizontal Sync Timing

In addition to using HSYNC as a timing base to synthesize a low-jitter pixel sampling clock, HSYNC is also used as a reference point to provide several on-chip and system level timing signals. An output horizontal sync (HSOUT) signal whose leading edge is synchronized to the falling edge of DCK is generated from HSYNC. The leading edge of HSOUT is pipelined in a fixed timing relationship with the ADC data.

### COAST Timing

In some systems the HSYNC signal timing is disturbed during the vertical sync (VSYNC) period.    During the

VSYNC period in these systems, the COAST input should be asserted to signal the MST9883 to ignore the invalid HSYNC timing.
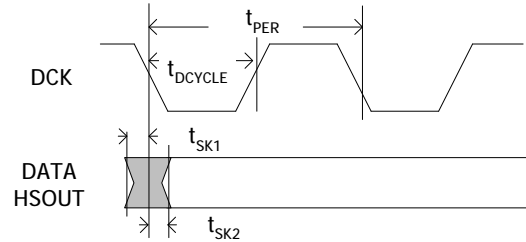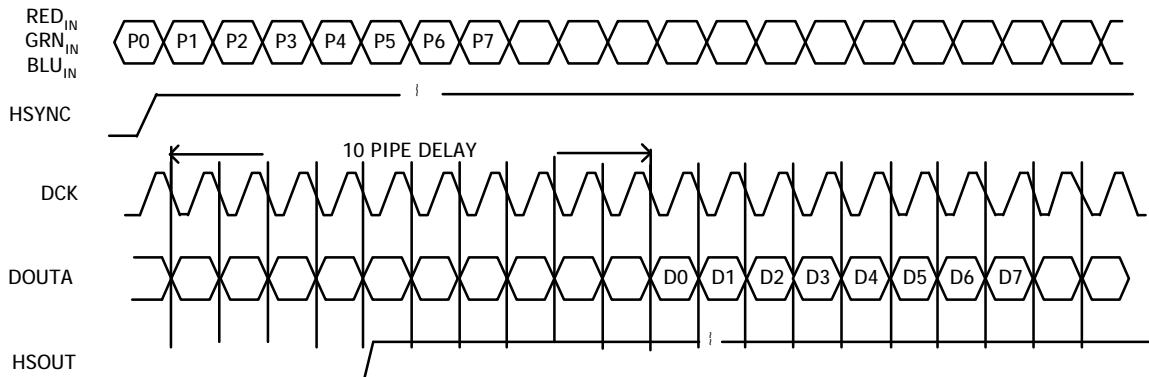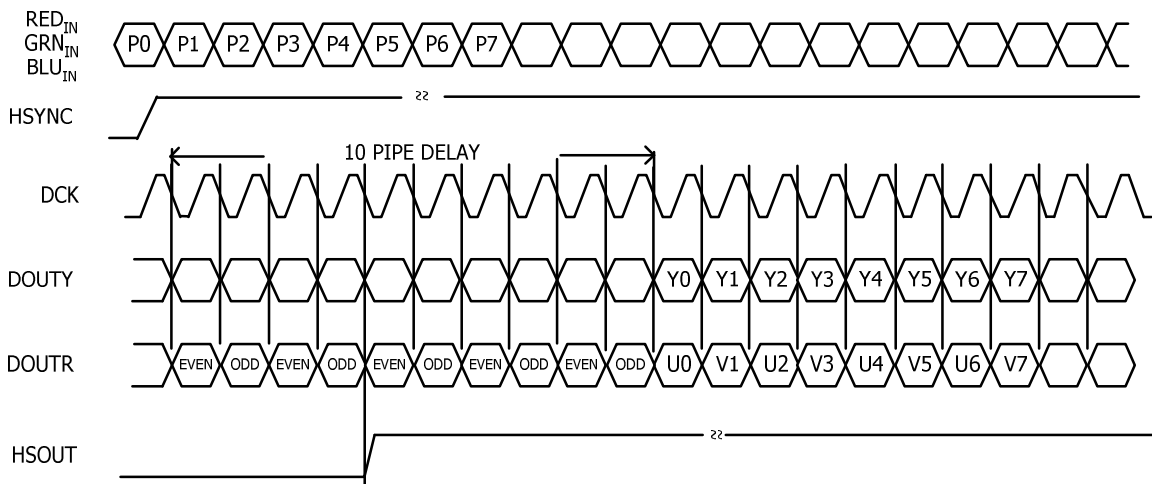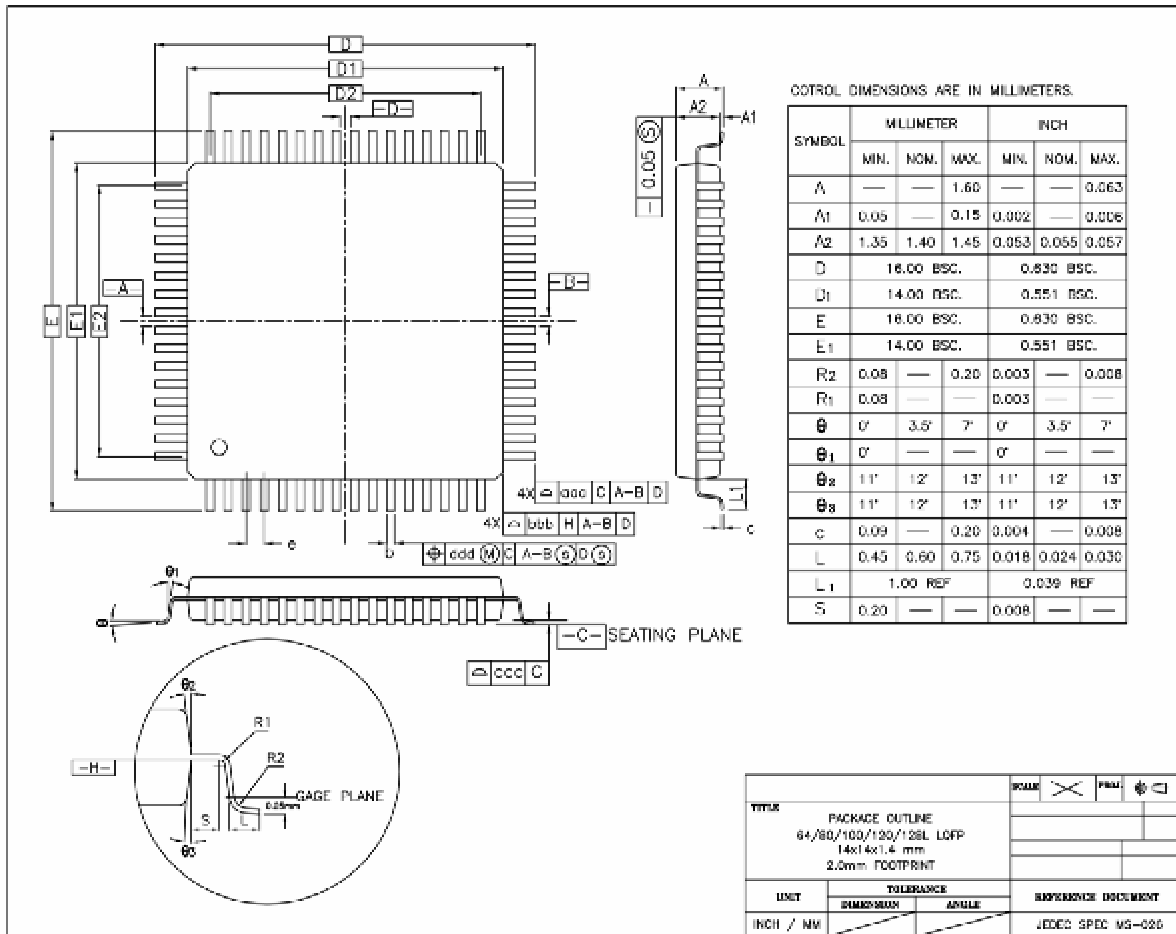


Figure 9. Ouput Timing



Figure 10. Single Port  Mode



Figure 11. 4:2:2 Mode

| Standard | Resolution | Refresh Rate | Horizontal Frequency | Pixel Rate | VCORNGE | CURRENT |
|----------|------------|--------------|----------------------|------------|---------|---------|
| VGA | 640 X 480 | 60 Hz<br>72 Hz<br>75 Hz<br>85 Hz | 31.5 kHz<br>37.7 kHz<br>37.5 kHz<br>43.3 kHz | 25.175 MHz<br>31.500 MHz<br>31.500 MHz<br>36.000 MHz | 00<br>00<br>00<br>00 | 101<br>110<br>110<br>110 |
| SVGA | 800 X 600 | 56 Hz<br>60 Hz<br>72 Hz<br>75 Hz<br>85 Hz | 35.1 kHz<br>37.9 kHz<br>48.1 kHz<br>46.9 kHz<br>53.7 kHz | 36.000 MHz<br>40.000 MHz<br>50.000 MHz<br>49.500 MHz<br>56.250 MHz | 00<br>01<br>01<br>01<br>01 | 110<br>100<br>100<br>100<br>101 |
| XGA | 1024 X 768 | 60 Hz<br>70 Hz<br>75 Hz<br>80 Hz<br>85 Hz | 48.4 kHz<br>56.5 kHz<br>60.0 kHz<br>64.0 kHz<br>68.3 kHz | 65.000 MHz<br>75.000 MHz<br>78.750 MHz<br>85.500 MHz<br>94.500 MHz | 01<br>10<br>10<br>10<br>10 | 110<br>100<br>100<br>100<br>100 |
| SXGA | 1280 X 1024 | 60 Hz<br>75 Hz | 64.0 kHz<br>80.0 kHz | 108.000 MHz<br>135.000 MHz | 10<br>11 | 110<br>101 |

Table I. Recommended VCORNGE and CURRENT Settings for Standard Display Formats

## MECHANICAL DIMENSIONS

COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC. | | | 0.630 BSC. | | |
| D1 | 14.00 BSC. | | | 0.551 BSC. | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| E1 | 14.00 BSC. | | | 0.551 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |

TITLE: PACKAGE OUTLINE
64/80/100/120/128L LQFP
14x14x1.4 mm
2.0mm FOOTPRINT

REFERENCE DOCUMENT: JEDEC SPEC MS-026

## Revision History

| Document | Description | Date |
|---|---|---|
| MST9883 v1.0 | Ÿ  Initial release | Sep 2002 |
| MST9883 v1.3 | Ÿ  Updated for clarification | Dec 2002 |
| MST9883 v1.5 | Ÿ  Add sync separator threshold count documentation<br>Ÿ  Offset registers changed to 8-bit | Jan 2003 |
| MST9883 v1.6 | Ÿ  Updated for clarification<br>Ÿ  Enhanced for TV operation compatibility with noise reduction filter<br>Ÿ  Edit to Electrical Specifications, page 10 | Mar 2003 |