September 1999

8 - Bit Micro-controller

with 32KB flash embedded

Product List

MSU2958C16, 16 MHz 32 KB internal memory MCU
MSU2958C25, 25 MHz 32 KB internal memory MCU
MSU2958C40, 40 MHz 32 KB internal memory MCU

Description

The MVI MSU2958 series product is an 8 - bit single chip microcontroller with 32 KB flash embedded. It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 32 K byte memory either for program or for data or mixed.
To program the flash block, a commercial programmer is capable to do it.

Ordering Information

MSU2958ihhk (blank chip)
MSU2958ihh - yyyk

i: process identifier {L, C}.
hh: working clock in MHz {16, 25, 40}.
yyy: production code {001, ..., 999}
k: package type postfix {as below table}.

Postfix	Package	Pin/Pad Configuration	Dimension	Logo Size at Top Marking
P	40L PDIP	page 2	page 11	5.0 x 4.2 mm
J	44L PLCC	page 2	page 13	4.5 x 3.8 mm
Q	44L PQFP	page 2	page 12	2.8 x 2.4 mm
U	44L LQFP	page 2	-	2.8 x 2.4 mm

Features

- Working voltage : 4.5 V through 5.5 V
  Programming voltage : 5 V
- General 80C51 family compatible
- 12 clocks per machine cycle
- 32 K byte internal flash memory
- 256 byte data RAM
- Three 16 bit Timers/Counters
- Four 8 -bit I/O ports
- Full duplex serial channel
- Bit operation instructions
- Page free jumps
- 8 - bit Unsigned Division
- 8 - bit Unsigned Multiply
- BCD arithmatic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
  Idle mode and Power down mode
- Working at 16/25/40 MHz Clock
- Code protention by provided

China (ShenZhen)
#3901, Block A , United Plaza No. 5022 Binhe Road, North ShenZhen , China
518026 , China
TEL : 86-755-2711963
TEL: 86-755-2711938
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TEL : 86-21-64853816 ext:2837
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#1 Creation Road I,
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Ming Chuang E. Road,
Taipei,105
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Hongkong
#19, Dai Fu Street,
Taipo Industrial Estate,
Taipo, N.T.
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TEL: 852-2665-4883
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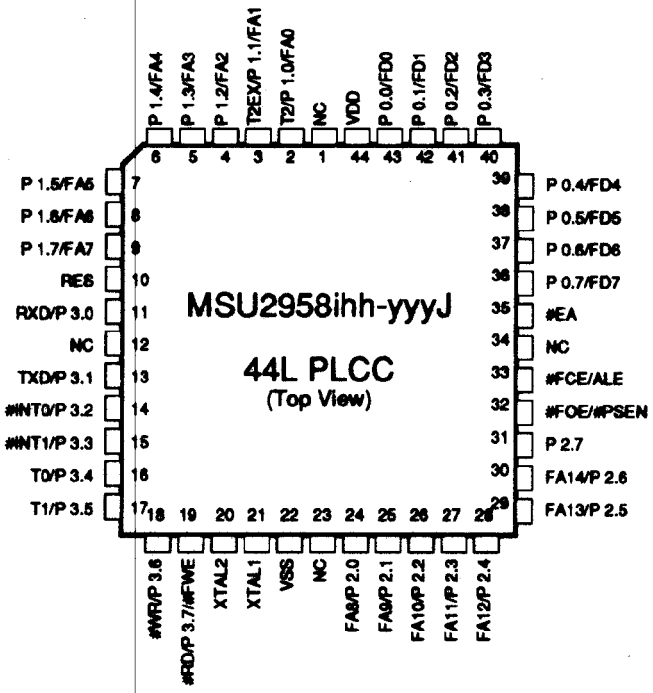
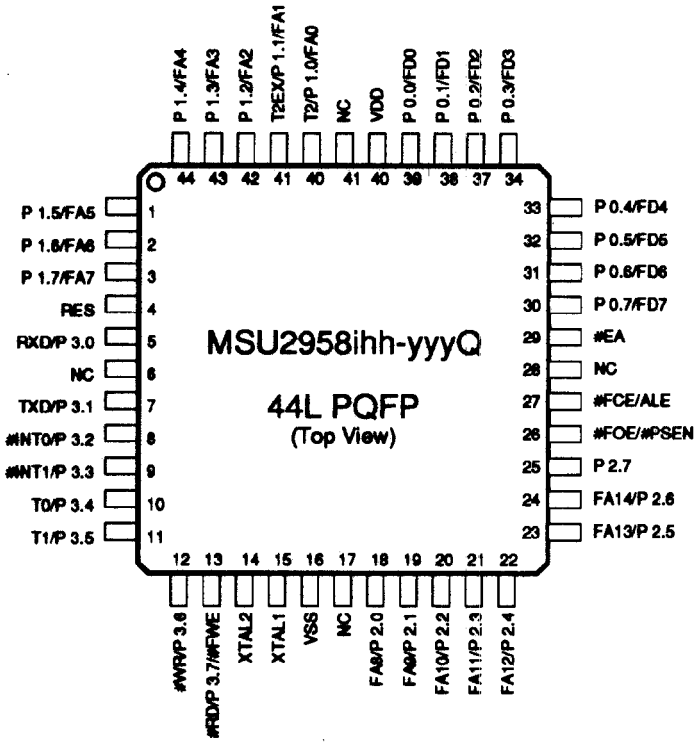
Japan
WBG Marive West 25F
6, Nakase 2 - chome,
Mihama - Ku, Chiba-shi,
Chiba 261-7125,
Japan
TEL: 043 - 2996000
FAX: 043 - 2996555

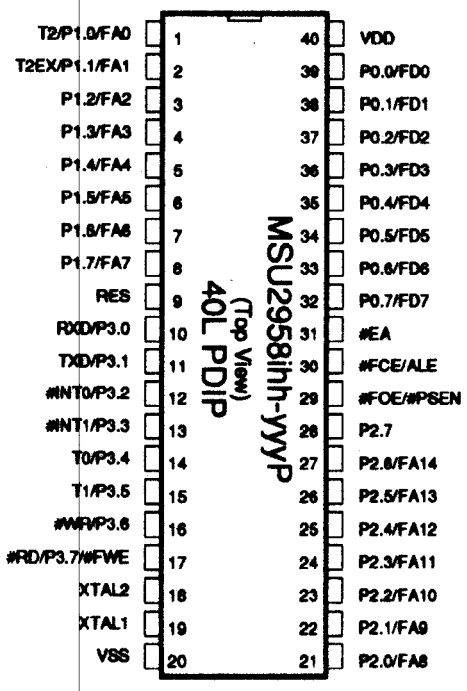
U.S.A.
#3910, North First Street,
San Jose,
CA. 95134-1501
U.S.A.
TEL: 1-408-433-6000
FAX: 1-408-433-0952

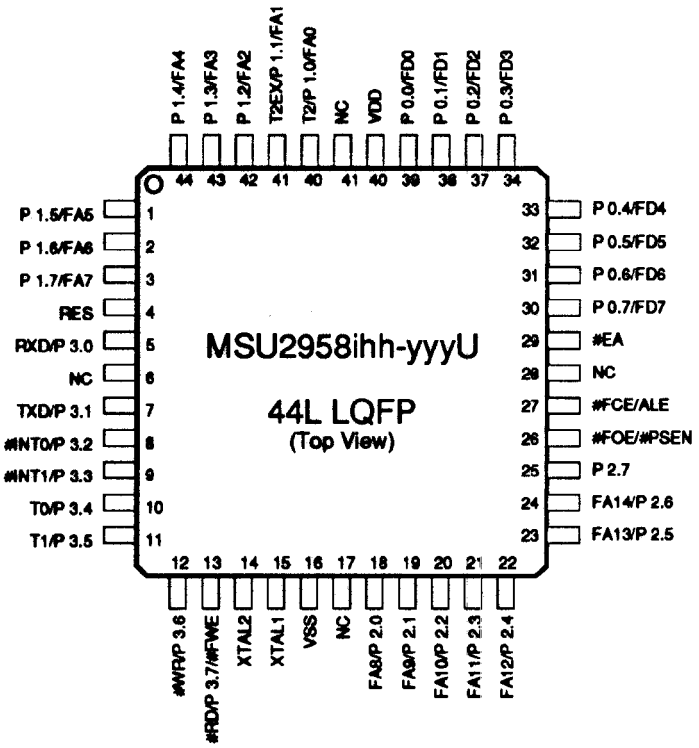
http:\\www.moselvitelic.com

Pin Configurations

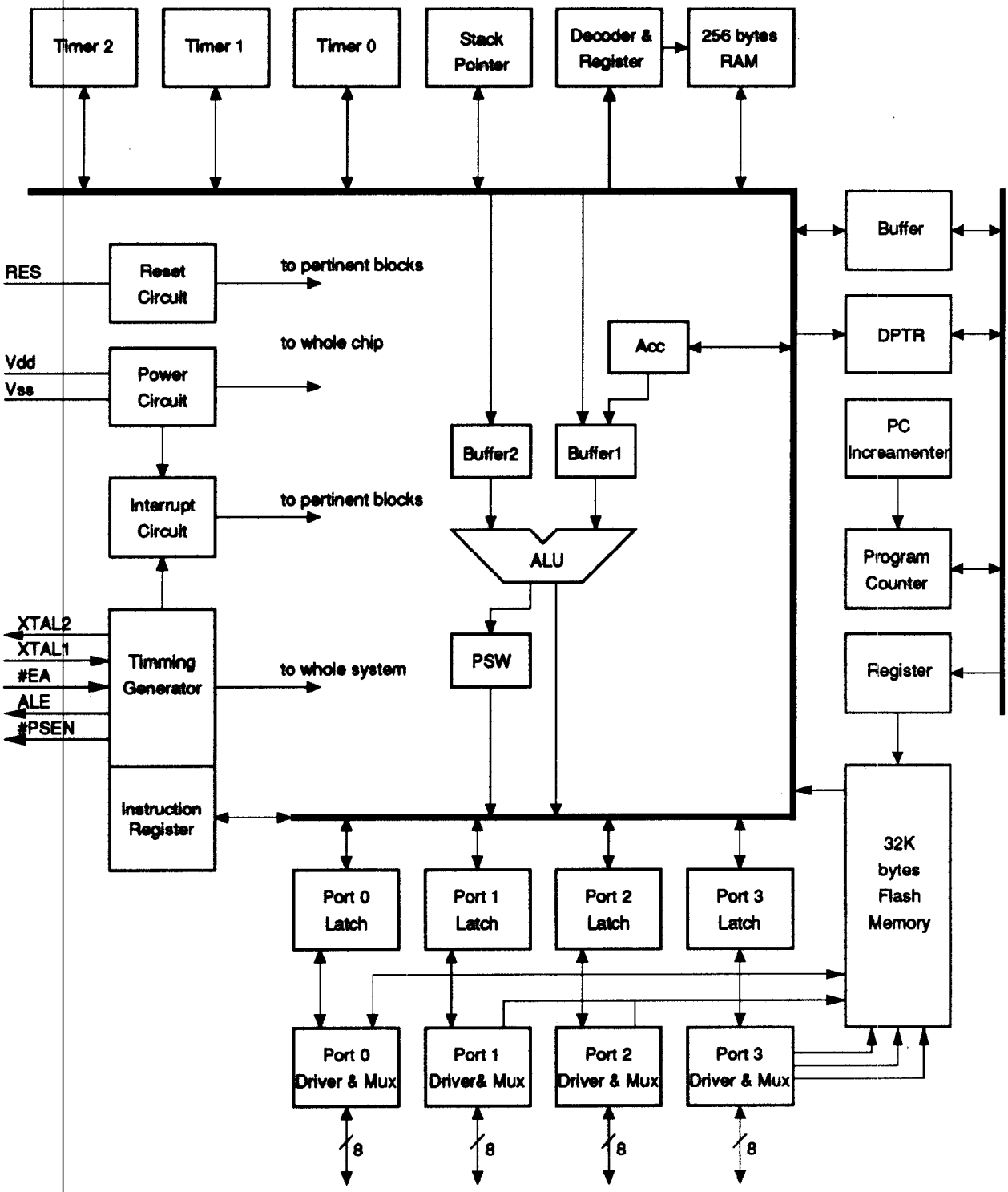








Block Diagram



Pin Descriptions

40L PDIP Pin#		44L LQFP Pin#	44L PQFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1		40	40	2	T2/P1.0/FA0		I/o	bit 0 of Port 1 & timer 2 & bit 0 of flash block address
2		41	41	3	T2EX/P1.1/FA1		I/o	bit 1 of Port 1 & timer control & bit 1 of flash block addr.
3		42	42	4	P1.2/FA2		I/o	bit 2 of Port 1 & bit 2 of flash block address
4		43	43	5	P1.3/FA3		I/o	bit 3 of Port 1 & bit 3 of flash block address
5		44	44	6	P1.4/FA4		I/o	bit 4 of Port 1 & bit 4 of flash block address
6		1	1	7	P1.5/FA5		I/o	bit 5 of Port 1 & bit 5 of flash block address
7		2	2	8	P1.6/FA6		I/o	bit 6 of Port 1 & bit 6 of flash block address
8		3	3	9	P1.7/FA7		I/o	bit 7 of Port 1 & bit 7 of flash block address
9		4	4	10	RES	H	I	Reset
10		5	5	11	RXD/P3.0		I/o	bit 0 of Port 3 & Receive data & flash block enable
11		7	7	13	TXD/P3.1		I/o	bit 1 of Port 3 & Transmit data
12		8	8	14	#INT0/P3.2	L/ -	I/o	bit 2 of Port 3 & low true interrupt 0
13		9	9	15	#INT1/P3.3	L/ -	I/o	bit 3 of Port 3 & low true interrupt 1
14		10	10	16	T0/P3.4		I/o	bit 4 of Port 3 & Timer 0
15		11	11	17	T1/P3.5		I/o	bit 5 of Port 3 & Timer 1
16		12	12	18	#WR/P3.6	L/ -	I/o	bit 6 of Port 3 & o/p enable to flash block (low enable)
17		13	13	19	#RD/P3.7/#FWE	L/ - /L	I/o	bit 7 of Port 3 & write enable to flash block (low enable)
18		14	14	20	XTAL2		o	Crystal out
19		15	15	21	XTAL1		I	Crystal in
20		16	16	22	VSS			Sink Voltage, Ground
21		18	18	24	P2.0/FA8		I/o	bit 0 of Port 2 & bit 8 of flash block address
22		19	19	25	P2.1/FA9		I/o	bit 1 of Port 2 & bit 9 of flash block address
23		20	20	26	P2.2/FA10		I/o	bit 2 of Port 2 & bit 10 of flash block address
24		21	21	27	P2.3/FA11		I/o	bit 3 of Port 2 & bit 11 of flash block address
25		22	22	28	P2.4/FA12		I/o	bit 4 of Port 2 & bit 12 of flash block address
26		23	23	29	P2.5/FA13		I/o	bit 5 of Port 2 & bit 13 of flash block address
27		24	24	30	P2.6/FA14		I/o	bit 6 of Port 2 & bit 14 of flash block address
28		25	25	31	P2.7		I/o	bit 7 of Port 2
29		26	26	32	#PSEN/#FOE	L/L	o/I	program storage enable
30		27	27	33	ALE/#FCE	- /L	o/I	address latch enable
31		29	29	35	#EA	L	I	external access
32		30	30	36	P0.7/FD7		I/o	bit 7 of Port 0 & data bit 7 of flash block
33		31	31	37	P0.6/FD6		I/o	bit 6 of Port 0 & data bit 6 of flash block
34		32	32	38	P0.5/FD5		I/o	bit 5 of Port 0 & data bit 5 of flash block
35		33	33	39	P0.4/FD4		I/o	bit 4 of Port 0 & data bit 4 of flash block
36		34	34	40	P0.3/FD3		I/o	bit 3 of Port 0 & data bit 3 of flash block
37		35	35	41	P0.2/FD2		I/o	bit 2 of Port 0 & data bit 2 of flash block
38		36	36	42	P0.1/FD1		I/o	bit 1 of Port 0 & data bit 1 of flash block
39		37	37	43	P0.0/FD0		I/o	bit 0 of Port 0 & data bit 0 of flash block
40		38	38	44	VDD			Drive Voltage, +5 Vcc

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
t A	Ambient temperature under bias	0	25	70	°C	
V CC5	Supply voltage	4.5	5.0	5.5	V	U2958C
f osc 16	Oscillator Frequency	3.0	16	16	MHz	U2958C16
f osc 25		16	25	25	MHz	U2958C25
f osc 40		25	40	40	MHz	U2958C40

AC Characteristics

(16/25/40 MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Outputs=80pF)

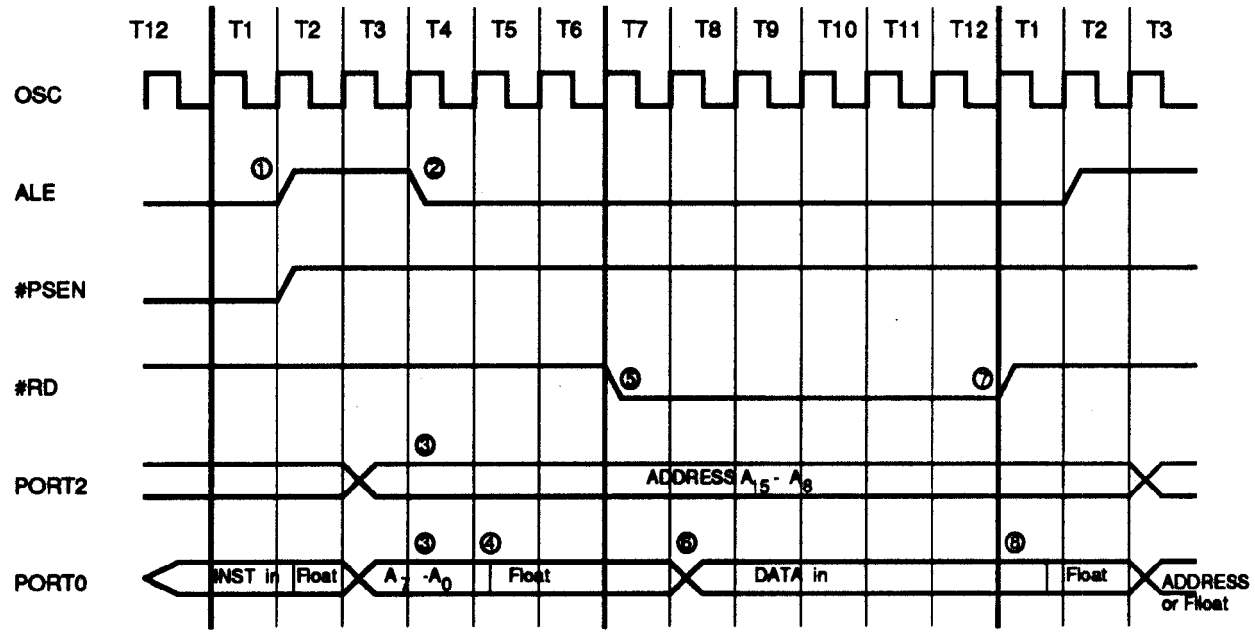
		Valid	f osc 16			Variable f osc				
Symbol	Parameter	Cycle	Min.	Typ.	Max	Min.	Typ.	Max.	Unit	Remarks
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T-10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T-10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data in	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YHLH	#WR or #RD high to ALE high	RD/WRT	53		72	T - 10		T + 10	nS	
T CHCL	Clock fall time								nS	
T CLCX	Clock low time								nS	
T CLCH	Clock rise time								nS	
T CHCX	Clock high time								nS	
T, T CLCL	Clock period			63			1/ fosc		nS	

DC Characteristics

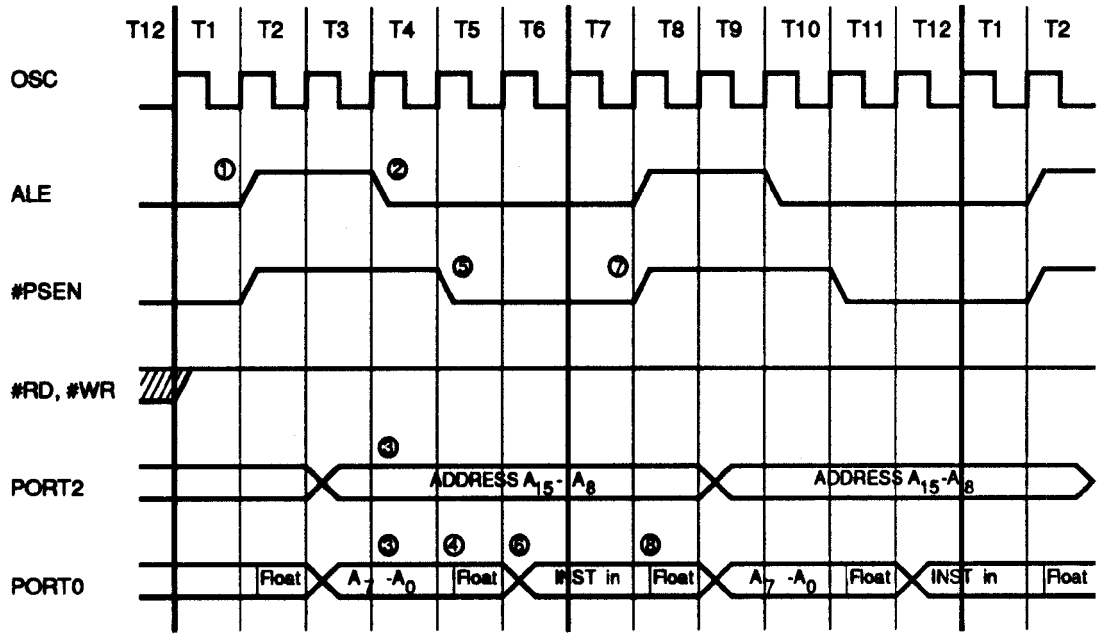
(16/25/40 MHz, typical operating conditons, valid for U2958C series)

Symbol	Parameter	Valid	Min.	Typ.	Max	Unit	Test Conditions
V ILX	Input Low Voltage	XTAL1	-0.5		20%Vcc-0.1	V	
		#EA	0		20%Vcc-0.3	V	
V ILR	"	RES	-0.5		20%Vcc-0.1	V	
V IHX	Input High Voltage	XTAL1	70%Vcc		Vcc+0.5	V	
		#EA	20%Vcc + 0.9		Vcc+0.5	V	
V IHR	"	RES	70%Vcc		Vcc+0.5	V	
	Output Low Voltage	ALE, #PSEN			450	mV	I OL = 3.2 mA
V OL0	"	ports 0,3			450	mV	I OL = 3.2 mA
V OL1	"	ports 1,2			450	mV	I OL = 1.6 mA
	Output High Voltage	ALE, #PSEN	2.4			V	I OH = -60 uA
	"		90%Vcc			V	I OH = -10 uA
V OH0	"	port 0	2.4			V	I OH = -800 uA
	"		90%Vcc			V	I OH = -80 uA
V OH1	"	ports 1,3	2.4			V	I OH = -60 uA
	"		90%Vcc			V	I OH = -10 uA
V OH2	"	port 2	2.4			V	I OH = -60 uA
	"		90%Vcc			V	I OH = -10 uA
I OL0	Output Low Current	ports 0,3				mA	V OL = 0.45V, note 1
I IL	Logical 0 Input Current	ports 1,2,3			50	uA	V in = 0.45 V
I IH	Logical 1 Input Current	port 0			1.5	uA	V in = 5.0 V
I TL	Logic Transition Current	ports 1,2,3			650	uA	V in = 2.0 V
I LI	Input Leakage Current	port 0			10	uA	0.45V < Vin < Vcc
R RES	Reset Pulldown Resistance	RES	50		150	Kohm	
R X	Crystal feedback Resistance	XTAL1,2	90		330	Kohm	
C IO	Pin Capacitance				10	pF	Freq=1MHz, Ta=25 °C
I CC	Power Supply Current	Vdd			8	mA	Active mode, 16 MHz
		Vdd			25	mA	Idle mode, 16MHz
		Vdd			25	mA	Power down mode

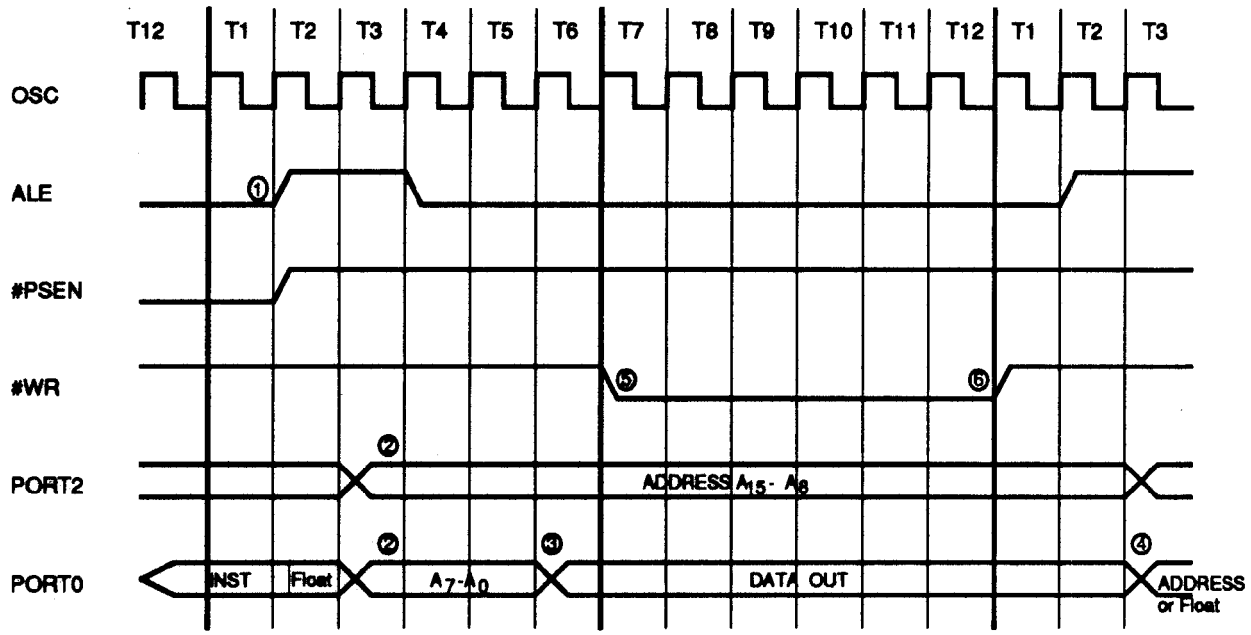
Data Memory Read Cycle Timing



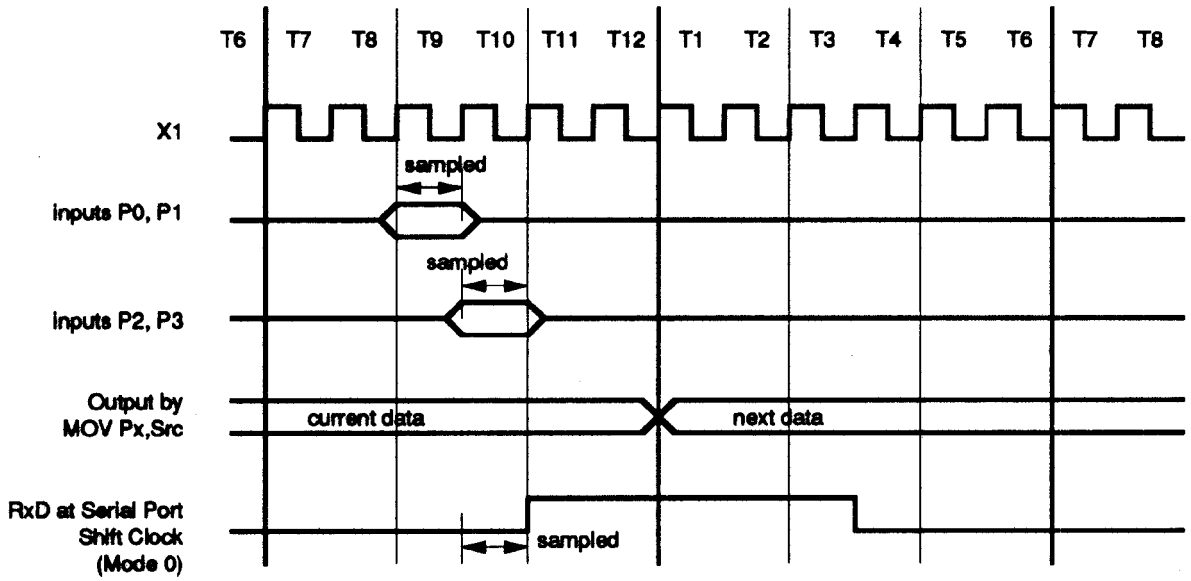
Program Memory Read Cycle Timing



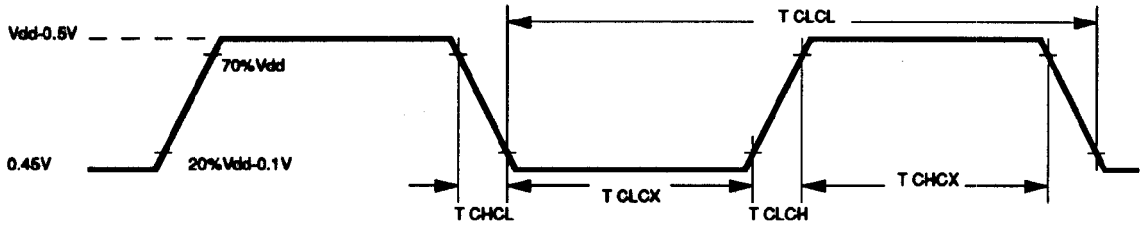
Data Memory Write Cycle Timing



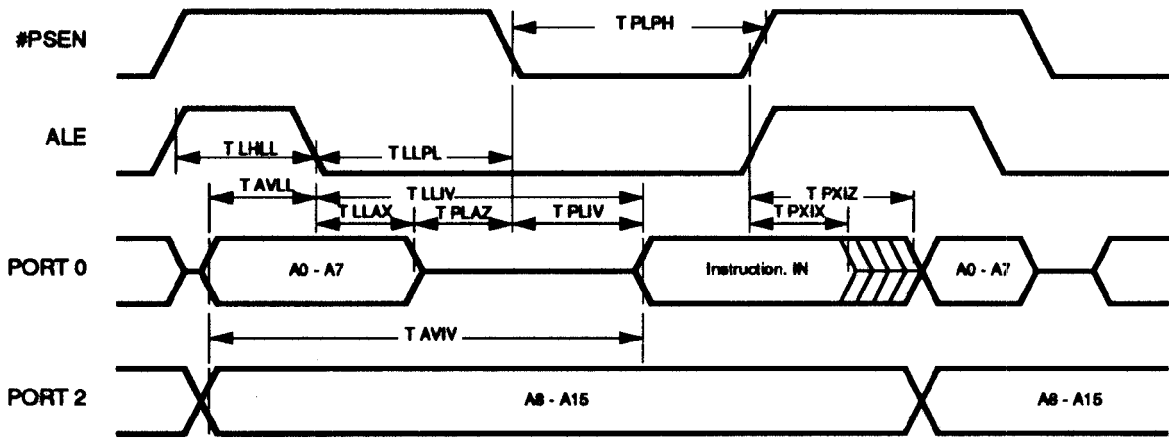
I/O Ports Timing



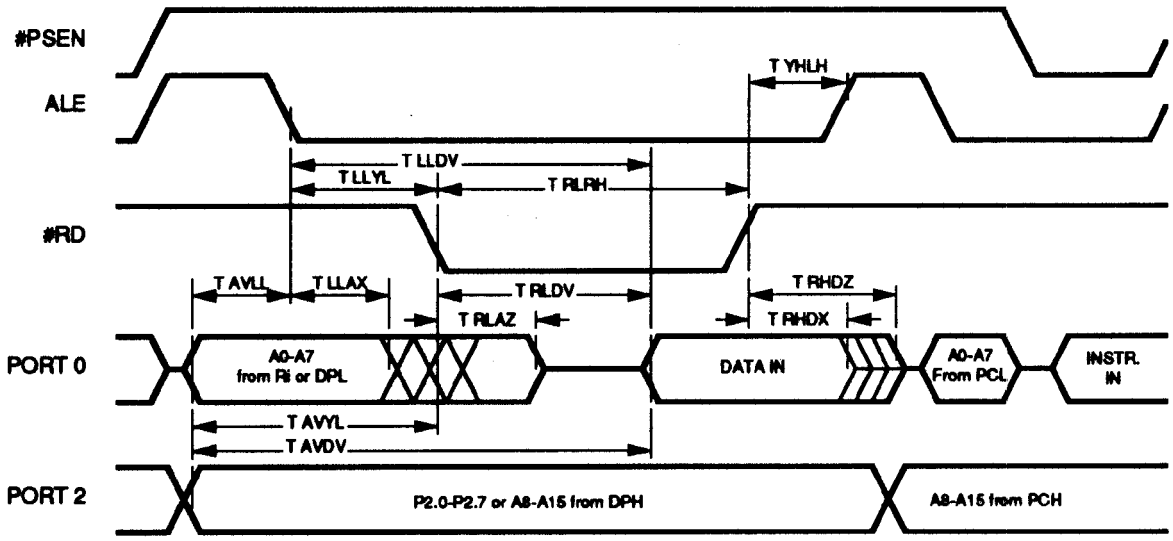
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



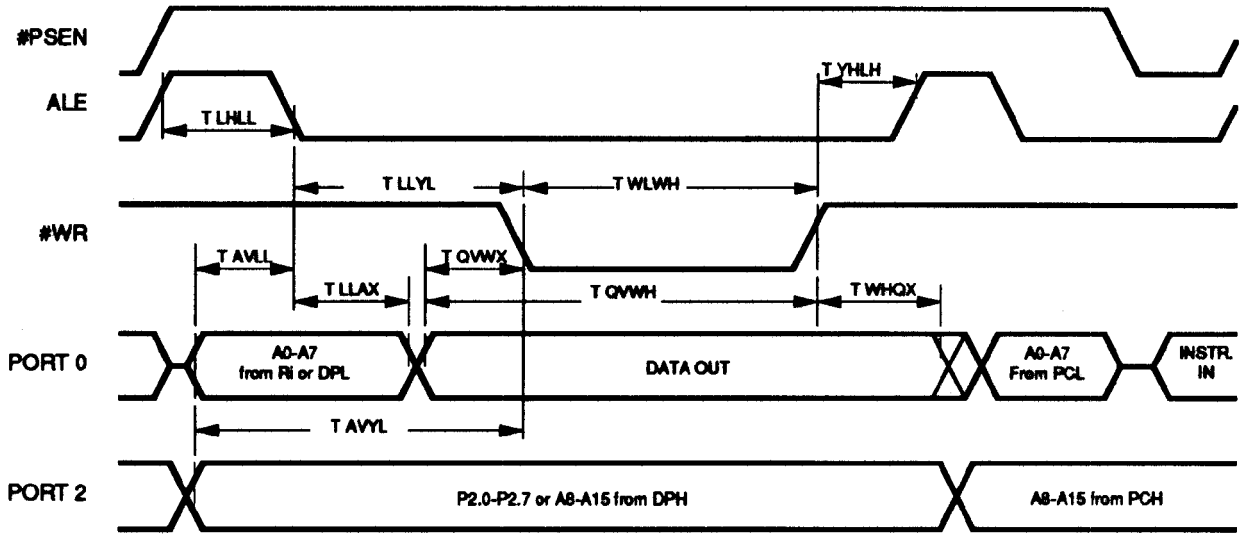
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle

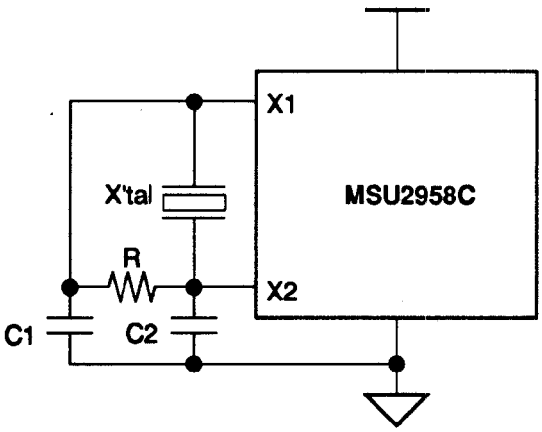


Tm.III External Data Memory Write Cycle

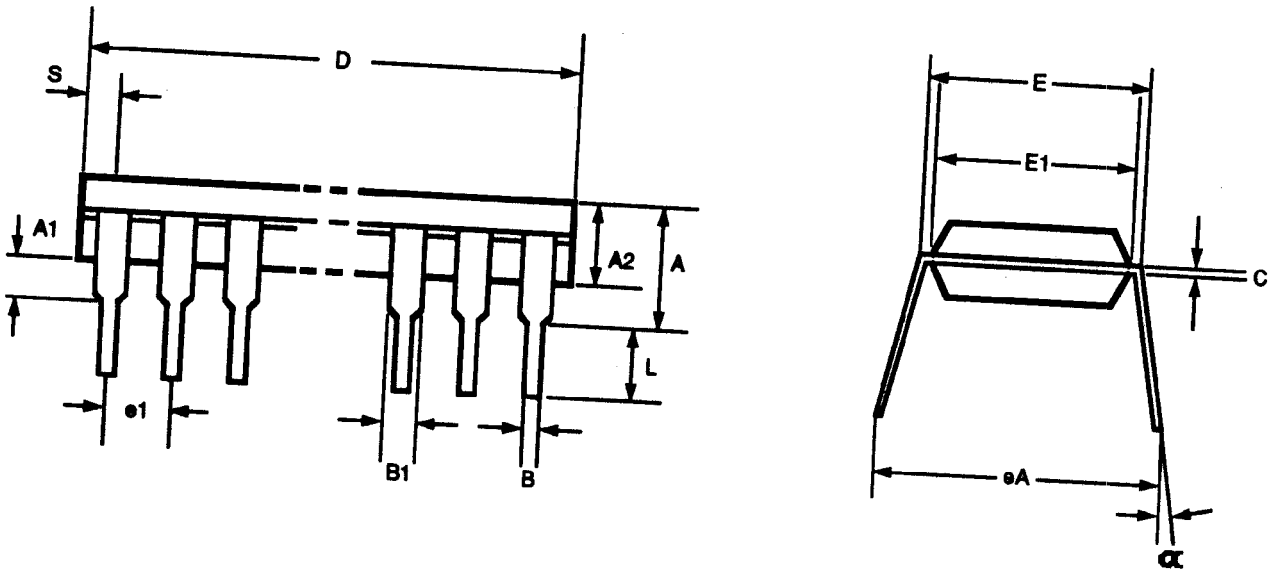


Application Reference

Valid for U2958C				
X'tal	3 MHz	6 MHz	9 MHz	12 MHz
C1	30 p	30 p	30 p	30 p
C2	30 p	30 p	30 p	30 p
R	open	open	open	open
X'tal	16 MHz	25 MHz	33 MHz	40 MHz
C1	30 pF	15 pF	10 p	5 pF
C2	30 pF	15 pF	10 p	5 pF
R	open	62 Kohm	6.8 K	4.7 Kohm



40L 600mil PDIP Information

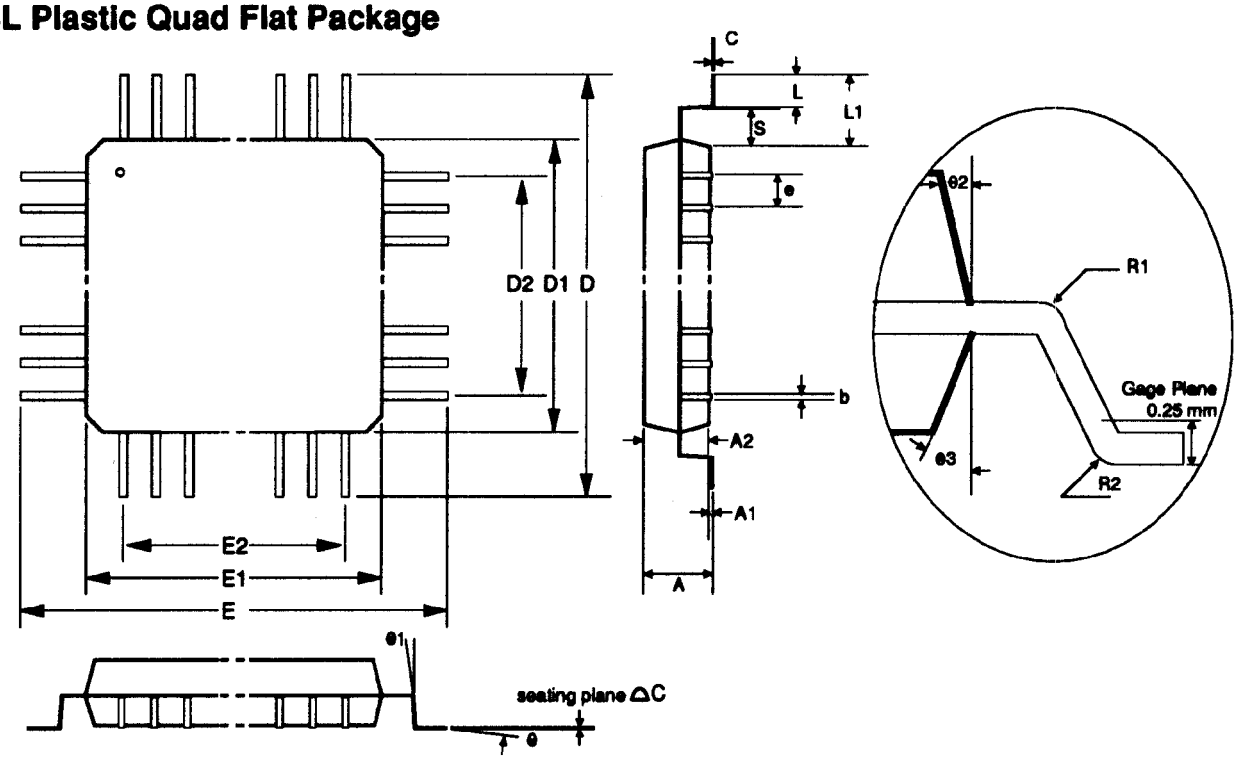


Note:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimenseion D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in Inch	Dimension in mm
	minimal/maximal	minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
α	0° / 15°	0° / 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Quad Flat Package



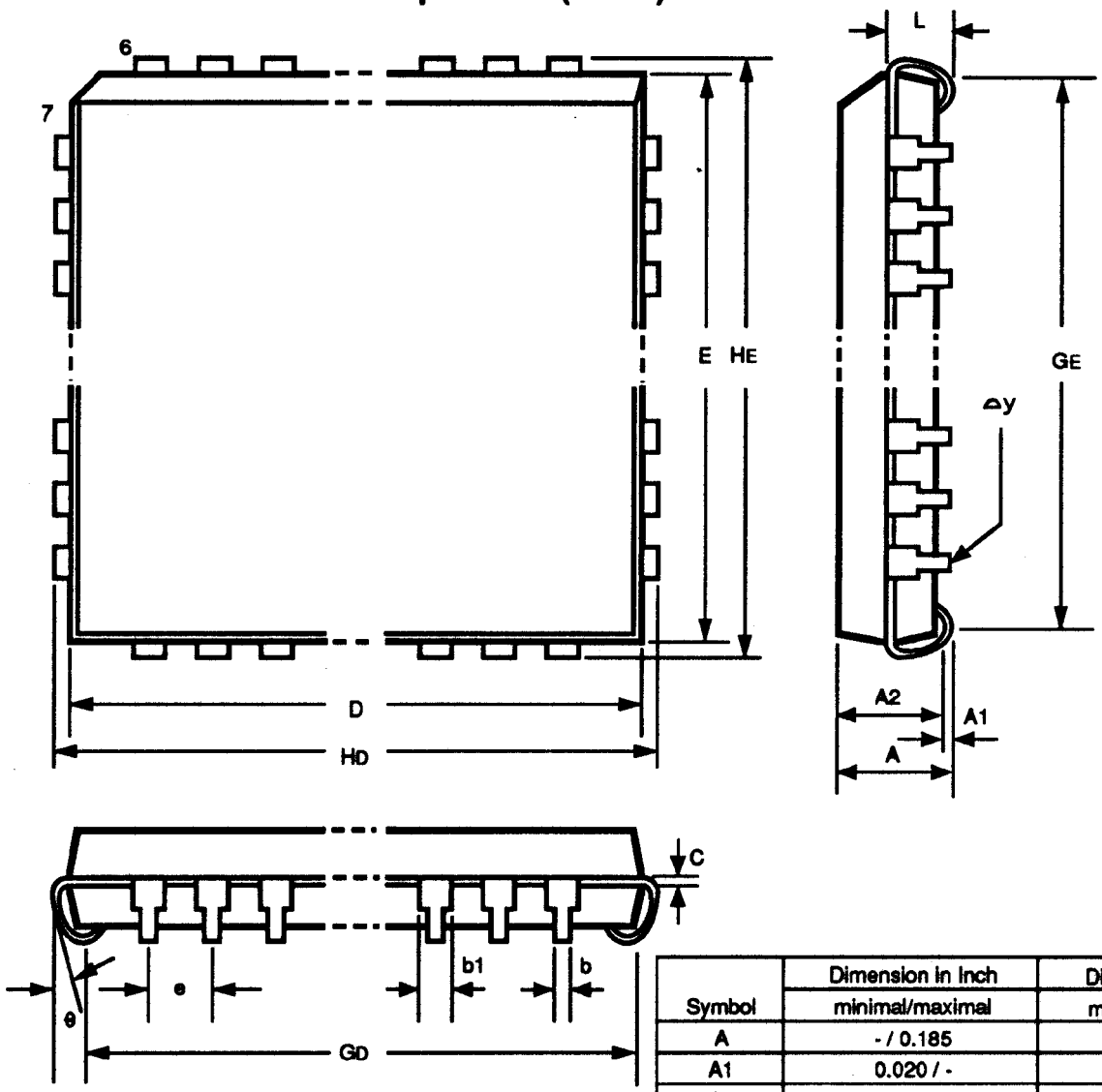
Note:

Dimension D1 and E1 do not include mold protrustion. Allowance protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane.

Dimension b does not include dambar protrusion. Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.067	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌓C	0.004	0.10

44L Plastic Leaded Chip Carrier (PLCC)



Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
∆y	- / 0.004	- / 0.10
θ	/	/

Note:

1. Dimension D & E does not include interlead flash.
2. Dimension b1 does not include dambar protrusion/ intrusion.
3. Controlling dimension:Inch
4. General appreance spec. should base on final visual inspection spec.

To: Mosel Vitelic Inc.
886-3-578-4732 (fax#)
Attn: S&M department of Strategic product division

Logo Top Marking Request & spec.

We hereby request MVI to have our logo printed on top of the device package. Below is the specification of our logo in 20:1 scale base. This logo diagram is clear enough and is able to be shrunk directly to fit into available top marking area described on page.

Phone # : _____ Fax # : _____

Company Name : _____

Signature : _____

Name (Typed) : _____

Position Title : _____

Department, Section : _____

Signature Date : _____