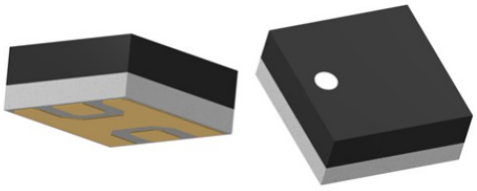
MSWSHC-050-10-CM35

PIN Diode Shunt Switch Element

Rev. V1

Features

- Supports up to 35 W Power
- Low Insertion Loss:
  - <0.10 dB @ 1 GHz
  - <0.35 dB @ 6 GHz
  - <0.70 dB @ 10 GHz (with input tuning)
- High Isolation:
  - >40 dB @ 2 GHz
- RoHS* Compliant



(CM35)
non-hermetic

Description

A broadband, high linearity, medium power shunt switch element in a 4.06 x 4.06 mm thermally highly conductive Alumina Nitride surface mount package. This part is designed for reliable power switch applications up to 35 watts and with a frequency range from 1 MHz to 10 GHz (with input tuning).

Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage (V_B)	I_R = 10 µA	V	200	—	—
Forward Voltage (V_F)	I_F = 50 mA	mV	—	900	950
Insertion Loss (I_L)	V_F = -40 V, <2 GHz V_F = -40 V, <6 GHz V_F = -40 V, <10 GHz	dB	—	0.15 0.35 0.70	0.30 — —
Isolation (I_{SO})	I_F = 100 mA, <1 GHz I_F = 10 mA, <6 GHz	dB	35 —	42 32	—
Input / Output Return Loss (R_L)	V_F = -40 V, <2 GHz V_F = -40 V, <6 GHz V_F = -40 V, <10 GHz	dB	25 — —	30 30 20	—
Minority Carrier Lifetime (T_L)	I_F = 10 mA, I_R = 6 mA, @ 50%	ns	—	3000	—

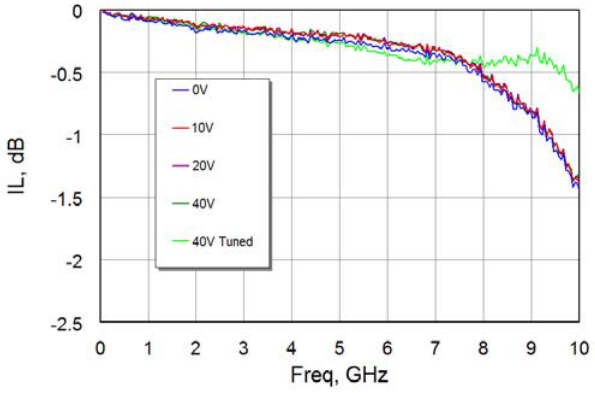
Absolute Maximum Ratings

Parameter	Absolute Maximum
Reverse Voltage	200 V
Forward Current	200 mA
Thermal Resistance	10°C/W
Junction Temperature	-40°C to +175°C
Storage Temperature	-55°C to +150°C
Assembly Temperature	+260°C, Per JEDEC STD-J-20C

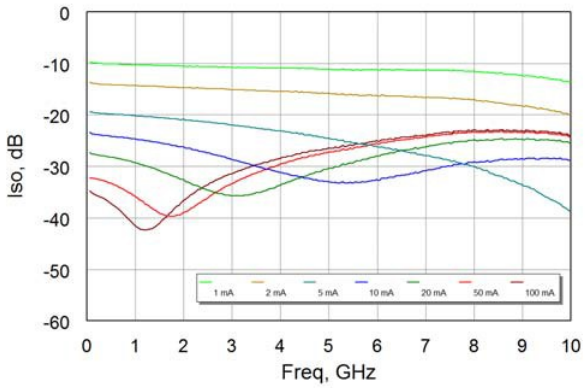
* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Typical Performance Curves

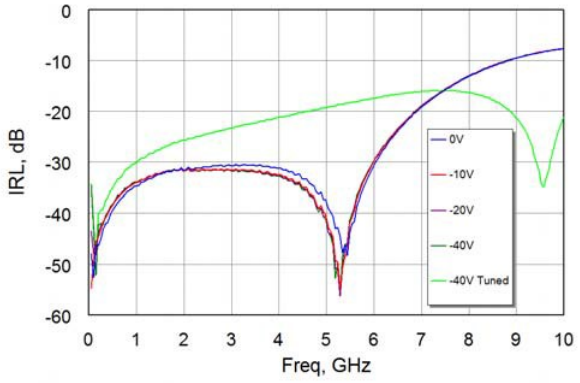
Insertion Loss



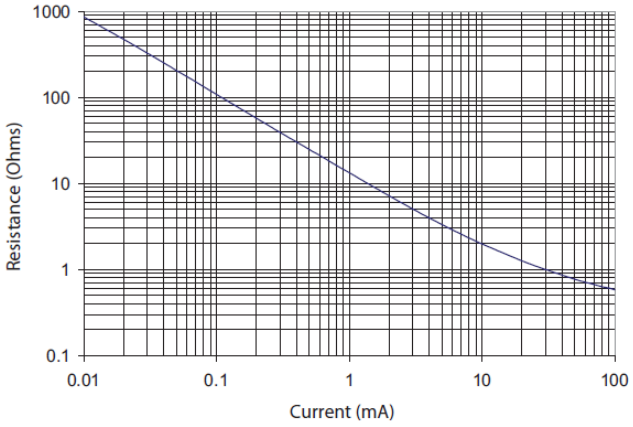
Isolation



Return Loss

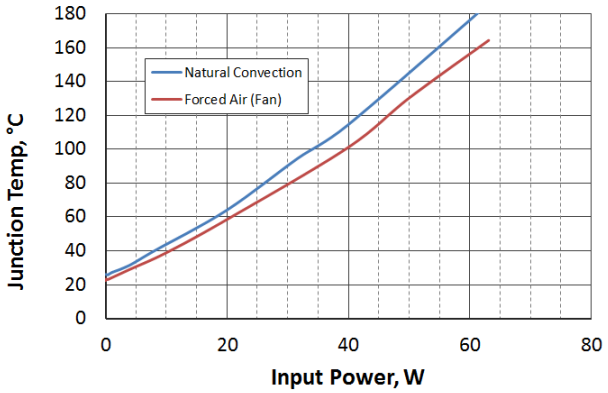


Resistance vs. Bias Current @ 500 MHz

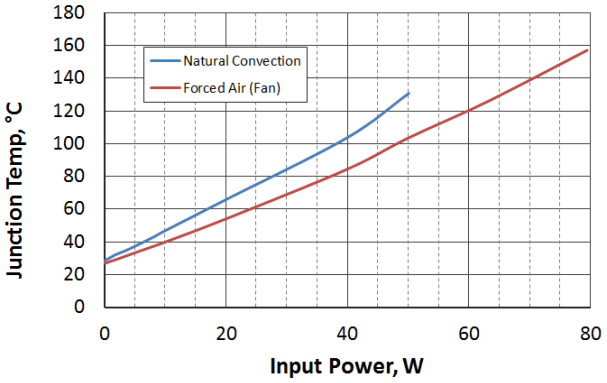


Typical Performance Curves

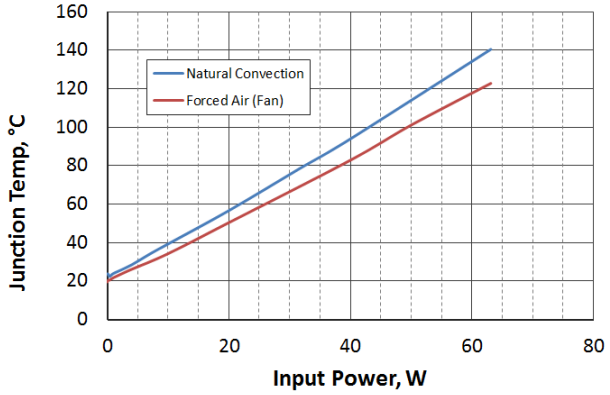
Junction Temperature vs. Input Power
PCB[1] Mounted on Heat Sink
T_A = 25°C, 1.3 GHz, 50 mA Bias



Junction Temperature vs. Input Power
PCB[1] Mounted on Heat Sink
T_A = 25°C, 1.3 GHz, 100 mA Bias

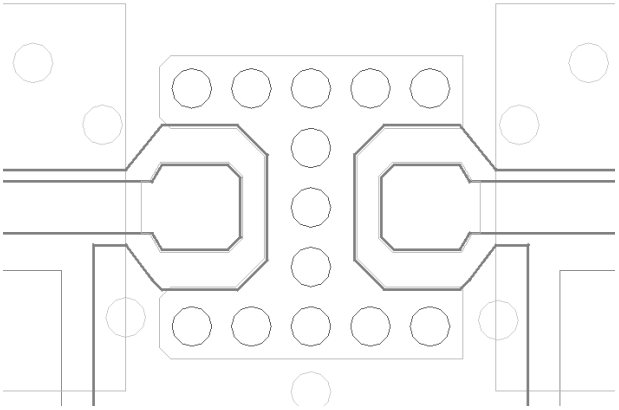


Junction Temperature vs. Input Power
PCB[1] Mounted on Heat Sink
T_A = 25°C, 1.3 GHz, 200 mA Bias



1. 20 mils Rogers RO4350B with 1 oz. copper clad and copper plated thru 10 mil diameter vias under package thermal ground.

Printed Circuit Board Layout



For RF ground and thermal vias use copper filled and plated over 10 mil diameter vias on 17 mil centers.

Solder mask should provide 60 µm clearance between copper pad and solder mask. Rounded package pads should have matching rounded solder mask openings. On the outer edges of package, use 100 µm clearance.

For the solder paste stencil design, use circles or squares such that only get 60 to 80% solder paste coverage.

Outline (CM35)