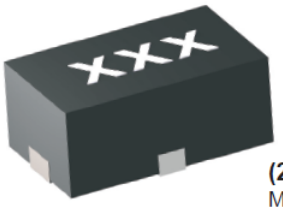
MSWSSB-020-30

PIN Diode Shunt Switch Element

Rev. V1

Features

- Supports up to 20 watt
- Low Insertion Loss 0.3 dB @ 2.7 GHz
- Low Insertion Loss 0.4 dB @ 10.0 GHz
- High Isolation 55 dB @ 2.7 GHz
- High Isolation 33 dB @ 10.0 GHz
- RoHS* Compliant



(2012)
Molden Plastic DFN

Description

A broadband, high linearity medium power series shunt switch element in a plastic 1.9 x 1.1 mm DFN package.

This device is designed for wireless telecommunication infrastructure and test instrument applications. It is also suited for other applications in 0.1 ~ 10 GHz.

Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Breakdown Voltage	I_R = 10 mA	200	—	—	V
Junction Capacitance	V_R = 50 V, F = 1 MHz Shunt Series	—	0.26 0.048	—	pF
Series Resistance	I_F = 100 mA, F = 500 MHz Shunt Series	—	0.40 0.98	—	Ohms
Lifetime	I_F = 10 mA, I_R = 6 mA , 10%/90% Shunt Series	—	4300 150	8000 250	ns
Insertion Loss	I = -50 mA[1] F = 2.3 ~ 2.7 GHz F = <10 GHz	—	0.3 0.6	0.5 0.8	dB
Input Return Loss	I = -50 mA[1] F = 2.3 ~ 2.7 GHz F = <10 GHz	20 15	25 20	—	dB
Output Return Loss	I = -50 mA[1] F = 2.3 ~ 2.7 GHz F = <10 GHz	20 15	25 18	—	dB
Isolation	I = -50 mA[1] F = 2.3 ~ 2.7 GHz F = <10 GHz	45 28	55 35	—	dB

1. Positive current is defined as current going into pin 2.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

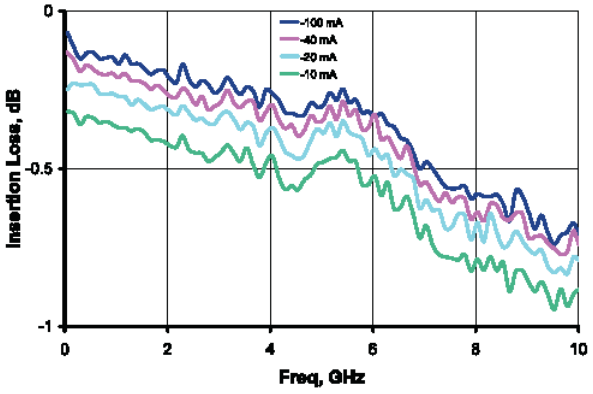
Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Breakdown Voltage	200 V
Forward Current	100 mA
Input Power	20 W CW
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C
Solder Temperature	+260°C per JEDEC STD-J-20C

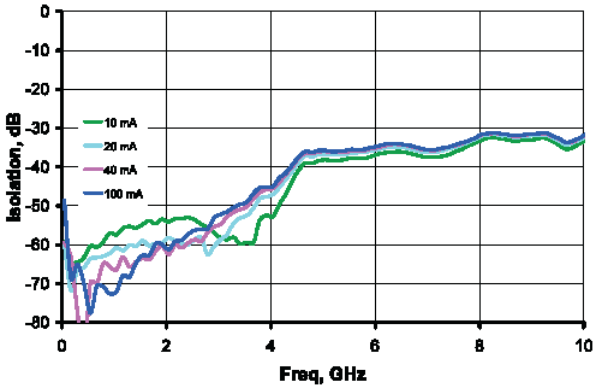
3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Typical RF Performance Curves @ +25°C

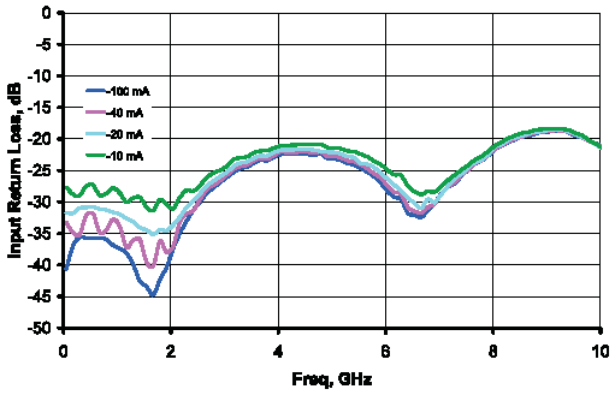
Insertion Loss



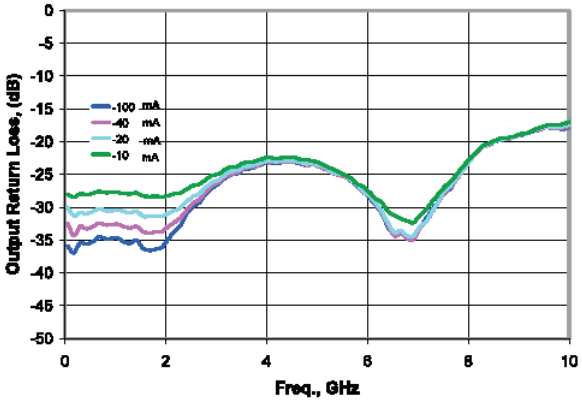
Isolation



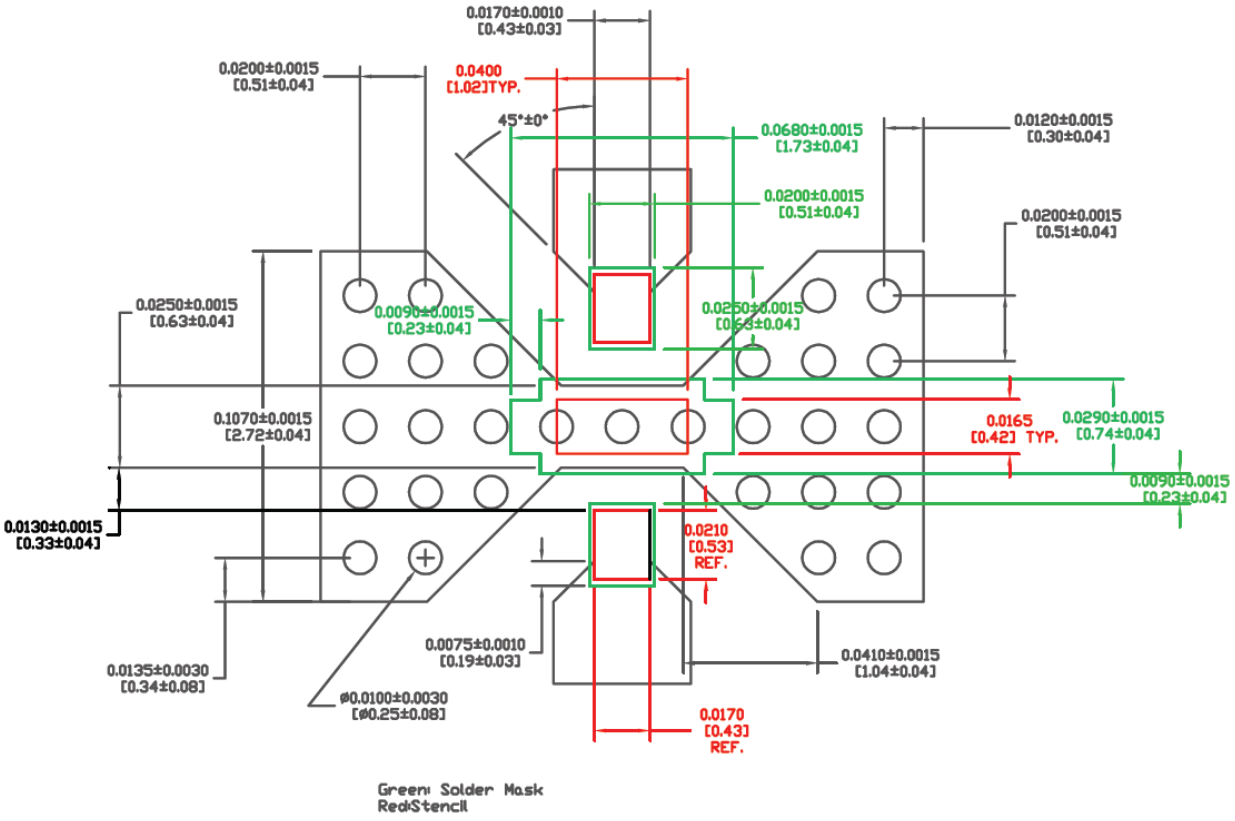
Input Return Loss



Output Return Loss



Printed Circuit Board Layout



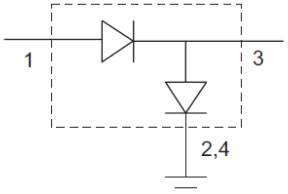
Assembly

If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

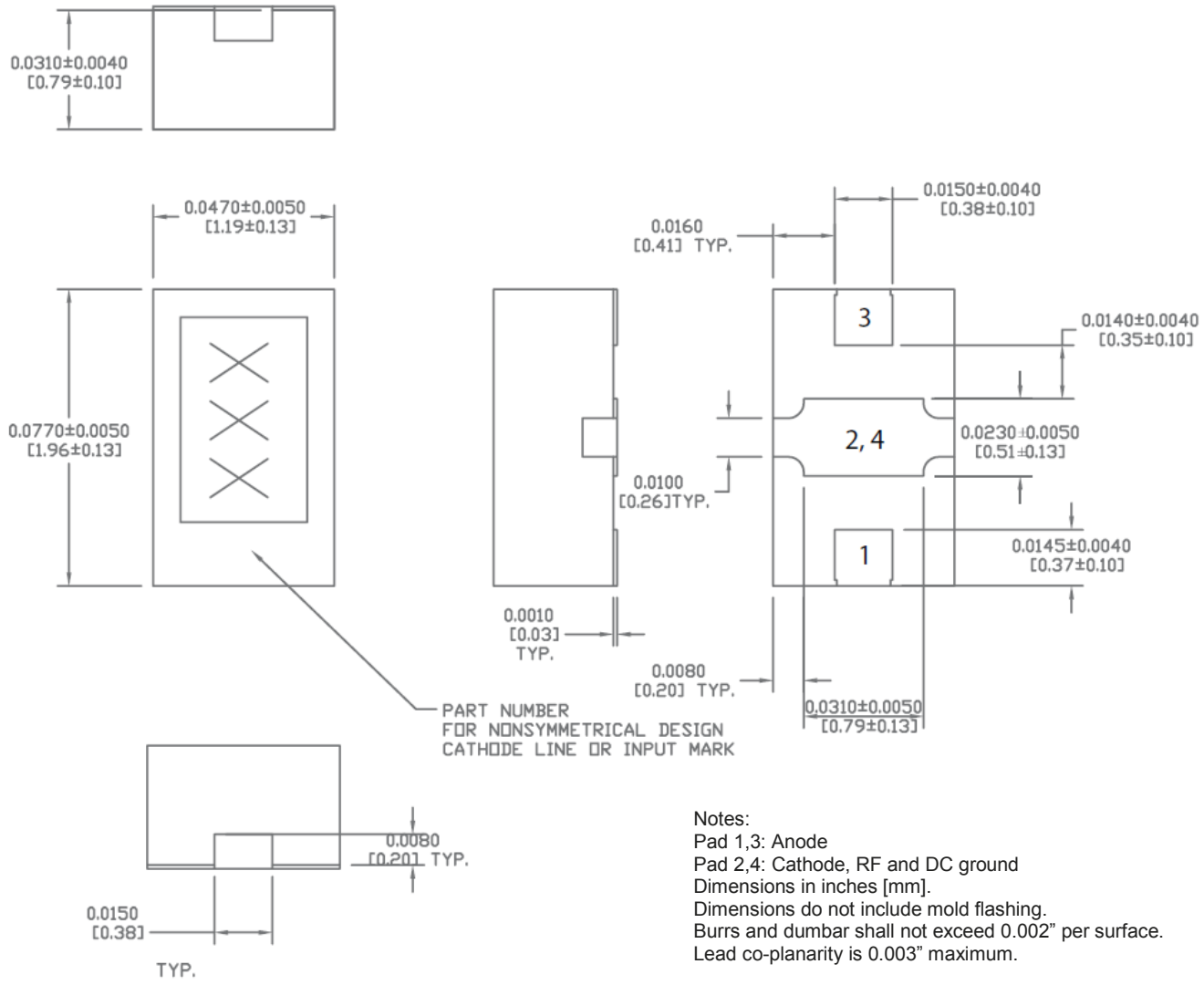
Solder mask should provide a 60 µm clearance between copper pad and solder mask underneath package and 125 µm clearance on outside edges of package. Rounded package pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that there is only 50% to 80% solder paste coverage.

Electrical Schematic



Outline: 2012 (molded plastic DFN)



Notes:
Pad 1,3: Anode
Pad 2,4: Cathode, RF and DC ground
Dimensions in inches [mm].
Dimensions do not include mold flashing.
Burrs and dumbar shall not exceed 0.002” per surface.
Lead co-planarity is 0.003” maximum.