DRAM MODULE

MT8D132(X)
MT16D232(X)

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single in-line memory module (SIMM)
- 4MB (1 Meg x 32) and 8MB (2 Meg x 32)
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Multiple RAS# lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode

OPTIONS — MARKING

- Timing
  60ns access — -6
- Packages
  72-pin SIMM — M
  72-pin SIMM (gold) — G
- Operating Modes
  FAST PAGE MODE — Blank
  EDO PAGE MODE — X

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	PLATING
MT8D132G-xx X	1 Meg x 32	Gold
MT8D132M-xx X	1 Meg x 32	Tin/Lead
MT16D232G-xx X	2 Meg x 32	Gold
MT16D232M-xx X	2 Meg x 32	Tin/Lead

xx = speed

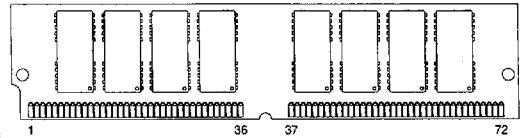
FPM Operating Mode

PART NUMBER	CONFIGURATION	PLATING
MT8D132G-xx	1 Meg x 32	Gold
MT8D132M-xx	1 Meg x 32	Tin/Lead
MT16D232G-xx	2 Meg x 32	Gold
MT16D232M-xx	2 Meg x 32	Tin/Lead

xx = speed

PIN ASSIGNMENT (Front View)

72-Pin SIMM
(DD-3) 1 Meg x 32
(DD-4) 2 Meg x 32



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	NC (A10)	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0#	58	DQ29
5	DQ18	23	DQ22	41	CAS2#	59	Vcc
6	DQ3	24	DQ7	42	CAS3#	60	DQ30
7	DQ19	25	DQ23	43	CAS1#	61	DQ14
8	DQ4	26	DQ8	44	RAS0#	62	DQ31
9	DQ20	27	DQ24	45	NC*/RAS1#	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC (A11)	47	WE#	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC*/RAS3#	51	DQ10	69	PRD3
16	A4	34	RAS2#	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*4MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	26ns	30ns	17ns	13ns

FPM Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

GENERAL DESCRIPTION

The MT8D132(X) and MT16D232(X) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits. A READ or WRITE cycle is selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. EARLY WRITE occurs when WE# goes LOW prior to CAS# going LOW, and the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. (Reference MT4C4007J DRAM data sheet for additional information on EDO functionality.)

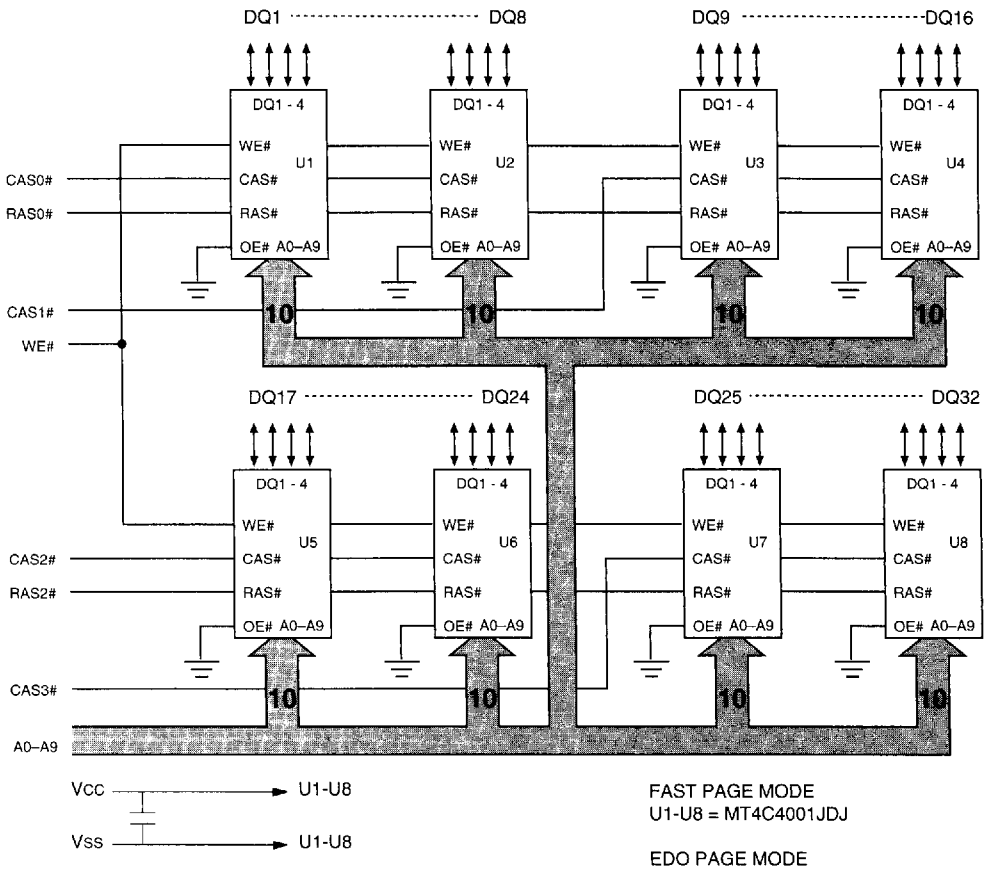
REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR or HIDDEN) so that all 1,024 combination of RAS# addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS# pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0# to CAS2# and CAS1# to CAS3#). Each RAS# is then a bank select for the x16 memory organization.

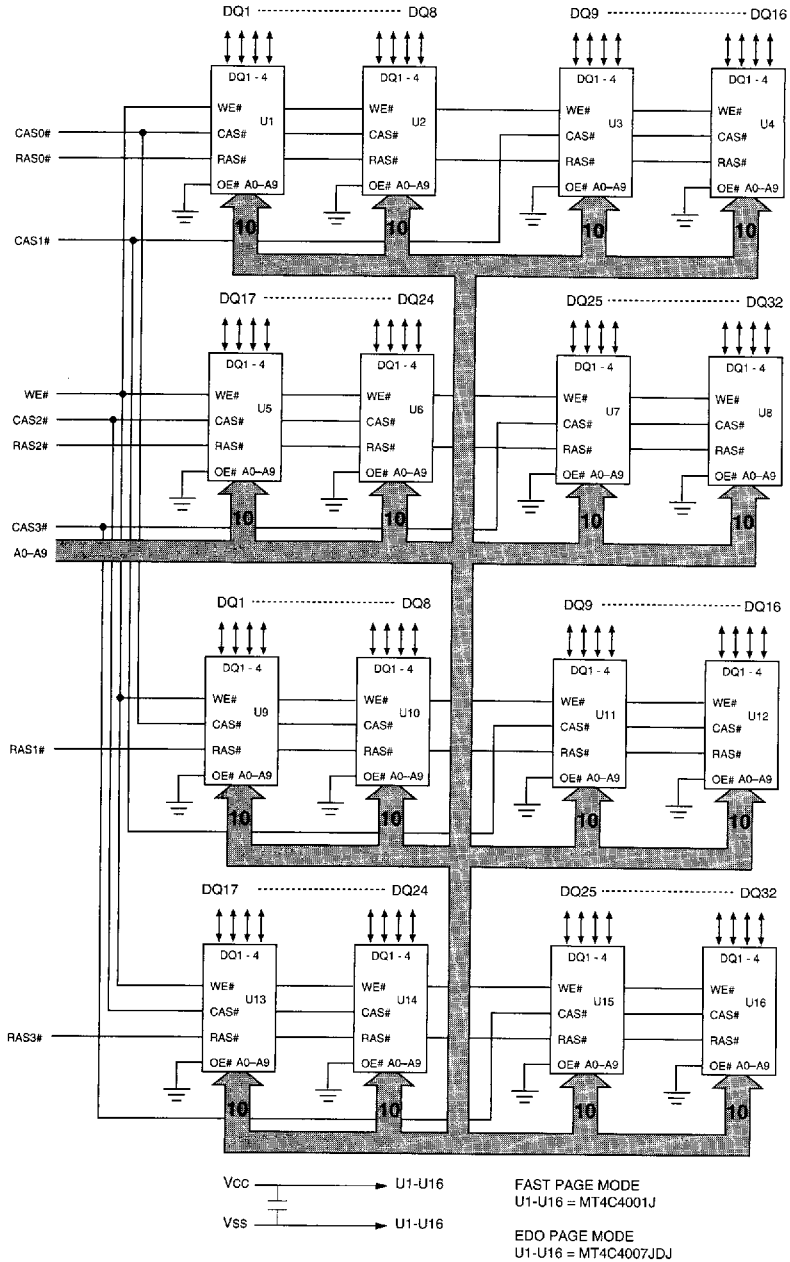
FUNCTIONAL BLOCK DIAGRAM
MT8D132(X) (4MB)



FAST PAGE MODE
U1-U8 = MT4C4001JDJ

EDO PAGE MODE
U1-U8 = MT4C4007JDJ

FUNCTIONAL BLOCK DIAGRAM
MT16D232(X) (8MB)



FAST PAGE MODE
U1-U16 = MT4C4001J

EDO PAGE MODE
U1-U16 = MT4C4007JDJ

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS#-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

JEDEC-DEFINED PRESENCE-DETECT – MT8D132(X) (4MB)

SYMBOL	PIN	-6
PRD1	67	Vss
PRD2	68	Vss
PRD3	69	NC
PRD4	70	NC

JEDEC-DEFINED PRESENCE-DETECT – MT16D232(X) (8MB)

SYMBOL	PIN	-6
PRD1	67	NC
PRD2	68	NC
PRD3	69	NC
PRD4	70	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc +1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	CAS0#-CAS3#	II1	-8	8	µA	23
Any input 0V ≤ VIN ≤ Vcc +1V	A0-A9, WE#	II2	-32	32	µA	23
(All other pins not under test = 0V)	RAS0#-RAS3#	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ32	IOZ	-20	20	µA	23
OUTPUT LEVELS		VOH	2.4		V	
High Voltage (IOUT = -5mA)		VOL		0.4	V	
Low Voltage (IOUT = 4.2mA)						

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = VIH)	ICC1	4MB 8MB	16 32	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = other inputs = Vcc -0.2V)	ICC2	4MB 8MB	8 16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: tRC = tRC [MIN])	ICC3	4MB 8MB	880 896	mA	2, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = VIL, CAS#, address cycling: tPC = tPC [MIN])	ICC4	4MB 8MB	640 656	mA	2, 22
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = VIL, CAS#, address cycling: tPC = tPC [MIN])	ICC5 (X only)	4MB 8MB	640 656	mA	2
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = VIH: tRC = tRC [MIN])	ICC6	4MB 8MB	880 896	mA	2, 22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: tRC = tRC [MIN])	ICC7	4MB 8MB	880 896	mA	2, 17

DRAM SIMM

6111549 0019947 953

CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	48	95	pF	15
Input Capacitance: WE#	C_{I2}	64	127	pF	15
Input Capacitance: RAS0#-RAS3#	C_{I4}	32	32	pF	15
Input Capacitance: CAS0#-CAS3#	C_{I5}	16	32	pF	15
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	18	pF	15

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 3, 4, 5, 6, 7, 8, 9, 14) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR REFRESH)	^tCHR	10		ns	17
CAS# to output in Low-Z	^tCLZ	0		ns	
CAS# precharge time	^tCP	10		ns	16
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	10		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR REFRESH)	^tCSR	10		ns	17
Write command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	13
Data-in setup time	^tDS	0		ns	13
Output buffer turn-off delay	^tOFF	3	15	ns	10, 21, 24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	20
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	11
Read command hold time (referenced to CAS#)	^tRCH	0		ns	12
Read command setup time	^tRCS	0		ns	
Refresh period (1,024 cycles)	^tREF		16	ms	
RAS# precharge time	^tRP	40		ns	
RAS# to CAS# precharge time	^tRPC	0		ns	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 3, 4, 5, 6, 7, 8, 9, 14) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command hold time	^{t}RRH	0		ns	12
RAS# hold time	^{t}RSH	15		ns	
Write command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	3	50	ns	
Write command hold time	^{t}WCH	10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	
Write command pulse width	^{t}WP	10		ns	
WE# hold time (CBR REFRESH)	^{t}WRH	10		ns	
WE# setup time (CBR REFRESH)	^{t}WRP	10		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

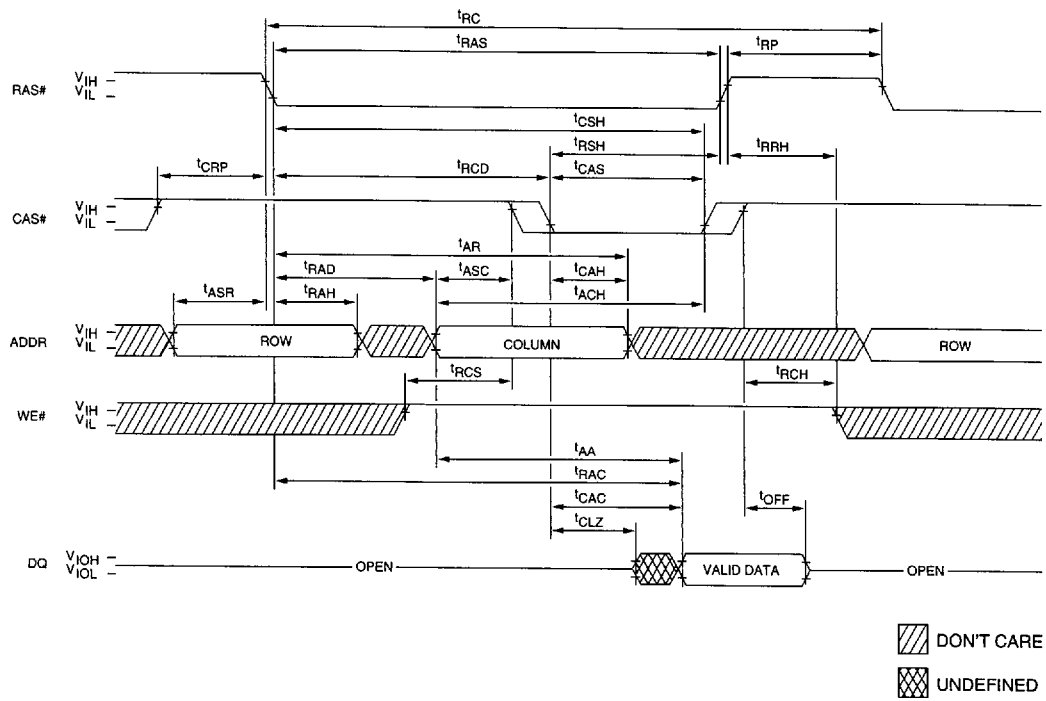
(Notes: 3, 4, 5, 6, 7, 8, 9, 14) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		30	ns	
Column-address setup to CAS# precharge during WRITE	^tACH	15		ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Access time from CAS#	^tCAC		17	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	13	10,000	ns	
CAS# hold time (CBR REFRESH)	^tCHR	10		ns	17
CAS# to output in Low-Z	^tCLZ	3		ns	21
Data output hold after CAS# LOW	^tCOH	5		ns	
CAS# precharge time	^tCP	10		ns	16
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	10		ns	
CAS# hold time	^tCSH	50		ns	
CAS# setup time (CBR REFRESH)	^tCSR	10		ns	17
Write command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	9		ns	13
Data-in setup time	^tDS	0		ns	13
Output buffer turn-off delay	^tOFF	3	15	ns	10, 21, 24
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	26		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	20
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	11
Read command hold time (referenced to CAS#)	^tRCH	0		ns	12
Read command setup time	^tRCS	0		ns	
Refresh period (1,024 cycles)	^tREF		16	ms	
RAS# precharge time	^tRP	40		ns	
RAS# to CAS# precharge time	^tRPC	5		ns	
Read command hold time	^tRRH	0		ns	12
RAS# hold time	^tRSH	15		ns	
Write command to RAS# lead time	^tRWL	15		ns	
Transition time (rise or fall)	^tT	1.5	50	ns	5, 14
Write command hold time	^tWCH	10		ns	
Write command hold time (referenced to RAS#)	^tWCR	45		ns	
WE# command setup time	^tWCS	0		ns	
Output disable delay from WE# (CAS# HIGH)	^tWHZ	3	15	ns	
Write command pulse width	^tWP	10		ns	
WE# pulse width for output disable when CAS# HIGH	^tWPZ	10		ns	
WE# hold time (CBR REFRESH)	^tWRH	10		ns	
WE# setup time (CBR REFRESH)	^tWRP	10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns for FAST PAGE MODE and ^{t}T = 1.5ns for EDO PAGE MODE.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. If CAS# and RAS# = V_{IH}, data output is High-Z.
9. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
10. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
12. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
13. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
14. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
15. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 4.5V, DC bias = 2.4V at 15mV RMS).
16. If CAS# is LOW at the falling edge of RAS#, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
17. On-chip refresh and address counters are enabled.
18. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW.
19. LATE WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE# being grounded on U1-U8/U16.
20. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 4MB module values will be half of those shown.
24. For FAST PAGE MODE option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
25. Applies to both EDO and FAST PAGE MODEs.

READ CYCLE [25]

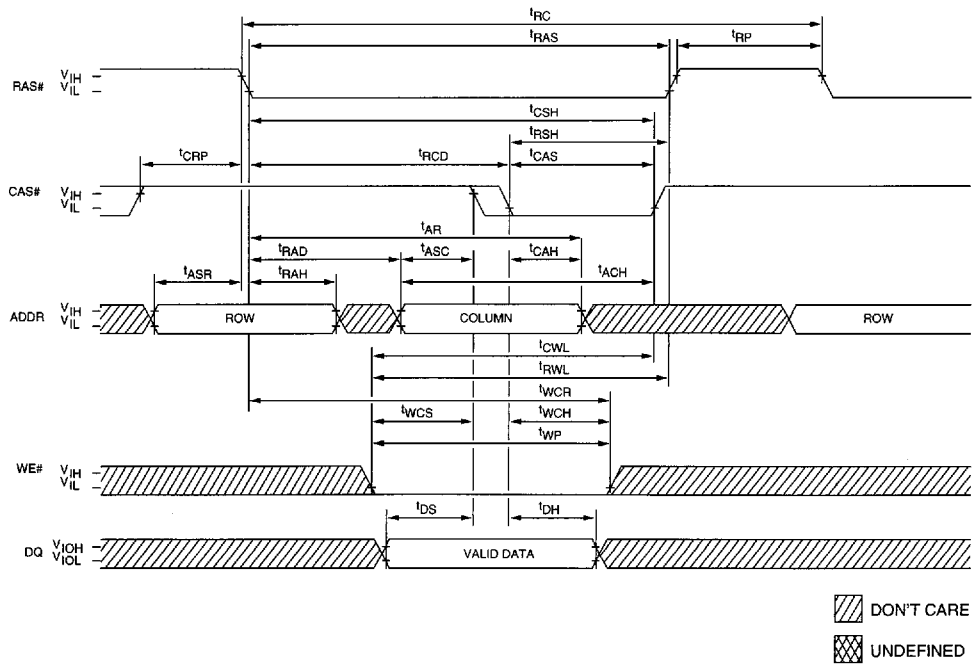


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tACH	15		ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC (FPM)		15	ns
tCAC (EDO)		17	ns
tCAH	10		ns
tCAS (FPM)	15	10,000	ns
tCAS (EDO)	13	10,000	ns
tCLZ (FPM)	0		ns
tCLZ (EDO)	3		ns
tCRP	10		ns
tCSH (FPM)	60		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tCSH (EDO)	50		ns
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EARLY WRITE CYCLE [25]



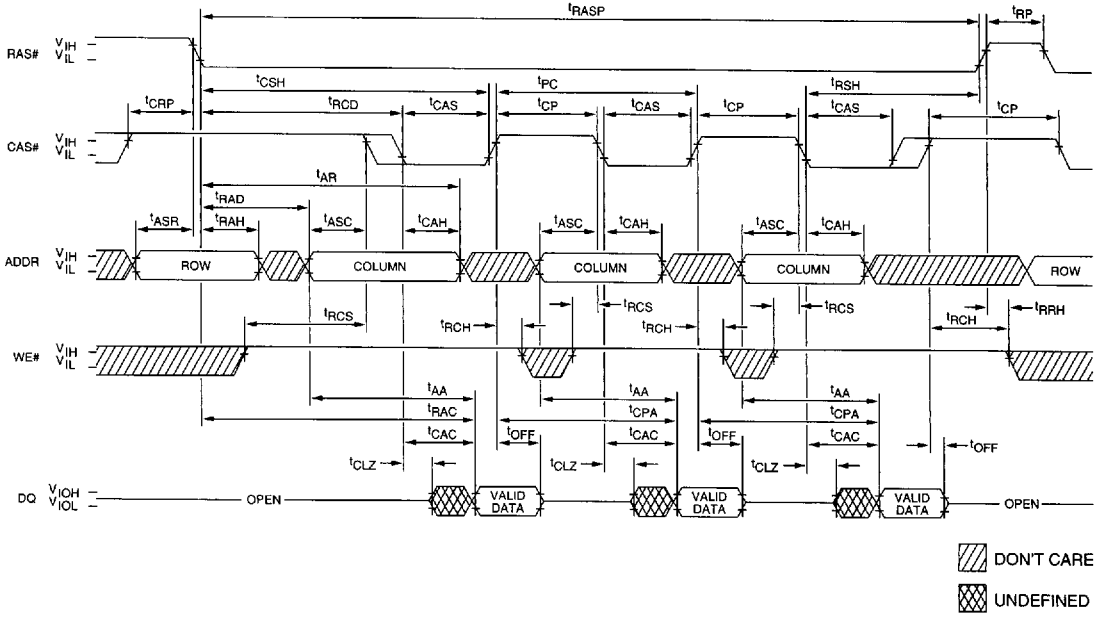
DRAM SIMM

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tACH (EDO)	15		ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS (FPM)	15	10,000	ns
tCAS (EDO)	13	10,000	ns
tCRP	10		ns
tCSH (FPM)	60		ns
tCSH (EDO)	50		ns
tCWL	15		ns
tDH (FPM)	10		ns
tDH (EDO)	9		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tDS	0		ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ CYCLE

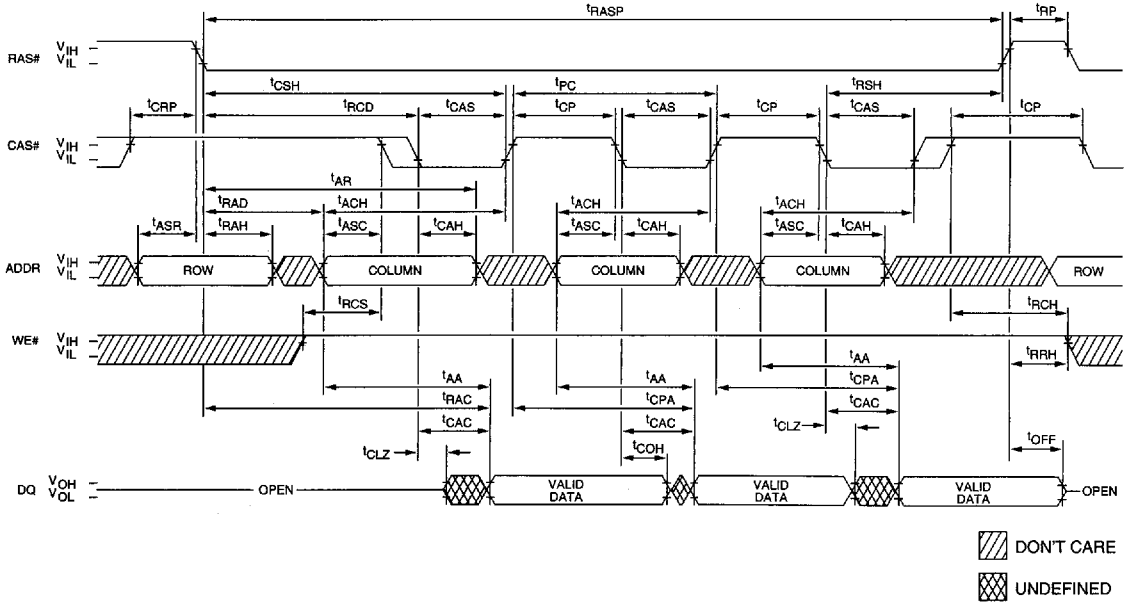


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EDO-PAGE-MODE READ CYCLE



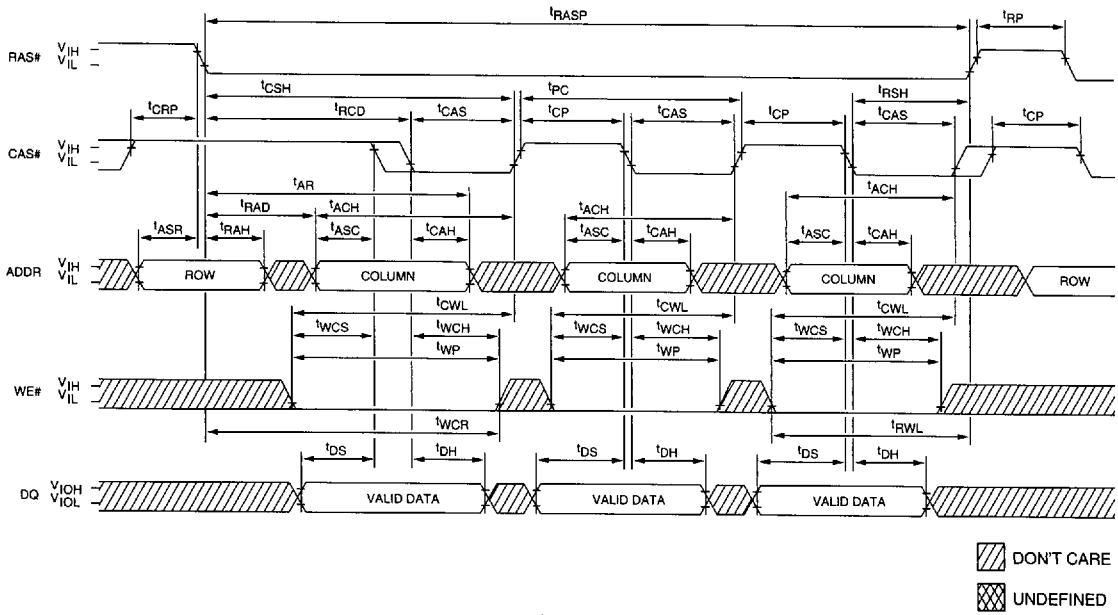
DRAM SIMM

EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		17	ns
tCAH	10		ns
tCAS	13	10,000	ns
tCLZ	3		ns
tCOH	5		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	50		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	26		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST/EDO-PAGE-MODE EARLY-WRITE CYCLE [25]

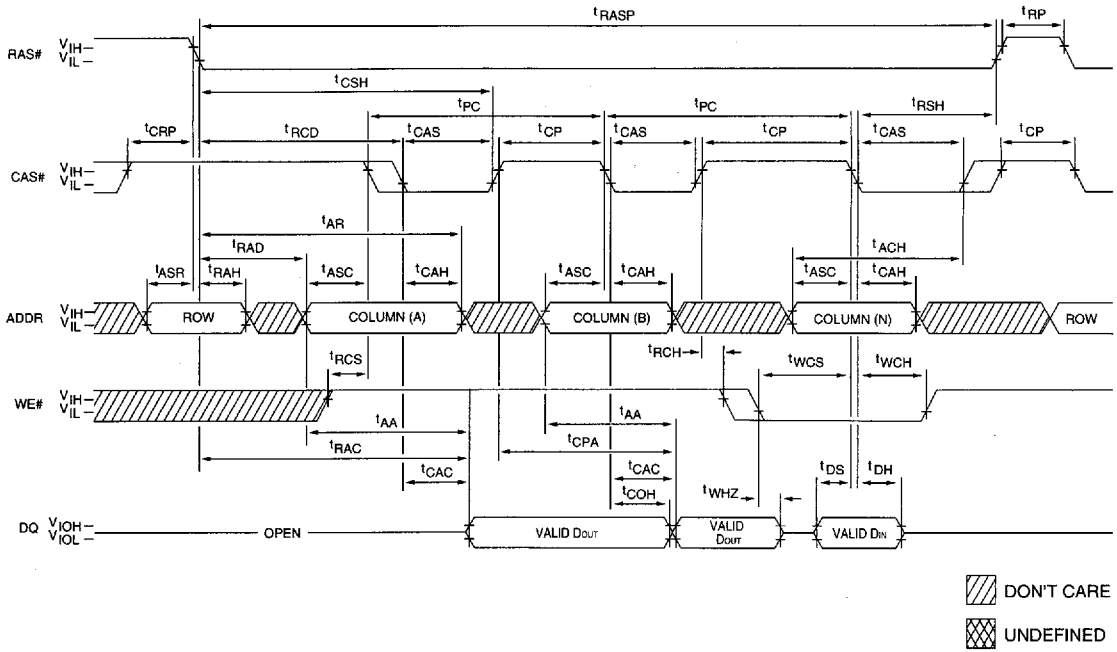


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS (FPM)	15	10,000	ns
tCAS (EDO)	13	10,000	ns
tCP	10		ns
tCRP	10		ns
tCSH (FPM)	60		ns
tCSH (EDO)	50		ns
tCWL	15		ns
tDH (FPM)	10		ns
tDH (EDO)	9		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tPC (FPM)	35		ns
tPC (EDO)	26		ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



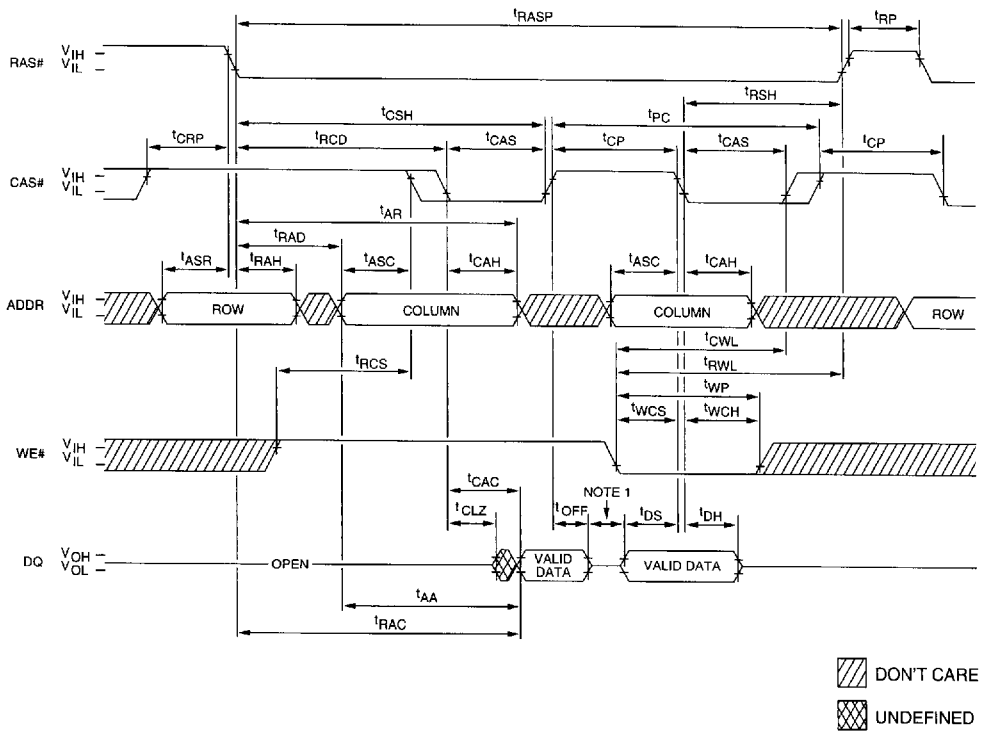
DRAM SIMM

EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tACH	15		ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		17	ns
tCAH	10		ns
tCAS	13	10,000	ns
tCOH	5		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	50		ns
tDH	9		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tDS	0		ns
tPC	26		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tWCH	10		ns
tWCS	0		ns
tWHZ	3	15	ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



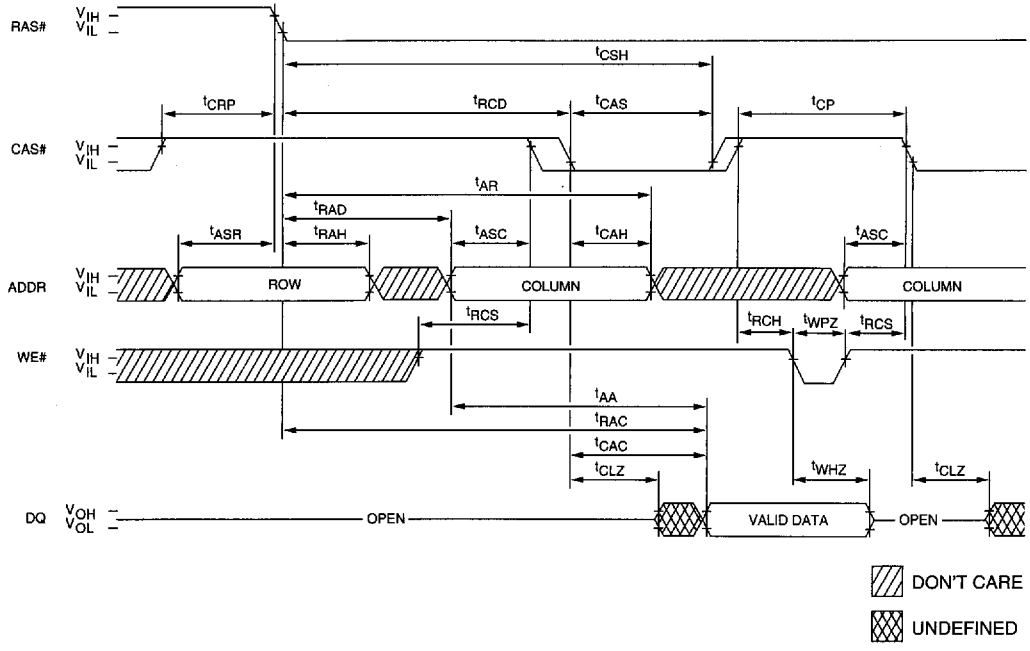
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	0		ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

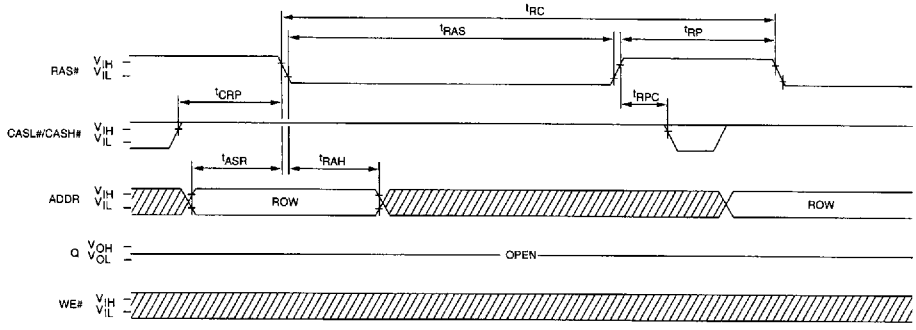


EDO PAGE MODE TIMING PARAMETERS

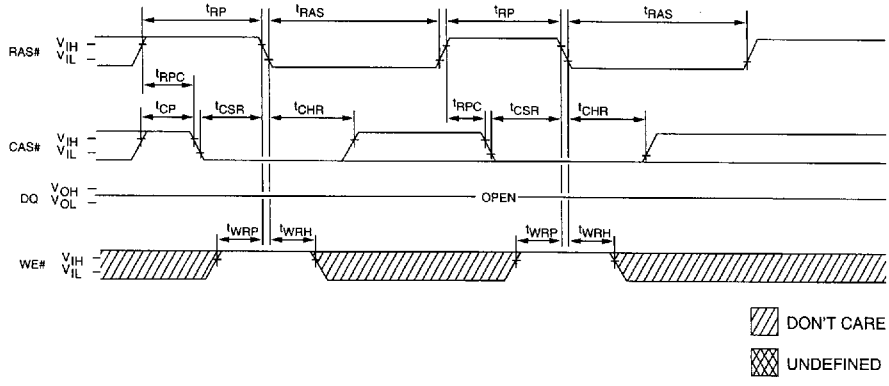
SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		17	ns
tCAH	10		ns
tCAS	13	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tCSH	50		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tWHZ	3	15	ns
tWPZ	10		ns

RAS#-ONLY REFRESH CYCLE [25]



CBR REFRESH CYCLE [25]
(Addresses = DON'T CARE)

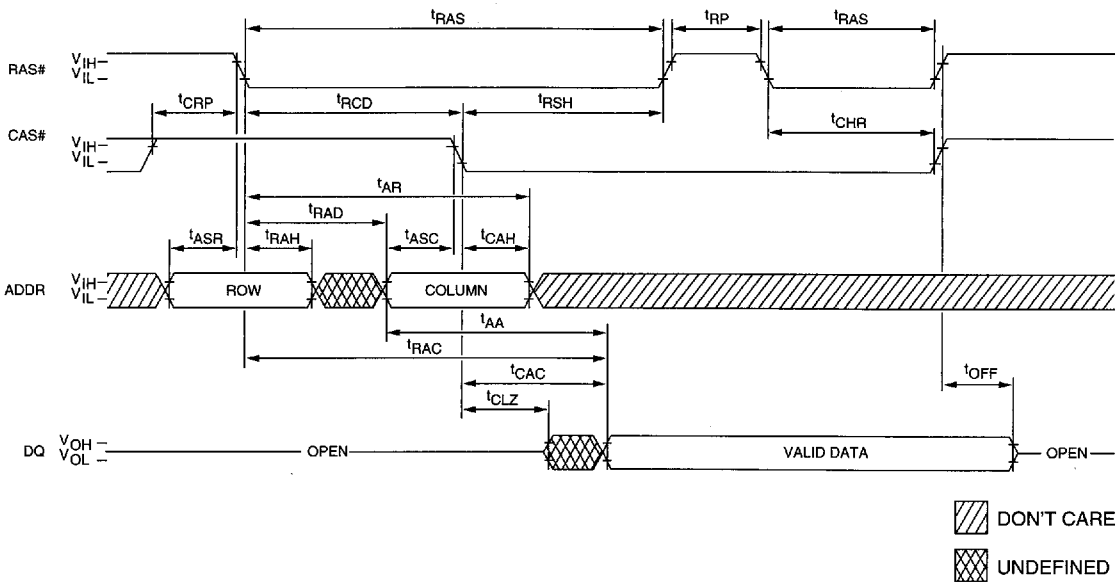


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tASR	0		ns
tCHR	10		ns
tCP	10		ns
tCRP	10		ns
tCSR	10		ns
tRAH	10		ns
tRAS	60	10,000	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRC	110		ns
tRP	40		ns
tRPC (FPM)	0		ns
tRPC (EDO)	5		ns
tWRH	10		ns
tWRP	10		ns

HIDDEN REFRESH CYCLE [18, 25]
(WE# = HIGH)



DRAM SIMM

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC (FPM)		15	ns
tCAC (EDO)		17	ns
tCAH	10		ns
tCHR	10		ns
tCLZ	3		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tCRP	10		ns
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns