Evaluation of ceramic resonator oscillation characteristics

This paper is prepared to explain characteristics, test methods, and glossary of the oscillation circuit composed of a CMOS inverter and ceramic resonator.

(A) Test samples

[Ceramic resonators]

We use the following two samples for evaluation:

Typical sample:	sample with average resonant impedance, (TYP.)
Worst sample:	sample with worst resonant impedance, (WST.)

[IC]

In case of providing random IC samples from IC manufacturers.

IC dependence :	Test all samples at room temperature.
Temperature dependence:	Test sample with worst oscillation start voltage.
Power supply dependence:	Test sample with worst oscillation start voltage.
Open loop characteristics:	Test sample with worst oscillation start voltage.

By combining these samples(ceramic resonator and IC),
you can find the typical and worst characteristics of the oscillation circuit.

(B) CMOS inverter characteristics

Measure a CMOS inverter's gain vs. frequency characteristics to check on the gain margin.

(C) Oscillation characteristics

Fig. 1 shows a basic oscillation circuit composed of a CMOS inverter and ceramic resonator.
Each character represents the following.

CL1:	Input Loading Capacitor
CL2:	Output Loading Capacitor
Rf:	Feedback Resistor (Some Ics have built-in feedback resistor)
Rd:	Damping Resistor
V_{DD}:	Power Supply Voltage
(T_A:	Ambient Temperature)

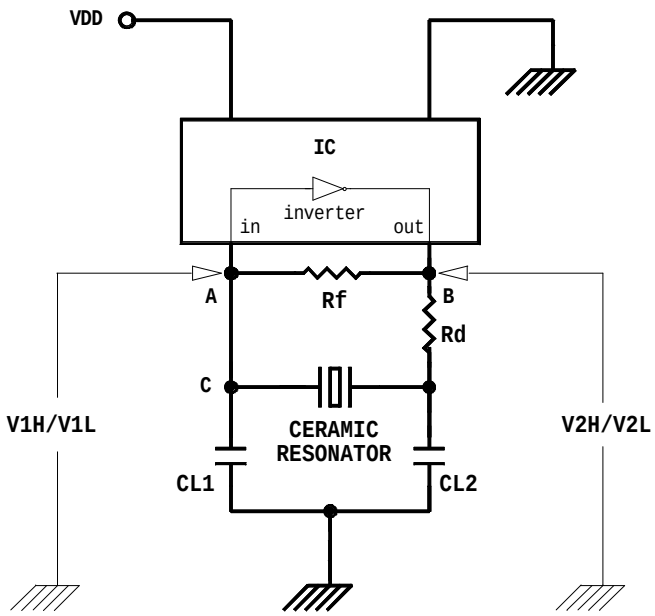


Fig. 1 Basic oscillation circuit using a CMOS inverter

Evaluate the circuit with the following factors:

(1) Oscillating levels (V_{1H}/V_{1L}, V_{2H}/V_{2L})
(2) Oscillating frequency change ratio ($\Delta Fosc/Fosc$)
(3) Oscillation start voltage (Vstart)
(4) Oscillation hold voltage (Vhold)
(5) Oscillating rise time (Trise)
(6) Duty ratio (Duty)

c-1 **Oscillating levels** (V_{1H}/V_{1L}, V_{2H}/V_{2L})

V_1 and V_2 represent input and output oscillating voltages respectively.
V_{1H}/V_{1L} and V_{2H}/V_{2L} represent the high and low voltage levels of V_1 and V_2.
Measure oscillation levels by applying high impedance probes(10Mohm//2pF).

c-2 **Oscillating frequency change ratio** ($\Delta Fosc/Fosc$)

Oscillating frequency is measured with a frequency counter at a clock out terminal. For an IC without this terminal, measure directly the output oscillating voltage (V_2), and calculate the change ratio.

c-3 **Oscillation start voltage** (Vstart)

Gradually increasing the power supply voltage (V_{DD}) in the state of no-oscillation, determine the minimum power supply voltage of starting oscillation.

c-4 **Oscillation hold voltage** (Vhold)

Gradually decreasing the power supply voltage (V_{DD}) in the state of oscillation, determine the minimum power supply voltage of holding oscillation.

c-5 **Oscillating rise time** (Trise)

An oscillating rise time is the time that the output voltage level becomes 80% of stable state after step voltage with a several nanosecond rise time is applied to IC as shown in Fig. 2.

c-6 **Duty ratio** (Duty)

Duty is the ratio of exceeding half the value of V_{PP} to the period as shown in Fig. 3, expressed as a percentage.

V_{PP} represent the voltage difference between the maximum and minimum voltage.

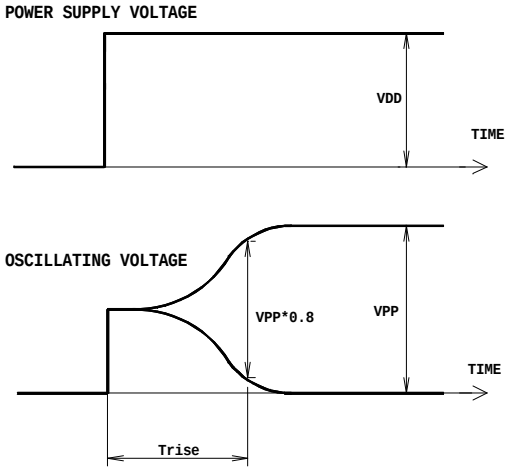
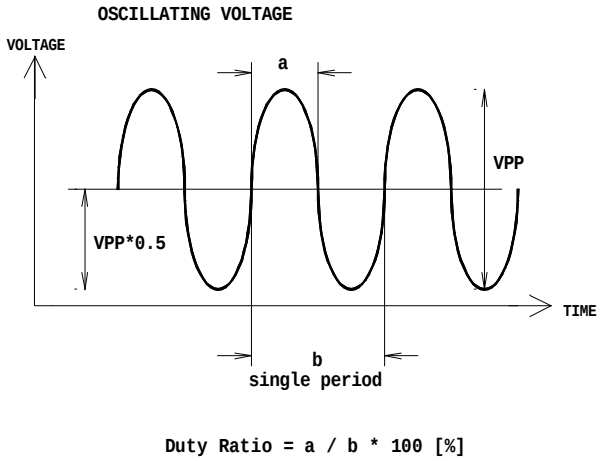


Fig. 2 Oscillation rise time



Duty Ratio = a / b * 100 [%]

Fig. 3 Duty ratio

(D) IC dependence

Measure oscillation characteristics on all IC samples with the typical ceramic resonator at room temperature.

Call the IC with the highest oscillation start voltage the worst sample.

(E) Damping resistance/Loading capacitance dependence

Measure damping resistance and loading capacitance dependence of oscillating characteristics to optimize the circuit conditions.

(F) Power supply voltage dependence

Measure power supply voltage dependence of oscillating characteristics.
Power supply voltage conform to the IC's recommended operating range.

(G) Ambient temperature dependence

Measure ambient temperature dependence of oscillating characteristics.
Ambient temperature conform to the IC's recommended operating range.

(H) Oscillating frequency correlation

Determine the evaluated IC's oscillating frequency relative to that of TDK's standard circuit.
(HEX CMOS INVERTER 4069UBP/74HCU04 type).

(I) Open loop characteristics

For the oscillation circuit, the following two conditions are necessary:

(1) Loop gain $\geq$ 0 dB
(2) Loop phase = 360° x n (n: integer)

The oscillating conditions cannot be evaluated on a continuing basis.

(1) Information about oscillation is not available when the circuit does not oscillate.
(2) Information about modes other than the desired is not obtainable.

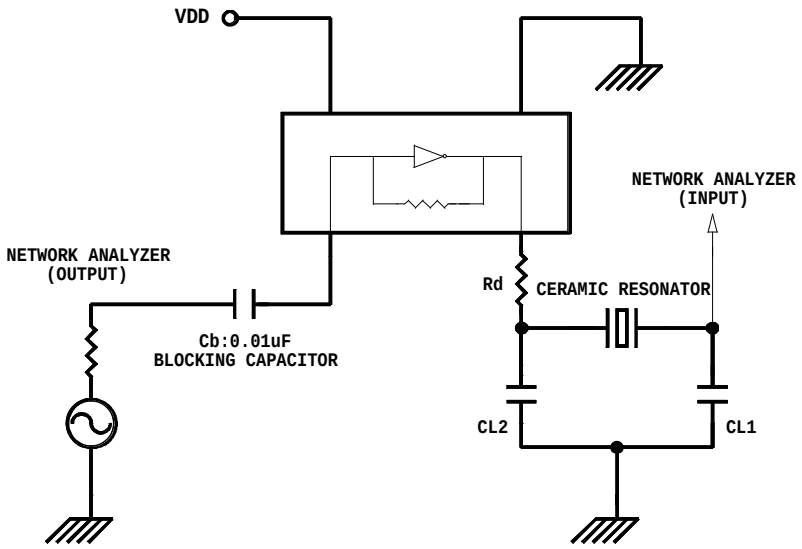


Fig. 4 Open loop circuit for oscillation circuit analysis

Therefore, cut the circuit between points A and C to get an open loop circuit as shown in Fig. 4. This permits measurment of responses to an external input signal and evaluation of the continuous oscillating conditions.

Conditions for judging oscillation are;(as shown in Fig. 5)

(1) Loop gain margin for C-A must be greater than 0 dB at a particular frequency where C-A loop phase is -360°.

(2) Loop phase margin for C-A must be less than -360° at a particular frequency where C-A loop gain is 0 dB.

Use the above measurement methods and oscillation conditions to check on the desired mode oscillation margin and spurious mode oscillation capability.
We recommend the best circuit condition; a stable oscillation is guaranteed.

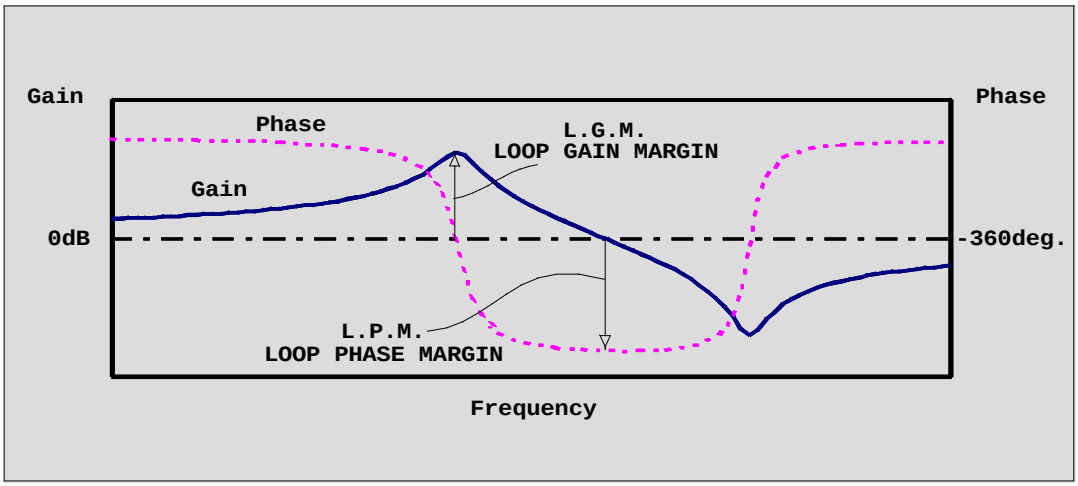


Fig. 5 Open loop characteristics