MT1389G

High Definition DVD Player SOC with HDMI™ Tx

Approval Sheet

Version 1.0

Specifications are subject to change without notice

Revision History

Revised date	Contents of revision	Reason for revision	Page	Remarks
2009 4 9	1st Release	Initial Version		Ver 1.0

Contents of Specifications

1 Applications

This present specifications are applied to IC MT1389G.

2 Type

MT1389G

3 Usage

High Definition DVD Player SOC with HDMI™[1] Tx

4 Structure

0.13um CMOS process, Silicon material, Monolithic IC, 128pin LQFP with EPAD, 3.3/1.2 Dual operation voltages.

[1] "HDMI™, the HDMI™ logo and High-Definition Multimedia Interface are trademarks or registered trademark of HDMI™ Licensing LLC."

5 Function

5-1 General Description

MediaTek MT1389G is a cost-effective DVD system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high quality TV encoder ,state-of-art de-interlace processing, and HDMI™ 1.3 compatible transmitter. The MT1389G enables consumer electronics manufacturers to build high quality, USB2.0, MS/SD/MMC reader, feature-rich DVD players, portable DVD players or any other home entertainment audio/video devices.

World-Leading Technology: Based on MediaTek's world-leading DVD player SOC architecture, the MT1389G is the New generation of the DVD player SOC. It integrates the MediaTek 3rd generation front-end digital RF amplifier and the Servo/MPEG AV decoder.

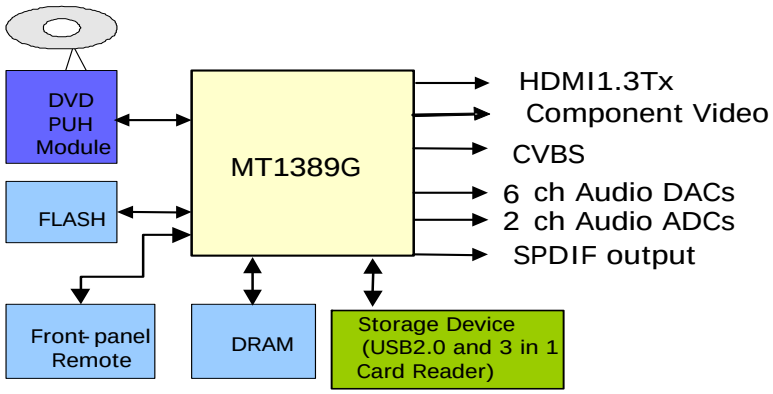
Enjoy the attractive video on digital TV: The most popular HDTV input format is HDMI™ interface and it provides up to 1080P high resolution video output and high quality audio output.

Rich Feature for High Valued Product: To enrich the feature of DVD player, the MT1389 equips a simplified MPEG-4 advanced simple profile (ASP) video decoder to fully support the DivX[2] Home Theater profile. It makes the MT1389-based DVD player be capable of playback MPEG-4 content which become more and more popular.

Incredible Audio/Video Quality: The progressive scan of the MT1389G utilized MediaTek's MDDi™ advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect. The 148MHz/12-bit video DACs provide users a whole new viewing experience. It also supports a 3:2 pull down algorithm to give the best film effect. Built-in 6ch audio DACs and 2ch audio ADCs could give the variable function solutions.

High Performance Memory Storage Device: As the core of Portable DVD players need more capability to support current multimedia contents. The MT1389G provides the interface for the 3-in-1 card reader, which supports Memory-Stick, Secure Digital Memory Card, and MultiMediaCard, to connect with the mainstream digital camera FLASH cards. For the USB application, we adopt USB2.0 High speed specification to reach rich-contents transference. USB 2.0 High speed will support for high-speed devices. USB 2.0 High Speed is suitable for high-performance devices such as high-density storage devices. In addition, USB 2.0 High Speed supports USB 1.0/1.1 devices, offering impressive and even better compatibility to customers

[2] DivX is a trademark of DivXNetworks
[3] USB High Speed : maximum 480Mbit/sec. USB Full Speed : maximum 12Mbit/sec.



DVD Player System Diagram

Key Features

RF/Servo/MPEG Integration

DivX Home Theater Level MPEG4 ASP Video decoder

Support DivX Ultra

High Performance Audio Processor

Progressive Scan

Internal 6CH Audio DAC

Internal 2CH Audio ADC

MDDi: Motion-Adaptive, Pure Edge™ De-interlacing

148MHz/12-bit TV Encoder

USB2.0 High Speed (Host)

3-in-1 MS/SD/MMC reader

HDMI™1.3 Tx with CEC support

USB2.0 High Speed (Host)

Applications

Standard DVD Players

5-2 Key Features

- RF/Servo/MPEG Integration
- Embedded 6ch Audio DAC
- Embedded 2ch Audio ADC for Karaoke
- High Performance Audio Processor
- High Performance Progressive Video Processor
- HDMI™1.3 Tx with CEC support
- MDDi: Motion-Adaptive, Pure Edge™ De-interlacing
- High Quality 148MHz/12-bit TV Encoder
- Support DivX Ultra
- USB 2.0 High-Speed

5-3 General Feature lists

- **Super Integration DVD player single chip**
  - High performance analog RF amplifier
  - Servo controller and data channel processing
  - MPEG-1/MPEG-2/JPEG video
  - Dolby AC-3/DTS Decoder
  - Unified memory architecture
  - Versatile video scaling & quality enhancement
  - OSD & Sub-picture
  - Built-in clock generator
  - Built-in progressive video processor
  - HDMI™1.3 Tx with CEC support
  - MDDi: Motion-Adaptive, Pure Edge™ De-interlacing
  - Built-in High Quality 148MHz/12-bit TV Encoder
  - Audio effect post-processor
  - Built-in 5.1-ch Audio DAC
  - Built-in 2-ch Audio ADC for Karaoke
  - USB 2.0 High-Speed
  - MS/SD/MMC 3-in-1 card reader

- **Speed Performance on Servo/Channel Decoding**
  - DVD-ROM up to 4XS
  - CD-ROM up to 24XS

- **Channel Data Processor**
  - Digital data slicer for small jitter capability
  - Built-in high performance data PLL for channel data demodulation
  - EFM/EFM+ data demodulation
  - Enhanced channel data frame sync protection & DVD-ROM sector sync protection

- **Servo Control and Spindle Motor Control**
  - Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
  - Built-in ADCs and DACs for digital servo control
  - Provide 2 general PWM
  - Tray control can be PWM output or digital output

- **Embedded Micro controller**
  - Built-in 8032 micro controller
  - Built-in internal 373 and 8-bit programmable lower address port
  - 1024-bytes on-chip RAM
  - Up to 2M bytes FLASH-programming interface
  - Supports 5/3.3-Volt. FLASH interface
  - Supports power-down mode
  - Supports additional serial port

- **DVD-ROM/CD-ROM Decoding Logic**
  - High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
  - Automatic sector Mode and Form detection
  - Automatic sector Header verification
  - Decoder Error Notification Interrupt that signals various decoder errors
  - Provide error correction acceleration

- **Buffer Memory Controller**
  - Supports 16Mb/32Mb/64Mb/128Mb SDRAM
  - Supports 16-bit SDRAM data bus
  - Provides the self-refresh mode SDRAM
  - Block-based sector addressing

- **Video Decode**
  - Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
  - Decodes MPEG-4 Advanced Simple Profile
  - Support DivX 3.11/4.x/5.x Home Theater Profile
  - Support DivX Ultra
  - Smooth digest view function with I, P and B picture decoding
  - Baseline, extended-sequential and progressive JPEG image decoding
  - Support CD-G titles

- **Video/OSD/SPU/HLI Processor**
  - Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
  - 65535/256/16/4/2-color bitmap format OSD,
  - 256/16 color RLC format OSD
  - Automatic scrolling of OSD image
  - Support 480i/480p/576i/576p Display
  - Support 720p/1080i Display
  - Support 1080p Display
  - Simultaneous HD/SD output

- **2-D Graphic Engine**
  - Support decode Text and Bitmap
  - Support line, rectangle, and gradient fill
  - Support bitblt
  - Chroma key copy operation

Audio Effect Processing

- Dolby Digital (AC-3)
- DTS decoding
- MPEG-1 layer 1/layer 2 audio decoding
- High Definition Compatible Digital (HDCD)
- Windows Media Audio (WMA)
- Dolby ProLogic II
- IEC 60958/61937 output
  - PCM / bit stream / mute mode
- Pink noise and white noise generator
- Karaoke functions
  - Microphone echo
  - Microphone tone control
  - Vocal mute/vocal assistant
  - Key shift up to +/- 8 keys
  - Chorus/Flanger/Harmony/Reverb
- Channel equalizer
- 3D surround processing include virtual surround and speaker separation

TV Encoder

- Four 148MHz/12-bit DACs
- Support NTSC, PAL-BDGHINM, PAL-60
- Support 525p, 625p progressive TV format
- Support Macrovision 7.1 L1 and 1.3 (525p/625p).
- CGMS-A/WSS
- Closed Caption

MDDi ™ Progressive Scan Video

- Automatic detect film or video source
- 3:2 pull down source detection
- Advanced Motion adaptive de-interlace
- PureEdge™ edge preserving technology
- PureEdge™ edge preserving technology V2
- Minimum external memory requirement

HDMI™ Tx V1.3

- Compatible with HDMI™ 1.3, DVI 1.0, HDCP 1.3
- Support EIA/CEA 861B 480i/ 480p/ 576i/ 576p/ 720p/ 1080i/ 1080p
- Maximum 8 channels 192k audio output
- Support audio sampling rate conversion
- Hot-plug and power-on detection
- HDMI™ display full screen
- CEC function support
- Deep Color support
- xvYcc Support

Image Resizer

Video case

- Support progressive / Interlaced frame scaling
- Support input & output maximum size: 4096x4096

JPEG case

- Input memory layout of source images must be scan line based
- Deal with one block line (height:8 / 16) each round
- Input maximum size: 65535x65535
- Output maximum size: 4096x4096
- Support a output scaling window at arbitrary location in an output frame buffer
- Y / Cb / Cr separated

Serial Flash Interface

- Supports 4Mb/8Mb/16Mb/32Mb/64Mb SPI interface Serial Flash

External Interface

- USB2.0 High Speed (Host)
- Memory-Stick, Secure Digital Memory Card, and MultiMediaCard Interface

Outline

- 128-pins EPAD LQFP package
- 3.3/1.2-Volt. Dual operating voltages

Version 1.0

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General Feature – Third Party Proprietary Right

1. Dolby License

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3. DTS License

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4. Microsoft License

This product included technology owned by Microsoft Corporation and cannot be used or distributed without a license from Microsoft GP.

5-4 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- 4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
Analog Interface (66)				
119	RFIP		Analog Input	AC coupled DVD RF signal input RFIP
120	RFIN	OPOUT GPI36	Analog Input	1) AC coupled DVD RF signal input RFIN 2) GPI36
121	RFG	OPINP	Analog Input	Main beam, RF AC input path
122	RFH	OPINN	Analog Input	Main beam, RF AC input path
123	RFA		Analog Input	RF main beam input A
124	RFB		Analog Input	RF main beam input B
125	RFC		Analog Input	RF main beam input C
126	RFD		Analog Input	RF main beam input D
127	RFE		Analog Input	RF sub beam input E
128	RFF		Analog Input	RF sub beam input E
1	AVDD12_2		Analog power	Analog 1.2V power
2	AVDD33_1		Analog Power	Analog 3.3V power
3	XTALI		Input	27MHz crystal input
4	XTALO		Output	27MHz crystal output
5	V20		Analog output	Reference voltage 2.0V
6	V14		Analog output	Reference voltage 1.4V
7	REXT	GPO5	Analog Input / Digital output	1) Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS. 2) GPO5
8	MDI1		Analog Input	Laser power monitor input
9	LDO1		Analog Output	Laser driver output
10	LDO2		Analog Output	Laser driver output
11	AVDD33_2		Analog Power	Analog 3.3V power
12	DMO		Analog Output	Disk motor control output. PWM output

Pin	Main	Alt.	Type	Description
13	FMO		Analog Output	Feed motor control. PWM output
14	TRAY_OPEN	GPIO	Analog Output	Tray PWM output/Tray open output
15	TRAY_CLOSE	GPIO	Analog Output	Tray PWM output/Tray close output
16	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator
17	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
18	FG	GPIO2	Analog	1) Motor Hall sensor input 2) GPIO2
19	USB_DP		Analog Inout	USB port DPLUS analog pin
20	USB_DM		Analog Inout	USB port DMINUS analog pin
21	VDD33_USB		USB Power	USB Power pin 3.3V
22	PAD_VRT	GPIO37	Analog	1) USB generating reference current 2) GPIO37
23	VDD12_USB		USB Power	USB Power pin 1.2V
82	EXT_RES		Analog Input	EXTERNAL RESISTER FOR HDMI™ TX
83	AVDD33_12		Analog Power	3.3V VDD FOR HDMI™ TX
84	TXCN		Analog Output	Negative TX CLK
85	TXCP		Analog Output	Postive TX CLK
86	AVDD12_C		Analog Power	1.2V VDD FOR HDMI™ TX
87	TX0N		Analog Output	Negative TX CH0
88	TX0P		Analog Output	Postive TX CH0
89	ASS12		Analog Power	1.2V GND FOR HDMI™ TX
90	TX1N		Analog Output	Negative TX CH1
91	TX1P		Analog Output	Postive TX CH1
92	AVDD12_D		Analog Power	1.2V VDD FOR HDMI™ TX
93	TX2N		Analog Output	Negative TX CH2
94	TX2P		Analog Output	Postive TX CH2
95	DACVDDC		Power	3.3V power pin for video DAC circuitry
96	VREF	GPO14	Analog	1) Bandgap reference voltage 2) GPO14
97	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
98	CVBS		Analog	Analog CVBS or C
99	DACVDDB		Power	3.3V power pin for video DAC circuitry
100	Y/G		Analog	Green, Y, SY, or CVBS
101	B/CB/PB		Analog	Blue, CB/PB, or SC

Pin	Main	Alt.	Type	Description
102	R/CR/PR		Analog	Red, CR/PR, CVBS, or SY
103	AKIN2	GPIO19	Analog	1) Y5 2) HSYN/VSYN output 3) Audio Mute 4) SPDIF 5) MCDATA 6) GPIO19
104	ADVCM	GPIO20	Analog	1) Y6 2) HPLG 3) GPIO20
105	AKIN1	GPIO21	Analog	1) Y7 2) HSYN/VSYN output 3) Audio Mute 4) ASDATA3 5) GPIO21
106	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
107	APLLVDD_GPIO	GPIO34	Analog	1) 3.3V Power pin for audio clock circuitry 2) SPDIF out(89G) 3) GPIO34 4) SPDIF output3
108	PAPLLCAP	GPIO35	Analog	1) APLL external capacitance connection 2) GPIO35
109	LFE	GPIO	Analog Output	1) ACLK 2) GPIO_LFE
110	ARS	GPIO	Analog Output	1) ABCK 2) GPIO_ARS
111	AR	GPIO0	Analog Output	1) RXD2 2) ASDATA2 3) GPIO_AR
112	AVCM		Analog	Audio DAC reference voltage
113	AL	GPIO	Analog Output	1) TXD2 2) ASDATA1 3) GPIO_AL
114	ALS	GPIO	Analog Output	1) ALRCK 2) GPIO_ALS
115	CENTER	GPIO	Analog Output	1) Audio Mute 2) ASDATA0 3) GPIO_CENTER
116	ADACVDD1		Analog Power	3.3V power pin for audio DAC circuitry
117	ADACVDD2		Analog Power	3.3V power pin for audio DAC circuitry
118	AVDD12		Analog Power	Analog 1.2V power
General Power (4)				
52, 79	DVDD12		Power	1.2V power pin for internal digital circuitry
40, 71	DVDD33		Power	3.3V power pin for internal digital circuitry

Pin	Main	Alt.	Type	Description
Micro Controller , Flash Interface and GPIO(11)				
34	GPIO3	INT_	InOut 8mA, SR SMT	1) INT_ 2) MS_CLK set B 3) Microcontroller port 3-1 (Internal Pull-Up) 4) iPod_TXD 5) GPIO3 6) CEC
35	GPIO4		InOut 4mA, PD	1) MS_BS set B 2) ASDATA0 3) ALRCK 4) Microcontroller port 3-4 (Internal Pull-Up) 5) GPIO4
31	GPIO6		InOut 4mA, PU	1) TXD1 2) Y3 3) SD_CLK set B 4) MS_D0 set B 5) ASDATA2 6) Microcontroller port 3-5 (Internal Pull-Up) 7) GPIO6
24	SF_CS_		InOut 8mA, SR PU, SMT	1) Serial Flash Chip Select 2) Trap value in power-on reset : 1 : Serial Flash ATMEL mode 0 : Serial ST/SST mode
25	SF_DO		InOut 8mA, SR PD, SMT	Serial Flash Dout
26	SF_DI		InOut 8mA, SR PU, SMT	1) Serial Flash Din 2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
27	SF_CK		InOut 8mA, SR PD, SMT	Serial Flash Clock
28	UP1_6	SCL	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-6 2) RXD3 3) DDC 4) I2C SCK
29	UP1_7	SDA	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-7 2) TXD3 3) DDC 4) I2C SDA
32	PRST_		Input 4mA, SR PU, SMT	Power on reset input, active low
33	IR	GPI	Input 4mA, SR SMT	1) IR control signal input 2) GPI
Dram Interface (37) (Sorted by position)				

Pin	Main	Alt.	Type	Description
41	RD0		InOut, 2mA	DRAM data 0
42	RD1		InOut 2mA	DRAM data 1
43	RD2		InOut 2mA	DRAM data 2
44	RD3		InOut 2mA	DRAM data 3
45	RD4		InOut 2mA	DRAM data 4
46	RD5		InOut 2mA	DRAM data 5
47	RD6		InOut 2mA	DRAM data 6
48	RD7		InOut 2mA	DRAM data 7
49	DQM0		InOut 2mA, PD	Data mask 0
50	RD15		InOut 2mA	DRAM data 15
51	RD14		InOut 2mA	DRAM data 14
53	RD13		InOut 2mA	DRAM data 13
54	RD12		InOut 2mA	DRAM data 12
55	RD11		InOut 2mA	DRAM data 11
56	RD10		InOut 2mA	DRAM data 10
57	RD9		InOut 2mA	DRAM data 9
58	RD8		InOut 2mA	DRAM data 8
59	DQM1		InOut 2mA, PD	Data mask 1
60	RCLK		InOut 4mA, PD	Dram clock
61	RA11		InOut 2mA, PD	DRAM address bit 11
62	RA9		InOut 2mA, PD	DRAM address 9
63	RA8		InOut 2mA, PD	DRAM address 8
64	RA7		InOut 2mA, PD	DRAM address 7
65	RA6		InOut 2mA, PD	DRAM address 6
66	RA5		InOut 2mA, PD	DRAM address 5

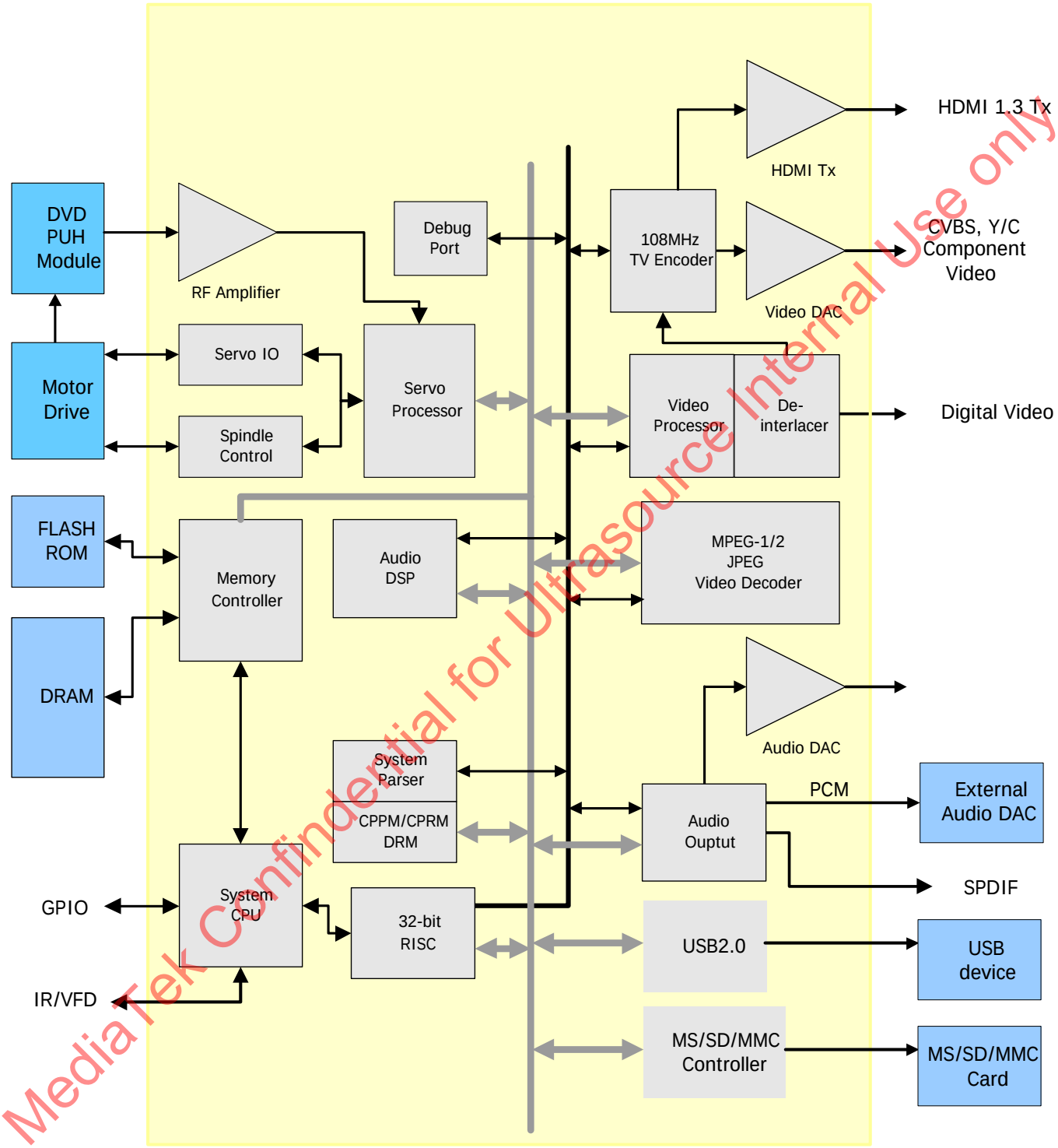
Pin	Main	Alt.	Type	Description
67	RA4		InOut 2mA, PD	DRAM address 4
68	RWE		Output 2mA, PD	DRAM Write enable, active low
69	CAS		Output 2mA, PD	DRAM column address strobe, active low
70	RAS		Output 2mA, PD	DRAM row address strobe, active low
72	BA0		InOut 2mA, PD	DRAM bank address 0
73	BA1		InOut 2mA, PD	DRAM bank address 1
74	RA10		InOut 2mA, PD	DRAM address 10
75	RA0		InOut 2mA, PD	DRAM address 0
76	RA1		InOut 2mA, PD	DRAM address 1
77	RA2		InOut 2mA, PD	DRAM address 2
78	RA3		InOut 2mA, PD	DRAM address 3
39	GPIO7	CKE_	InOut 4Ma PD	1) Y0 2) HSYN/VSYN output 3) HSYN/VSYN input 4) SD_CLK set A 5) MS_CLK set A 6) ACLK 7) ASDATA1 8) MCDATA 9) CEC 10) Microcontroller port 1-4 (Internal Pull-Up) 11) GPIO7
GPIO (6)				
38	GPIO8		InOut 4mA, PD	1) Y1 2) HSYN/VSYN output 3) HSYN/VSYN input 4) SD_CMD set A 5) MS_BS set A 6) ASDATA2 7) ACLK 8) Audio Mute 9) MCDATA 10) DDC 11) Microcontroller port 1-5 (Internal Pull-Up) 12) GPIO8

Pin	Main	Alt.	Type	Description
37	GPIO9		InOut 4mA, PD	1) Y2 2) SD_DATA set A 3) MS_D0 set A 4) ASDATA1 5) ABCK 6) DDC 7) GPIO9
81	GPIO10	HPLG	InOut 4mA, PD	1) DDC 2) GPIO10
30	GPIO11		InOut 4mA	1) RXD1 2) Y4 3) HSYN/VSYN output 4) SD_CMD set B 5) ABCK 6) ASDATA0 7) Audio Mute 8) CEC 9) DDC 10) Microcontroller port 3-0 (Internal Pull-Up) 11) iPod_RXD 12) GPIO11
80	SPDIF	GPIO12	InOut 2mA, PD	1) SPDIF output 2) GPIO12
36	GPIO13		InOut 4mA, PD	1) YCLK 2) SD_D0 set B 3) ALRCK 4) Audio Mute 5) GPIO13

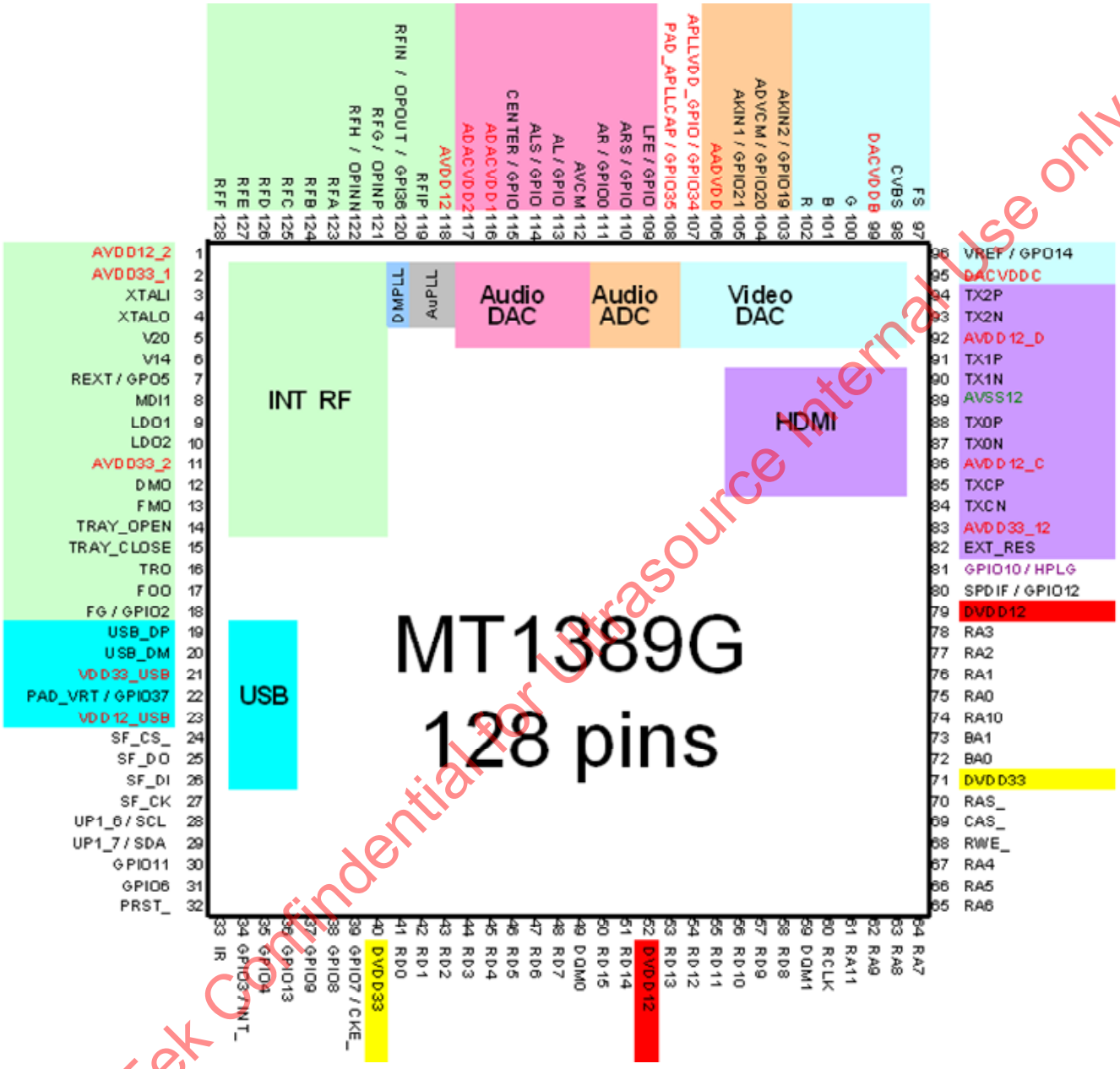
Note:

1. The Main column is the main function, Alt. means alternative function.

5-5 Functional Block



6 Pin Assignment



7 Absolute Maximum Ratings

Symbol	Parameters	Suggest Value	Unit
VDD3	3.3V Supply voltage	-0.2 to 3.6	V
VDD2	1.2V Supply voltage	-0.1 to 1.3	V
VDDA	Analog Supply voltage	-0.2 to 3.6	V
V_{IN}(3.3V)	Input Voltage (3.3V IO)	-0.2 to 3.6	V
V_{IN}(5V-tolerance)	Input Voltage (5V-tolerance IO)	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.2 to VDD3+0.3	V
T_{STG}	Storage Temperature	-45 to 150	°C

8 Recommend Operation Condition

Symbol	Parameters	Min	Typ	Max	Unit
T_{OP}	Operating Temperature	0		70	°C
T_J	Junction Operation Temp.	0	25	115	°C
VDD3	3.3V Supply voltage	3.1	3.3	3.6	V
VDD2	1.2V Supply voltage	1.1	1.2	1.3	V
VDDA	Analog Supply voltage	3.1	3.3	3.6	V
V_{IH} (3.3V)	Input voltage high (3.3V IO)	2.0	-	-	V
V_{IL} (3.3V)	Input voltage low (3.3V IO)	-	-	0.8	V
I_{IH}	High level input current			10	UA
I_{IL}	Low level input current	-10			UA
P_D	Power dissipation		1.5		W
P_{DOWN}	Power down mode			0.1	W
fclk	Input frequency of clock		27		MHz

9 Electrical Characteristics

9-1 DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{OH} (3.3V)	Output voltage high (3.3V IO) (*I_{OH} = 2 ~ 16mA)	2.4	-	-	V
V_{OL} (3.3V)	Output voltage low (3.3V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
Rpu	Pull-up Resistance	40	75	190	KΩ
Rpd	Pull-down Resistance	40	75	190	KΩ
FOO_{OFF}	Offset voltage between FOO zero output and V_{REF}	-50	0	50	mV
TRO_{OFF}	Offset voltage between TRO zero output and V_{REF}	-40	0	40	mV
DMO_{OFF}	Offset voltage between DMO zero output and V_{REF}	-30	0	30	mV

Note * : The driving current of some IO pad are programmable according to the different application and environment . All setting will be defined according to the F/W progress and test result.

9-2 Built-in Audio-DAC Characteristics

Note *: All parameters is measured on MediaTek's DVD player reference DVD board, the actual performance depends on different PCB design.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{out}	Output swing level: Digital i/p level =0 dBFS , ADACVDD =3.3V (V_{out} = 1.0 * ADACVDD / 3.3)	0.9	1.0	1.1	V_P
Ro	Output impedance @ 1kHz		50	100	Ω
R_{L_min}	Minimum resister load	5			K
C_{L_max}	Maximum capacitor load			20	PF
S/(THD+N)	S/(THD+N) @ 0 dBFS; f_{in} = 1kHz; Fs = 48kHz, A-weighted		81		dBr(A)
DR	Dynamic Range		82		dBr(A)
SNR	Signal to noise ratio; A-weighted		92		dBr(A)
Channel Separation	Close-talk of Left and Right Channel		81		dB

9-3 Built-in Audio-ADC Characteristics

Test signal : 1K Hz sin wave	Vpp(V)	
Max Input (with output THD+N <60 dbfs)	3.227V	59.9dBFS
DC bias level	1.66V	
AKIN DC Level	1.632V	
Test signal : 1K Hz sin wave		
Input (Vpp)	Output THD+N(dBFs)	filter=A-weighting
3V	-62.27	
2.95	-63.9	
2.9	-65.7	
2.828V	-67.7	
2.75V	-69.9	
2.5V	-75.4	
1.5V	-81.9	
0.5V	-84.9	
0V (remove input and short ADVCM with AKIN)	-133.9	
Test signal : 2.8 Vpp		
Input frequency:	Amp(dBFS)	filter=none
1 KHz	-0.422	
4KHz	-0.447	
8khz	-0.518	
16KHz	-0.791	
20KHz	-1.822	
22KHz	-6.848	
Dynamic range	283mVpp	

9-4 Built-in Video-DAC Specifications

Input Codes for Video Application:

	NTSC	NTSC w/setup	525_I	525_I w/setup	525_P
WHITE (235)	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3290
BLACK (16)	960	1120	960	1120	1008
PEDESTAL	960	960	960	960	1008
SYNC TIP	64	64	64	64	64

	525_P w/s	PAL	625_I	625_P	RGB
WHITE (235)	---	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 2282
BLACK (16)	---	1008	1008	1008	0
PEDESTAL	---	1008	1008	1008	-
SYNC TIP	---	64	64	64	-

9-5 Video Output Voltage Level:

High / Low Impedance Mode:

Please contact with FW window for setting High / Low impedance mode.

9-6 Video DAC DC Electrical Characteristics

(Operating Free-Air Temperature, AVDD 3.3V, DVDD = 3.3V).

Analog Output		**MIN**	**TYP**	**MAX**	**UNIT**
Full Scale Output Current CVBS/Y/C/R/G/B	(low impedance mode)	34.3	34.8	35.7	mA
Full Scale Output Current CVBS/Y/C/R/G/B	(high impedance mode)	8.52	8.70	8.91	mA
LSB current CVBS/Y/C/R/G/B	(low impedance mode)	33.5	34.0	34.86	uA
LSB current CVBS/Y/C/R/G/B	(high impedance mode)	8.375	8.500	8.715	uA
DAC-to-DAC Mis-Matching		--	1.48	--	%
Output Compliance		0	--	1.38	V
DAC Output Delay		--	1.5	10	ns
DAC Rise/Fall Time		--	2.1	5	
Voltage Reference					
Reference Voltage Output			1.22		V
Reference Input Current			2.179		MA
Static Performance					

DAC Resolution		12		Bits
DNL Differential Non-Linearity	+/-0.26	+/-0.48	+/-0.6	LSB
INL Integral Non-Linearity	+/-0.40	+/-0.67	*/-0.9	LSB
Dynamic Performance				
Differential Gain		0.77	1.5	%
Differential Phase		0.23	1.5	□
S/N Ratio	70			dB
Power Supply				
Supply Voltage	3.0	3.3	3.6	V

9-7 RF specification

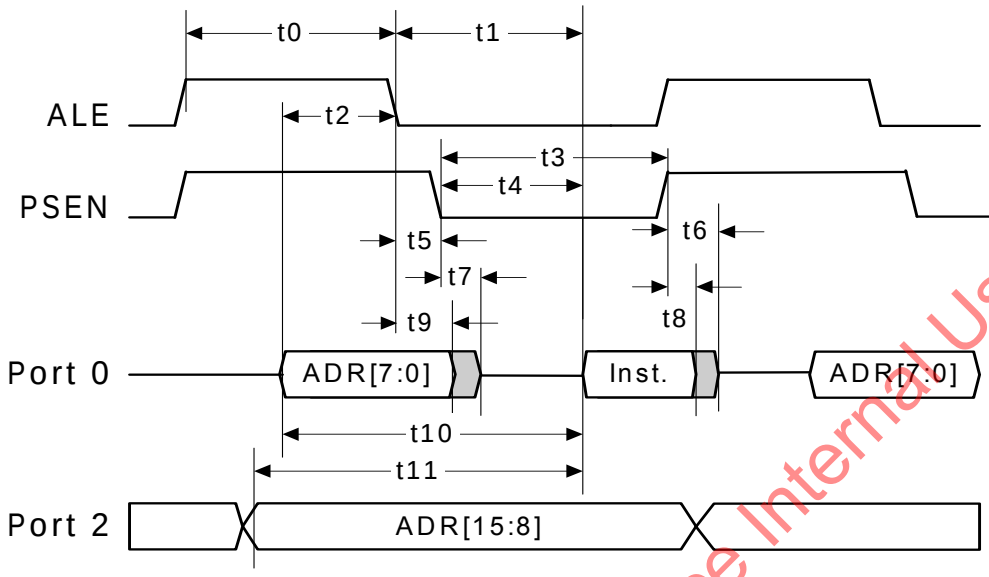
Item	Designator	Conditions	Min	Typ	Max	Unit
3.3V POWER			3.00	3.30	3.60	Volts
Power Down Mode		Enable power down	10	27	50	mA
		Chip Reset	90	151	200	mA
Reference Voltage	V20	Force current =0A	1.85	1.99	2.15	Volts
Reference Voltage	V14	Force current =0A	1.25	1.39	1.55	Volts
APC1(CD)	MDI1	0Ah=10 ;APC1 on MDI1=180mV	166	184	202	mV
	LDO1	0Ah=00 ;APC1 off	3.00	3.28		V
	MDI1→LDO1	0Ah=10; APC1 on	212	254	295	V/V
APC2(DVD)	MDI2	0Bh=10 ;APC2 on MDI2=180mV	166	184	202	mV
	LDO2	0Bh=00 ;APC2 off	3.00	3.28		V
	MDI2→LDO2	0Bh=10; APC2 on High gain	210	265	298	V/V
Focusing Error Gain	MA → FEO	05h=30; low gain With 10KHz Sin Input	7.5	10.3	11.5	dB
Focusing Error Frequency Response	MA → FEO	05h=7C; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	23.9		dB
Focusing Error Common Mode Gain	MA → FEO MB → FEO	05h=3F; low gain With 10KHz Sin Input		-34	-20	dB

Item	Designator	Conditions	Min	Typ	Max	Unit
Focusing Error H/L Gain	MA → FEO	Toggle 05h bit5 : FELG With 10KHz Sin Input	2.75	2.99	3.25	V/V
Focusing Error offset Adjustment step	Input Floating Measure FEO	Toggle 4Dh : FEOS[6:0]	65	103	140	mV
Focusing Error THD	MA → FEO	05h=7C; low gain With 10KHz Sin Input	30	54		dB
Central Servo Gain	MA → CSO	06h=F0; low gain With 10KHz Sin Input	12.5	14.1	15.5	dB
Central Servo Frequency Response	MA → CSO	06h=FF; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	21.4		dB
Central Servo Common Mode Gain	MA → CSO MB → CSO	06h=F0; low gain With 10KHz Sin Input		-30	-10	dB
Central Servo H/L Gain	MA → CSO	Toggle 06h bit5 : CSOLG With 10KHz Sin Input	2.75	2.97	3.25	V/V
Central Servo offset Adjustment step	Input Floating Measure CSO	Toggle 4Eh : CSOOS[6:0]	65	108	140	mV
Central Servo THD	MA → CSO	06h=F0; low gain With 10KHz Sin Input	30	53		dB
Tracking Error Gain	MA → TEO	07h=70; low gain With 10KHz Sin Input	13	15	17	dB
Tracking Error Frequency Response	MA → TEO	07h=70; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	24.2		dB
Tracking Error Common Mode Gain	MA → TEO MB → TEO	07h=7F; low gain With 10KHz Sin Input		-22	-10	dB
Tracking Error H/L Gain	MA → TEO	Toggle 07h bit6, 5 With 10KHz Sin Input	4	5.8	8	V/V
Tracking Error offset Adjustment step	Input Floating Measure TEO	Toggle 4Fh : TEOS[6:0]	65	110	140	mV

Item	Designator	Conditions	Min	Typ	Max	Unit
Tracking Error THD	MA → TEO	07h=7F; low gain With 10KHz Sin Input	30	42		dB
RFL Gain	MA → LVL	08h=60; low gain With 10KHz Sin Input	-6.5	-4.6	-3.5	dB
RFL Frequency Response	MA → LVL	08h=7F; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	22.7		dB
RFL H/L Gain I	MA → LVL	Toggle 09h bit1 : LVLATN With 10KHz Sin Input	0.3	0.52	0.7	V/V
RFL H/L Gain II	SA → LVL	Toggle 09h bit2 : SBADHG With 10KHz Sin Input	2.5	2.77	3.1	V/V
RFL offset Adjustment step	Input Floating Measure LVL	Toggle 50h : LVLOS[6:0]	65	113	140	mV
RFL THD	MA → LVL	08h=7F; low gain With 10KHz Sin Input	30	44		dB

9-8 Micro Controller Interface

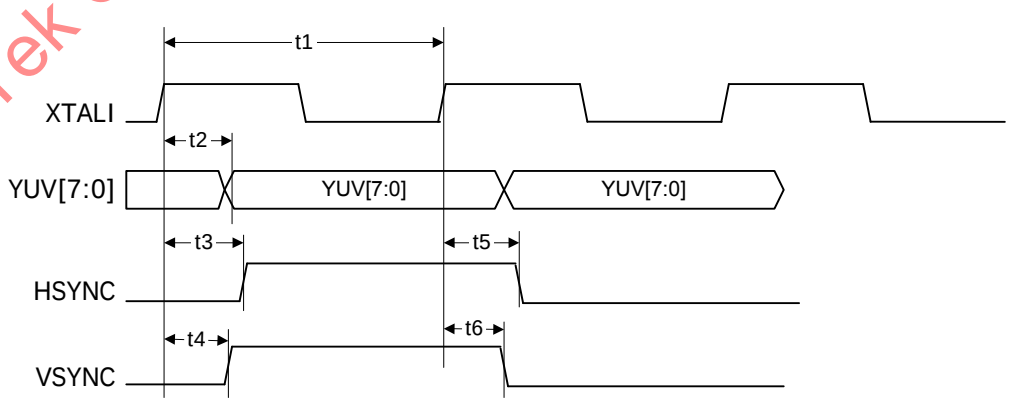
Parameter	Symbol	Min.	Max.	Units
Oscillator Frequency	1/Tf	0	23.3	MHz
ALE Pulse Width	T0	1.5Tf-5		ns
ALE Low to Valid Instruction	T1		2.5Tf-20	ns
ALE Low to PSEN Low	T5	0.5Tf-5		ns
Address Valid to ALE Low	T2	0.5Tf-5		ns
Address Hold After ALE Low	T9	0.5Tf-5		ns
PSEN Pulse Width	T3	2.0Tf-5		ns
PSEN Low to Valid Instruction	T4		2.0Tf-20	ns
Input Instruction Hold After PSEN high	T8	0		ns
Input Instruction Float After PSEN high	T6		1.0Tf-5	ns
Port 0 Address to Valid Instruction	T10		3.0Tf-20	ns
Port 2 Address to Valid Instruction	T11		3.5Tf-20	ns
PSEN Low to Address Float	T7		0	ns



Program Memory Read Cycle Timing Diagram

9-9 Digital Video Output Interface

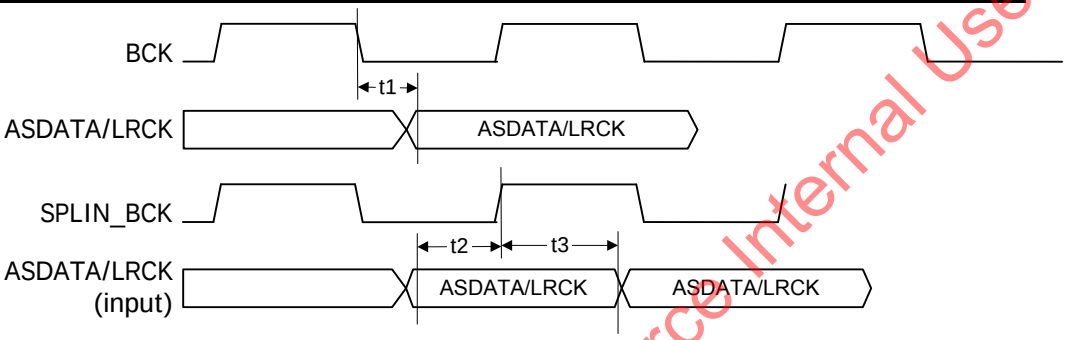
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/T1		27		MHz
YUV digital output delay	T2			15	ns
HSYNC Rising delay	T3			15	ns
VSYNC Rising delay	T4			15	ns
HSYNC Falling delay	T5			20	ns
VSYNC Falling delay	T6			20	ns



Digital Video Output Interface Timing Diagram

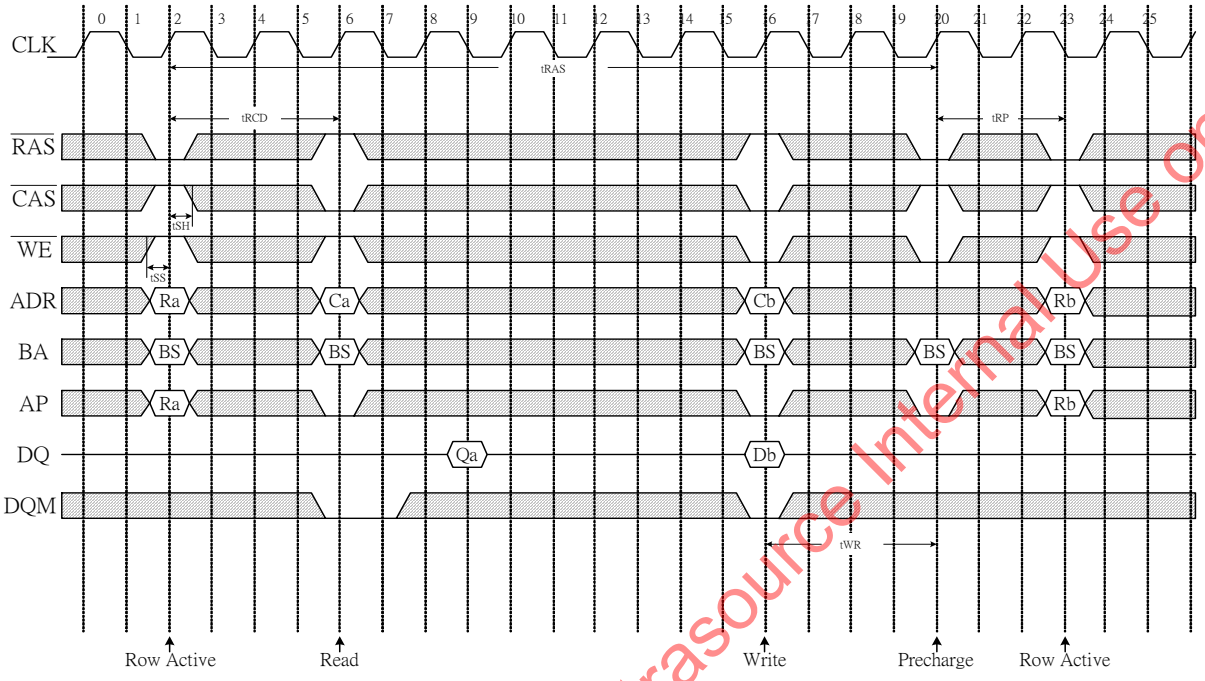
9-10 SPDIF I/O Interface

Parameter	Symbol	Min	Typ	Max	Units
BCK negative edge to ASDATA valid	T1	1.0		3.0	ns
ASDATA/LRCK input setup	T2			3.0	ns
ASDATA/LRCK input hold	T3	1.2			ns



SPDIF Input/Output Timing Diagram

9-11 DRAM Interface



Parameter		Symbol	-6		-7		-75		Units
			Min	Max	Min	Max	Min	Max	
CLK cycle time	CAS latency = 3	tCC	7.5	-	7.5	-	7.5	-	ns
SDRAM input setup time		tSS	1.5		1.75		1.75		ns
SDRAM input hold time		tSH	1		1		1		ns
Active to Precharge command period		tRAS	42	100K	49	100K	52	100K	ns
Precharge to Active command period		tRP	18		20		20		ns
Active to read/write command delay		tRCD	18		20		20		ns
Write recovery time	CL = 3	tWR	6		7		7.5		ns

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

-6T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		42ns	18ns	18ns	6ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	2	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		49ns	20ns	20ns	7ns/10ns
133MHz (7.5ns)	3	7	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7.5T

(Unit: number of clock)

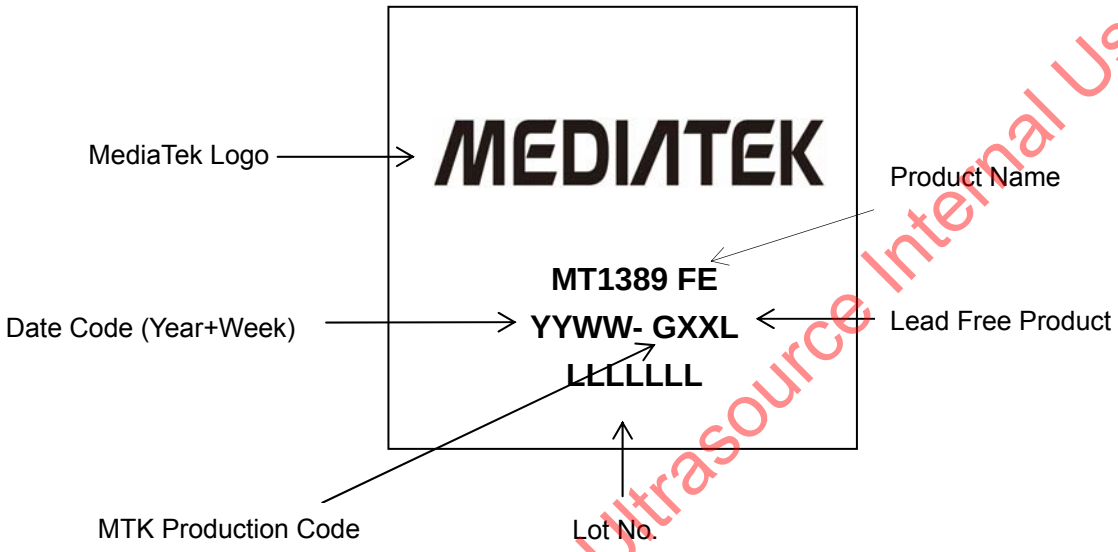
Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		45ns	20ns	20ns	7.5ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-8T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		48ns	20ns	20ns	8ns/10ns
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	3	5	2	2	1

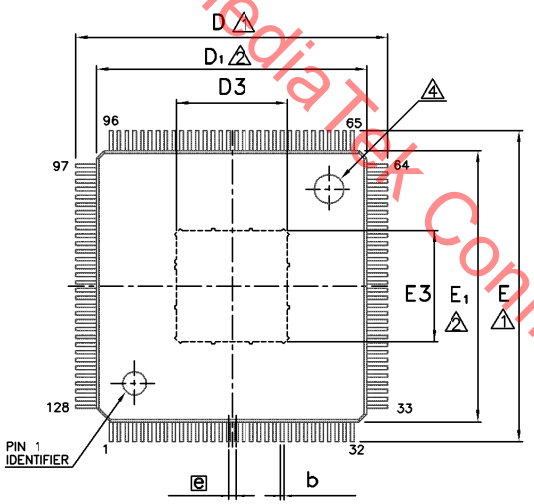
10 Marking on Devices

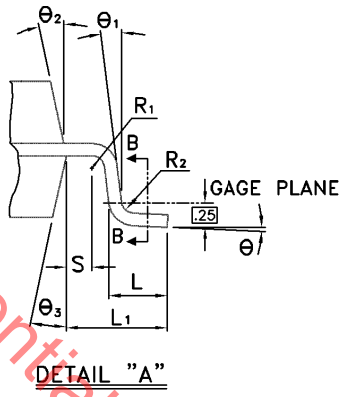


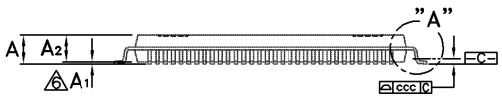
11 Package Description

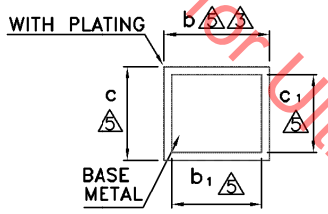
11-1 Package Outline Dimension

The bend lead are controlled under the criteria 0.075mm (2.5mil).









SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Exposed Pad Size			
L/F		Dimension in mm	Dimension in inch
①	D3/E3	3.61 REF	0.142 REF
②	D3/E3	5.72 REF	0.225 REF
③	D3/E3	8.00 REF	0.315 REF
④	D3/E3	7.75 / 6.60 REF	0.305 / 0.260 REF

TITLE: 128LD E-PAD LQFP (14x14x1.4mm)PACKAGE OUTLINE Cu L/F,FOOTPRINT 2.0mm			
L/F MATERIAL: C7025 1/2H			
APPR.		DWG NO.	DB128-SW1
ENG.		REV NO.	C
Q.M		PRODUCT CODE	DB1283C
CHK.		DATE	09/07/'07
DWG.	Mechane SieChang	SHT NO.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	Add exposed pad size ④	09/07/'07

REV.B

01-5700-10

11-2 Weight of the chip

0.65g

11-3 Material and Finish of Lead Terminals

For Lead-free Package, Materials of terminal is Sn(98%) and Bi (2%) and thickness is 300~600u inch, similar as SnPb.

11-4 Package Material

Lead frame: Cu

Epoxy: 1033BF

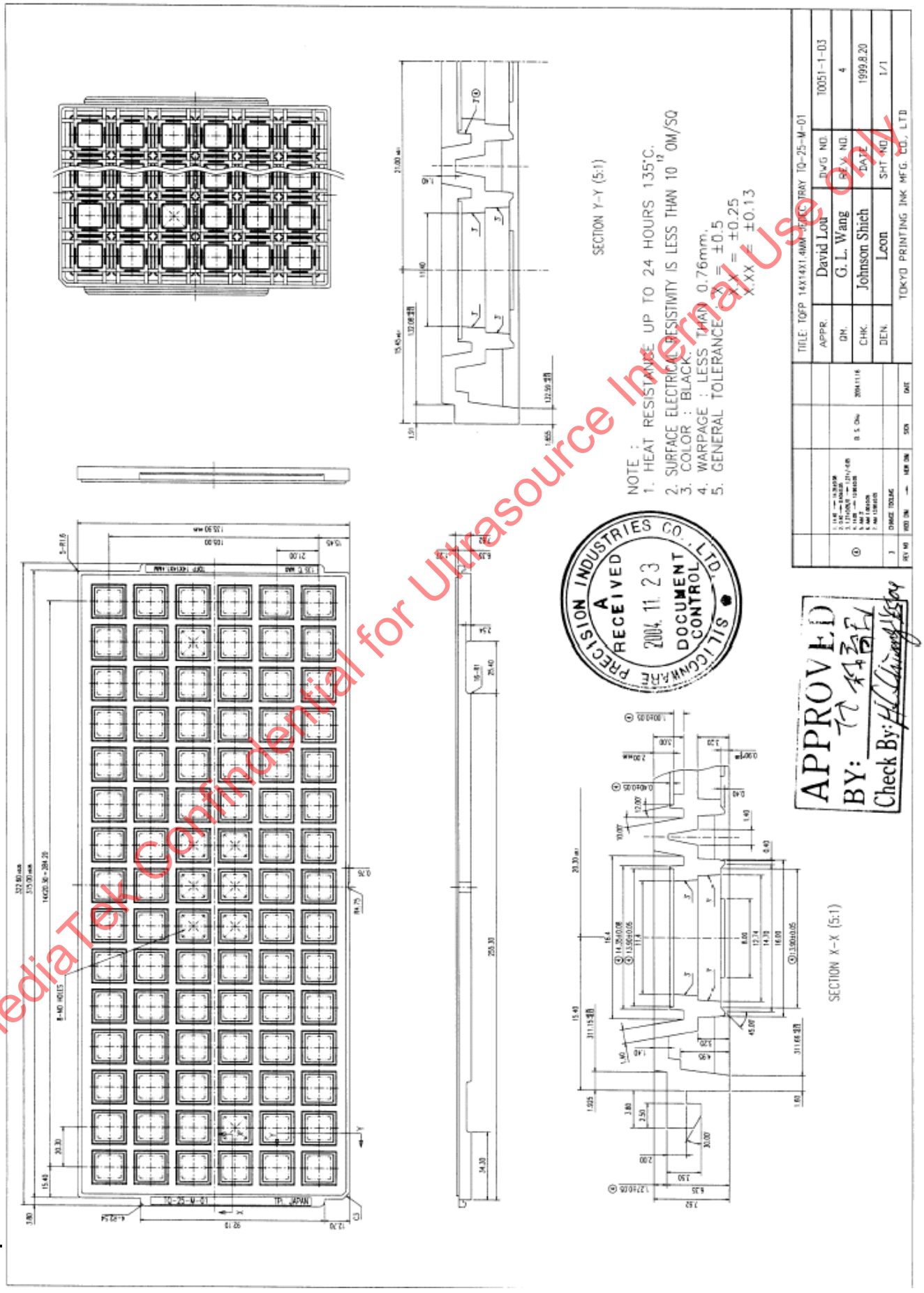
Molding compound: G700

12 Packing Description

Package	Pin / Ball count	EA / Tray	Tray / Box	Full Box Q'ty	Box / Carton	Full carton Q'ty
LQFP	128	90	10	900	6	5400

12-1 Tray Description

90ea/ Hard Tray (150°C resistance).



12-2 Desiccants

Size: 130*80 mm.

Weight: 20g

12-3 Aluminum Foil Bag

Size: 250*500 mm.

Thickness: 0.12 +/- 0.005 mm.

Surface impedance: 10^{8}-10^{12} Ohm/SQ

12-4 Box Description

Material: 3 Layer B corrugated paper.

Strength: 1176000 PA.

Box size: 355(L)*157(W)*90.5(H) mm.

Printing: Black (words, warning, index)

12-5 Side Plank

Material: 5 Layer AB corrugated paper

Strength: 1793400 PA.

Size: 405(L)*237(W) mm.

Fixture: 3 pieces of EPE (recyclable material).

Thickness: 20 mm.

12-6 Carton Description

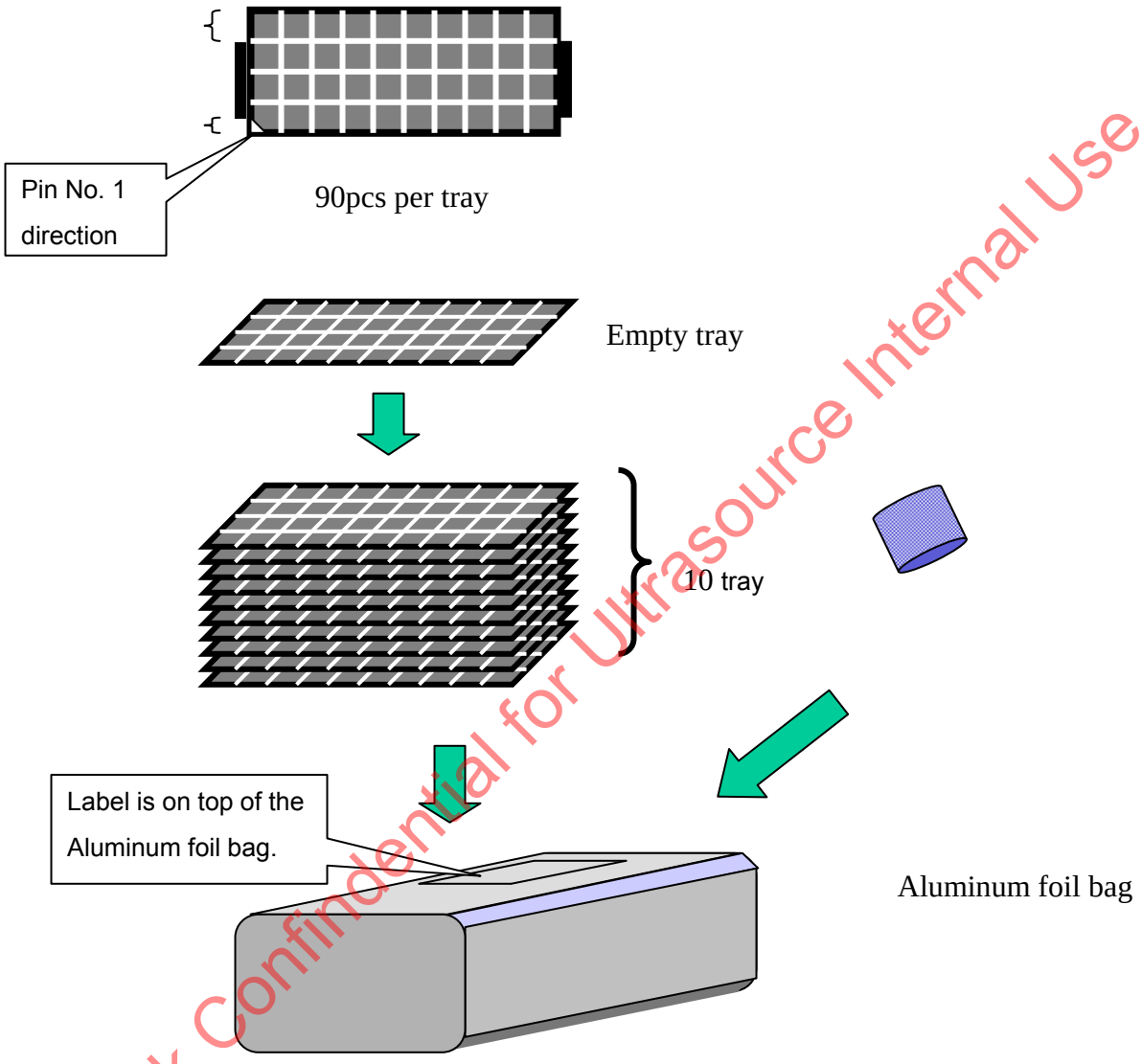
Material: 5 Layer AB corrugated paper.

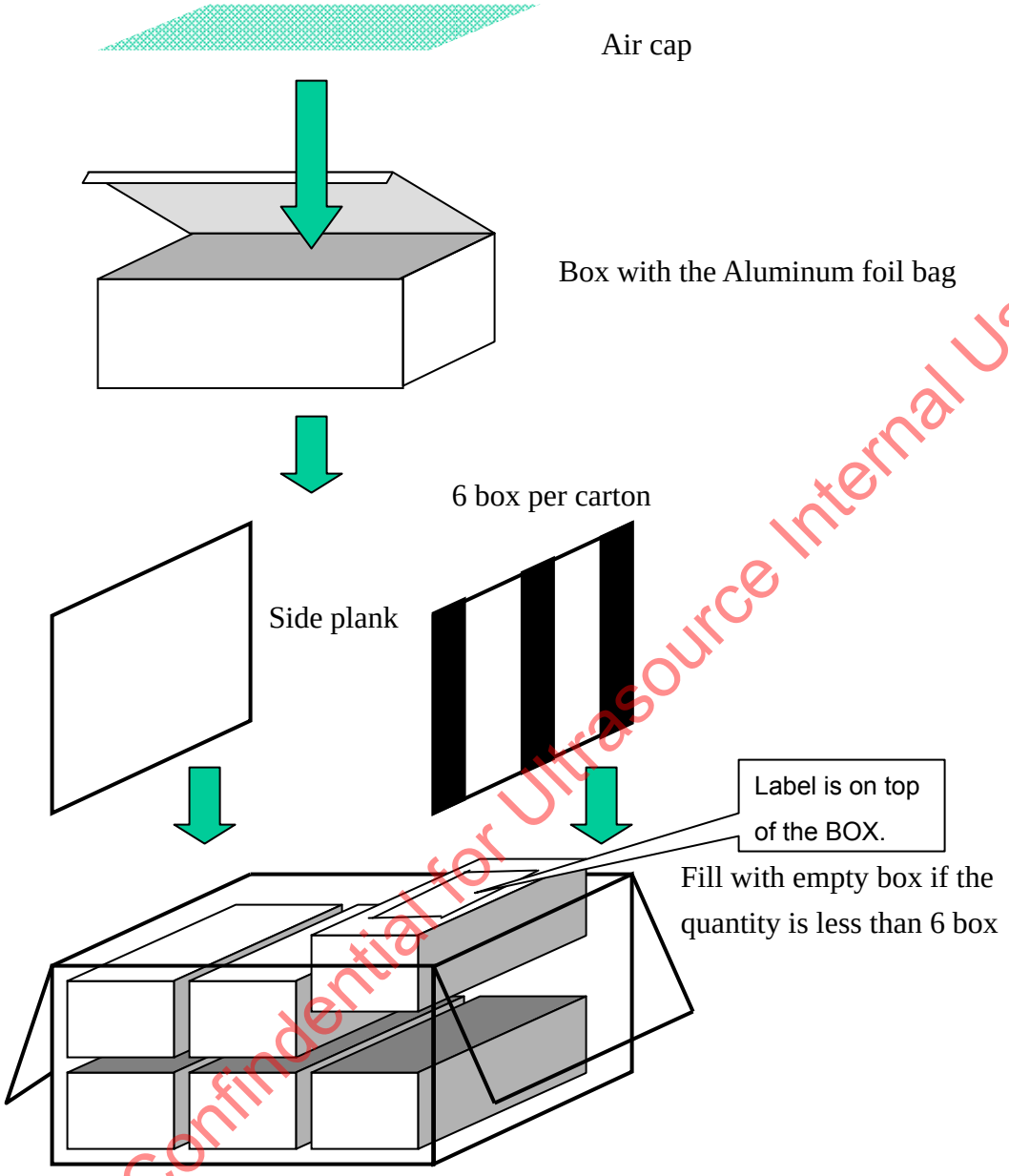
Strength: 1793400 PA.

Carton size: 558(L)*428(W)*264(H) mm.

Printing: Black (words, warning, index)

12-7 Packing Flow





13 Solder-Reflow Condition

13-1 Reflow Condition

MediaTek can guarantee 3 times IR reflow based on the reflow profile (Figure 1).

Average ramp-up rate (Ts to peak): 3 °C /sec. max.

Preheat & Soak: Pb-Free 150~200 °C (SnPb Eutectic 100~150 °C) for 60~120 seconds

Liquidous temperature maintained above Pb-Free 217 °C (SnPb Eutectic 183 °C) for 60~150 seconds

Time within 5 °C of specified classification temperature: Pb-Free 30 seconds (SnPb Eutectic 20 seconds)

Note:

Reflow profiles in this document are for classification/preconditioning and ***are not meant to specify board assembly profiles.*** Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1.

For example, if Tc is 260 °C and time tp is 30 seconds, this means the following for the supplier and user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Peak temperature: Defined in Table 2-1 and Table 2-2.

Ramp-down rate: 6 °C /sec. max.

Time 25 °C to peak temperature: Pb-Free: 8 minutes max. (SnPb Eutectic 6 minutes max.)

Time between reflows: 5 minutes minimum and 60 minutes maximum

Table 1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 2-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

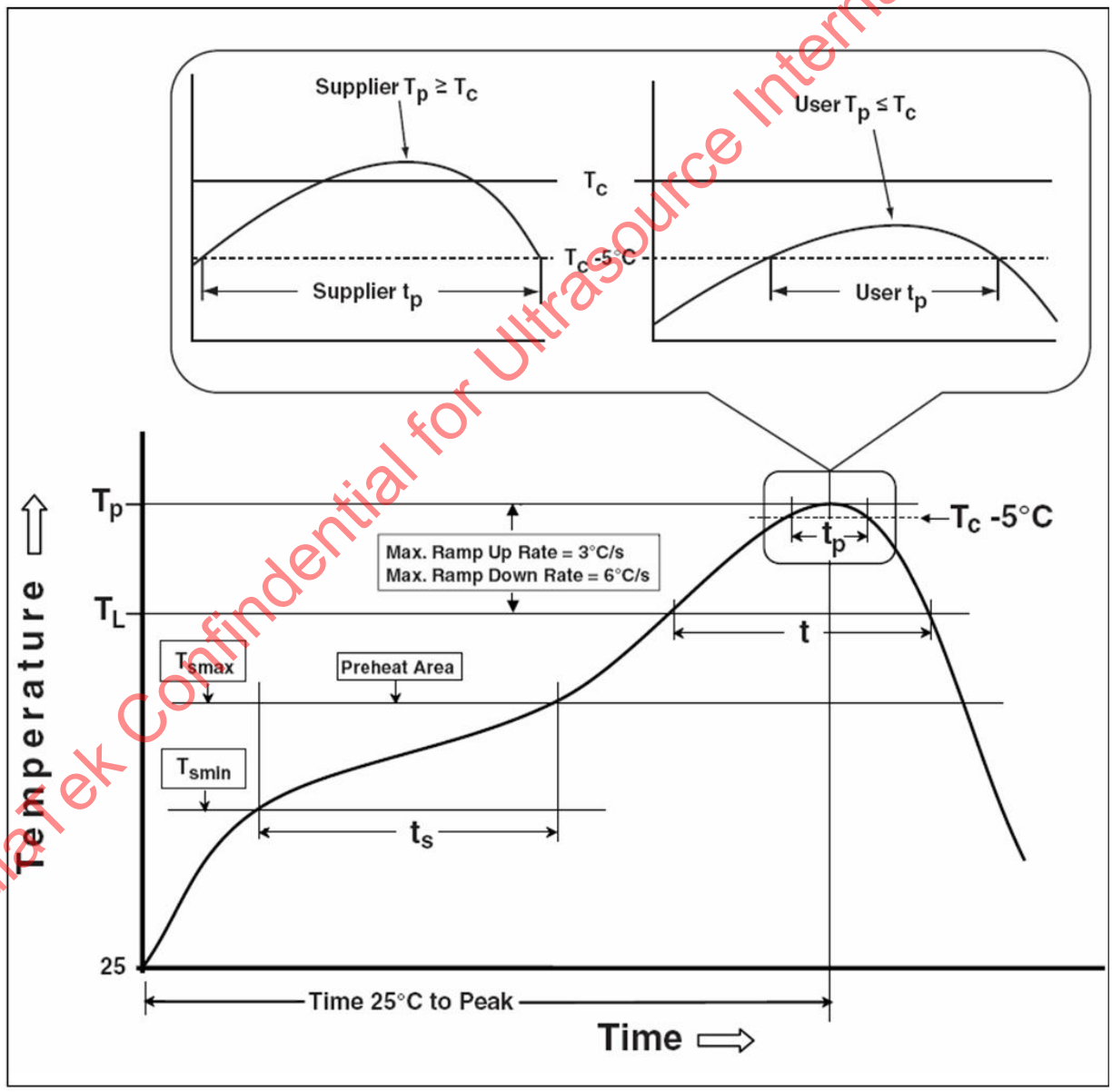


Figure 1 Classification Profile

13-2 Pre-process and Heat Treatment

Procedure: (MRT L3)

[Package opening] → [Baking] → [Humidification] → [Reflow]

A. Conditions between each step of procedure

   Be lift for duration of 2 hours or longer at temperature of 30 °C or lower and a humidity of 60% R.H. or lower.

B. Baking 125 °C, 24 hours.

C. Humidification: 30 °C, 60% R.H., 192 Hours

D. Reflow: 3 x 260 °C

14 Manual Solder Condition

The specimen should be in the as-delivered condition. Set the soldering iron at a temperature of 300 +/- 10 °C (at the iron bit). Place the iron and flux-cored solder in parallel with each and every terminal/lead on the back of the board for a duration which does not exceed 5 seconds without applying any mechanical stress on the component body.

It can also be applied under 350 +/- 10 °C at the iron bit within 3 seconds, please treat it carefully under such condition.

The chip can't do DIP soldering.

15 Storage Condition

15-1 Storage Duration

A. Notice the Sealing time.

B. 12 monthly and storage condition: <= 40°C , <= 90% R.H.

C. Warehouse control: First in and First out.

15-2 After Open the Bag

A. SMT: Should finish the SMT process within 168 hours

B. Check the humidity check card: The value should < 20% (blue), if the value >= 30% (red), it means the IC has got moisture.

C. Factory environment control: <= 30°C, <= 60% R.H.

16 Other

If a doubt related to the present specifications arises, the problem will be solved based on discussion between the both parties.