Revision History

Revised date	Contents of revision	Reason for revision	Page	Remarks
2006 3 16	1st Release	Initial Version		Ver 1.0
2006 3 20	2nd Release	Update descriptions		Ver 1.1
2006 4 25	3rd Release	Update features		Ver 1.2
2006 5 19	4th Release	Update Mark		Ver 1.3
2006 9 18	5th Release	Update ATA device features and GPIO lists		Ver 1.4
2006 12 5	6th Release	Update IO status		Ver 1.5

Contents of Specifications

No	Specifications	Page
	Revision History	1
	Contents of Specification	2
1	Applications	3
2	Type	3
3	Usage	3
4	Structure	3
5	Function	3
6	Pin Assignment	23
7	Absolute Maximum Ratings	24
8	Recommend Operation Conditions	24
9	Electrical Characteristics	25
10	Marking on Devices	35
11	Package Description	36
12	Packing Description	38
13	Solder-Reflow Condition	43
14	Manual Solder Condition	44
15	Storage Condition	45
16	Other	45

1 Applications

This present specifications are applied to IC MT1389P.

2 Type

MT1389P

3 Usage

Single Chip IC for Portable DVD Player

4 Structure

0.18um CMOS process, Silicon material, Monolithic IC, 256pin LQFP, 3.3/1.8 Dual operation voltages.

5 Function

5-1 General Description

MediaTek MT1389P is a DVD system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high quality TV encoder, USB2.0, MS/SD/MMC reader, state-of-art de-interlace processing, TCON, and high-quality TV Decoder. The MT1389P enables consumer electronics manufacturers to build high quality, feature-rich portable DVD players or any other portable multimedia devices.

World-Leading Technology: Based on MediaTek's world-leading DVD player SOC architecture, the MT1389P is the 4th generation of the DVD player SOC. It integrates the MediaTek 3rd DVD chip and 3-in-1 video controller including TVD, Scaler and Timing controller.

Rich Feature for High Valued Product: To enrich the feature of portable DVD player, the MT1389P equips a MPEG-4 video decoder supporting the MPEG-4/DivX[1] advanced simple profile (ASP). It makes the MT1389P-based Portable DVD player be capable of playback MPEG-4 content becoming more and more popular. Furthermore, MT1389P integrates TV decoder to receive external video input. It also has build-in scaler including upscaling and downscaling. Of course, it also integrates the timing controller to output the adjusting timing to the panels.

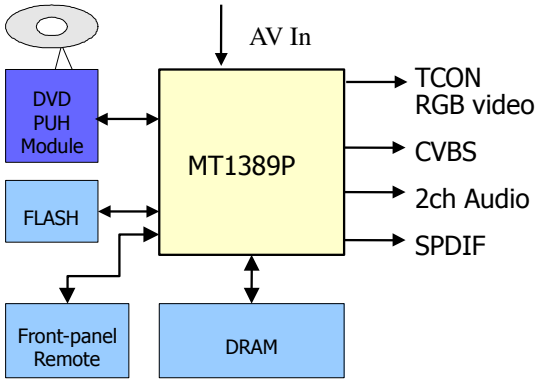
Incredible Audio/Video Quality: The progressive scan of the MT1389P utilized MediaTek's MDDi™ advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect. The 108MHz/12-bit video DAC provides users a whole new viewing experience. Built-in 2ch audio DACs could give the cost-efficient solution.

High Performance Memory Storage Device: As the core of Portable DVD players need more capability to support current multimedia contents. The MT1389P provides the interface for the 3-in-1 card reader, which supports Memory-Stick, Secure Digital Memory Card, and MultiMediaCard, to connect with the mainstream digital camera FLASH cards. For the USB application, we adopt USB2.0 High speed specification to reach rich-contents transference. USB 1.0/1.1 support data transfer at up to 1.5 Mbps for low-speed devices and up to 12 Mbps for full-speed devices. USB 2.0 will support up to 480 Mbps for high-speed devices. USB 2.0 is suitable for high-performance devices such as high-density storage devices. In addition, USB 2.0 supports old USB 1.0/1.1 software and peripherals, offering impressive and even better compatibility to customers

Integrated Panel Control system: To let the system become more easily, we integrated the TV_Decoder, Scaler and Programmable Timing Control. Build-in 3-in-1 video controller, we could save the system cost and reach the high video display quality.

Enhanced-IDE (ATAPI) device interface: MT1389P supports the ATA device interface as a DVD-ROM. Users can access data in discs via ATA/ATAPI interface.

[1] DivX is a trademark of DivXNetworks, Inc.
[2] USB High Speed : 480Mbit/sec. USB Full Speed : 12Mbit/sec.



Portable DVD Player System Diagram

Key Features

RF/Servo/MPEG integration

DivX/MPEG-4 ASP Video decoder

Support Nero-Digital

Support DivX Ultra

High Performance Audio Processor

2-channel audio DACs

MDDi: Motion-Adaptive, Pure Edge™ De-interlacing

108MHz/12-bit, 4ch TV Encoder

USB2.0 High Speed (Host/Device)

3-in-1 MS/SD/MMC reader

Built-in 3-in-1 video controller (TV decoder, Scaler and Timing controller)

Embedded ATA device interface

Applications

Portable DVD Players

Portable Multimedia Devices

5-2 General Feature lists

■ Super Integration Portable DVD player Single Chip

- High performance analog RF amplifier
- Servo controller and data channel processing
- MPEG-1/MPEG-2/JPEG video
- MPEG-4 ASP video
- Dolby AC-3/DTS
- Unified memory architecture
- USB 2.0 High Speed (Host/Device)
- MS/SD/MMC interface
- Versatile video scaling & quality enhancement
- OSD & sub-picture
- 2-D graphic engine
- Audio effect post-processor
- Audio input port
- Video Input port
- Built-in clock generator
- Built-in high quality TV encoder
- Built-in progressive video processor
- Built-in 2ch audio DACs
- Build-in TV Decoder
- Build-in Audio –in Switch for Channel-L and Channel-R
- Embedded ATA device interface

■ High Performance Analog RF Amplifier

- Programmable fc
- Dual automatic laser power control
- Defect and blank detection
- RF level signal generator

■ Speed Performance on Servo/Channel Decoding

- DVD-ROM up to 4XS
- CD-ROM up to 24XS

■ Channel Data Processor

- Digital data slicer for small jitter capability
- Built-in high performance data PLL for channel data demodulation
- EFM/EFM+ data demodulation
- Enhanced channel data frame sync protection & DVD-ROM sector sync protection

■ Servo Control and Spindle Motor Control

- Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
- Built-in ADCs and DACs for digital servo control
- Provide 2 general PWM
- Tray control can be PWM output or digital output

■ Embedded Micro Controller

- Built-in 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 1024-bytes on-chip RAM
- Up to 4M bytes FLASH-programming interface
- Supports 5/3.3-Volt. FLASH interface
- Supports power-down mode
- Supports additional serial port

■ DVD-ROM/CD-ROM Decoding Logic

- High-speed ECC logic capable of correcting one error each P-codeword or Q-codeword
- Automatic sector mode and form detection
- Automatic sector header verification
- Decoder Error Notification Interrupt that signals various decoder errors
- Provide error correction acceleration

■ Buffer Memory Controller

- Supports 16Mb/32Mb/64Mb/128Mb SDRAM
- Supports 16-bit SDRAM data bus
- Provides the self-refresh mode SDRAM
- Block-based sector addressing

■ Video Decode

- Decodes MPEG1 video and MPEG2 main level, main profile video (720x480 and 720x576)
- Decodes MPEG-4 Advanced Simple Profile
- Support DivX 3.11/4.x/5.x/6.x
- Support Nero-Digital
- Support DivX Ultra
- Smooth digest view function with I, P, and B picture decoding
- Baseline, extended-sequential and progressive JPEG image decoding
- Support CD-G titles

■ Video/OSD/SPU/HLI Processor

- Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
- Scaler for standard-definition to high-definition conversion
- 65535/256/16/4/2-color bitmap format OSD
- Automatic scrolling of OSD image
- Digital video output(CCIR601/656)

■ 2-D Graphic Engine

- Support decode Text and Bitmap
- Support line, rectangle, and gradient fill
- Support bitblt
- Chroma key copy operation

■ Audio Effect Processing

- Dolby Digital (AC-3)/EX decoding
- DTS/DTS-ES decoding
- MPEG-1 layer 1/layer 2 audio decoding
- MPEG-2 layer1/layer2 2-channel audio
- High Definition Compatible Digital (HDCD)
- Windows Media Audio (WMA)
- Dolby ProLogic II
- Concurrent multi-channel and downmix out
- IEC 60958/61937 output
  - PCM / bit stream / mute mode
  - Custom IEC latency up to 2 frames
- Pink noise and white noise generator
- Karaoke functions
  - Microphone echo
  - Microphone tone control
  - Vocal mute/vocal assistant
  - Key shift up to +/- 8 keys
  - Chorus/Flanger/Harmony/Reverb
- Channel equalizer
- 3D surround processing including virtual surround and speaker separation
- Audio –in Switch for Channel-L and Channel-R

TV Encoder

- Four 108MHz/12-bit DACs
- Support NTSC, PAL-BDGHINM, PAL-60
- Support 525p, 625p progressive TV format
- Automatically turn off unconnected channels
- Support PC monitor (VGA)
- Support Macrovision 7.1 L1, Macrovision 525P and 625P
- CGMS-A/WSS
- Closed Caption

TV Decoder

- Support CVBS analog video input
- Support NTSC, PAL-BDGHIKN, PAL-M, PAL-Nc, SECAM, NTSC-4.43, PAL-60
- Automatic signal detection
- Automatic TV standard detection
- Automatic gain control
- Automatic color control
- 5H Adaptive 2D comb filter
- Video quality adjustments and enhancements
- 2D Peaking, CTI, and flesh-tone adjustments.
- Automatically detect Macrovision protection.
- Built-in VBI slicer that support closed-caption, Teletext, CGMS-A/WSS, and other VBI services for both 525- and 625-line systems

LCD Interface

- Provide gamma correction and sharpness adjustment
- Programmable timing control
- RGB triple DAC output

MDDi ™ Progressive Scan Video

- Automatic detect film or video source
- 3:2 pull down source detection
- Advanced Motion adaptive de-interlace
- PureEdge™ edge preserving technology
- Minimum external memory requirement

External Interface

- USB2.0 High Speed (Host/Device)
- Memory-Stick, Secure Digital Memory Card, and MultiMediaCard Interface

Embedded ATA device interface

- Supports an ATA/ATA-2 PIO (Programmed input/output) data transfer mode and a multiword-DMA data transfer mode.
- Supports an ATA/ATAPI Ultra DMA transfer mode with data rate greater than 100 Mbytes/s. (Ultra DMA mode 0 ~ 5)
- Automatic sector data transfer to/from Host in GPIO, DMA or UDMA mode.
- Provides hardware macros to accelerate the ATAPI command processing.
- Supports IDE flash programming by vendor-specific ATA commands.

Outline

- 256-pin LQFP package
- 3.3/1.8-Volt. Dual operating voltages

Dolby License

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5-3 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- XmA~YmA: Output buffer driving strength from XmA to YmA

Pin	Main	Alt.	Type	Description
RF Interface (21)				
232	RFGND18		Ground	Analog ground
233	RFVDD18		Power	Analog power 1.8V
252	OSP		Analog output	RF Offset cancellation capacitor connecting
253	OSN		Analog output	RF Offset cancellation capacitor connecting
254	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	MA		Analog Input	DC coupled main-beam RF signal input A
8	MB		Analog Input	DC coupled main-beam RF signal input B
9	MC		Analog Input	DC coupled main-beam RF signal input C
10	MD		Analog Input	DC coupled main-beam RF signal input D
11	SA		Analog Input	DC coupled sub-beam RF signal input A
12	SB		Analog Input	DC coupled sub-beam RF signal input B
13	SC	TNI	Analog Input	1) DC coupled sub-beam RF signal input C 2) 3 beam satellite PD signal negative input

Pin	Main	Alt.	Type	Description
14	SD	TPI	Analog Input	1) DC coupled sub-beam RF signal input D 2) 3 beam satellite PD signal positive input
ALPC (4)				
15	MDI1		Analog Input	Laser power monitor input
16	MDI2		Analog Input	Laser power monitor input
17	LDO2		Analog Output	Laser driver output
18	LDO1		Analog Output	Laser driver output
ADC Power (2)				
244	ADCVDD3		Power	Analog 3.3V Power for ADC
245	ADCVSS		Ground	Analog ground for ADC
Reference Voltage (3)				
23	V2REFO		Analog output	Reference voltage 2.8V
24	V20		Analog output	Reference voltage 2.0V
25	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
19	SVDD3		Power	Analog power 3.3V
20	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
21	RFLVL	RFON	Analog output	1) RFRP low pass, or 2) Negative main beam summing output
22	SGND		Ground	Analog ground
26	FEO		Analog output	Focus error monitor output
27	TEO		Analog output	Tracking error monitor output
28	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (6)				
246	RFVDD3		Power	Analog Power
247	RFRPDC		Analog output	RF ripple detect output
248	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)

Pin	Main	Alt.	Type	Description
249	HRFZC		Analog Input	High frequency RF ripple zero crossing
250	CRTPLP		Analog output	Defect level filter capacitor connecting
251	RFGND		Ground	Analog Power
RF Data PLL Interface (8)				
236	JITFO		Analog output	The output terminal of RF jitter meter.
237	JITFN		Analog Input	The input terminal of RF jitter meter.
238	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.
239	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
240	LPFON		Analog Output	The negative output of loop filter amplifier
241	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
242	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
243	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
29	OP_OUT		Analog output	Op amp output.
30	OP_INN		Analog input	Op amp negative input
31	OP_INP		Analog input	Op amp positive input
32	DMO		Analog Output	Disk motor control output. PWM output.
33	FMO		Analog Output	Feed motor control. PWM output.
34	TROPENPWM		Analog Output	Tray PWM output / Tray open output.
35	PWMOUT1	ADIN	Analog Output	1) 1st General PWM output, or 2) ADIN
36	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
37	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
51	FG (Digital pin)		Inout 2MA, SMT, PU	1) Motor Hall sensor input 2) GPIO16
General Power/Ground (22)				

Pin	Main	Alt.	Type	Description
50, 55,93, 142,160, 174, 205	DVDD18		Power	1.8V power pin for internal digital circuitry
53, 81,178	DVSS18		Ground	1.8V Ground pin for internal digital circuitry
49, 65,96,118, 131,145,156, 170, 200	DVDD3		Power	3.3V power pin for internal digital circuitry
52, 90, 148	DVSS33		Ground	3.3V Ground pin for internal digital circuitry
Micro Controller and Flash Interface (47)				
62	HIGHA0		Inout 4~16MA, SR PU	Microcontroller address 8
74	HIGHA1		Inout 4~16MA, SR PU	Microcontroller address 9
73	HIGHA2		Inout 4~16MA, SR PU	Microcontroller address 10
72	HIGHA3		Inout 4~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Inout 4~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Inout 4~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Inout 4~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Inout 4~16MA, SR PU	Microcontroller address 15
89	AD7		Inout 4~16MA, SR	Microcontroller address/data 7
86	AD6		Inout 4~16MA, SR	Microcontroller address/data 6
85	AD5		Inout 4~16MA, SR	Microcontroller address/data 5
84	AD4		Inout 4~16MA, SR	Microcontroller address/data 4
83	AD3		Inout 4~16MA, SR	Microcontroller address/data 3

Pin	Main	Alt.	Type	Description
82	AD2		Inout 4~16MA, SR	Microcontroller address/data 2
80	AD1		Inout 4~16MA, SR	Microcontroller address/data 1
79	AD0		Inout 4~16MA, SR	Microcontroller address/data 0
92	IOA0		Inout 4~16MA, SR PU	Microcontroller address 0 / IO
77	IOA1		Inout 4~16MA, SR PU	Microcontroller address 1 / IO
56	IOA2		Inout 4~16MA, SR PU	Microcontroller address 2 / IO
57	IOA3		Inout 4~16MA, SR PU	Microcontroller address 3 / IO
58	IOA4		Inout 4~16MA, SR PU	Microcontroller address 4 / IO
59	IOA5		Inout 4~16MA, SR PU	Microcontroller address 5 / IO
60	IOA6		Inout 4~16MA, SR PU	Microcontroller address 6 / IO
61	IOA7		Inout 4~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Inout 4~16MA, SR PU	Flash address 16
91	A17		Inout 4~16MA, SR PU	Flash address 17
63	IOA18		Inout 4~16MA, SR SMT, PD	Flash address 18 / IO
64	IOA19		Inout 4~16MA, SR SMT, PD	Flash address 19 / IO
75	IOA20		Inout 4~16MA, SR SMT, PD	Flash address 20 / IO

Pin	Main	Alt.	Type	Description
87	IOA21		Inout 4~16MA, SR SMT, PD	1) Flash address 21 / IO 2) While External FLASH size <= 4MBytes(32 Mbits) 3) **ATA_DEV MONITOR3** 4) GPIO
54	IOA22		Inout 4~16MA, SR SMT, PD	1) Flash address 22 / IO 2) While External FLASH size <= 8MBytes(64 Mbits) 3) **ATA_DEV MONITOR7** 4) GPIO
88	ALE		Inout 4~16MA, SR SMT, PU	1) Microcontroller address latch enable 2) GPO 3) **ATA_DEV MONITOR6**
78	IOOE#		Inout 4~16MA, SR SMT	Flash output enable, active low / IO
66	IOWR#		Inout 4~16MA, SR SMT, PU	Flash write enable, active low / IO
76	IOCS#		Inout 4~16MA, SR SMT	Flash chip select, active low / IO
94	UWR#		Inout 4~16MA, SR SMT, PU	1) Microcontroller write strobe, active low 2) GPO 3) **ATA_DEV MONITOR 5**
95	URD#		Inout 4~16MA, SR SMT, PU	1) Microcontroller read strobe, active low 2) GPO 3) **ATA_DEV MONITOR 4**
97	UP1_2		Inout 4MA, SR SMT, PU	Microcontroller port 1-2
98	UP1_3		Inout 4MA, SR SMT, PU	Microcontroller port 1-3
99	UP1_4		Inout 4MA, SR SMT, PU	Microcontroller port 1-4
100	UP1_5		Inout 4MA, SR SMT, PU	Microcontroller port 1-5
101	UP1_6	SCL	Inout 4MA, SR SMT, PU	1) Microcontroller port 1-6 2) I^2C clock pin
102	UP1_7	SDA	Inout 4MA, SR SMT, PU	1) Microcontroller port 1-7 2) I^2C data pin

Pin	Main	Alt.	Type	Description
103	UP3_0	RXD	Inout 4MA, SR SMT, PU	1) Microcontroller port 3-0 2) 8032 RS232 RXD
104	UP3_1	TXD	Inout 4MA, SR SMT, PU	1) Microcontroller port 3-1 2) 8032 RS232 TXD
105	UP3_4	RXD SCL	Inout 4MA, SR SMT, PU	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin
106	UP3_5	TXD SDA	Inout 4MA, SR SMT, PU	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
Audio interface (20)				
201	ALRCK	GPIO7	Input 2~8MA, PD	1) Audio left/right channel clock 2) GPIO7 3) **ATA_DEV DD1**
202	ABCK	GPIO8	Input 2~8MA, PD	1) Audio bit clock 2) GPIO8 3) **ATA_DEV DD14**
203	ACLK	GPIO9	Input 2~8MA, PD	1) Audio DAC master clock 2) GPIO9 3) **ATA_DEV DD0**
197	ASDATA0	GPIO4	Input 2~8MA, PD	1) Audio serial data 0 (Front-Left/Front-Right) 2) GPIO4 3) TCON Delta Output Order 4) **ATA_DEV DD12**
198	ASDATA1	GPIO5	Input 2~8MA, PD	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) GPIO5 3) TCON Horizontal Sampling/Shift Clock 3 4) **ATA_DEV DD2**
199	ASDATA2	GPIO6	Input 2~8MA, PD	1) Audio serial data 2 (Center/LFE) 2) GPIO6 3) TCON Horizontal Sampling/Shift Clock 2 4) **ATA_DEV DD13**
204	ASDATA3	GPIO10	Input 2~8MA, PD	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) GPIO10 3) **ATA_DEV DD15**
206	ASDATA4	GPIO11	Input 2~8MA, PD	1) Audio serial data 4 (Down-mixed Left/Right) 2) GPIO11 3) **ATA_DEV DMARQ**

Pin	Main	Alt.	Type	Description
207	MC_DATA	GPIO12 YUVCLK	Input 2~8MA, PD	1) Microphone serial input 2) GPIO12 3) Digital Video output clock (CCIR656) 4) **ATA_DEV DIOW#**
208	SPDIF	GPIO	Inout 2~8MA, SR : ON/OFF Non-pull	1) SPDIF output 2) GPIO
222	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
223	APLLCAP		Analog Inout	APLL External Capacitance connection
224	APLLVSS		Ground	Ground pin for audio clock circuitry
225	ADACVSS2		Ground	Ground pin for AUDIO DAC circuitry
226	ADACVSS1		Ground	Ground pin for AUDIO DAC circuitry
227	AR	GPIO0	Analog output/ Digital GPIO	1) AUDIO DAC Right channel output 2) While internal AUDIO DAC not used: a. GPIO0
228	AVCM		Analog	AUDIO DAC reference voltage
229	AL	GPIO1	Analog output/ Digital GPIO	1) AUDIO DAC Left Surround channel output 2) While internal AUDIO DAC not used: a. GPIO1
230	ADACVDD2		Power	3.3V power pin for AUDIO DAC circuitry
231	ADACVDD1		Power	3.3V power pin for AUDIO DAC circuitry
Video Interface (13)				
196	VCOM	GPIO3	Analog	1) VCOM DAC Output 2) GPIO3 3) TCON Output Polarity 4) **ATA_DEV MONITOR2**
195	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
194	VREF		Analog	Bandgap reference voltage
193	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
192	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
191	CVBS		Analog	Analog CVBS output
190	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
189	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
188	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
187	G	Y/G	Analog	Green or Y

Pin	Main	Alt.	Type	Description
186	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
185	B	B/Cb/Pb	Analog	Blue or CB
184	R	R/Cr/Pr	Analog	Red or CR
TVD (13)				
209	DGND_ADC		TVD Ground	TVD Ground for digital circuits
210	DVDD33_ADC		TVD Power	TVD power pin 3.3V for digital circuits
211	AGND_ADC		TVD Ground	TVD Ground for analog circuits
212	AVDD33_ADC		TVD Power	TVD power pin 3.3V for analog circuits
213	CVBS_INN	Battery Detect	Analog Inout	1) TVD Test input 2) Battery detection
214	AVDD33_VFE		TVD Power	TVD power pin 3.3V for video front end circuits
215	CVBS_INP		Analog Inout	Video input signal
216	AGND_VFE		TVD Ground	TVD ground pin for video front end circuits
217	VFE_TSTN		Analog Inout	Video front end test pin 1
218	VFE_TSTP		Analog Inout	Video front end test pin 2
219	AGND18_VPLL		VPLL power	VPLL power pin 1.8V
220	VPLL_TST		Analog Inout	VPLL test pin
221	AVDD18_VPLL		VPLL ground	VPLL ground pin
FPD (10)				
183	HCK	GPIO	Input 2~8MA PD	1) TCON Horizontal Sampling/Shift Clock 2) **ATA_DEV RESET#**
182	HSTR	GPIO	Input 2~8MA PD	1) TCON Horizontal Start Pulse Right 2) **ATA_DEV DD7**
181	HSTL	GPIO	Input 2~8MA PD	1) TCON Horizontal Start Pulse Left 2) **ATA_DEV DD8**
180	HOE	GPIO	Input 2~8MA PD	1) TCON Horizontal Output Enable/Data Load 2) **ATA_DEV DD6**
179	LR	GPIO	Input 2~8MA PD	1) TCON Horizontal Scan Direction 2) **ATA_DEV DD9**
177	VOE	GPIO	Input 2~8MA PD	1) TCON Vertical Output Enable 2) **ATA_DEV DD5**

Pin	Main	Alt.	Type	Description
176	UD	GPIO	Input 2~8MA PD	1) TCON Vertical Scan Direction 2) ATA_DEV DD10
175	VCK	GPIO	Input 2~8MA PD	1) TCON Vertical Shift Clock 2) ATA_DEV DD4
173	VSTU	GPIO	Input 2~8MA PD	1) TCON Vertical Start Pulse Up 2) ATA_DEV DD11
172	VSTD	GPIO	Input 2~8MA PD	1) TCON Vertical Start Pulse Down 2) ATA_DEV DD3
Card interface and GPIO (16)				
171	GPIO100	Y_0	Input 2~8MA PD	1) GPIO 2) Digital Video output Y bit 0 (CCIR656) 3) ATA_DEV DIOR#
169	GPIO101	Y_1	Input 2~8MA PD	1) GPIO 2) Digital Video output Y bit 1 (CCIR656) 3) ATA_DEV IORDY
168	GPIO102	Y_2	Input 2~8MA PD	1) GPIO 2) Digital Video output Y bit 2 (CCIR656) 3) ATA_DEV CSEL
167	GPIO103	Y_3	Input 2~8MA PD	1) GPIO 2) Digital Video output Y bit 3 (CCIR656) 3) ATA_DEV DMACK#
166	SD_D3	Y_4	Input 2~8MA PD	1) SD DATA3(IO) 2) Digital Video output Y bit 4 (CCIR656) 3) GPIO 4) ATA_DEV INTRQ
165	SD_D2	Y_5	Input 2~8MA PD	1) SD DATA2(IO) 2) Digital Video output Y bit 5 (CCIR656) 3) GPIO 4) ATA_DEV IOCS16#
164	SD_D1	Y_6	Input 2~8MA PD	1) SD DATA1(IO) 2) Digital Video output Y bit 6 (CCIR656) 3) GPIO 4) ATA_DEV DA1
163	MS_D3	Y_7	Input 2~8MA PD	1) MS DATA3 (IO) 2) Digital Video output Y bit 7 (CCIR656) 3) HSYNC or VSYNC 4) GPIO 5) ATA_DEV PDIAG#

Pin	Main	Alt.	Type	Description
162	MS_D2	C_0	Input 2~8MA PD	1) MS DATA2(IO) 2) Digital Video output C bit 0 3) HSYNC or VSYNC 4) GPIO 5) **ATA_DEV DA0**
161	MS_D1	C_1	Input 2~8MA PD	1) MS DATA1(IO) 2) Digital Video output C bit 1 3) GPIO 4) **ATA_DEV DA2**
159	MS_CLK	C_2	Input 2~8MA PD	1) MS CLK 2) Digital Video output C bit 2 3) GPIO 4) **ATA_DEV CS0#**
158	MS_BS	C_3	Input 2~8MA PD	1) MS BS 2) Digital Video output C bit 3 3) GPIO 4) **ATA_DEV CS1#**
157	MS_D0	C_4	Input 2~8MA PD	1) MS DATA0(IO) 2) Digital Video output C bit 4 3) GPIO 4) **ATA_DEV DASP#**
130	SD_CMD	C_5	Input 2~8MA PD	1) MS CLK 2) Digital Video output C bit 5 3) GPIO20
112	SD_CLK	C_6	Input 2~8MA PD	1) MS BS 2) Digital Video output C bit 6 3) GPIO21 4) **ATA_DEV MONITOR0**
110	SD_D0	C_7	Input 2~8MA PD	1) MS DATA0(IO) 2) Digital Video output C bit 7 3) GPIO22 4) INT0# 5) **ATA_DEV MONITOR1**
USB2.0 (9)				
40	USB_DP		Analog Inout	USB port DPLUS analog pin
41	USB_DM		Analog Inout	USB port DMINUS analog pin
42	VDD33_USB		USB Power	USB Power pin 3.3V
43	VSS33_USB		USB Ground	USB ground pin
44	PAD_VRT		Analog Inout	USB generating reference current
45	VDD18_USB		USB Power	USB Power pin 1.8V
46	VSS18_USB		USB Ground	USB ground pin
47	USB_XTALO		Output	30M crystal out for USB 2.0
48	USB_XTALI		Input	30M crystal in for USB 2.0

Pin	Main	Alt.	Type	Description
MISC (7)				
107	ICE		Input 4MA, SR SMT, PD	Microcontroller ICE mode enable
108	PRST#		Input 4MA, SR SMT, PU	Power on reset input, active low
109	IR		Input 4MA, SR SMT	IR control signal input
234	XTALO		Output	27M crystal out
235	XTALI		Input	27M crystal in
38	AGND33_DMPLL		Analog Ground	Analog ground for DMPLL
39	AVDD33_DMPLL		Analog Power	Analog power pin 3.3V for DMPLL
Dram Interface (38)				
155	RA4		output 2~16MA SMT, PD	DRAM address 4
154	RA5		output 2~16MA SMT, PD	DRAM address 5
153	RA6		output 2~16MA SMT, PD	DRAM address 6
152	RA7		output 2~16MA SMT, PD	DRAM address 7
151	RA8		output 2~16MA SMT, PD	DRAM address 8
150	RA9		output 2~16MA SMT, PD	DRAM address 9
149	RA11		output 2~16MA SMT, PD	DRAM address bit 11
147	CKE		output 2~16MA SMT, PD	DRAM clock enable

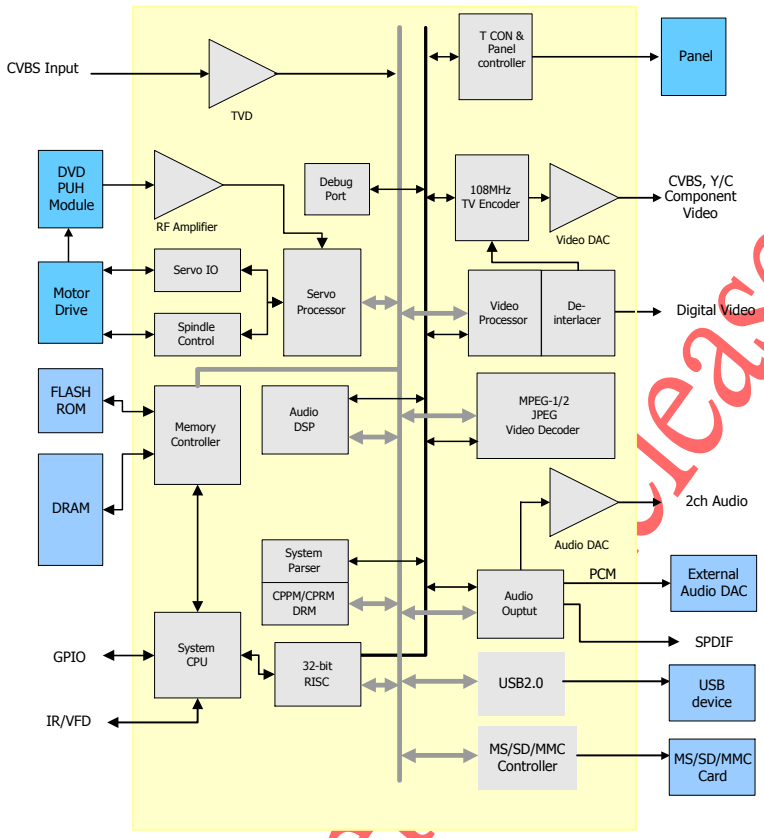
Pin	Main	Alt.	Type	Description
146	RCLK		output 2~16MA PD	Dram clock
144	RA3		output 2~16MA SMT, PD	DRAM address 3
143	RA2		output 2~16MA SMT, PD	DRAM address 2
141	RA1		output 2~16MA SMT, PD	DRAM address 1
140	RA0		output 2~16MA SMT, PD	DRAM address 0
139	RA10		output 2~16MA SMT, PD	DRAM address 10
138	BA1		output 2~16MA SMT, PD	DRAM bank address 1
137	BA0		output 2~16MA SMT, PD	DRAM bank address 0
136	RCS#		output 2~16MA SMT, PD	DRAM chip select, active low
135	RAS#		output 2~16MA SMT, PD	DRAM row address strobe, active low
134	CAS#		output 2~16MA SMT, PD	DRAM column address strobe, active low
133	RWE#		output 2~16MA SMT, PD	DRAM Write enable, active low
132	DQM1		output 2~16MA SMT, PD	Data mask 1
129	RD8		inout 2~16MA	DRAM data 8
128	RD9		inout 2~16MA	DRAM data 9
127	RD10		inout 2~16MA	DRAM data 10
126	RD11		inout 2~16MA	DRAM data 11

Pin	Main	Alt.	Type	Description
125	RD12		inout 2~16MA	DRAM data 12
124	RD13		inout 2~16MA	DRAM data 13
123	RD14		inout 2~16MA	DRAM data 14
122	RD15		inout 2~16MA	DRAM data 15
121	RD0		inout 2~16MA	DRAM data 0
120	RD1		inout 2~16MA	DRAM data 1
119	RD2		inout 2~16MA	DRAM data 2
117	RD3		inout 2~16MA	DRAM data 3
116	RD4		inout 2~16MA	DRAM data 4
115	RD5		inout 2~16MA	DRAM data 5
114	RD6		inout 2~16MA	DRAM data 6
113	RD7		inout 2~16MA	DRAM data 7
111	DQM0		output 2~16MA SMT, PD	Data mask 0

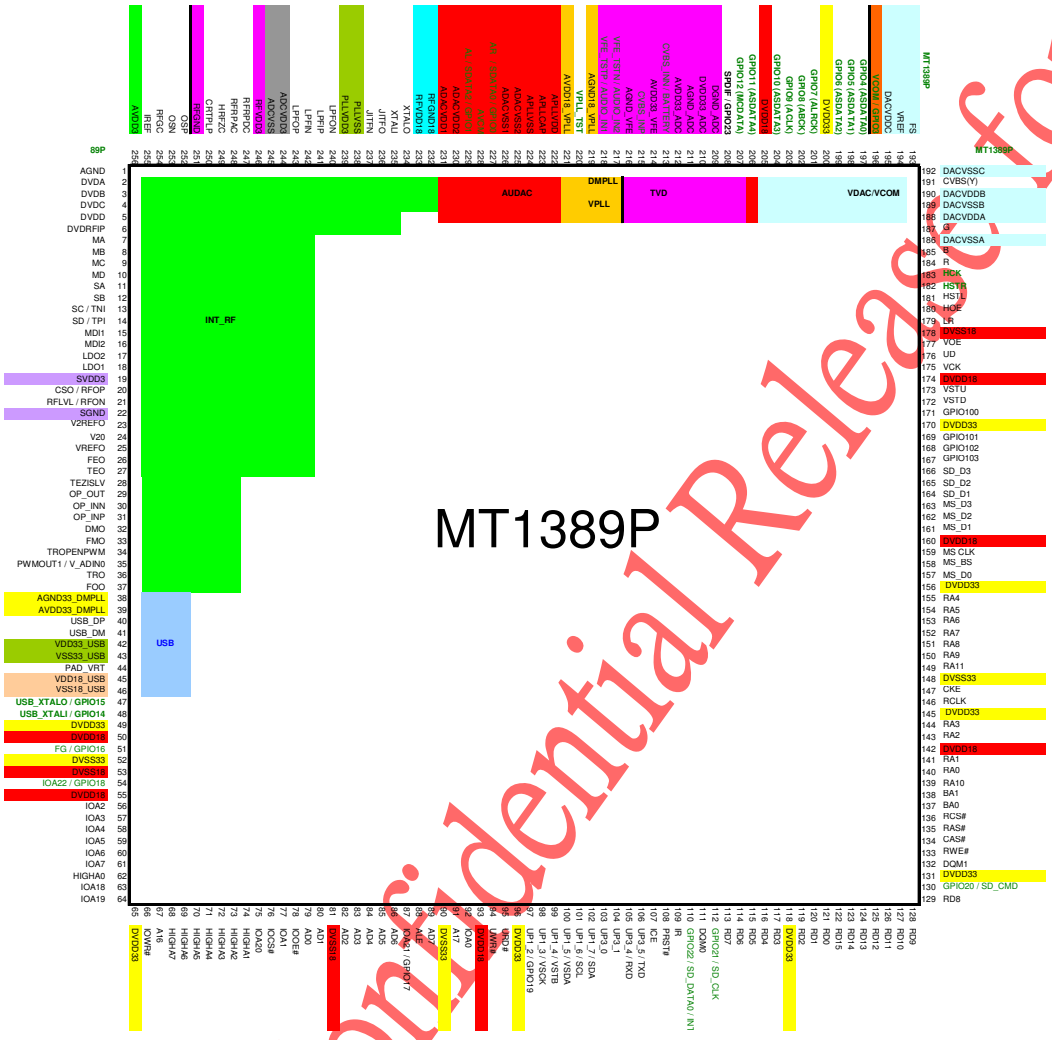
Note:

1. The Main column is the main function, Alt. Means alternative function.

5-4 Functional Block



6 Pin Assignment



7 Absolute Maximum Ratings

Symbol	Parameters	Value	Unit
VDD3	3.3V Supply voltage	-0.3 to 3.6	V
VDD2	1.8V Supply voltage	-0.3 to 2.1	V
VDDA	Analog Supply voltage	-0.3 to 3.6	V
V_{IN}(3.3V)	Input Voltage (3.3V IO)	-0.3 to 3.63	V
V_{IN}(5V-tolerance)	Input Voltage (5V-tolerance IO)	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.3 to VDD3+0.3	V
T_{STG}	Storage Temperature	-45 to 150	°C

8 Recommend Operation Condition

Symbol	Parameters	Min	Typ	Max	Unit
T_{OP}	Operating Temperature	0		70	°C
T_J	Junction Operation Temp.	0	25	115	°C
VDD3	3.3V Supply voltage	3.0	3.3	3.6	V
VDD2	1.8V Supply voltage	1.7	1.8	2.0	V
VDDA	Analog Supply voltage	3.0	3.3	3.6	V
V_{IH} (1.8V)	Input voltage high (1.8V IO)	1.05	-	-	V
V_{IL} (1.8V)	Input voltage low (1.8V IO)	-	-	0.69	V
V_{IH} (3.3V)	Input voltage high (3.3V IO)	2.0	-	-	V
V_{IL} (3.3V)	Input voltage low (3.3V IO)	-	-	0.8	V
I_{IH}	High level input current			10	UA
I_{IL}	Low level input current	-10			UA
P_D	Power dissipation		1.5		W
P_{DOWN}	Power down mode			0.1	W
fclk	Input frequency of clock		27		MHz

9 Electrical Characteristics

9-1 DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{OH} (1.8V)	Output voltage high (1.8V IO) (*I_{OH} = 2 ~ 16mA)	1.22	-	-	V
V_{OL} (1.8V)	Output voltage low (1.8V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
V_{OH} (3.3V)	Output voltage high (3.3V IO) (*I_{OH} = 2 ~ 16mA)	2.4	-	-	V
V_{OL} (3.3V)	Output voltage low (3.3V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
FOO_{OFF}	Offset voltage between FOO zero output and V_{REF}	-50	0	50	mV
TRO_{OFF}	Offset voltage between TRO zero output and V_{REF}	-40	0	40	mV
DMO_{OFF}	Offset voltage between DMO zero output and V_{REF}	-30	0	30	mV

Note * : The driving current of some IO pad are programmable according to the different application and environment . All setting will be defined according to the F/W progress and test result.

9-2 Built-in Audio-DAC Characteristics

带格式的: 项目符号和编号

Note *: All parameters is measured on MediaTek's DVD player reference DVD board, the actual performance depends on different PCB design.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{out}	Output swing level: Digital i/p level =0 dBFS , ADACVDD =3.3V (V_{out} = 1.0 * ADACVDD / 3.3)	0.9	1.0	1.1	V_P
Ro	Output impedance @ 1kHz		50	100	
R_{L_min}	Minimum resister load	5			K
C_{L_max}	Maximum capacitor load			20	PF
S/(THD+N)	S/(THD+N) @ 0 dBFS; f_{in} = 1kHz; Fs = 48kHz, A-weighted		90		dBr(A)
DR	Dynamic Range		88		dBr(A)
SNR	Signal to noise ratio; A-weighted		95		dBr(A)
Channel Separation	Close-talk of Left and Right Channel		85		dB

9-3 Built-in Video-DAC Specifications

带格式的: 项目符号和编号

Input Codes for Video Application:

	NTSC	NTSC w/setup	525_I	525_I w/setup	525_P
WHITE (235)	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3290
BLACK (16)	960	1120	960	1120	1008

PEDESTAL	960	960	960	960	1008
SYNC TIP	64	64	64	64	64

	525_P w/s	**PAL**	**625_I**	**625_P**	**RGB**
WHITE (235)	---	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 2282
BLACK (16)	---	1008	1008	1008	0
PEDESTAL	---	1008	1008	1008	-
SYNC TIP	---	64	64	64	-

9-4 Video Output Voltage Level:

High Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 2.2 KOhm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3237 V, R_{LOAD} = 150 Ohm

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

Low Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 560 Ohm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3 V, R_{LOAD} = 37.5 Ohm (75 Ohm || 75 Ohm)

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

9-5 Video DAC DC Electrical Characteristics

(Operating Free-Air Temperature, AVDD 3.3V, DVDD = 3.3V).

带格式的: 项目符号和编号

Analog Output		**MIN**	**TYP**	**MAX**	**UNIT**
Full Scale Output Current CVBS/Y/C/R/G/B	(low impedance mode)	33.6	34.6	34.9	mA
Full Scale Output Current CVBS/Y/C/R/G/B	(high impedance mode)	8.40	8.65	8.73	mA
LSB current CVBS/Y/C/R/G/B	(low impedance mode)	32.8	33.8	34.1	uA
LSB current CVBS/Y/C/R/G/B	(high impedance mode)	8.20	8.45	8.52	uA
DAC-to-DAC Mis-Matching		--	1.28	--	%
Output Compliance		0	--	1.35	V
DAC Output Delay		--	1.5	10	ns
DAC Rise/Fall Time		--	2.1	5	
Voltage Reference					

Reference Voltage Output		1.27		V
Reference Input Current		2.267		MA
Static Performance				
DAC Resolution		12		Bits
DNL Differential Non-Linearity	+/-0.2	*/-0.25	+/-0.3	LSB
INL Integral Non-Linearity	+/-0.35	*/-0.4	+/-0.49	LSB
Dynamic Performance				
Differential Gain		0.8	1.5	%
Differential Phase		0.6	1.5	°
S/N Ratio	70			dB
Power Supply				
Supply Voltage	3.0	3.3	3.6	V

9-6 RF specification

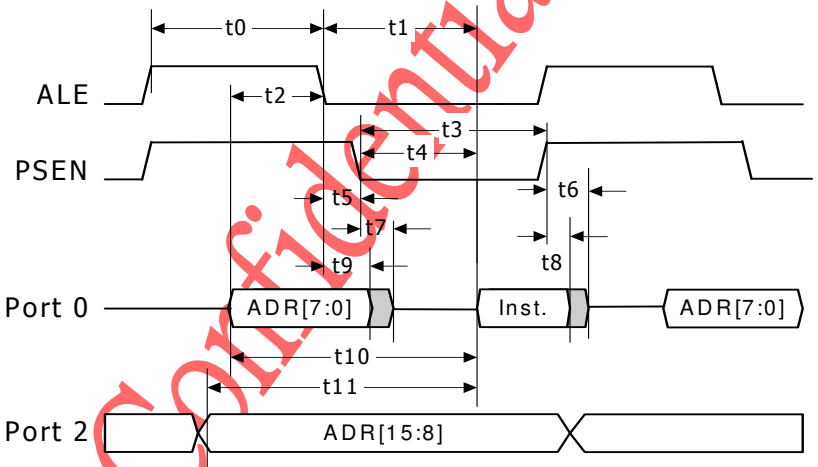
Item	Designator	Conditions	Min	Typ	Max	Unit
3.3V POWER			3.00	3.30	3.60	Volts
Power Down Mode		Enable power down	10	27	50	mA
		Chip Reset	90	151	200	mA
Reference Voltage	V20	Force current =0A	1.85	1.99	2.15	Volts
Reference Voltage	VREFO	Force current =0A	1.25	1.39	1.55	Volts
Reference Voltage	V2REFO	Force current =0A	2.65	2.78	2.95	Volts
APC1(CD)	MDI1	0Ah=10 ;APC1 on MDI1=180mV	166	184	202	mV
	LDO1	0Ah=00 ;APC1 off	3.00	3.28		V
	MDI1→LDO1	0Ah=10; APC1 on	212	254	295	V/V
APC2(DVD)	MDI2	0Bh=10 ;APC2 on MDI2=180mV	166	184	202	mV
	LDO2	0Bh=00 ;APC2 off	3.00	3.28		V

Item	Designator	Conditions	Min	Typ	Max	Unit
	MDI2→LDO2	0Bh=10; APC2 on High gain	210	265	298	V/V
Focusing Error Gain	MA → FEO	05h=30; low gain With 10KHz Sin Input	7.5	10.3	11.5	dB
Focusing Error Frequency Response	MA → FEO	05h=7C; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	23.9		dB
Focusing Error Common Mode Gain	MA → FEO MB → FEO	05h=3F; low gain With 10KHz Sin Input		-34	-20	dB
Focusing Error H/L Gain	MA → FEO	Toggle 05h bit5 : FELG With 10KHz Sin Input	2.75	2.99	3.25	V/V
Focusing Error offset Adjustment step	Input Floating Measure FEO	Toggle 4Dh : FEOS[6:0]	65	103	140	mV
Focusing Error THD	MA → FEO	05h=7C; low gain With 10KHz Sin Input	30	54		dB
Central Servo Gain	MA → CSO	06h=F0; low gain With 10KHz Sin Input	12.5	14.1	15.5	dB
Central Servo Frequency Response	MA → CSO	06h=FF; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	21.4		dB
Central Servo Common Mode Gain	MA → CSO MB → CSO	06h=F0; low gain With 10KHz Sin Input		-30	-10	dB
Central Servo H/L Gain	MA → CSO	Toggle 06h bit5 : CSOLG With 10KHz Sin Input	2.75	2.97	3.25	V/V
Central Servo offset Adjustment step	Input Floating Measure CSO	Toggle 4Eh : CSOOS[6:0]	65	108	140	mV
Central Servo THD	MA → CSO	06h=F0; low gain With 10KHz Sin Input	30	53		dB

Item	Designator	Conditions	Min	Typ	Max	Unit
Tracking Error Gain	MA → TEO	07h=70; low gain With 10KHz Sin Input	13	15	17	dB
Tracking Error Frequency Response	MA → TEO	07h=70; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	24.2		dB
Tracking Error Common Mode Gain	MA → TEO MB → TEO	07h=7F; low gain With 10KHz Sin Input		-22	-10	dB
Tracking Error H/L Gain	MA → TEO	Toggle 07h bit6, 5 With 10KHz Sin Input	4	5.8	8	V/V
Tracking Error offset Adjustment step	Input Floating Measure TEO	Toggle 4Fh : TEOS[6:0]	65	110	140	mV
Tracking Error THD	MA → TEO	07h=7F; low gain With 10KHz Sin Input	30	42		dB
RFL Gain	MA → LVL	08h=60; low gain With 10KHz Sin Input	-6.5	-4.6	-3.5	dB
RFL Frequency Response	MA → LVL	08h=7F; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	22.7		dB
RFL H/L Gain I	MA → LVL	Toggle 09h bit1 : LVLATN With 10KHz Sin Input	0.3	0.52	0.7	V/V
RFL H/L Gain II	SA → LVL	Toggle 09h bit2 : SBADHG With 10KHz Sin Input	2.5	2.77	3.1	V/V
RFL offset Adjustment step	Input Floating Measure LVL	Toggle 50h : LVLOS[6:0]	65	113	140	mV
RFL THD	MA → LVL	08h=7F; low gain With 10KHz Sin Input	30	44		dB

9-7 Micro Controller Interface

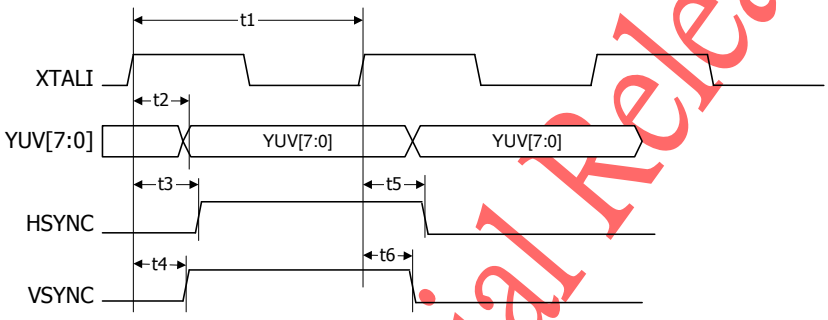
Parameter	Symbol	Min.	Max.	Units
Oscillator Frequency	1/Tf	0	23.3	MHz
ALE Pulse Width	T0	1.5Tf-5		ns
ALE Low to Valid Instruction	T1		2.5Tf-20	ns
ALE Low to PSEN Low	T5	0.5Tf-5		ns
Address Valid to ALE Low	T2	0.5Tf-5		ns
Address Hold After ALE Low	T9	0.5Tf-5		ns
PSEN Pulse Width	T3	2.0Tf-5		ns
PSEN Low to Valid Instruction	T4		2.0Tf-20	ns
Input Instruction Hold After PSEN high	T8	0		ns
Input Instruction Float After PSEN high	T6		1.0Tf-5	ns
Port 0 Address to Valid Instruction	T10		3.0Tf-20	ns
Port 2 Address to Valid Instruction	T11		3.5Tf-20	ns
PSEN Low to Address Float	T7		0	ns



Program Memory Read Cycle Timing Diagram

9-8 Digital Video Output Interface

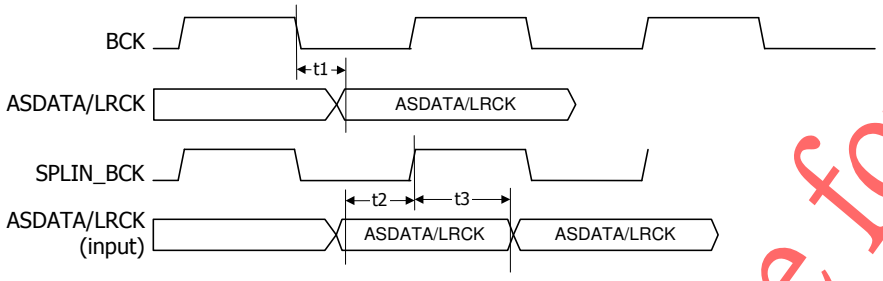
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/T1		27		MHz
YUV digital output delay	T2			15	ns
HSYNC Rising delay	T3			15	ns
VSYNC Rising delay	T4			15	ns
HSYNC Falling delay	T5			20	ns
VSYNC Falling delay	T6			20	ns



Digital Video Output Interface Timing Diagram

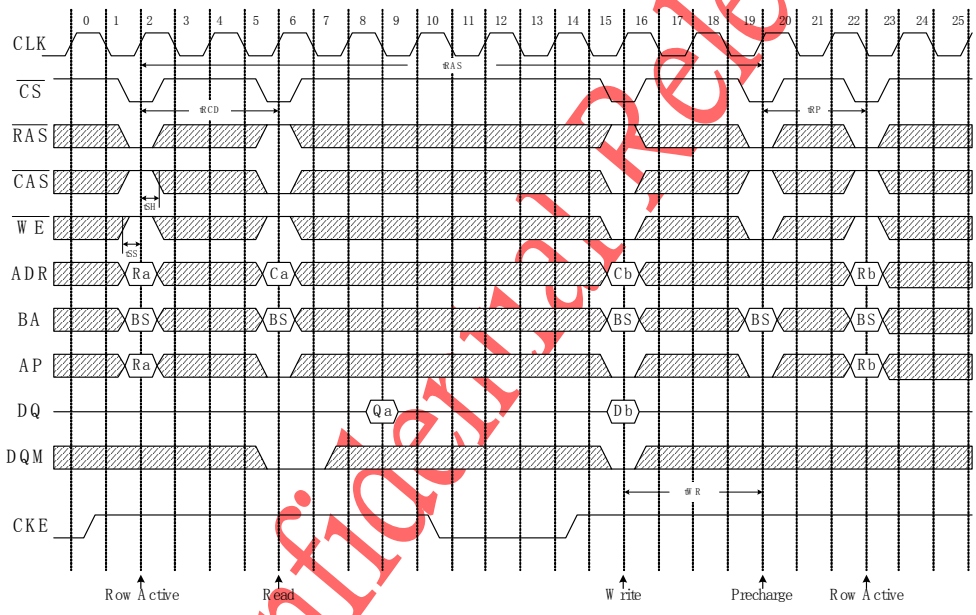
9-9 SPDIF I/O Interface

Parameter	Symbol	Min	Typ	Max	Units
BCK negative edge to ASDATA valid	T1	1.0		3.0	ns
ASDATA/LRCK input setup	T2			3.0	ns
ASDATA/LRCK input hold	T3	1.2			ns



SPDIF Input/Output Timing Diagram

9-10 DRAM Interface



Parameter		Symbol	-6		-7		-8		Units
			Min	Max	Min	Max	Min	Max	
CLK cycle time	CAS latency = 3	tCC	7.5	-	7.5	-	8	-	ns
	CAS latency = 2		8		10		10		
SDRAM input setup time		tSS	1.5		1.75		2		ns
SDRAM input hold time		tSH	1		1		1		ns

Active to Precharge command period		tRAS	42	100K	49	100K	48	100K	ns
Precharge to Active command period		tRP	18		20		20		ns
Active to read/write command delay		tRCD	18		20		20		ns
Write recovery time	CL = 3	tWR	6		7		8		ns
	CL = 2		10		10		10		

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

-6T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		42ns	18ns	18ns	6ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	2	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		49ns	20ns	20ns	7ns/10ns
133MHz (7.5ns)	3	7	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7.5T

(Unit: number of clock)

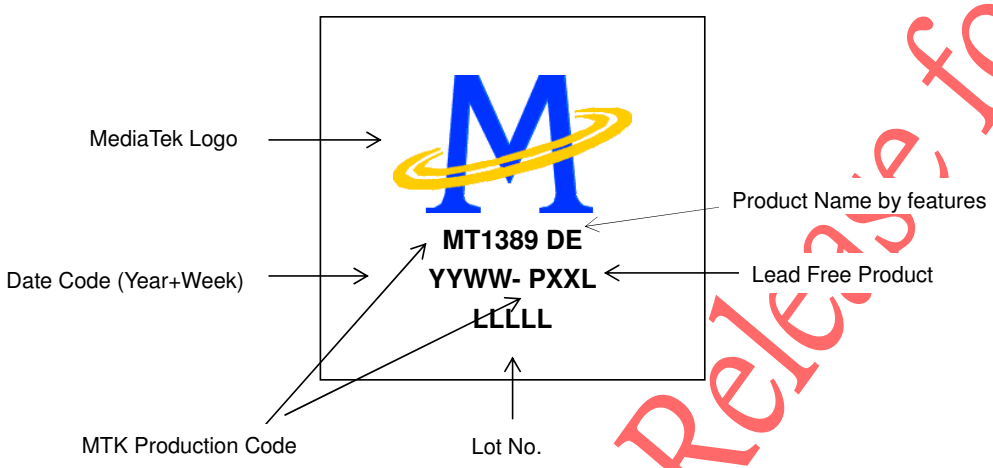
Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		45ns	20ns	20ns	7.5ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-8T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		48ns	20ns	20ns	8ns/10ns
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	3	5	2	2	1

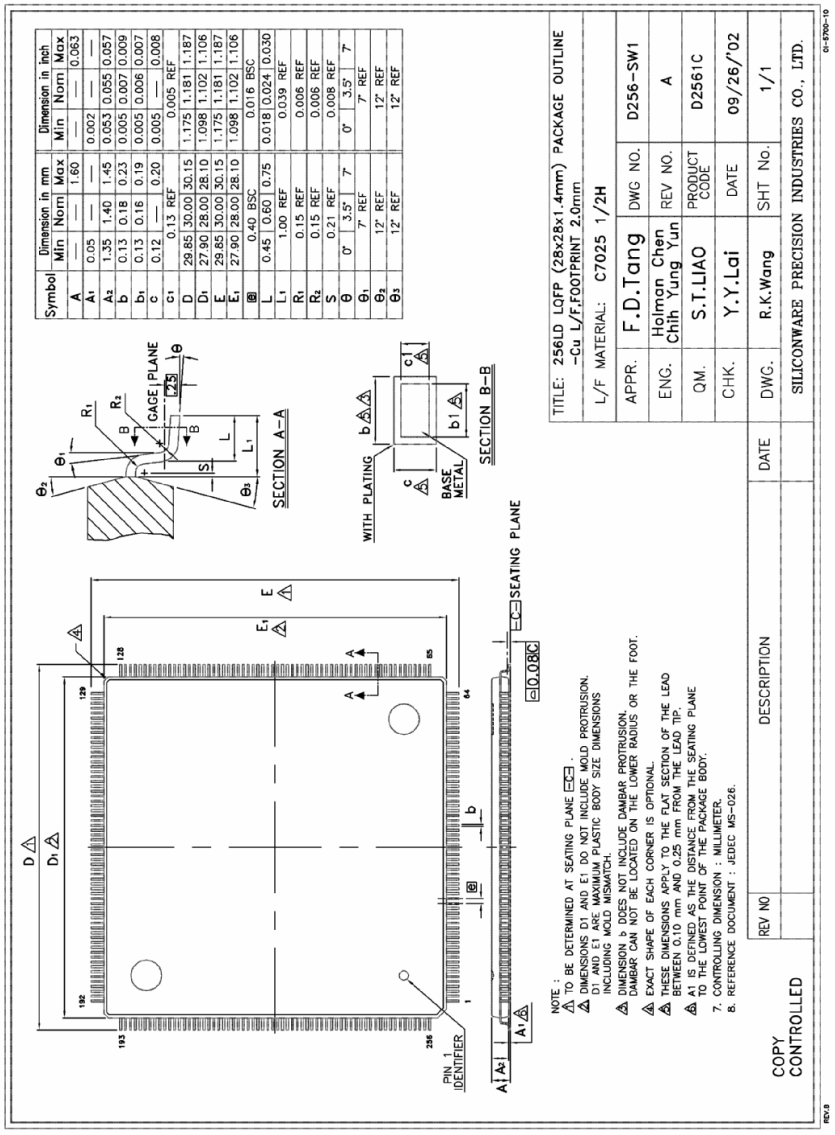
10 Marking on Devices



11 Package Description

11-1 Package Outline Dimension

The bend lead are controlled under the criteria 3mil.



11-2 Weight of the chip

2.51g

11-3 Material and Finish of Lead Terminals

For Normal Package, (Materials of terminal is Sn(85%) and Pb (15%)and thickness is 300~800u inch.

For Lead-free Package, (Materials of terminal is Sn(98%) and Bi (2%)and thickness is 300~800u inch, similar as SnPb.

11-4 Package Material

Lead frame: Cu

Epoxy: 2200S

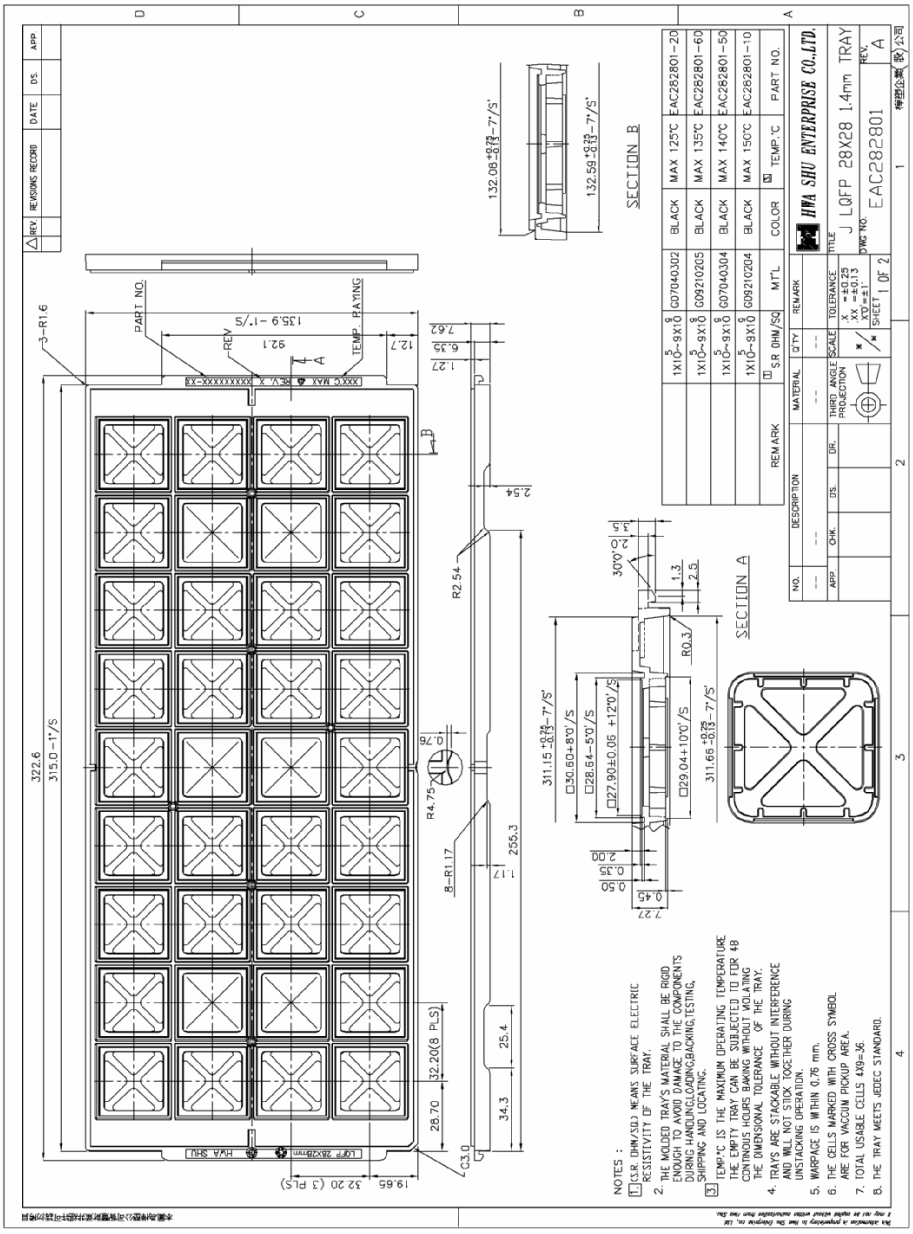
Molding compound: G700

12 Packing Description

Package	Pin / Ball count	EA / Tray	Tray / Box	Full Box Q'ty	Box / Carton	Full carton Q'ty
LQFP	256	36	10	360	6	2160

12-1 Tray Description

36ea/ Hard Tray (150°C resistance).



12-2 Desiccants

Size: 110*120 mm.

Weight: 66g

12-3 Aluminum Foil Bag

Size: 250*500 mm.

Thickness: 0.12 +/- 0.005 mm.

Surface impedance: 10^{8}-10^{12} Ohm/SQ

12-4 Box Description

Material: 3 Layer B corrugated paper.

Strength: 1176000 PA.

Box size: 355(L)*157(W)*90.5(H) mm.

Printing: Black (words, warning, index)

12-5 Side Plank

Material: 5 Layer AB corrugated paper

Strength: 1793400 PA.

Size: 405(L)*237(W) mm.

Fixture: 3 pieces of EPE (recyclable material).

Thickness: 20 mm.

12-6 Carton Description

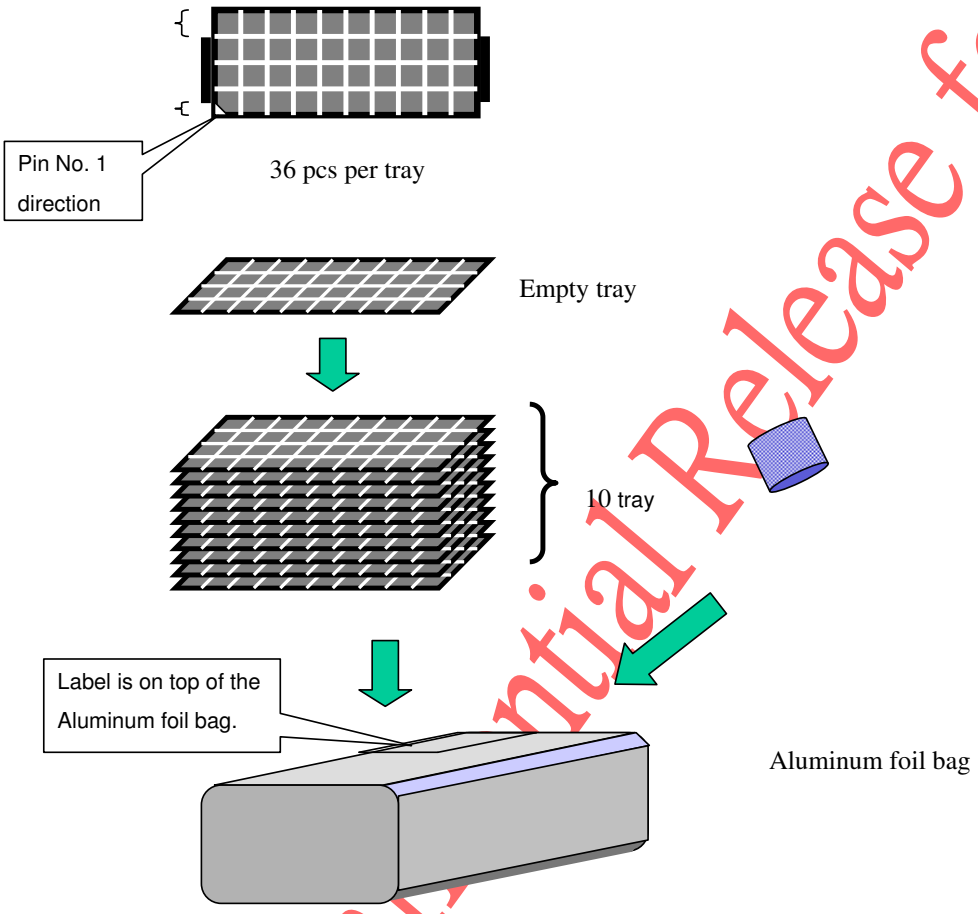
Material: 5 Layer AB corrugated paper.

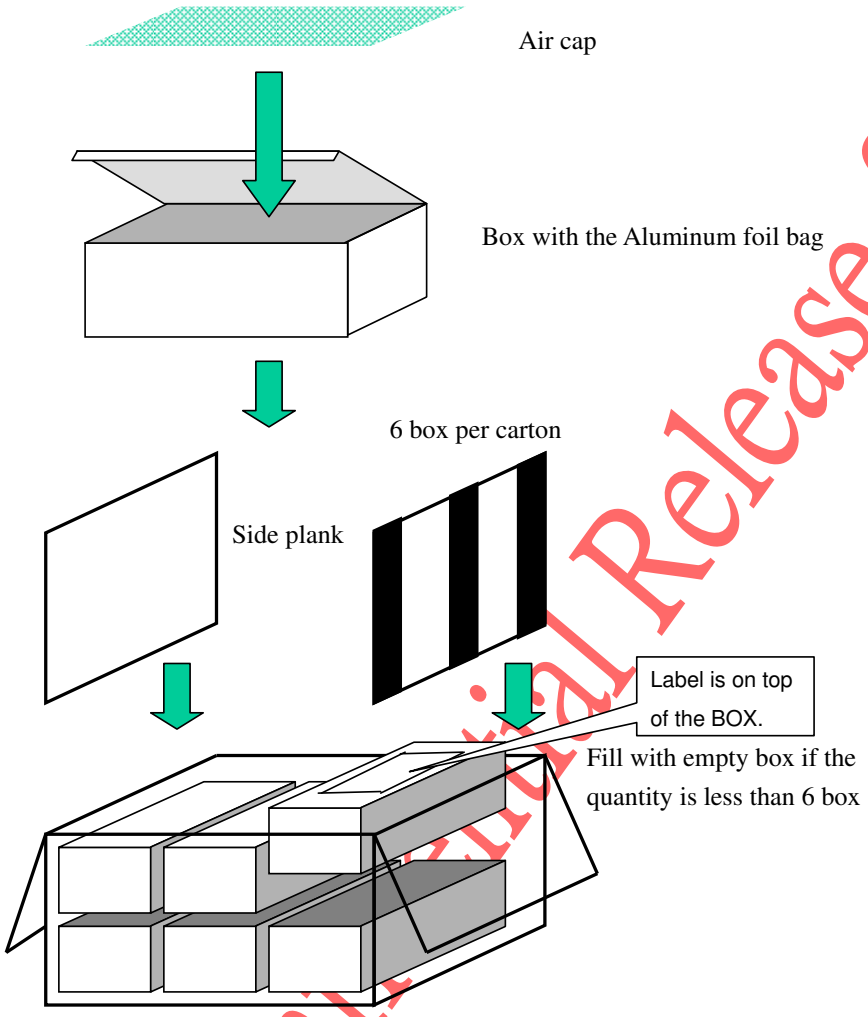
Strength: 1793400 PA.

Carton size: 558(L)*428(W)*264(H) mm.

Printing: Black (words, warning, index)

12-7 Packing Flow





13 Solder-Reflow Condition

13-1 Reflow Condition

MTK can guarantee 3 times IR reflow base on the reflow curve.

Average ramp-up rate (217°C to peak) : 3 °C /sec. max.

Preheat : 150~200°C、60~180 seconds

Temperature maintained above 217°C : 60~150 seconds

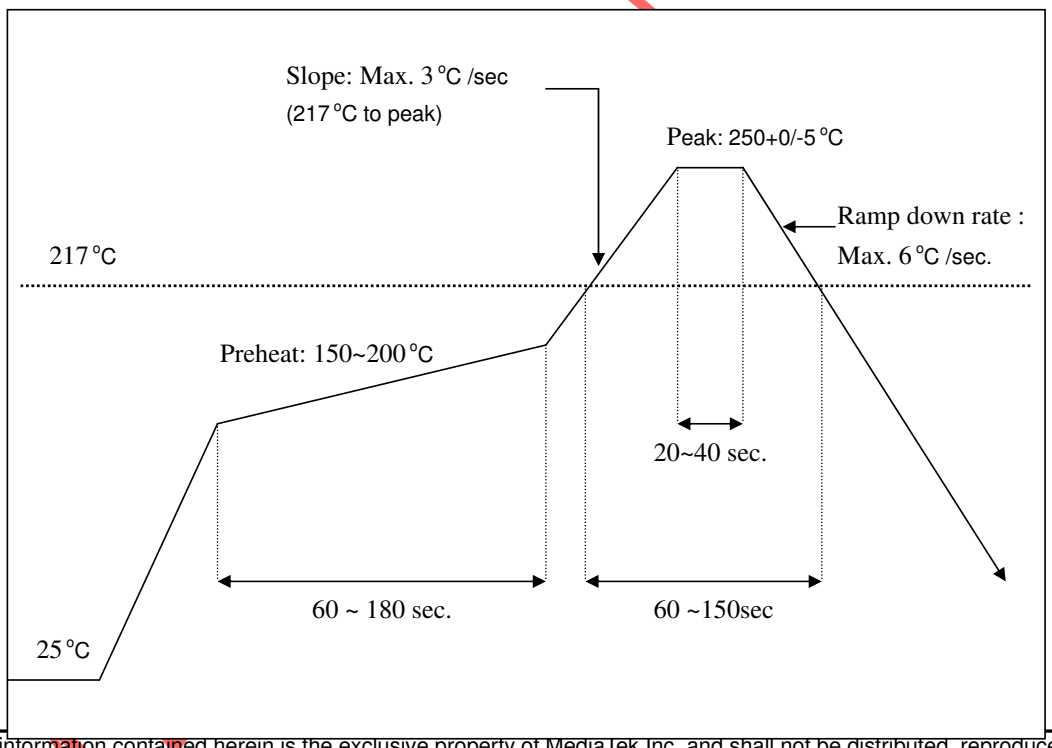
Time within 5°C of actual peak temperature : 20 ~ 40 sec.

Peak temperature : 250+0/-5°C

Ramp-down rate : 6°C /sec. max.

Time 25°C to peak temperature : 8 minutes max.

Cycle interval : 5 minus



13-2 Pre-process and Heat Treatment

Procedure: (MRT L3)

[Package opening] → [Baking] → [Humidification] → [Reflow]

A. Conditions between each step of procedure

Be lift for duration of 2 hours or longer at temperature of 30 °C or lower and a humidity of 60% R.H. or lower.

B. Baking 125 °C, 24 hours.

C. Humidification: 30 °C, 60% R.H., 192 Hours

D. Reflow: 3 x 260oC

14 Manual Solder Condition

The specimen should be in the as-delivered condition. Set the soldering iron at a temperature of 300 +/- 10 °C (at the iron bit). Place the iron and flux-cored solder in parallel with each and every terminal/lead on the back of the board for a duration which does not exceed 5 seconds without applying any mechanical stress on the component body.

It can also be applied under 350 +/- 10 °C at the iron bit within 3 seconds, please treat it carefully under such condition.

The chip can't do DIP soldering.

15 Storage Condition

15-1 Storage Duration

A. Notice the Sealing time.

B. 12 monthly and storage condition: <= 40°C , <= 90% R.H.

C. Warehouse control: First in and First out.

15-2 After Open the Bag

A. SMT: Should finish the SMT process within 168 hours

B. Check the humidity check card: The value should < 20% (blue), if the value >= 30% (red), it means the IC has got moisture.

C. Factory environment control: <= 30°C, <= 60% R.H.

16 Other

If a doubt related to the present specifications arises, the problem will be solved based on discussion between the both parties.