Circuit Diagram and Component Layout

MPEG IC Block Diagrams

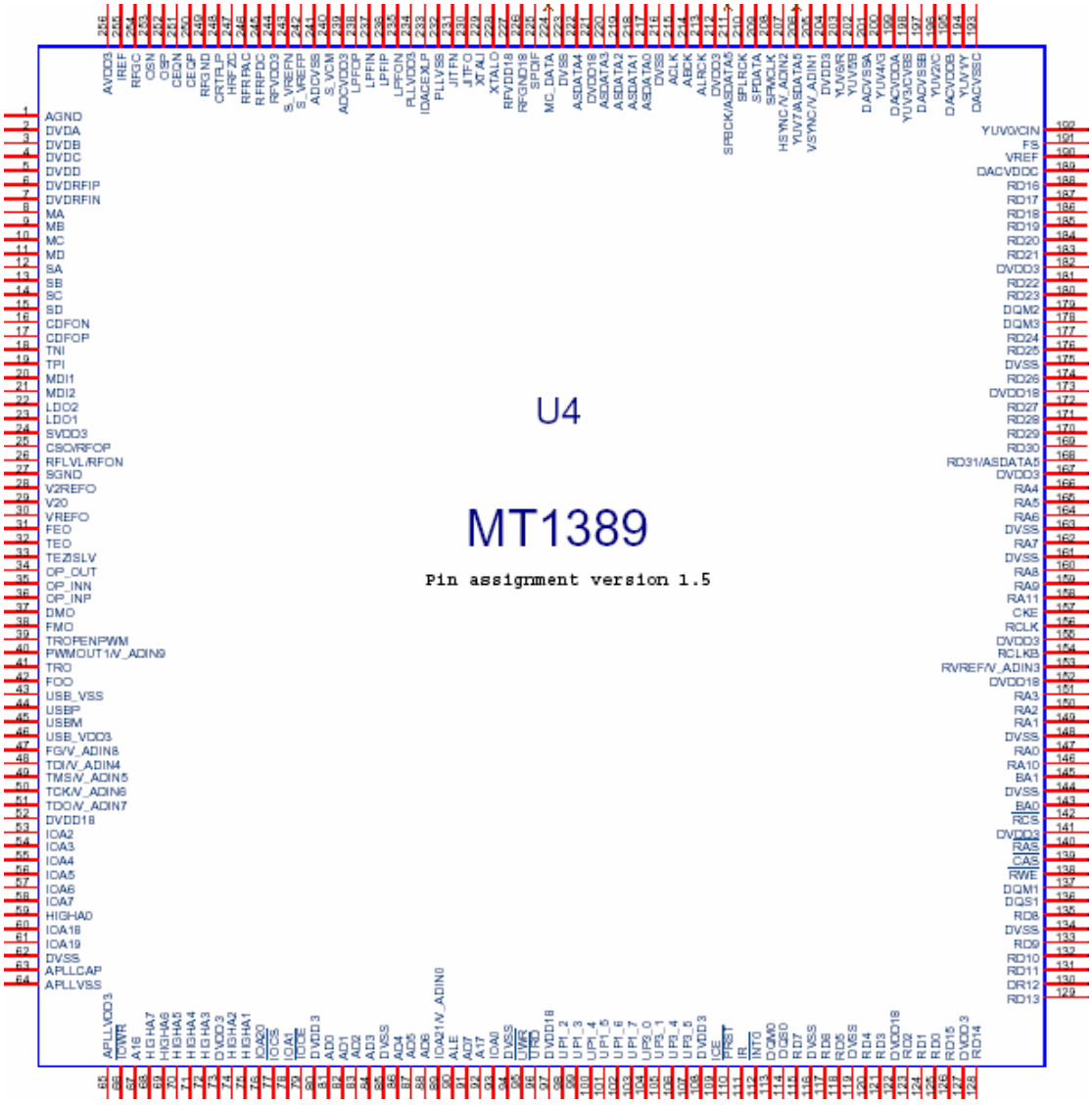

Fig. 2-1 MT1389

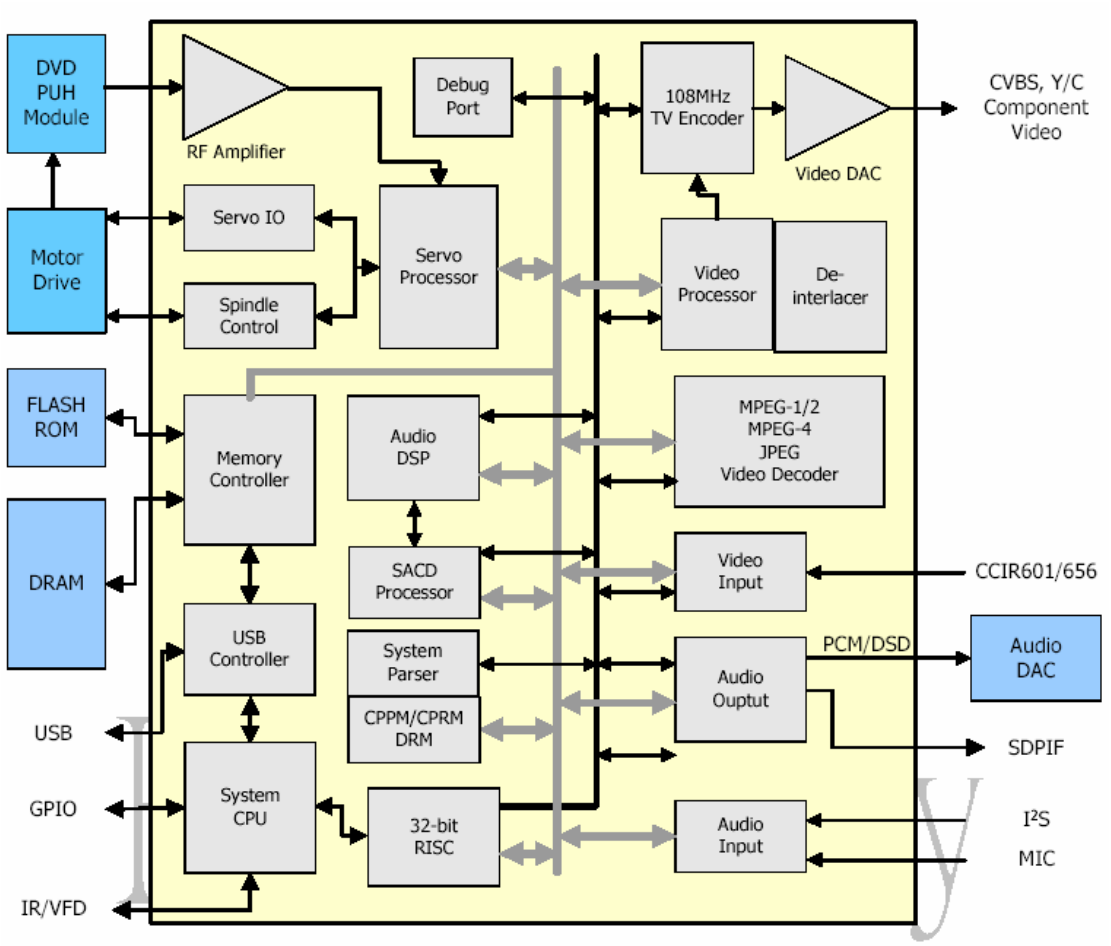

Fig. 2-2 Functional block diagram

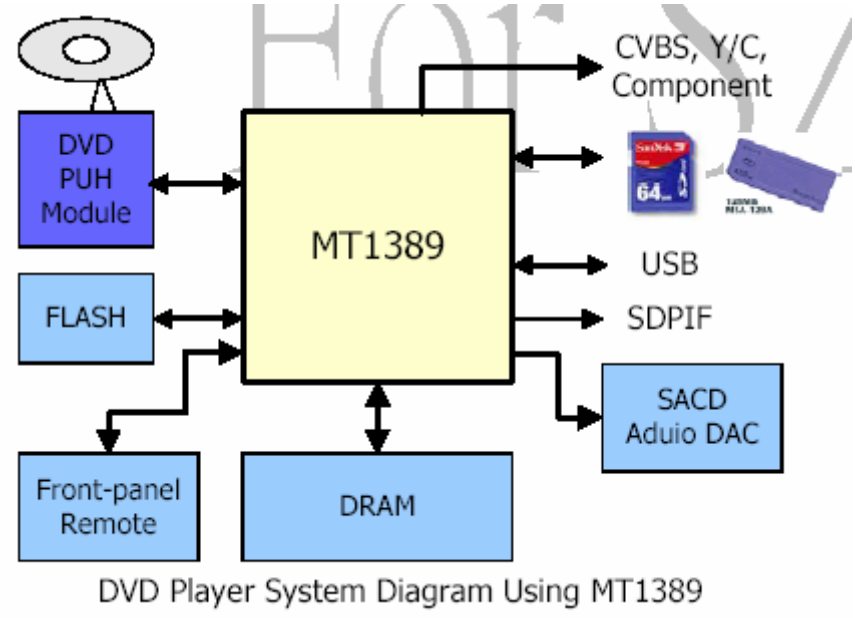

Fig.2-3 DVD Player system Diagram

Table1. 1389C Pin Description

Abbr. :

SR : Slew Rate

PU : Pull Up

PD : Pull Down

SMT : Schmitt Trigger

2MA~16MA : Output buffer driving strength.

Pin	Main	Alt.	Type	Description
			RF Interface (28)	
226	RFGND18		Ground	Analog ground
227	RFVDD18		Power	Analog power 1.8V
250	CEQP		Analog	
251	CEQN		Analog	
252	OSP		Analog	RF Offset cancellation capacitor connecting
253	OSN		Analog	RF Offset cancellation capacitor connecting
254	RFGC		Analog	RF AGC loop capacitor connecting for DVD-ROM
255	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
256	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
ALPC (4)				
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
ADC for SACD (5)				
239	ADCVDD3		Power	Analog 3.3V Power for ADC
240	S_VCM		Analog	
241	ADCVSS		Ground	Analog ground for ADC
242	S_VREFP		Analog	
243	S_VREFN		Analog	
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
26	RFLVL	RFON		1) RFRP low pass, or 2) Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output, or
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog	
Analog Servo Interface (6)				
244	RFVDD3		Power	Analog Power
245	RFRPDC		Analog output	RF ripple detect output
246	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
247	HRFZC		Analog Input	High frequency RF ripple zero crossing
248	CRTPLP		Analog	Defect level filter capacitor connecting
249	RFGND		Ground	Analog Power
RF Data PLL Interface (9)				
230	JITFO		Analog output	The output terminal of RF jitter meter.
231	JITFN		Analog Input	The input terminal of RF jitter meter.
232	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
233	IDACEXLP		Analog	
234	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
235	LPFON		Analog Output	The negative output of loop filter amplifier
236	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
237	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
238	LPFOP		Analog Output	The positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENPWM		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT1	V_ADIN9	Analog Output	1) 1st General PWM output, or 2) Version AD input 9
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
47	FG (Diogital pin)	V_ADIN8	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for V_ADIN8	1) Motor Hall sensor input, or 2) Version AD input 8
General Power/Ground (32)				
52,97,122,152,173,221	DVDD18		Power	1.8V power pin for internal digital circuitry
85,116,144,163,216	DVSS		Ground	1.8V Ground pin for internal digital circuitry
73,80,108,127,141,155,167,182,212	DVDD3		Power	3.3V power pin for internal digital circuitry
62,94,119,134,148,161,175,223	DVSS		Ground	3.3V Ground pin for internal digital circuitry
204	DVDD3		Power	3.3V power pin Video DAC digital circuitry only
63	APLLCAP		Analog	APLL External Capacitance connection
64	APLLVSS		Ground	Ground pin for audio clock circuitry
65	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
Micro Controller and Flash Interface (48)				

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
59	HIGHA0		Inout 2~16MA, SR PU	Microcontroller address 8
75	HIGHA1		Inout 2~16MA, SR PU	Microcontroller address 9
74	HIGHA2		Inout 2~16MA, SR PU	Microcontroller address 10
72	HIGHA3		Inout 2~16MA, SR PU	Microcontroller address 11
71	HIGHA4		Inout 2~16MA, SR PU	Microcontroller address 12
70	HIGHA5		Inout 2~16MA, SR PU	Microcontroller address 13
69	HIGHA6		Inout 2~16MA, SR PU	Microcontroller address 14
68	HIGHA7		Inout 2~16MA, SR PU	Microcontroller address 15
91	AD7		Inout 2~16MA, SR	Microcontroller address/data 7
88	AD6		Inout 2~16MA, SR	Microcontroller address/data 6
87	AD5		Inout 2~16MA, SR	Microcontroller address/data 5
86	AD4		Inout 2~16MA, SR	Microcontroller address/data 4
84	AD3		Inout 2~16MA, SR	Microcontroller address/data 3
83	AD2		Inout 2~16MA, SR	Microcontroller address/data 2
82	AD1		Inout 2~16MA, SR	Microcontroller address/data 1
81	AD0		Inout 2~16MA, SR	Microcontroller address/data 0
93	IOA0		Inout 2~16MA, SR PU	Microcontroller address 0 / IO
78	IOA1		Inout 2~16MA, SR PU	Microcontroller address 1 / IO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
53	IOA2		Inout 2~16MA, SR PU	Microcontroller address 2 / IO
54	IOA3		Inout 2~16MA, SR PU	Microcontroller address 3 / IO
55	IOA4		Inout 2~16MA, SR PU	Microcontroller address 4 / IO
56	IOA5		Inout 2~16MA, SR PU	Microcontroller address 5 / IO
57	IOA6		Inout 2~16MA, SR PU	Microcontroller address 6 / IO
58	IOA7		Inout 2~16MA, SR PU	Microcontroller address 7 / IO
67	A16		Output 2~16MA, SR	Flash address 16
92	A17		Output 2~16MA, SR	Flash address 17
60	IOA18		Inout 2~16MA, SR SMT	Flash address 18 / IO
61	IOA19		Inout 2~16MA, SR SMT	Flash address 19 / IO
76	IOA20		Inout 2~16MA, SR SMT	Flash address 20 / IO
89	IOA21	V_ADIN0	Inout 2~16MA, SR SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: I) Version AD input port 0, or II) GPIO
90	ALE		Inout 2~16MA, SR PU, SMT	Microcontroller address latch enable
79	IOOE#		Inout 2~16MA, SR SMT	Flash output enable, active low / IO
66	IOWR#		Inout 2~16MA, SR SMT	Flash write enable, active low / IO
77	IOCS#		Inout 2~16MA, SR PU, SMT	Flash chip select, active low / IO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
95	UWR#		Inout 2~16MA, SR PU, SMT	Microcontroller write strobe, active low
96	URD#		Inout 2~16MA, SR PU, SMT	Microcontroller read strobe, active low
98	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
99	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
100	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
101	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
102	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
103	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
104	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
105	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
106	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin
107	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
111	IR		Input SMT	IR control signal input
112	INT0#		Inout 2~16MA, SR PU, SMT	Microcontroller external interrupt 0, active low
Audio interface (14)				

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
208	SPMCLK	SCLK0	Inout	1) Audio DAC master clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 clock pin II) GPIO
209	SPDATA	SDIN0	Inout	1) Audio data of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-in II) GPIO
210	SPLRCK	SDO0	Inout	1) Audio left/right channel clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 data-out II) GPIO
211	SPBCK	SDCS0 ASDATA5	Inout	1) Audio bit clock of SPDIF input 2) While SPDIF input is not used: I) Serial interface port 0 chip select II) Audio serial data 5 part I : DSD data sub-woofer channel or Microphone output III) GPIO
213	ALRCK		Inout 4MA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I) 1: use external 378 II) 0: use internal 378
214	ABCK	Fs64	Output 4MA	1) Audio bit clock 2) Phase de-modulation
215	ACLK		Inout 4MA	Audio DAC master clock
217	ASDATA0		Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) DSD data left channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation
218	ASDATA1		Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) DSD data right channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO
219	ASDATA2		Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) 2) DSD data left surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
220	ASDATA3		Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) DSD data right surround channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) GPIO
222	ASDATA4	INT1#	Inout 4MA PD SMT	1) Audio serial data 4 (Down-mixed Left/Right) 2) DSD data center channel 3) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 4) While only 2 channels output: I) Microcontroller external interrupt 1 II) GPIO
224	MIC_DATA	INT2#	Inout	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPIO
225	SPDIF		Output 2~16MA, SR : ON/OFF	SPDIF output
Video Interface (18)				
189	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
190	VREF		Analog	Bandgap reference voltage
191	FS		Analog	Full scale adjustment
192	YUV0	CIN	Output 4MA, SR	1) Video data output bit 0 2) Compensation capacitor
193	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
194	YUV1	Y	Output 4MA, SR	1) Video data output bit 1 2) Analog Y output
195	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
196	YUV2	C	Output 4MA, SR	1) Video data output bit 2 2) Analog chroma output
197	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
198	YUV3	CVBS	Output 4MA, SR	1) Video data output bit 3 2) Analog composite output
199	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry
200	YUV4	Y/G	Output 4MA, SR	1) Video data output bit 4 2) Green or Y
201	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
202	YUV5	B/Cb/Pb	Output 4MA, SR	1) Video data output bit 5 2) Blue or CB

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
203	YUV6	R/Cr/Pr	Output 4MA, SR	1) Video data output bit 6 2) Red or CR
205	VSYN	V_ADIN1	Inout 4MA, SR SMT	1) Vertical sync input/output 2) While no External TV-encoder: I) Vertical sync for video-input II) Version AD input port 1 III) GPIO
206	YUV7	INT3# ASDATA5	Inout 4MA, SR SMT	1) Video data output bit 7 2) While no External TV-encoder: I) Microcontroller external interrupt 3 II) Audio serial data 5 part II : DSD data sub-woofer channel or Microphone output III) GPIO
207	HSYN	INT4# V_ADIN2	Inout 4MA, SR SMT	1) Horizontal sync input/output 2) While no External TV-encoder: I) Horizontal sync for video-input II) Microcontroller external interrupt 4 III) Version AD input port 2 IV) GPIO
MISC (8)				
43	USB_VSS			USB ground pin
44	USBP			USB port DPLUS analog pin
45	USBM			USB port DMINUS analog pin
46	USB_VDD3			USB Power pin 3.3V
110	PRST#		Input PU, SMT	Power on reset input, active low
109	ICE		Input PD, SMT	Microcontroller ICE mode enable
228	XTALO		Output	27M crystal out
229	XTALI		Input	27M crystal in
Dram Interface (63) (Sorted by position)				
188	RD16	LLC_CLK		1) DRAM data 16 2) While using 16-bits wide DRAM: I) Line Locked Clock input/output II) GPIO
187	RD17	YUVIN0		1) DRAM data 17 2) While using 16-bits wide DRAM: I) Video input data 0 II) GPIO
186	RD18	YUVIN1		1) DRAM data 18 2) While using 16-bits wide DRAM: I) Video input data 1 II) GPIO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
185	RD19	YUVIN2		1) DRAM data 19 2) While using 16-bits wide DRAM: I) Video input data 2 II) GPIO
184	RD20	YUVIN3		1) DRAM data 20 2) While using 16-bits wide DRAM: I) Video input data 3 II) GPIO
183	RD21	YUVIN4		1) DRAM data 21 2) While using 16-bits wide DRAM: I) Video input data 4 II) GPIO
181	RD22	YUVIN5		1) DRAM data 22 2) While using 16-bits wide DRAM: I) Video input data 5 II) GPIO
180	RD23	YUVIN6		1) DRAM data 23 2) While using 16-bits wide DRAM: I) Video input data 6 II) GPIO
179	DQM2	YUVIN7		1) Data Mask 2 2) While using 16-bits wide DRAM: I) Video input data 7 II) GPIO
178	DQM3	INT6# USB_CLK		1) Data Mask 3 2) While using 16-bits wide DRAM: I) Microcontroller external interrupt 6 II) USB port CLK input (48Mhz) part II III) GPIO
177	RD24	SDIN1 MS_BS		1) DRAM data 24 2) While using 16-bits wide DRAM: I) Serial interface port 1 data-in II) MS Card BS pin part II III) GPIO
176	RD25	SDO1 MS_SDIO		1) DRAM data 25 2) While using 16-bits wide DRAM: I) Serial interface port 1 data-out II) MS Card SDIO pin part II III) GPIO
174	RD26	SDCS1 MSCLK		1) DRAM data 26 2) While using 16-bits wide DRAM: I) Serial interface port 1 chip select II) Memory Stick Clock part II III) GPIO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
172	RD27	SCLK2 SDCLK		1) DRAM data 27 2) While using 16-bits wide DRAM: I) Serial interface port 2 clock pin II) Security Disk Clock part II III) GPIO
171	RD28	SDIN2 SD_CMD		1) DRAM data 28 2) While using 16-bits wide DRAM: I) Serial interface port 2 data-in II) SD Card CMD pin part II III) GPIO
170	RD29	SDO2 SD_DAT		1) DRAM data 29 2) While using 16-bits wide DRAM: I) Serial interface port 2 data-out II) SD Card Data pin part II III) GPIO
169	RD30	SDCS2		1) DRAM data 30 2) While using 16-bits wide DRAM: I) Serial interface port 2 chip select II) GPIO
168	RD31	INT5# ASDATA5		1) DRAM data 31 2) While using 16-bits wide DRAM: I) Microcontroller external interrupt 5 II) Audio serial data 5 part III : DSD data sub-woofer channel or Microphone output III) GPIO
166	RA4			DRAM address 4
165	RA5			DRAM address 5
164	RA6			DRAM address 6
162	RA7			DRAM address 7
160	RA8			DRAM address 8
159	RA9			DRAM address 9
158	RA11	GPIO		1) DRAM address bit 11 2) While using DRAM size <=4MB: I) GPIO
157	CKE			DRAM clock enable
156	RCLK			Dram clock
154	RCLKB	USB_CLK		1) Dram clock invert 2) While not using DDR: I) USB port CLK input (48Mhz) part I
153	RVREF	V_ADIN3		1) Reference voltage for DDR DRAM 2) While not using DDR : Version AD input port 3
151	RA3			DRAM address 3
150	RA2			DRAM address 2
149	RA1			DRAM address 1
147	RA0			DRAM address 0
146	RA10			DRAM address 10

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
145	BA1			DRAM bank address 1
143	BA0			DRAM bank address 0
142	RCS#			DRAM chip select, active low
140	RAS#			DRAM row address strobe, active low
139	CAS#			DRAM column address strobe, active low
138	RWE#			DRAM Write enable, active low
137	DQM1			Data mask 1
136	DQS1	INT7# MS_BS		1) Data strobe 1 for DDR DRAM 2) While not using DDR: I) Microcontroller external interrupt 7 II) MS Card BS pin part I III) GPIO
135	RD8			DRAM data 8
133	RD9			DRAM data 9
132	RD10			DRAM data 10
131	RD11			DRAM data 11
130	RD12			DRAM data 12
129	RD13			DRAM data 13
128	RD14			DRAM data 14
126	RD15			DRAM data 15
125	RD0			DRAM data 0
124	RD1			DRAM data 1
123	RD2			DRAM data 2
121	RD3			DRAM data 3
120	RD4			DRAM data 4
118	RD5			DRAM data 5
117	RD6			DRAM data 6
115	RD7			DRAM data 7
114	DQS0	SCLK1 MS_SDIO		1) Data strobe 0 for DDR DRAM 2) While not using DDR: I) Serial interface port 1 clock pin II) MS Card SDIO pin part I III) GPIO
113	DQM0			Data mask 0
JTAG Interface(4)				
48	TDI	SDO3 V_ADIN4 SD_DAT	Inout	1) JTAG data in 2) While not using Boundary Scan: I) Serial interface port 3 data-out II) Version AD input port 4 III) SD Card Data pin part I IV) GPIO

Table1. 1389C Pin Description (continued)

Pin	Main	Alt.	Type	Description
49	TMS	SDIN3 V_ADIN5 SD_CMD	Inout	1) 2) While not using Boundary Scan: I) Serial interface port 3 data-in II) Version AD input port 5 III) SD Card CMD pin part I IV) GPIO
50	TCK	SCLK3 V_ADIN6 SDCLK	Inout	1) JTAG clock 2) While not using Boundary Scan: I) Serial interface port 3 clock pin II) Version AD input port 6 III) Security Disk Clock part I IV) GPIO
51	TDO	SDCS3 V_ADIN7 MSCLK	Inout	1) JTAG data out 2) While not using Boundary Scan: I) Serial interface port 3 chip-select II) Version AD input port 7 III) Memory Stick Clock part I IV) GPIO

Note:

1. The Main column is the main function, Alt. Means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The video input port and external TV encoder mode can not both use CCIR-601 mode, at least one of them should be in CCIR-656 mode.