MT1803

N-Channel Enhancement Mode Field Effect Transistor

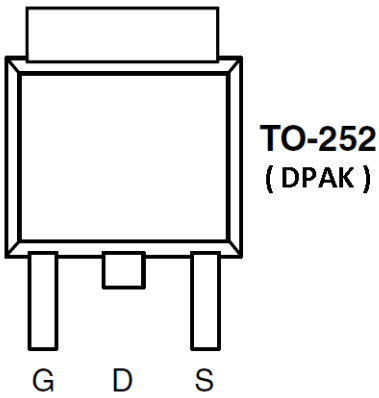
RoHS COMPLIANT

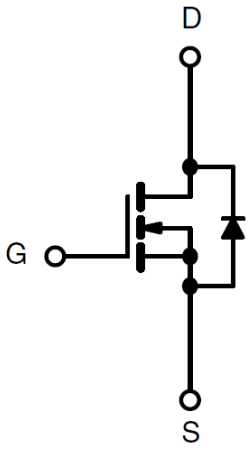
Features：

- V_{DS}=30V
- I_D=60A(Tc=25℃, V_{GS}=10V)
- $R_{DS(ON)}$≦6.5mΩ @V_{GS}=10V
- $R_{DS(ON)}$≦10mΩ @V_{GS}=4.5V
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.

Applications：

- Switching Applications.





N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		20	V
I_D	Continuous Drain Current	Tc=25℃	60	A
I_{DM}	Pulsed Drain Current [2]		160	A
I_S	Continuous Source Current (Diode Conduction) [1]		40	A
P_D	Maximum Power Dissipation [1]	Tc=25℃	50	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55 to 150	℃

Thermal Resistance Ratings

Symbol	Parameter	Ratings	Unit
R_{thJA}	Maximum Junction-to-Ambient	52	℃/W

Notes:

1. Surface Mounted on 1” x 1” FR4 Board, t≦10 Sec.

2. Pulse width limited by maximum junction temperature.

Electrical Characteristics (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
● Static Characteristics						
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}= 0V, I_{DS}= 250μA	30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= 250μA	1.0	1.6	2.0	V
I_{GSS}	Gate-Body Leakage Current	V_{DS}= 0V, V_{GS}= ±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 24V, V_{GS}= 0V	-	-	1	μA
		V_{DS}= 24V, V_{GS}= 0V, T_J= 85℃	-	-	30	
$R_{DS(on)}$	Drain Source On State Resistance [a]	V_{GS}= 10V, I_D= 25A	-	5	6.5	mΩ
		V_{GS}= 4.5V, I_D= 20A	-	7.5	10	
V_{SD}	Diode Forward Voltage [a]	I_S= 25A, V_{GS}= 0V	-	0.7	1.3	V
● Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS}= 15V, V_{GS}= 0V, f= 1MHz	-	2200	-	pF
C_{oss}	Output Capacitance		-	390	-	
C_{rss}	Reverse Transfer Capacitance		-	255	-	
Q_g	Total Gate Charge	V_{DS}= 15V, V_{GS}= 10V, I_D= 25A	-	37	-	nC
Q_{gs}	Gate-Source Charge		-	9	-	
Q_{gd}	Gate-Drain Charge		-	5	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}= 15V, V_{GS}= 10V I_D= 20A, R_G= 4.7Ω	-	10	-	nSec
t_r	Rise Time		-	128	-	
$T_{d(off)}$	Turn-Off Delay Time		-	44	-	
t_f	Fall Time		-	31	-	
R_g	Gate Resistance	V_{DS}= 0V, V_{GS}= 0V, f= 1MHz	-	1.9	-	Ω
t_{rr}	Source-Drain Reverse Recovery Time	I_S= 25A, di/dt= 100A/μs	-	32	-	nSec

Note:

a. Pulse test; pulse width≦300μs, duty cycle≦2%.

b. Guaranteed by design, not subject to production testing.

Typical Characteristics (Tc=25℃ unless otherwise noted)

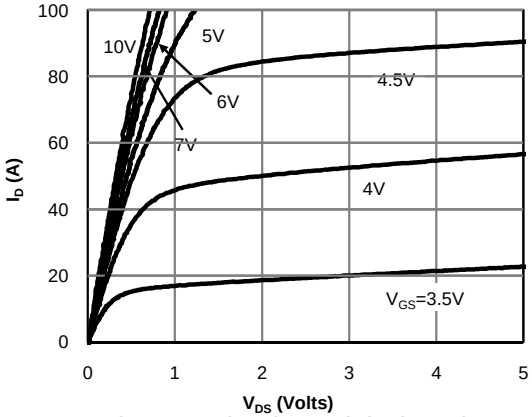


Fig 1: On-Region Characteristics (Note E)

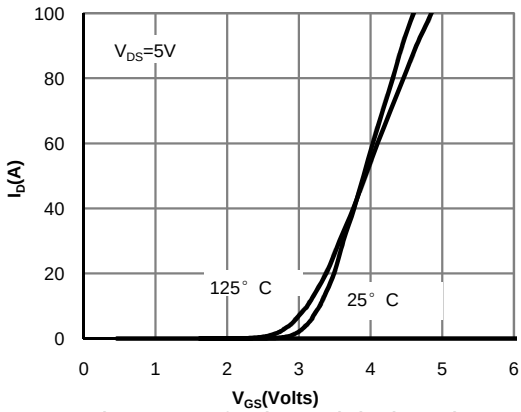


Figure 2: Transfer Characteristics (Note E)

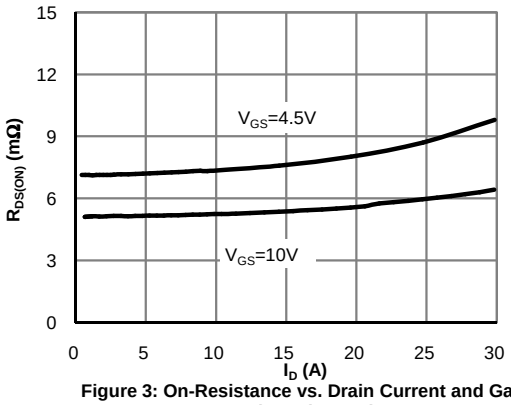


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

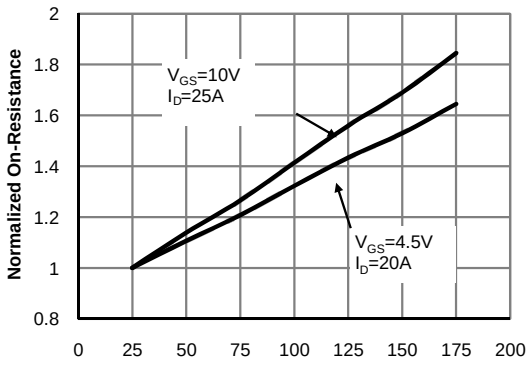


Figure 4: On-Resistance vs. Junction Temperature (Note E)

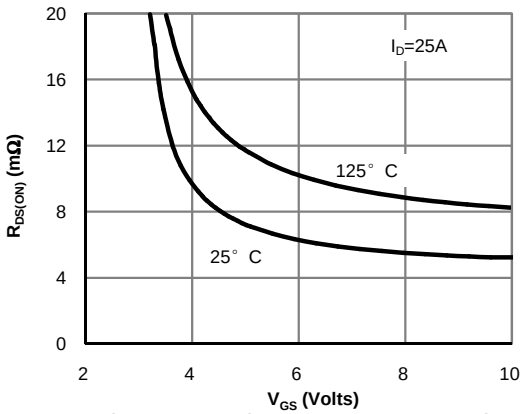


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

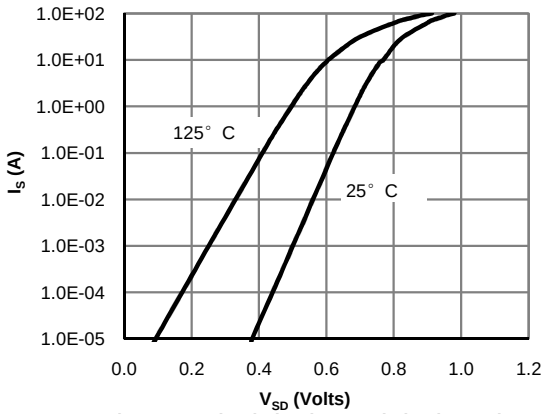


Figure 6: Body-Diode Characteristics (Note E)

Typical Characteristics (Tc=25℃ unless otherwise noted)

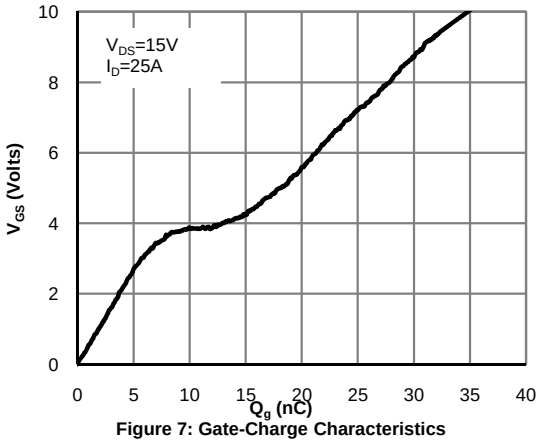


Figure 7: Gate-Charge Characteristics

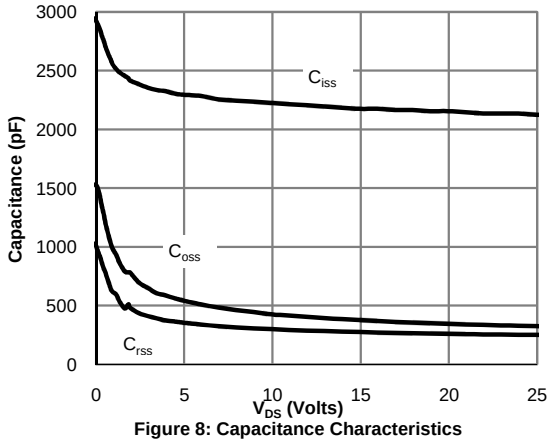


Figure 8: Capacitance Characteristics

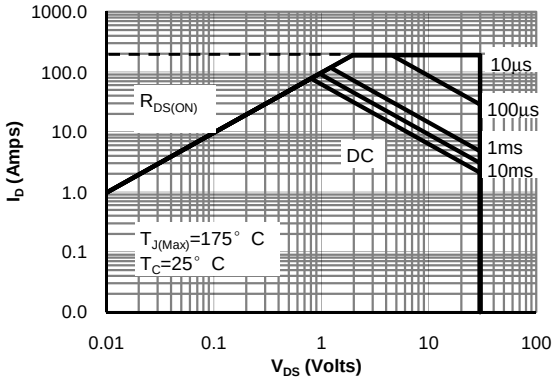


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

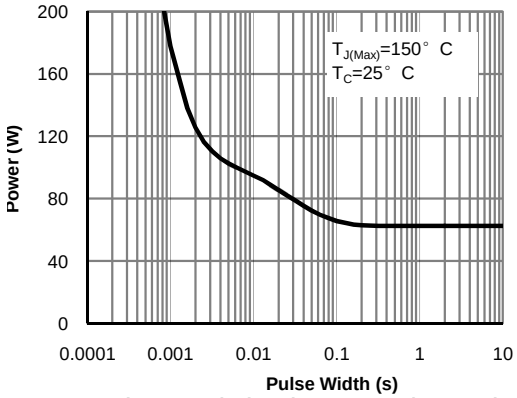


Figure 10: Single Pulse Power Rating Junction-to-

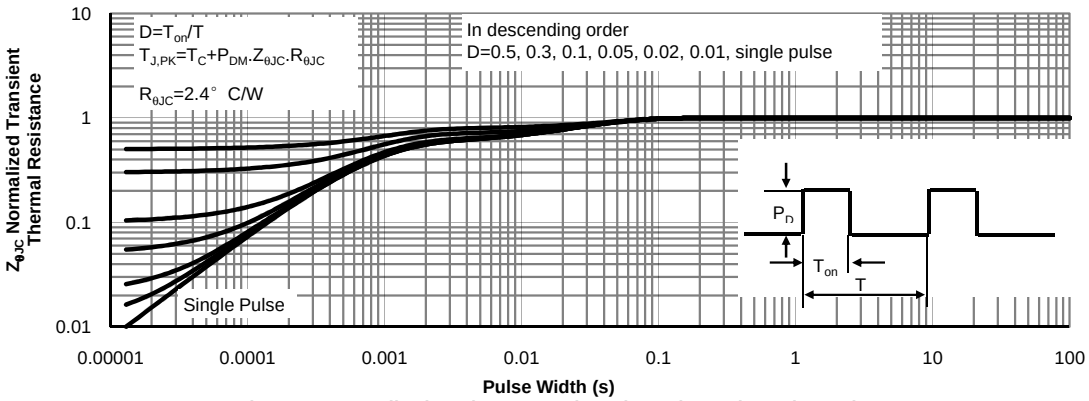


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Typical Characteristics (Tc=25℃ unless otherwise noted)

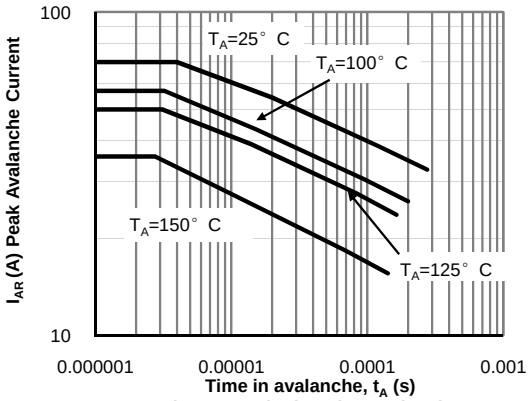


Figure 12: Single Pulse Avalanche capability (Note C)

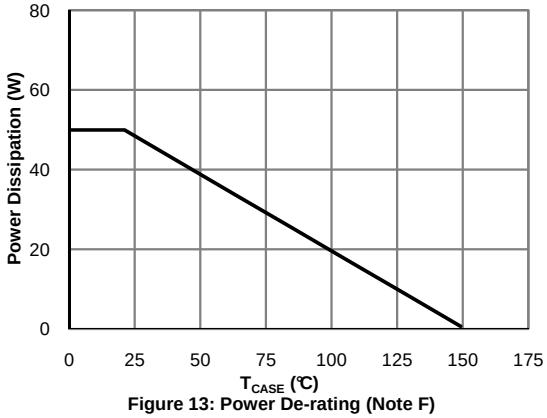


Figure 13: Power De-rating (Note F)

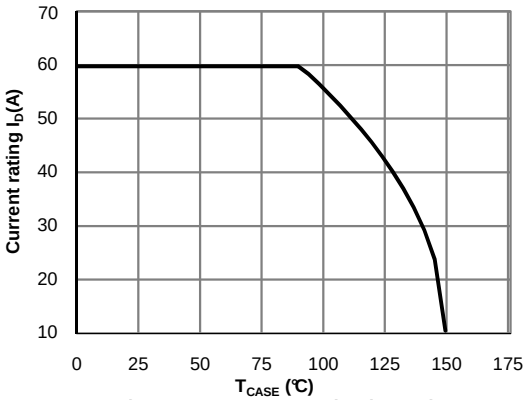


Figure 14: Current De-rating (Note F)

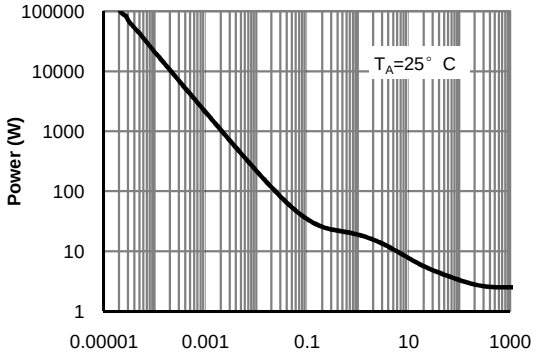


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

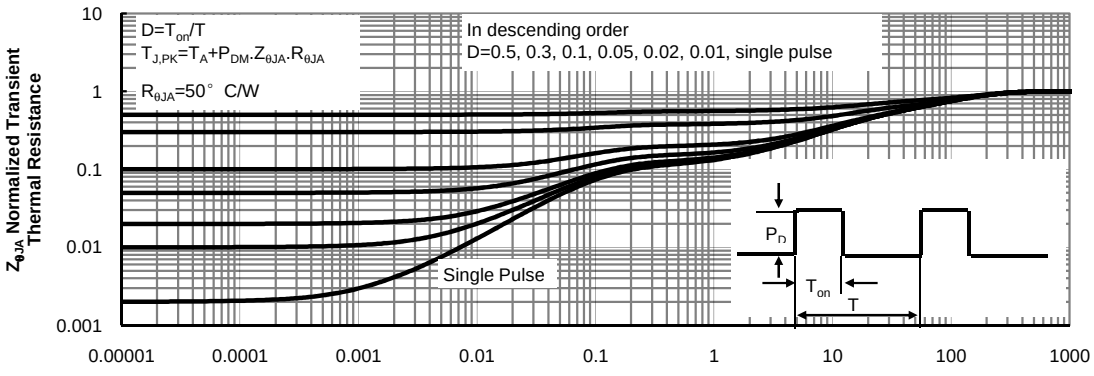
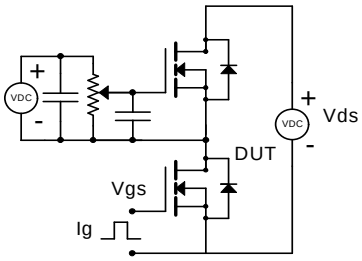
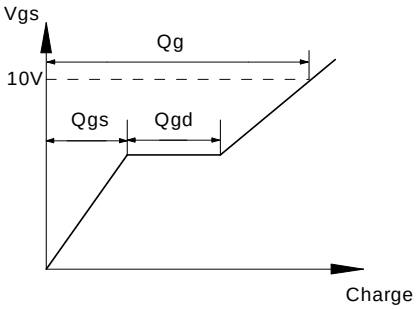


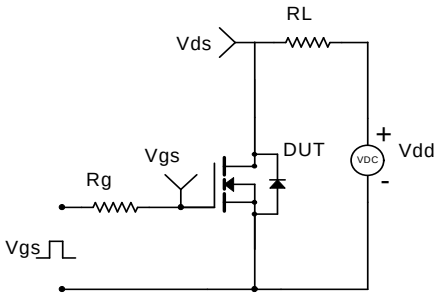
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

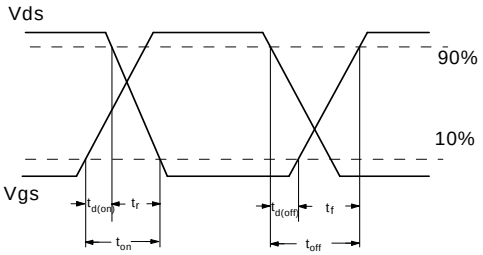
Gate Charge Test Circuit & Waveform



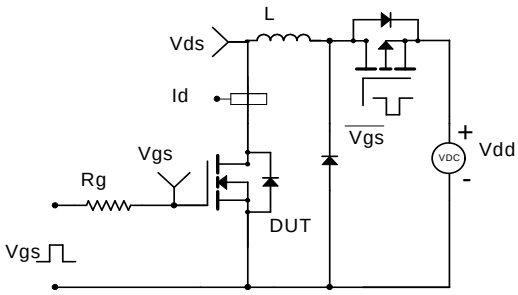


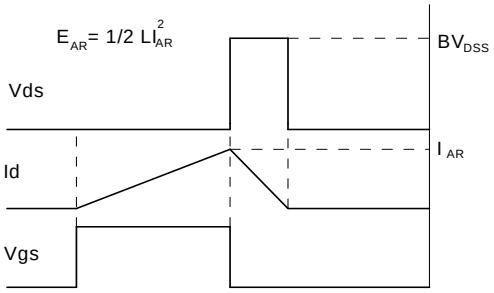
Resistive Switching Test Circuit & Waveforms



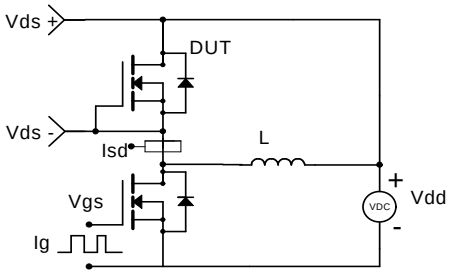


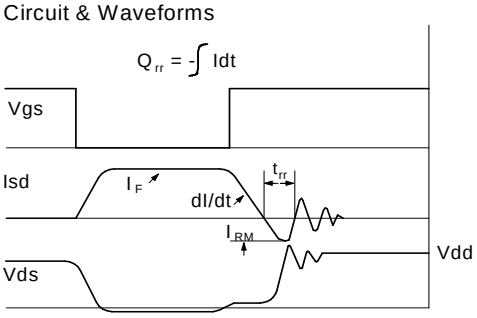
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.