MT2060 SINGLE-CHIP BROADBAND TUNER
DATA SHEET

CABLE MODEM AND
DIGITAL SET-TOP BOX APPLICATIONS

1. APPLICATIONS

The MicroTuner™ MT2060 is an advanced, low-power single-chip broadband tuner that has been optimized for high-performance cable modems and digital cable set-top boxes that require low composite distortion and noise under digital cable environments. It supports all high performance video, voice, and data applications:

- Voice over IP (VoIP) Telephony Modems
- Cable Modems
- Digital Set-top Boxes (STB)
- Home Gateways
- PC TV
- Multi-media Applications
- LCD Flat Panel TVs
- PacketCable™ E-MTAs
- Digital Terrestrial

2. FEATURES

- Fully integrated single-chip tuner with on-chip variable-gain low-noise amplifier (VLNA), first IF filter (FIFF), variable-gain IF amplifier (VGA), mixers and frequency synthesizers, integrated voltage controlled oscillators (VCOs), and serial interface
- 48MHz to 860MHz input frequency range
- 3.3V power supply with multiple power modes
- Single-ended RF input reduces BOM by eliminating input balun
- Eliminates the need for the 28V to 33V supplies typically required by traditional cable tuners
- Works seamlessly with all analog and digital demodulators
- Low power (1-Watt) dual-conversion architecture
- Minimal external components
- No tunable parts required
- Integrated IF variable gain amplifier for direct connection to digital demodulators
- Can drive two second IF SAW filters to support mixed analog/digital applications with no additional circuitry
- Low phase noise for excellent performance in QAM 64 and QAM 256 systems
- Low noise figure
- Software shutdown mode
- Frequency synthesizers fully programmable via serial-control interface
- Fully integrated VCO circuitry simplifies PCB layout
- Two general-purpose outputs controllable via serial-control interface
- Intermediate frequency (IF) output fully compatible with NTSC, PAL, SECAM, DAVIC, DVB-C, DOCSIS, EuroDOCSIS and other standards

- Integrated temperature sensor
- Operates with a 16MHz crystal
- Small 7mm x 7mm 48-pin MicroLeadFrame™ package
- Can be used in conjunction with Microtune's upstream amplifiers to create a complete RF front end for bi-directional cable modem and STB applications
- Software selectable power modes to 800 mW
- System Reference Oscillator output, with selectable sub-multiples of 1, 2, or 4 appropriate for driving an additional tuner or IC in a multiple tuner system

3. OVERVIEW

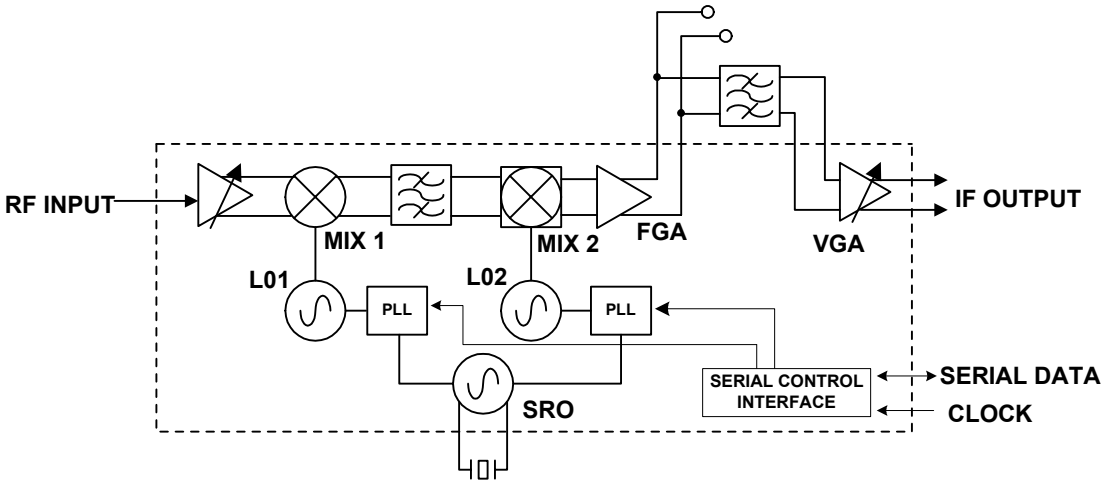

Figure 1 MT2060 Block Diagram

The Microtune® MT2060 is an advanced, low-power single-chip broadband tuner that has been optimized for high performance cable modems and digital cable STBs that require low composite distortion and noise under digital cable environments. The MT2060 includes all active circuitry required to implement total RF functionality. It is capable of receiving frequencies in the 48MHz to 860MHz range and of converting a selected channel to a standard intermediate frequency (IF). Supported IF frequencies include NTSC, PAL, SECAM, and digital standards including DOCSIS, EuroDOCSIS, and DVB-C.

The MT2060's low close-in phase noise allows it to be used for both digital and analog video signals. Its dual-conversion architecture, with no requirement for tracking filters, yields the desirable characteristics of traditional cable television tuners: controlled input impedance across the entire input band, low in-band emissions, and outstanding image rejection.

The device is completely integrated, with active on-chip components that include:

- Variable-gain low-noise amplifier with band selection filters
- First mixer (MIX1) that up-converts the input spectrum to a first IF of 1220MHz nominal
- First IF filter (FIFF) with on-chip calibration circuitry

- Image-reject mixer (MIX2) that down-converts the filtered first IF spectrum to a programmable second IF
- Buffer amplifier (FGA) for the second IF output that is capable of driving two IF SAW filters
- IF VGA amplifier
- Completely integrated frequency synthesis system, including on-chip phase-locked loops (PLLs), VCOs and varactors, to create the first and second local oscillator (LO1 and LO2) frequencies from an external 16.000MHz crystal
- Serial control interface that programs the device as well as reads back its status
- Additional on-chip functions to ease system implementation, including a programmable crystal reference output, two general-purpose outputs, and a temperature sensor

4. RELATED DOCUMENTS

AN-00043, Surface Mount Assembly of MicroLeadFrame Packages
AN-00084, MT2060 Series Programming Procedures
SC-000xx, MT2060 Evaluation Board Schematic (Viewdraw format)
GR-000xx, MT2060 Evaluation Board Gerber (274x format)
PCB-000xx, MT2060 Evaluation Board (PADS Power PCB format)
BM-000xx, MT2060 Evaluation Board Bill of Materials

5. ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 1 may cause permanent damage to the device. These are stress ratings only; functional operation of the device under conditions other than those listed in the operational sections of this document is not recommended or implied. Exposure to any of the absolute-maximum rating conditions for extended periods of time may affect reliability.

Table 1 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply voltage, +3.3V		3.6	V
Storage temperature	-50	150	°C
Lead solder temperature for 4 seconds		245	°C
Relative humidity		95	%
Input voltage	-0.3	VCC +0.3	V

6. RECOMMENDED OPERATING CONDITIONS

Application Notes for the MT2060 provide details for board layout, thermal considerations, and other implementation topics.

Table 2 Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Input frequency range	48		860	MHz
First intermediate center frequency		1220		MHz
Second intermediate center frequency (programmable)	30		60	MHz
Supply voltage	3.15	3.3	3.45	V
Supply voltage ripple			15	mV
Operating junction temperature			100	°C

7. ELECTRICAL TEST SPECIFICATIONS

Table 3 lists the electrical characteristics of the MT2060 as tested in the Microtune test environment.

- T_A = 25°C
- V_{CC} = 3.3V
- RFin at 376MHz
- Second IF = 44MHz

Table 3 Tuner Electrical Test Specifications

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power supply					
Active current	RFagc =1.3V		320	380	mA
Low-power mode current	RFagc =1.3V		240	290	mA
Shut-down current	All blocks shutdown		15	25	mA
RF signal path					
Input frequency range		48		860	MHz
Return loss	Referred to 75Ω w/ external matching ckt		8		dB
Noise figure	Z_S = 50Ω and RFagc ≥ 2.0V at FGA out		7.3	TBD	dB
Insertion power gain	Z_S = 50Ω and RFagc ≥ 2.0V at FGA out	TBD	42	TBD	dB
Gain variation at any frequency			±1		dB
AGC range	RFagc = 0.5V to 2.0V	30			dB
OIP3	RFagc ≥ 2.0V at f1 = 375.5MHz, f2 = 376.5MHz	77	80		dBmV
Input P1dB	RFagc = 0.5V	50			dBmV
FGA output frequency range		30		60	MHz
FGA output load impedance		450	900		Ω
Image rejection		55	65		dBc
LO1 frequency		1088		2214	MHz
LO1 step size	16.000MHz reference frequency	250			kHz
LO2 frequency		1041		1310	MHz
LO2 step size	16.000MHz reference frequency	50			kHz
Phase noise (1kHz) [1]			-82		dBc/Hz
Phase noise (10kHz) [1]			-86		dBc/Hz
Phase noise (100kHz) [1]			-107		dBc/Hz
LO Spurious[1]				-56	dBc
IF Variable Gain Amplifier (VGA)					
Frequency range		30		60	MHz
Output voltage	Balanced		2.0		Vp-p
Output load impedance		200	380		Ω
Terminal voltage gain	Z_S = 50Ω and IFagc ≥ 2.0V high gain range	50	52		dB
Terminal voltage gain	Z_S = 50Ω and IFagc ≤ 0.5V low gain range		10	12	dB
AGC range	IFagc = 0.5V to 2.0V	27	30		dB
OIP3	Z_S = 50Ω and max gain, R_L > 380Ω, 2 tone at output +51dBmV each 1MHz apart	70	73		dBmV
Input P1dB	IFagc = 0.5V	38			dBmV
Noise figure			10		dB
Serial Interface					
Serial control clock frequency				400	kHz
V_{IH}		2.3			V
V_{IL}				1.2	V

[1] Guaranteed by design and characterization.

8. TYPICAL TEST CIRCUIT

The circuit diagram shown in Figure 2 describes the MT2060 in the test configuration characterized in Table 4.

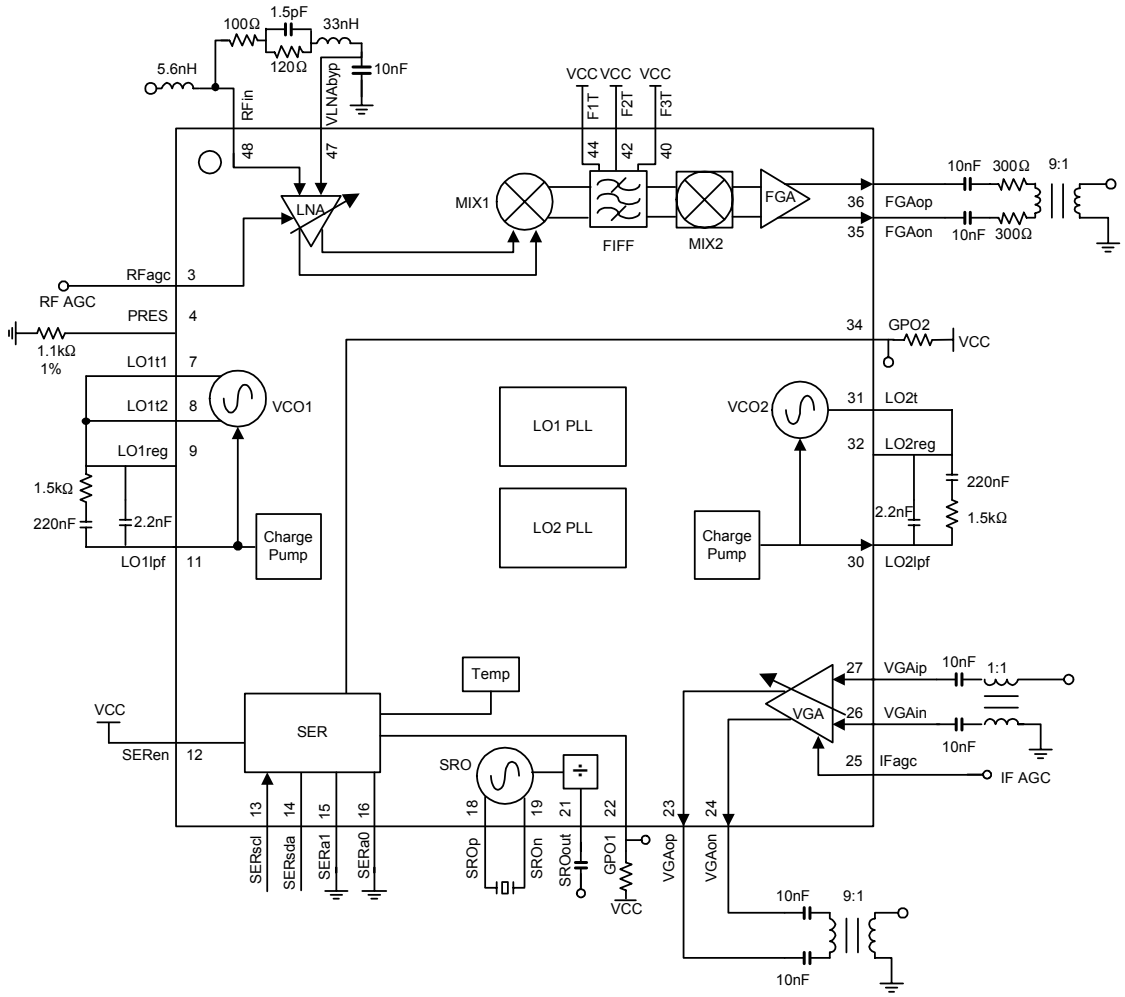

Figure 2 Typical Test Circuit

The baluns used in the typical test circuit are identified on Figure 2 and are described in Table 7.

Table 4 Baluns Used for Typical Test Circuit

DESIGNATION ON DRAWING	BALUN	MANUFACTURER PART NUMBER
FGA output	9:1	MiniCircuits T9-1
VGA input	1:1	Macom ETC1-IT
VGA output	9:1	MiniCircuits T9-1

9. TYPICAL APPLICATION CIRCUIT

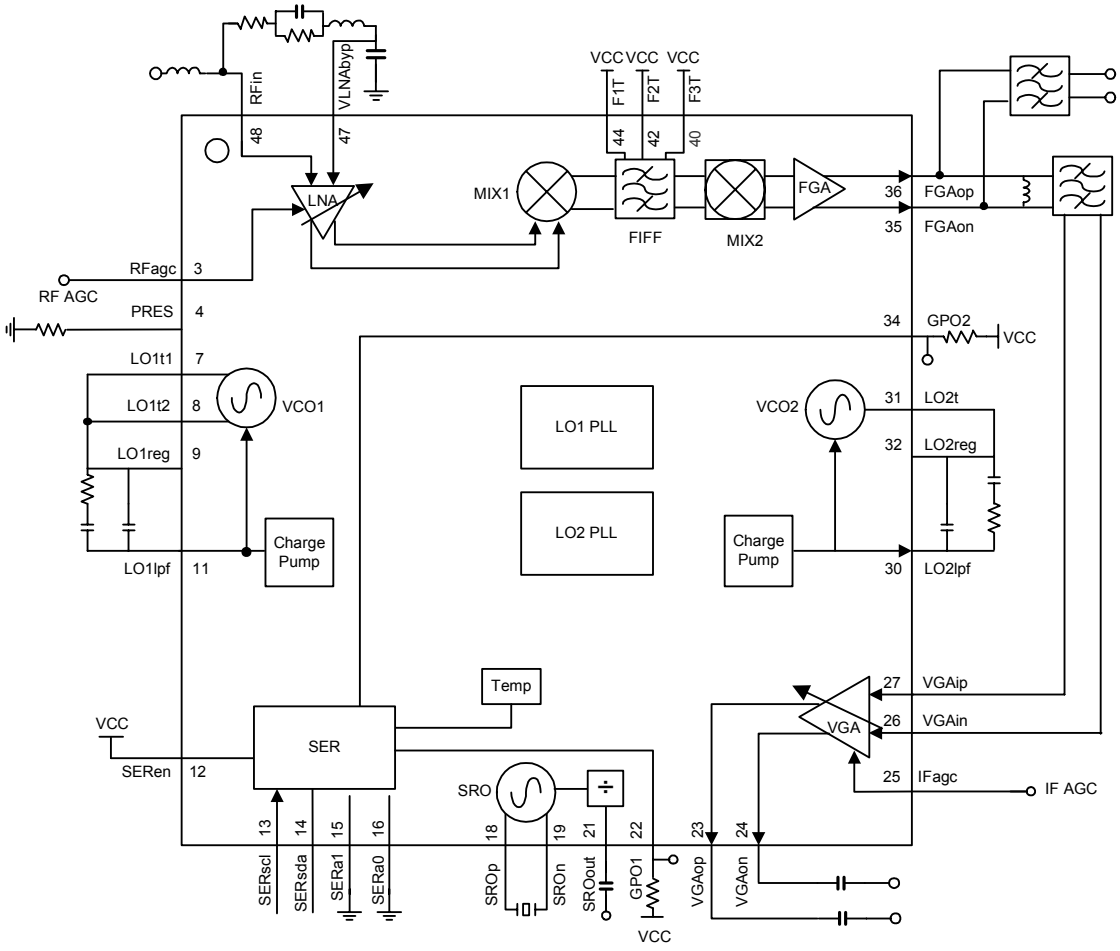

Figure 3 Typical Application Circuit

Table 5 Typical Tuner Performance

PARAMETER	CONDITION	RESULT	UNIT
CSO	Input 133 CW carriers @ +15dBmV, RF gain control voltage at pin 3 (RFagc) referenced to 0dBmV takeover point at 55.25MHz input frequency, IF gain control voltage at pin 25 (IFagc) for 1Vp-p output	-54	dBc
CTB		-56	dBc
Spurious		-50	dBc
Cross modulation	Same conditions as CSO/CTB/spurs, with the 132 undesired carriers 100% AM modulated at 15.75kHz	-50	dBc
Output carrier-to-noise ratio	Same conditions as CSO/CTB/spurs. Measured in a 6MHz bandwidth	51	dB
Noise figure, max RF gain, at VGA output 48 – 860MHz	RF gain control voltage at pin 3 (RFagc) set to maximum. Output is the VGA output (pins 23 and 24) 1Vp-p output.	9	dB

Table 6 Recommended Components

COMPONENT	COMMENTS	MANUFACTURER AND PART NUMBER
Reference crystal	Frequency: 16.000MHz, fundamental mode, series resonant. Tolerance @ 25°C: +/-50ppm max. Stability @ 0°C - 70°C: +/-50ppm max. Equivalent Series Resistance: 50Ω max.	

10. PERFORMANCE DATA

The following data is representative of a part measured in a typical application circuit with:

- Room ambient temperature
- TOP = 0dBmV
- Vcc = 3.3V
- VGA output (pins 23 and 24) = 51dBmV
- Measured on an MT2060 Evaluation Board
- Epcos X6864D second IF SAW

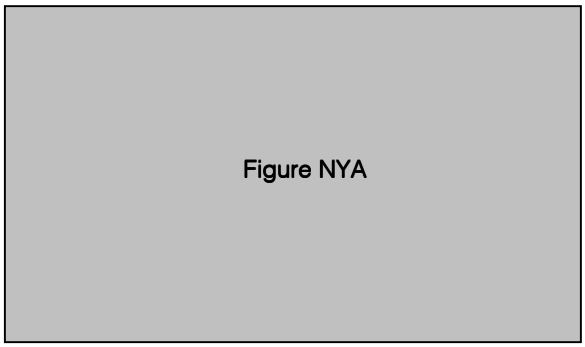

Figure 4 Tuner Gain vs. AGC Voltage, 375MHz

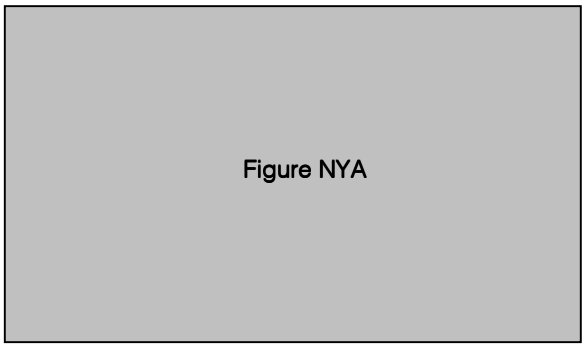

Figure 5 Phase Noise vs. Frequency

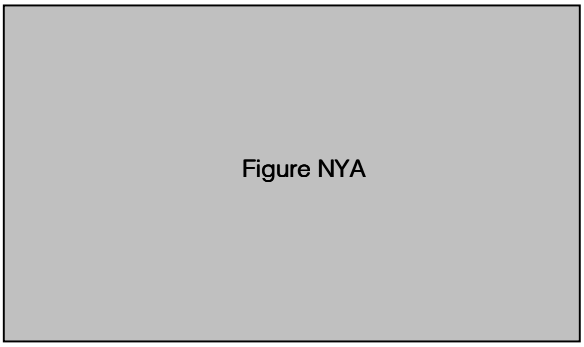

Figure 6 Noise Figure vs. Frequency

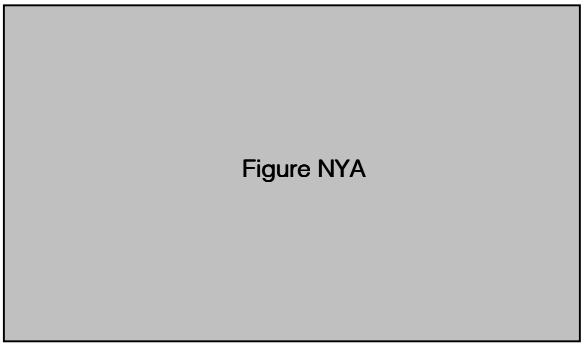

Figure 7 Image Rejection vs. Frequency

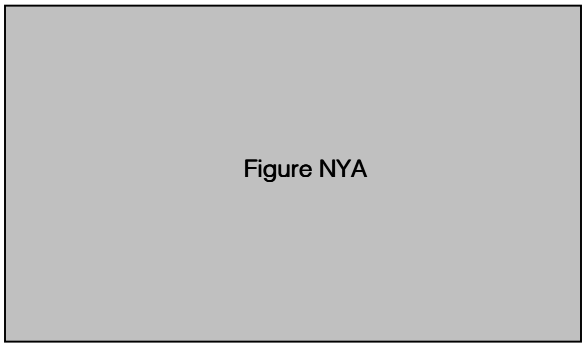

Figure 8 CSO and CTB vs. Frequency

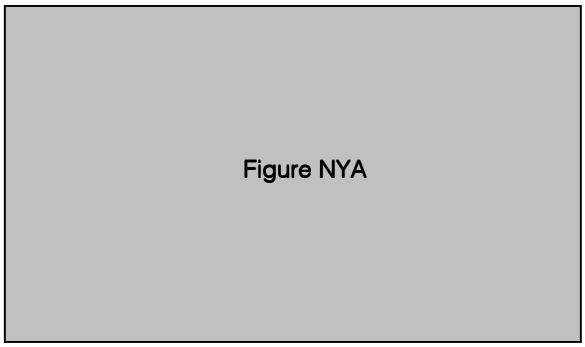

Figure 9 CNR vs. Frequency

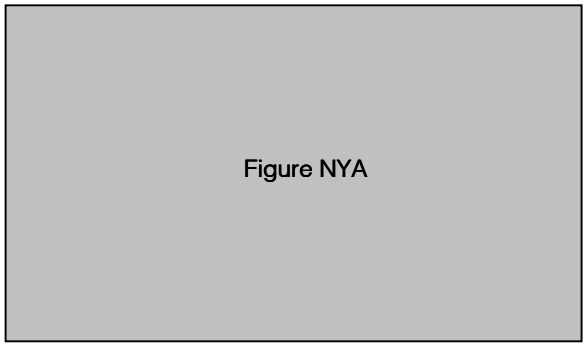

Figure 10 VGA CNR vs. Input Power

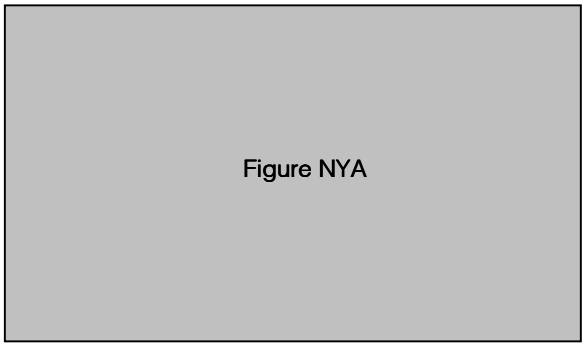

Figure 11 VGA CNR vs. IF AGC

11. RF BAND SELECTION

The MT2060 uses 11 programmable pre-selection filters in front of the VLNA for a lower overall system power dissipation and better performance in the presence of strong off-air interference or tilt conditions in a cable application. Application Note AN-00084 covers the use of these filters in detail while Table 7 shows the nominal RF filter selection frequencies versus filter band.

Table 7 RFin VS. RFB Register

RFB REGISTER	RFIN MIN	RFIN MAX
11	48	95
10	95	180
9	180	260
8	260	335
7	335	425
6	425	490
5	490	570
4	570	645
3	645	730
2	730	810
1	810	864

12. REFERENCE CRYSTAL

The MT2060 provides a system reference oscillator (SRO) on pin 18 and pin 19. Most applications will utilize a 16.000MHz fundamental mode series resonant crystal as described in Table 6.

The MT2060 can also be driven by an external reference frequency. For test purposes, a 50Ω source-impedance 200mVp-p signal AC coupled to either pin 18 or pin 19 is sufficient. The non-driven pin should be left open.

The MT2060 also provides a system reference oscillator output, appropriate for driving an additional tuner or IC in a multiple tuner system. This output, available on SROout (pin 21), may be AC coupled to an additional MT2060 as described above. This 2Vp-p, 1kΩ source-impedance square-wave output may be a sub-multiple of the reference frequency. (See Table 8.) A typical use divides the MT2060's 16MHz reference by 4, and utilizes the resulting 4MHz signal as reference for an analog demodulator.

Table 8 System Reference Oscillator Output Frequency

OUTPUT FREQUENCY	SRDV1	SRDV0
Off	0	0
Ref Freq / 4	0	1
Ref Freq / 2	1	0
Ref Freq / 1	1	1

13. FIFF CALIBRATION, SHUTDOWN MODE, LOW POWER MODE, INTERNAL DIE TEMPERATURE READING, LO STATUS, AND GENERAL PURPOSE OUTPUTS

The MT2060 provides six useful functions selected by serial bus addressable register settings: a calibration routine for the FIFF, a shutdown mode, a low power mode, die temperature sensor, LO lock status, and two general purpose open drain outputs.

13.1 FIFF CALIBRATION

The MT2060 has an integrated first intermediate frequency filter (FIFF) that has a nominal center frequency of 1220MHz, but because of manufacturing variations the center frequency can vary from a minimum of 1098MHz to a maximum of 1342MHz. Please see Microtune AN-00084 for a more detailed description of the FIFF calibration routine.

13.2 SHUTDOWN MODE FOR POWER CONSERVATION

In some applications, it may be desirable to disable most of the MT2060 to conserve power when it is not in use. This is accomplished easily via the serial bus. Several different levels of shutdown are available in the MT2060. Setting the bit SD to a 1 shuts down the RF signal path and local oscillators, but does not control the VGA or the SRO leaving both running if desired. The VGA is shut down independently by setting the VGSD bit to a 1. Setting SRSD to a 1 shuts down the SRO and in conjunction with the SD and VGSD bits puts the MT2060 into the lowest power mode. This configuration typically draws 15mA total current.

When re-enabled, the tuner will return to normal operation at the same tuned frequency as before shutdown, without need for any other initialization or tuning, within 100ms after the serial bus command is concluded.

13.3 LOW-POWER MODE FOR POWER CONSERVATION

The MT2060 has a low-power mode to allow the tuner to stay active, but draw considerably less current. The user can trade-off power versus linearity. Even though this mode involves setting several bits, it is easily accomplished via the serial bus. Complete low power mode, which draws 800mW typically, requires the bits M2LP, FMLP, and M1LP to be set to a 1, and the 3 bits LNAI to be set to 0.

Table 9 TBD

COMING		

13.4 INTERNAL DIE TEMPERATURE OUTPUT

The internal die temperature can be digitally read out in the 2-bit TEMP register. Device-to-device variations may be up to ±20°C.

Table 10 Tj(°C) Vs. TEMP Register

TEMP REGISTER	TJ(°C) MIN	TJ(°C) MAX
0		0
1	0	40
2	40	80
3	80	

13.5 LOCK STATUS

LO Status Register 0x06 contains L1LK and L2LK lock indicators and TAD1x and TAD2x three-bit tune line voltage A/D values read from LO1 and LO2 respectively. Table 11 gives the interpretation of the TAD1 and TAD2 values. The tune line voltage is inversely proportional to the oscillator frequency.

Table 11 TAD Thresholds

TAD1x	TAD2x	TAD0x	CONDITION
0	0	0	Tuned
0	1	0	Tune line low but OK
1	0	0	Tune line high but OK
x	x	1	Tune line not OK

13.6 GENERAL PURPOSE OPEN DRAIN OUTPUTS

There are two general-purpose open drain outputs that are controlled by the serial port. The GPOx bits in the register map set the output level. A '1' in the control bit results in a high impedance at the corresponding output pin. A '0' in the control bit results in a low impedance to ground. The maximum current sink is 1mA per pin. Ground the general purpose outputs if they are not used. Do not connect the output directly to power because this will damage the MT2060. The default state of '0' will sink current upon initial power up.

14. REGISTER MAP

Program the Microtune MT2060 tuner through a 400kHz serial interface. Accessing a register within the device requires several transfers over the serial bus. For a write, the chip is selected via an address byte (a write is indicated with the LSB address as 0), next the register address, and finally the data destined for that register. The serial master performs a read when it writes the address (LSB=1) and then reads the 8-bit data from the tuner. An auto-increment feature allows programming of successive registers with a single address cycle per burst.

The MT2060 does not support multiple master configurations; the tuner does not recognize bus arbitration from more than one master.

Table 12 Serial Bus Enable

SERIAL BUS ENABLE	SEREN
Disable	0
Enable	1

Table 13 Address Fields

	MSB 7	6	5	4	3	2	1	LSB 0
Address Byte	1	1	0	0	0	SERa1	SERa0	R/W

Table 14 Serial Communications Bus Data Format (Read/Write Mode)

	REGISTER ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0	DEF
Part/Rev Code	00	PC3	PC2	PC1	PC0	RC3	RC2	RC1	RC0	0x63
LO1C Byte 1	01	RFB3	RFB2	RFB1	RFB0	L1F5	L1F4	L1F3	L1F2	0x3F
LO1C Byte 2	02	L1N7	L1N6	L1N5	L1N4	L1N3	L1N2	L1N1	L1N0	0x74
LO2C Byte 1	03	F1CA	F1SS	L1F1	L1F0	L2F3	L2F2	L2F1	L2F0	0x00
LO2C Byte 2	04	L2F11	L2F10	L2F9	L2F8	L2F7	L2F6	L2F5	L2F4	0x08
LO2C Byte 3	05	L2N6	L2N5	L2N4	L2N3	L2N2	L2N1	L2N0	L2F12	0x93
LO Status	06	L1LK	TAD12	TAD11	TAD10	L2LK	TAD22	TAD21	TAD20	
FM1 Frequency	07	FMF7	FMF6	FMF5	FMF4	FMF3	FMF2	FMF1	FMF0	
Misc. Status	08		FMCAL		XLOW			TEMP1	TEMP0	
Misc. Control 1	09	SD	VGSD	1	0	SRSD	GPO2	GPO1	0	0x20
Misc. Control 2	0A	M2LP	FMLP	M1LP	LNAI2	LNAI1	LNAI0	1	0	0x1E
Misc. Control 3	0B	SRDV1	SRDV0	1	1	0	0	VGAG1	VGAG0	0x30
Reserved	0C									
Reserved	0D									
Reserved	0E									
Reserved	0F									
Reserved	10									
Reserved	11									
Reserved	12									
Reserved	13									
Reserved	14									

Table 15 Register Descriptions

FIELD	REGISTER	R/W	BITS	DEFAULT	DESCRIPTION
PC	Part/Rev Code	R	4	0x6	Part code
RC	Part/Rev Code	R	4	0x3	Revision code
RFB	LO1C Byte 1	R/W	4	0x3	RF band select
L1F	LO1C Byte 1, LO2C Byte 1	R/W	6	0x3C	LO1 fractional register
L1N	LO1C Byte 2	R/W	8	0x74	LO1 divide by N register
F1CA	LO2C Byte 1	R/W	1	0x0	FIFF calibration start bit
F1SS	LO2C Byte 1	R/W	1	0x0	FIFF calibration single step bit
L2F	LO2C Byte 1, 2, 3	R/W	13	0x1080	LO2 fractional register
L2N	LO2C Byte 3	R/W	7	0x49	LO2 divide by N register
L1LK	LO Status	R	1		LO1 lock detect
TAD1	LO Status	R	3		LO1 tune line ADC value
L2LK	LO Status	R	1		LO2 lock detect
TAD2	LO Status	R	3		LO2 tune line ADC value
FMF	FM1 Frequency	R	8		FIFF calibration output
FMCAL	Misc Status	R	1		FIFF calibration complete bit
XLOW	Misc Status	R	1		SRO amplitude detection
TEMP	Misc Status	R	2		Temperature sensor output
SD	Misc Control 1	R/W	1	0x0	Shutdown RF
VGSD	Misc Control 1	R/W	1	0x0	Shutdown VGA
SRSD	Misc Control 1	R/W	1	0x0	Shutdown SRO
GPO	Misc Control 1	R/W	2	0	General purpose open drain outputs
M2LP	Misc Control 2	R/W	1	0x0	MIX2 reduced power mode select
FMLP	Misc Control 2	R/W	1	0x0	FIFF reduced power mode select
M1LP	Misc Control 2	R/W	1	0x0	MIX1 reduced power mode select
LNAI	Misc Control 2	R/W	3	0x7	VLNA power mode select
SRDV	Misc Control 3	R/W	2	0x0	SRO output select
VGAG	Misc Control 3	R/W	2	0x0	VGA gain select

15. PIN CONNECTIONS

Pin connections for the MT2060 are described in Table 16

Table 16 Pin Connections

PIN	FUNCTION/ SYMBOL	DESCRIPTION
PAD	GNDpad	Ground connection via the die paddle on the bottom of the package
3	RFagc	VLNA AGC input
4	PRES	Precision resistor to set bias
5	NC	Do not connect
6	LO1Avcc	Analog voltage supply for LO1
7	LO1t1	LO1 VCO tank 1
8	LO1t2	LO1 VCO tank 2
9	LO1reg	LO1 regulator output
10	LO1Dvcc	Digital voltage supply for LO1
11	LO1lpf	LO1 loop filter
12	SERen	Serial bus enable
13	SERscl	Serial bus clock
14	SERsda	Serial bus data
15	SERa1	Serial address pin 1
16	SERa0	Serial address pin 0
17	SERvcc	Digital voltage supply for serial bus
18	SROp	SRO positive input
19	SROn	SRO negative input
20	SROvcc	Analog voltage supply for SRO
21	SROout	SRO output buffer
22	GPO1	General purpose open drain output 1
23	VGAop	VGA positive output
24	VGAon	VGA negative output

PIN	FUNCTION/ SYMBOL	DESCRIPTION
25	IFagc	VGA control voltage
26	VGAip	VGA positive input
27	VGAin	VGA negative input
28	VGAvcc	VGA analog voltage supply
29	LO2Dvcc	Digital voltage supply for LO2
30	LO2lpf	LO2 loop filter
31	LO2t	LO2 VCO tank
32	LO2reg	LO2 regulator output
33	LO2Avcc	Analog voltage supply for LO2
34	GPO2	General purpose open drain output 2
35	FGAon	FGA negative output
36	FGAop	FGA positive output
37	MIX2IFvcc	Analog voltage supply for MIX2
38	MIX2RFvcc	Analog voltage supply for MIX2
39	FMIX1vcc	Analog voltage supply for MIX1
40	F3t	Filter tank 3
41	NC	Do not connect
42	F2t	Filter tank 2
43	NC	Do not connect
44	F1t	Filter tank 1
46	VLNAvcc	Analog voltage supply for VLNA
47	VLNAbyp	Capacitor bypass for VLNA
48	RFin	RF input of tuner

16. PIN CONFIGURATION

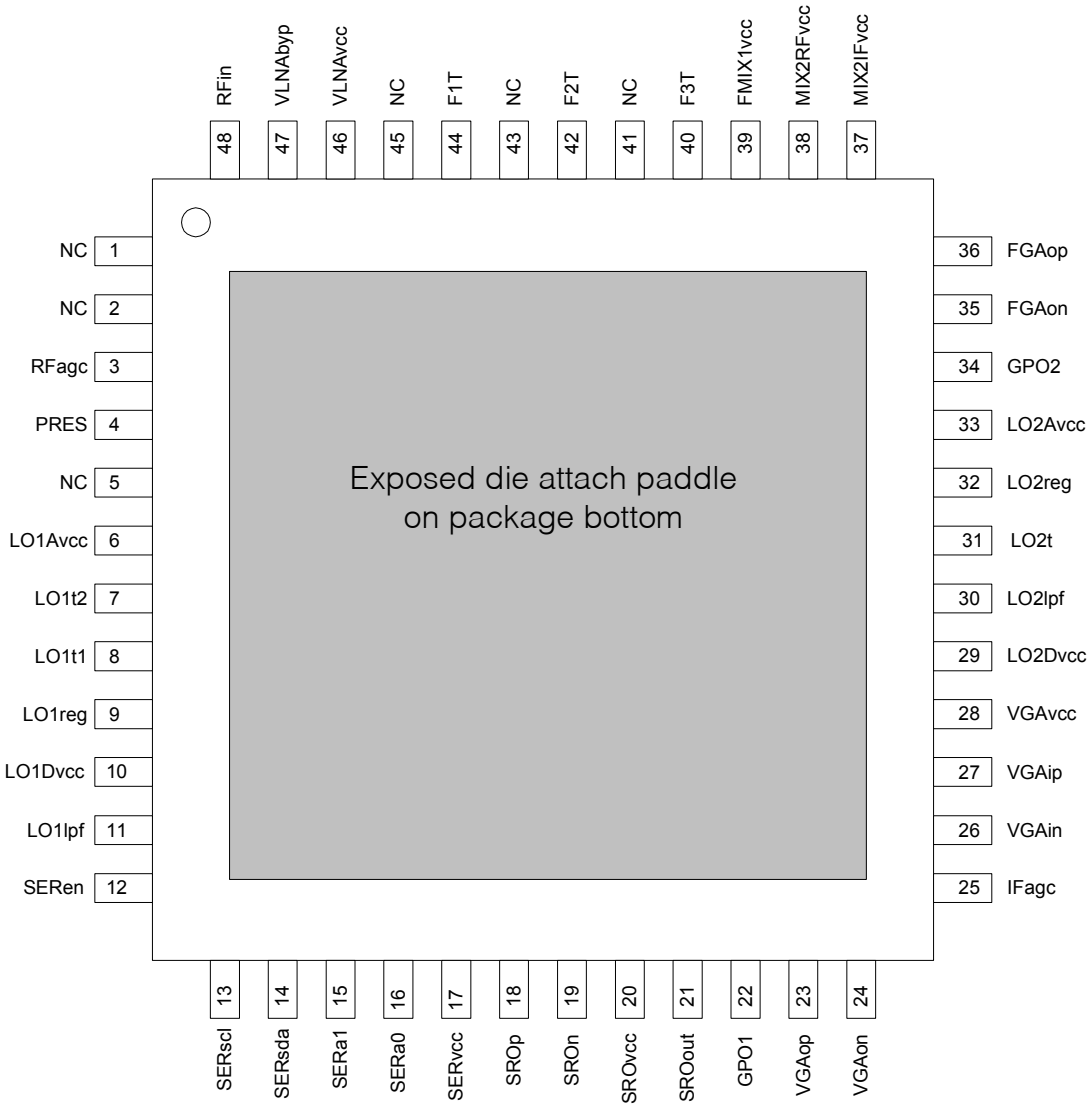

Figure 12 MT2060 Pin Diagram

17. THERMAL CHARACTERISTICS AND LIMITS

Information TBD.

18. PACKAGE DRAWING

The MT2060 is in a 48-pin MicroLeadFrame™ package.

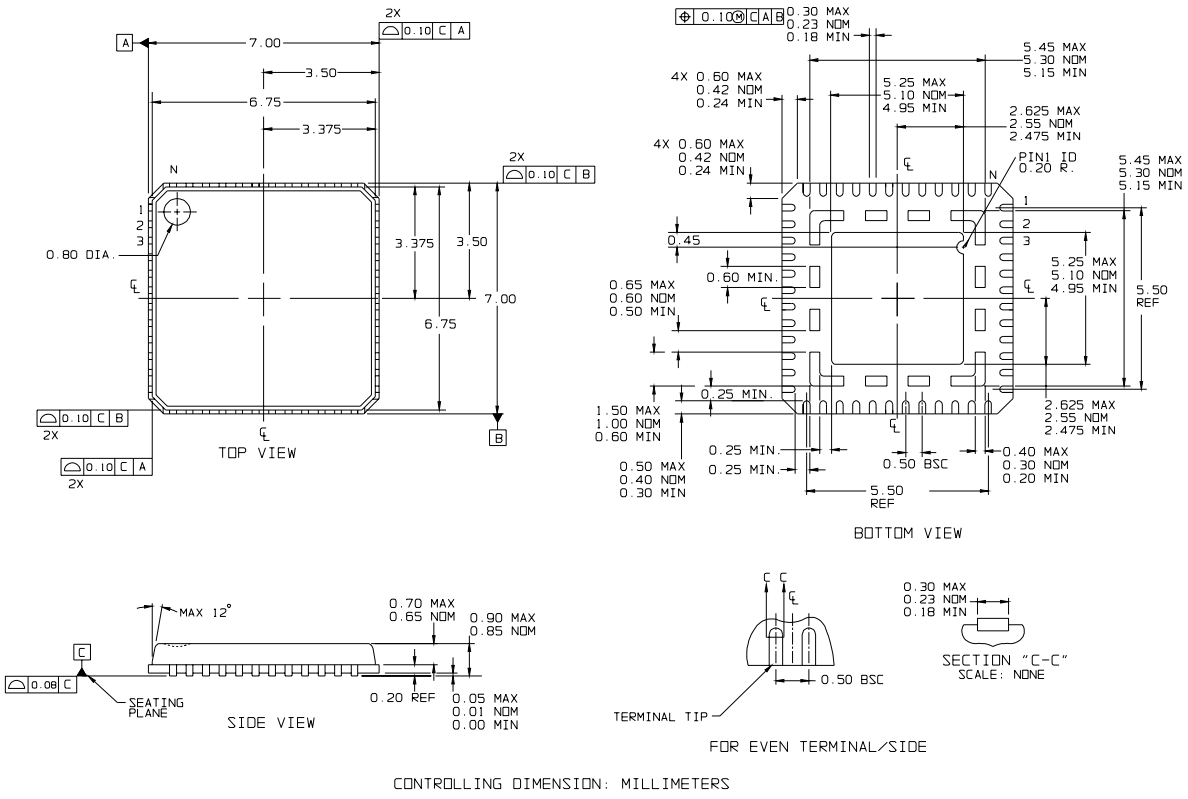

Figure 13 MT2060 Package Drawing

19. ORDERING INFORMATION

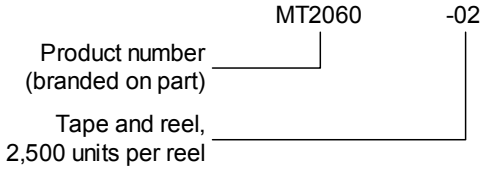

Figure 14 MT2060 Ordering Information

NOTICES

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