DRAM MODULE

2 MEG x 36, 4 MEG x 18

FAST PAGE MODE (MT24D236)
LOW POWER,
EXTENDED REFRESH (MT24D236 L)

FEATURES

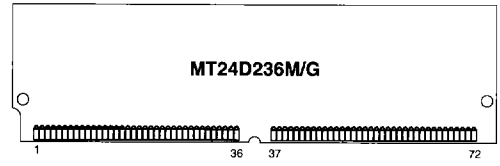
- Industry-standard pinout in a 72-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 72mW (18.4mW L-version) standby; 2,536mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended Refresh
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Multiple $\overline{RAS}$ lines allow x18 or x36 width

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
  - 80ns access — -8
- Packages
  - Leadless 72-pin SIMM — M
  - Leadless 72-pin SIMM (gold) — G
- Power/Refresh
  - Normal Power/16ms — Blank
  - Low Power/128ms — L
- Part Number Example: MT24D236G-6 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(DE-13)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ32
5	DQ20	23	DQ24	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ33
7	DQ21	25	DQ25	43	$\overline{CAS1}$	61	DQ15
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ34
9	DQ22	27	DQ26	45	$\overline{RAS1}$	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	$\overline{WE}$	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ11	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

GENERAL DESCRIPTION

The MT24D236 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

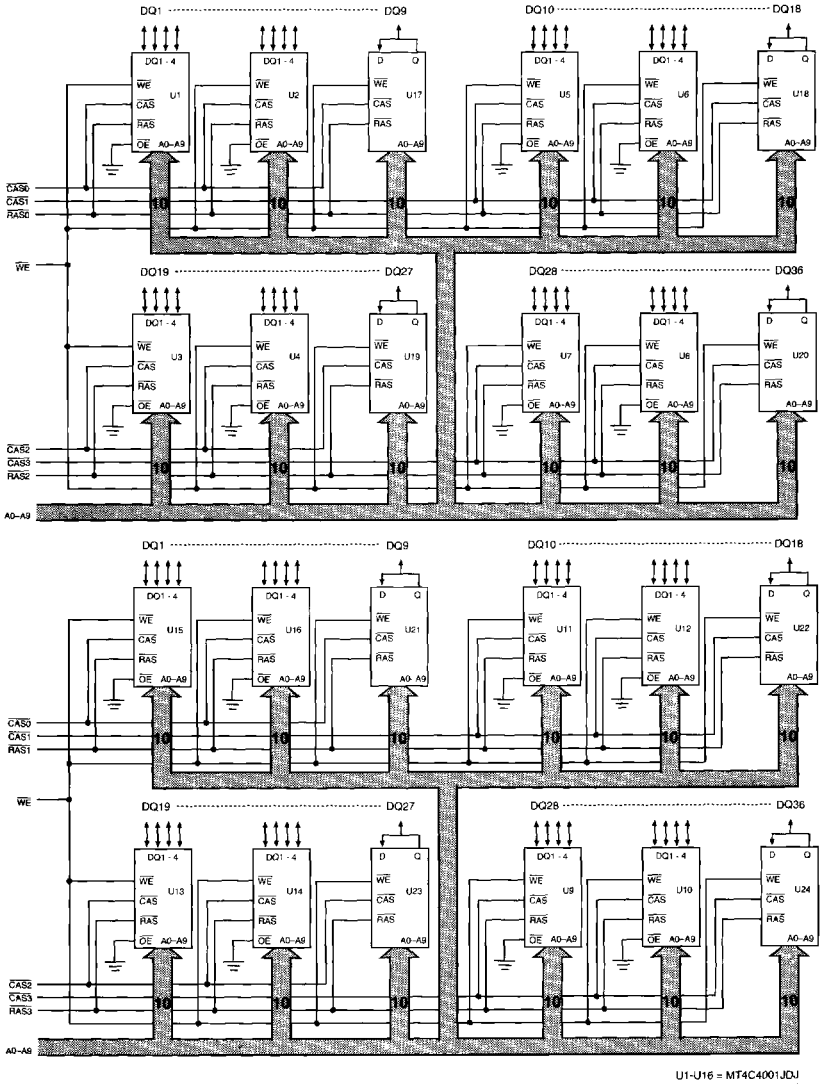
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its

correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

For x18 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x18 memory organization.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001JDJ
U17-U24 = MT4C1024DJ
or
U1-U16 = MT4C4001JDJ S (L-version)
U17-U24 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L-version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 24W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6, 22) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-12	12	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A0-A9, $\overline{WE}$	I_{I2}	-48	48	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	I_{I3}	-12	12	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ36	I_{OZ}	-10	10	µA	
OUTPUT LEVELS		V_{OH}	2.4		V	
Output High Voltage (I_{OUT} = -5mA)						
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	48	48	48	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	24	24	24	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		4.8	4.8	4.8	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	1264	1144	1024	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	944	824	704	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	1264	1144	1024	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	1264	1144	1024	mA	19, 22
REFRESH CURRENT: Extended CBR Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) $\overline{WE}$ = V_{CC} -0.2V; A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	6.4	6.4	6.4	mA	19, 22, 24, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		140	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		188	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}		50	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO}		18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	9
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		55		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = 5V ±10%)

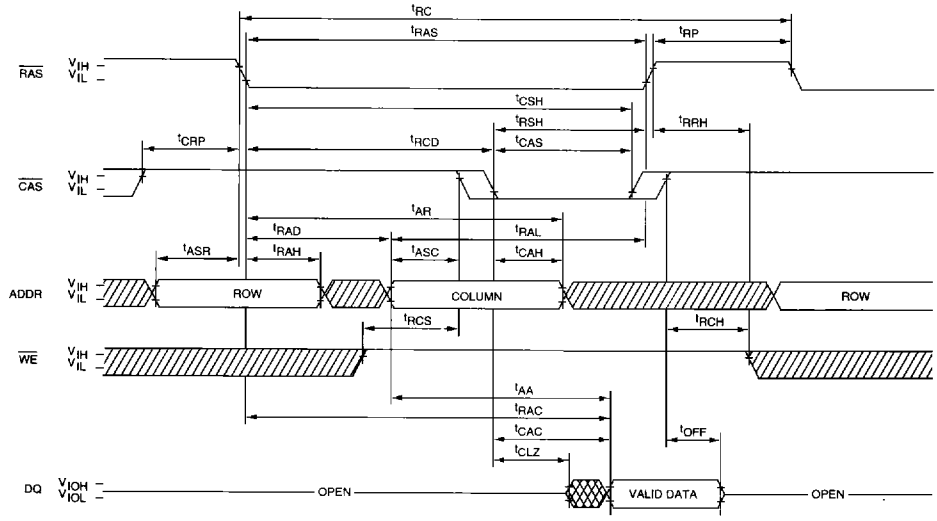
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	3	20	ns	12, 25
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^tREF		16/128*		16/128*		16/128*	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		15		ns	19
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	28
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		10		ns	28
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		10		ns	28

*L-version only

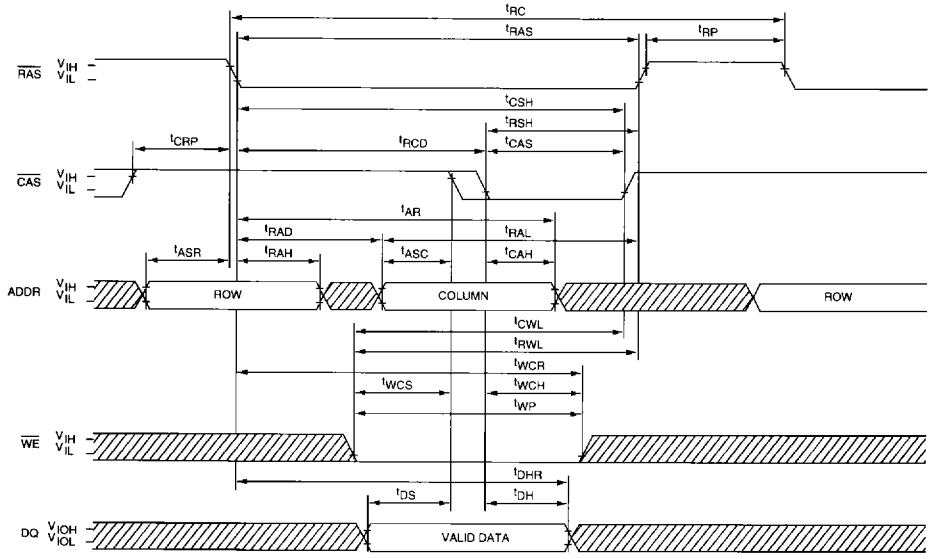
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on all 4 Meg DRAMs.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
24. Applies to L-version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
28. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.

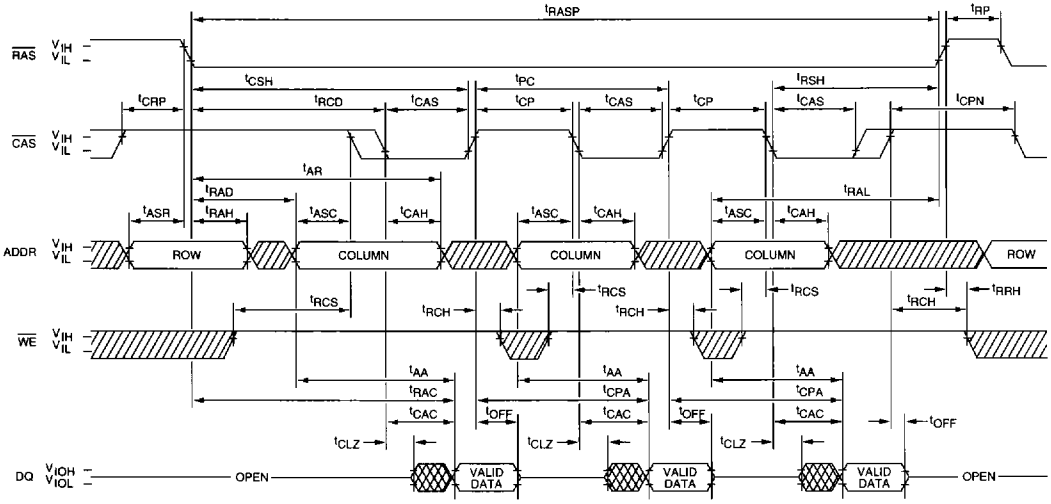
READ CYCLE



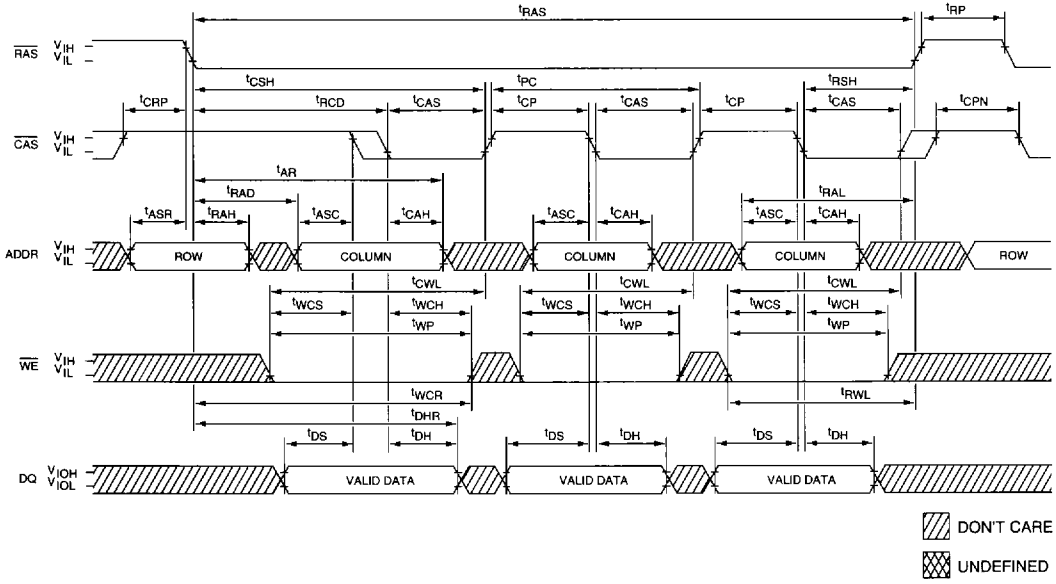
EARLY WRITE CYCLE



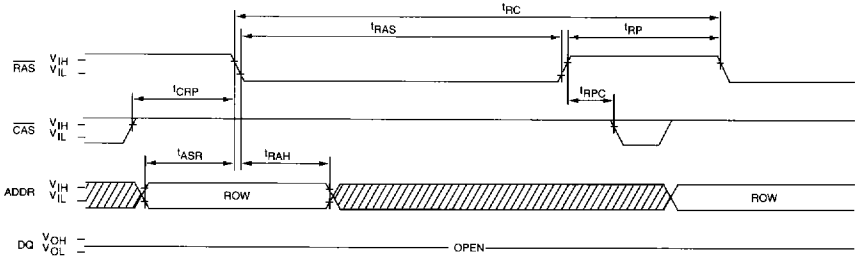
FAST-PAGE-MODE READ CYCLE



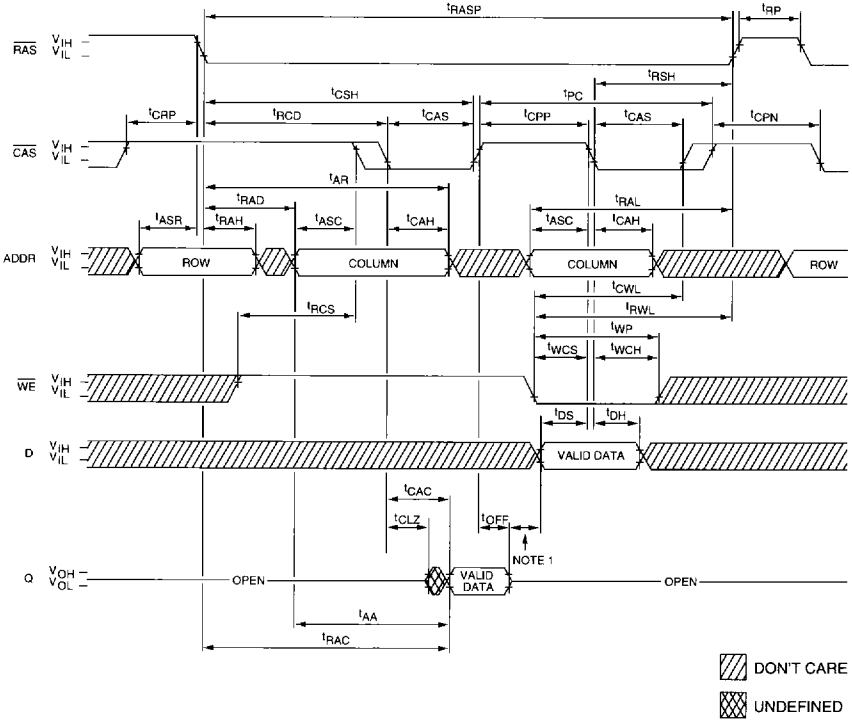
FAST-PAGE-MODE EARLY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A9; $\overline{WE}$ = DON'T CARE)

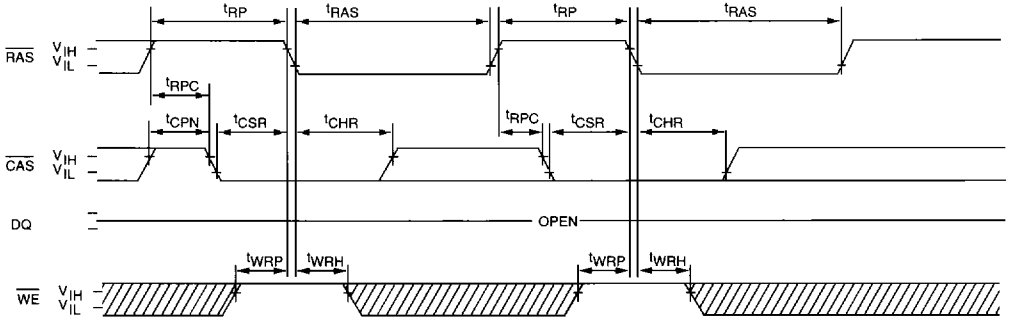


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

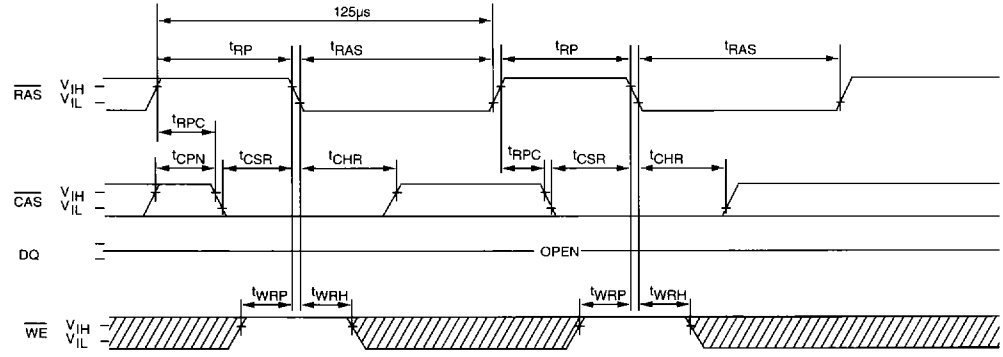


NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

CBR REFRESH CYCLE
(A0-A9 = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(A0-A9 = DON'T CARE)



DON'T CARE

UNDEFINED

HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)