ADVANCE‡

1 MEG x 16
3V ENHANCED+ BOOT BLOCK FLASH MEMORY

FLASH MEMORY MT28F160C34

FEATURES

- Thirty-nine erase blocks:
  - Eight 4K-word parameter blocks
  - Thirty-one 32K-word main memory blocks
- V_{CC}, $V_{CC}Q$ and V_{PP} voltages:
  - 3.3V ±5% V_{CC}
  - 3.3V ±5% $V_{CC}Q$
  - 1.65V–3.465V and 12V V_{PP}
- Address access times:
  - 90ns at 3.3V ±5%
- Low power consumption:
  - Standby and deep power-down mode < 1µA (typical I_{CC})
  - Automatic power saving feature (APS mode)
- Enhanced WRITE/ERASE SUSPEND (1µs typical)
- 128-bit OTP area for security purposes
- Industry-standard command set compatibility
- Software/hardware block protection

OPTIONS / NUMBER

- Timing
  90ns access — -9
- Boot Block Starting Address
  Top (FFFFFh) — T
  Bottom (00000h) — B
- Package
  46-ball FBGA (6 x 8 ball grid) — FD
- Temperature Range
  Extended (-40ºC to +85ºC) — ET

Part Number Example:
MT28F160C34FD-9 TET

BALL ASSIGNMENT (Top View)
46-Ball FBGA

	1	2	3	4	5	6	7	8
A	A13	A11	A8	V_{PP}	WP#	A19	A7	A4
B	A14	A10	WE#	RP#	A18	A17	A5	A2
C	A15	A12	A9			A6	A3	A1
D	A16	DQ14	DQ5	DQ11	DQ2	DQ8	CE#	A0
E	$V_{CC}Q$	DQ15	DQ6	DQ12	DQ3	DQ9	DQ0	V_{SS}
F	V_{SS}	DQ7	DQ13	DQ4	V_{CC}	DQ10	DQ1	OE#

(Ball Down)

NOTE: See page 3 for Ball Description Table.
See last page for mechanical drawing.

GENERAL DESCRIPTION

The MT28F160C34 is a nonvolatile, electrically block-erasable (flash), programmable memory containing 16,777,216 bits organized as 1,048,576 words (16 bits). The MT28F160C34 is manufactured on 0.22µm process technology in a 46-ball FBGA package.

The embedded WORD WRITE and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM), which simplifies these operations and relieves the system processor of secondary tasks. The WSM status can be monitored by an on-chip status register to determine the progress of program/erase tasks.

The device is equipped with 128 bits of one time programmable (OTP) area. The soft protection feature for blocks will mark them as read-only by configuring soft protection registers with command sequences.

ARCHITECTURE

The MT28F160C34 flash contains eight 4K-word parameter blocks and thirty-one 32K-word blocks. Memory is organized by using a blocked architecture to allow independent erasure of selected memory blocks. Any address within a block address range selects that block for the required READ, WRITE, or ERASE operation (see Figure 1).

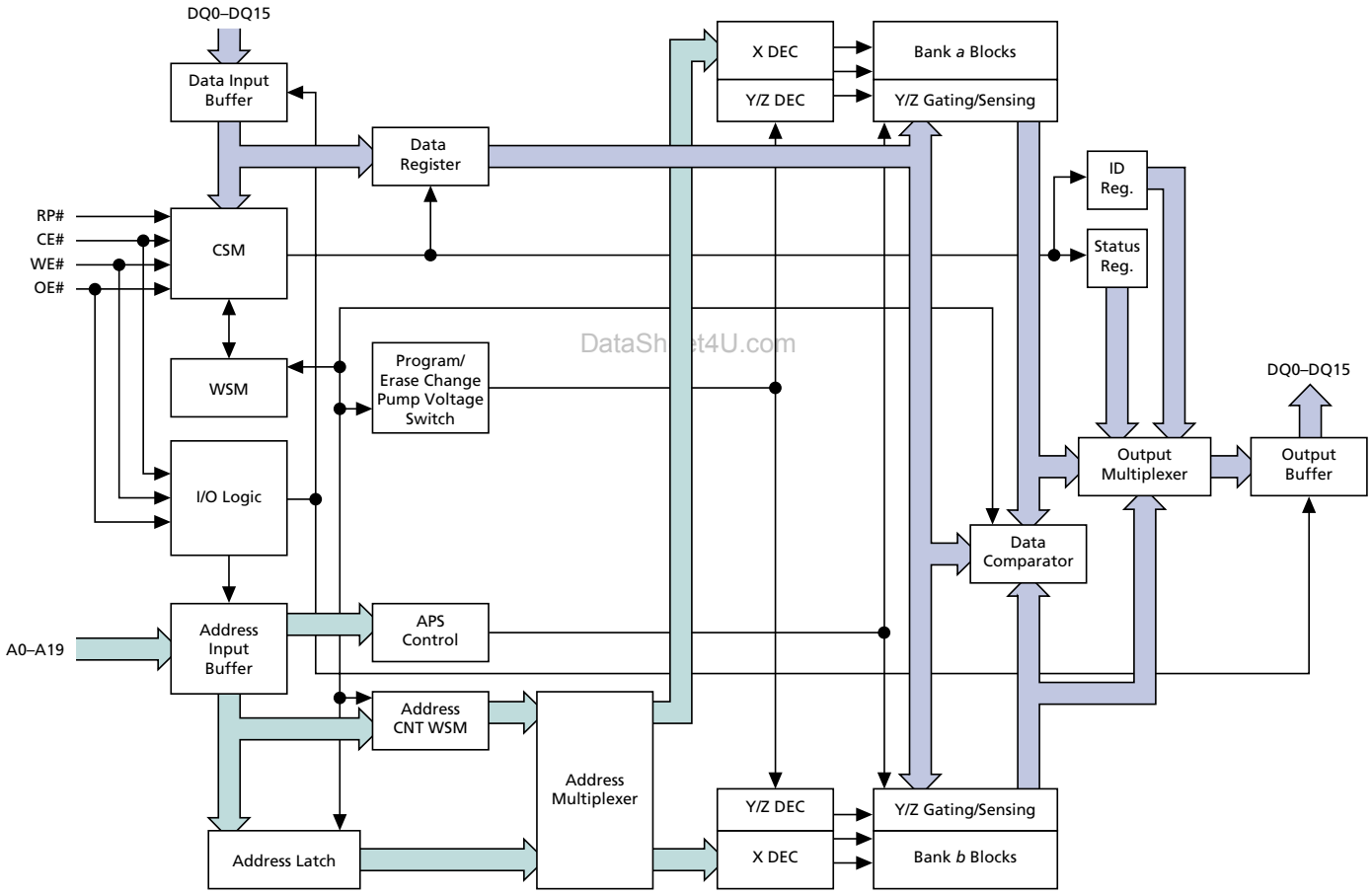
DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device mark is cross referenced to the Micron part numbers in Table 1.

Table 1
Cross Reference for Abbreviated Device Marks

PART NUMBER	PRODUCT MARKING	SAMPLE MARKING
MT28F160C34FD-9 TET	FW614	FX614
MT28F160C34FD-9 BET	FW615	FX615

FUNCTIONAL BLOCK DIAGRAM



BALL DESCRIPTIONS

46-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
3B	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command state machine (CSM) or to the memory array.
5A	WP#	Input	Write Protect: Unlocks the soft-protected blocks when HIGH if V_{PP} = 1.65V–3.465V or 12V and RP# = V_{IH} for WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
7D	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
4B	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the write state machine (WSM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
8F	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
1A, 1B, 1C, 1D, 2A, 2B, 2C, 3A, 3C, 5B, 6A, 6B, 6C, 7A, 7B, 7C, 8A, 8B, 8C, 8D	A0–A19	Input	Address Inputs: These address inputs select a unique, 16-bit word out of the 1,048,576 available.
2D, 2E, 2F, 3D, 3E, 3F, 4D, 4E, 4F, 5D, 5E, 6D, 6E, 6F, 7E, 7F	DQ0–DQ15	Input/ Output	Data I/O: These data I/O are data output lines during any READ operation or data input lines during a WRITE. Data I/O are used to input commands to the CSM.
4A	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the operation, V_{PP} must be 1.65V–3.465V or 12V. V_{PP} = "Don't Care" during all other operations.
5F	V_{CC}	Supply	Power Supply: 3.3V ±5%.
1E	$V_{CC}Q$	Supply	I/O Supply Voltage: 3.3V ±5%.
1F, 8E	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	V_{PP}	A0	DQ0–DQ7	DQ8–DQ15
Standby	H	H	X	X	X	X	X	High-Z	High-Z
RESET	L	X	X	X	X	X	X	High-Z	High-Z
READING									
READ	H	L	L	H	X	X	X	Data-Out	Data-Out
Output Disable	H	L	H	H	X	X	X	High-Z	High-Z
WRITE/ERASE (EXCEPT SOFT PROTECTED BLOCKS)[2]									
ERASE SETUP	H	L	H	L	X	X	X	20h	X
ERASE CONFIRM[3]	H	L	H	L	X	V_{PPH}	X	D0h	X
WRITE SETUP	H	L	H	L	X	X	X	10h/40h	X
WRITE[4]	H	L	H	L	X	V_{PPH}	X	Data-In	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	FFh	X
WRITE/ERASE (SOFT-PROTECTED BLOCKS)[2]									
ERASE SETUP	H	L	H	L	X	X	X	20h	X
ERASE CONFIRM[3]	H	L	H	L	H	V_{PPH}	X	D0h	X
WRITE SETUP	H	L	H	L	X	X	X	10h/40h	X
WRITE[4]	H	L	H	L	H	V_{PPH}	X	Data-In	Data-In
READ ARRAY[5]	H	L	H	L	X	X	X	FFh	X
DEVICE IDENTIFICATION[6]									
Manufacturer	H	L	L	H	X	X	L	2Ch	00h
Device (top boot)	H	L	L	H	X	X	H	92h	44h
Device (bottom boot)	H	L	L	H	X	X	H	93h	44h

NOTE: 1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH1} = 1.65V–3.465V and V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. See Table 3 for the IDENTIFY DEVICE command.

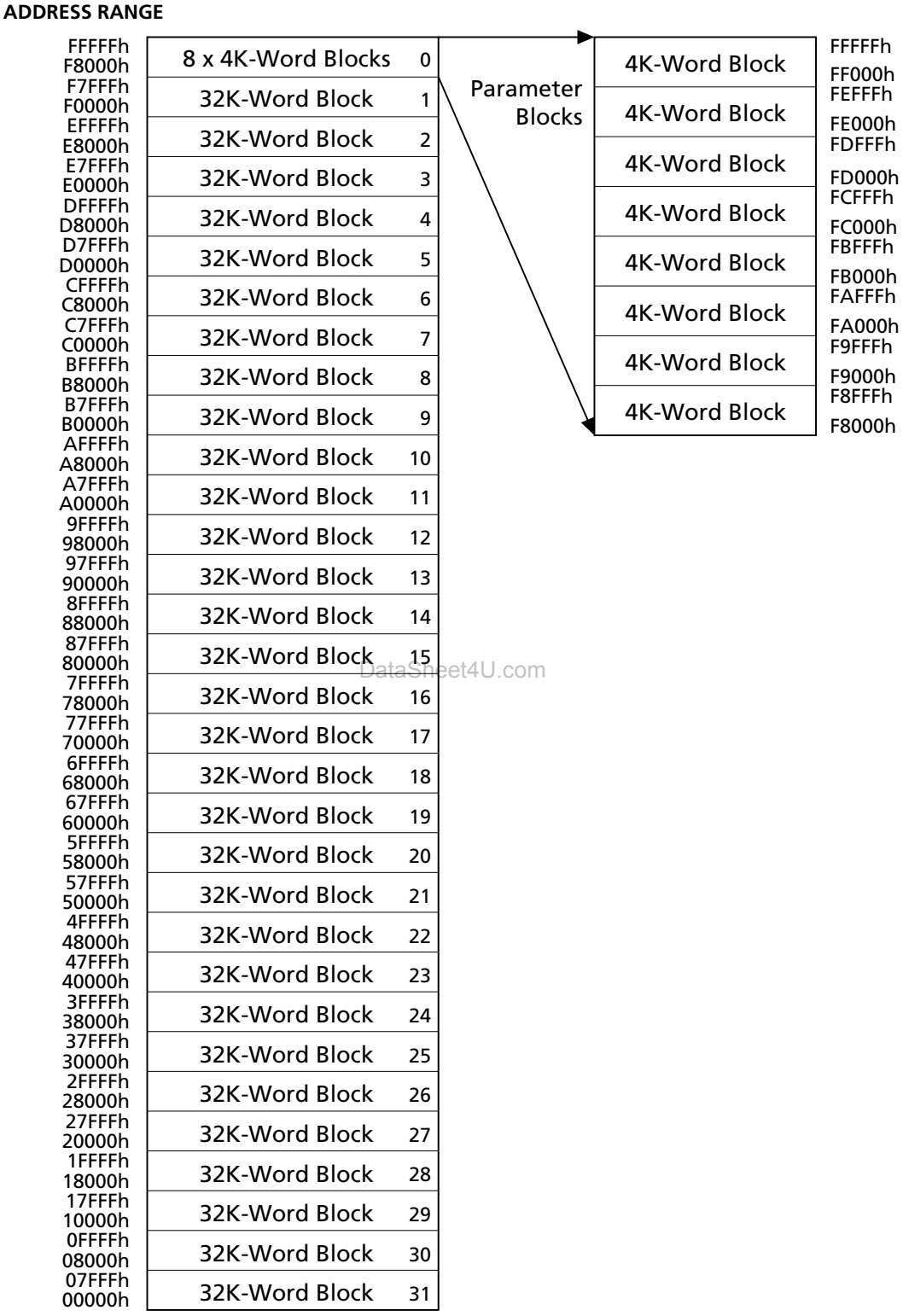


Figure 1
Top Boot Block Memory Address Map

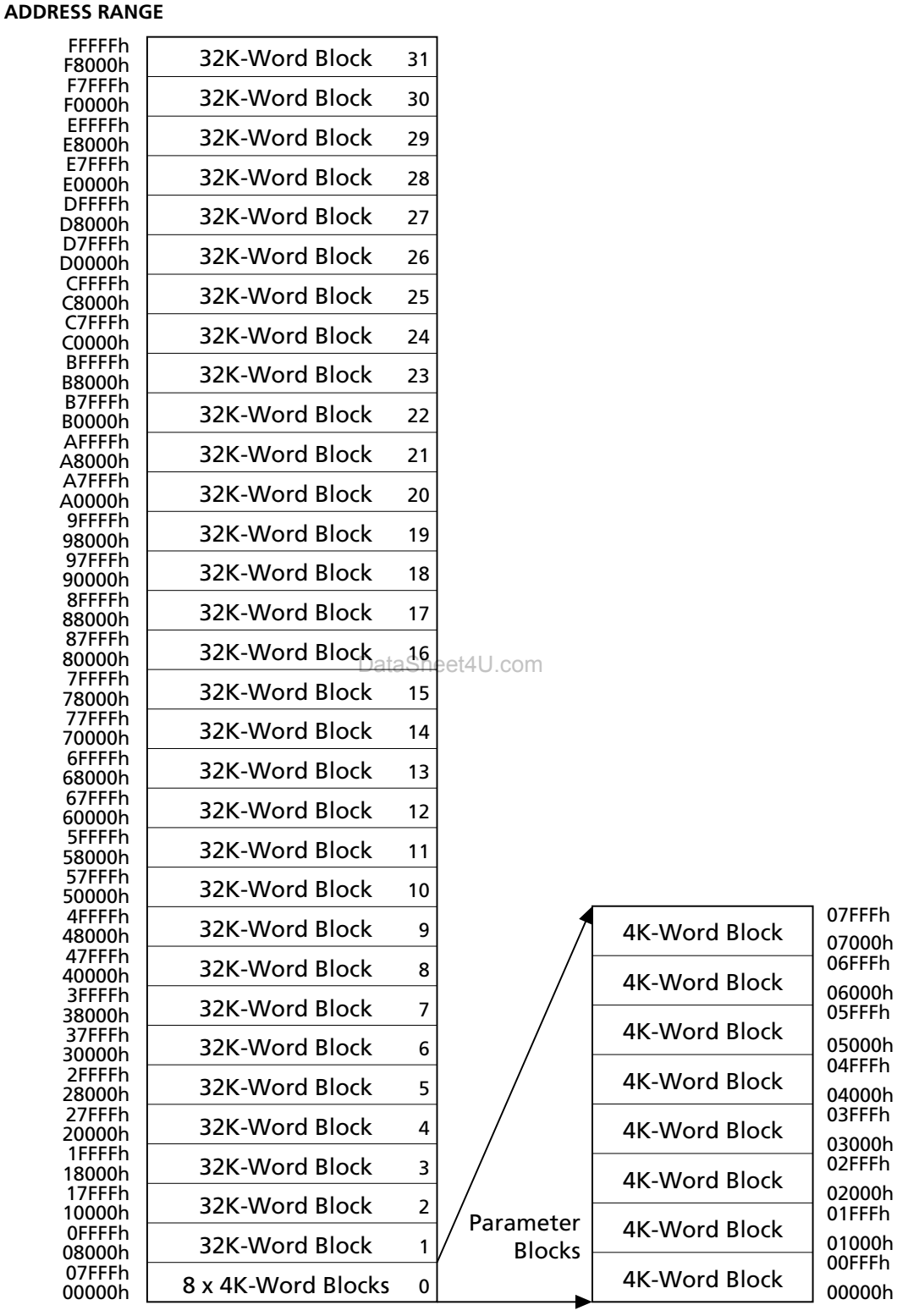


Figure 2
Bottom Boot Block Memory Address Map

MEMORY ORGANIZATION

The MT28F160C34 memory array is segmented into 31 blocks of 32K words, along with eight 4K-word parameter blocks. The device is available with block architecture mapped in either of the two configurations, with the parameter blocks located at the top or at the bottom of the memory array, as required by different microprocessors. The MT28F160C34 top boot configuration with the blocks and address ranges is shown in Figure 1, and the bottom boot configuration is shown in Figure 2.

COMMAND STATE MACHINE

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between the external microprocessor and the internal write state machine (WSM). The available commands are listed in Table 2, and the descriptions of these commands are shown in Table 3. Program and erase algorithms are automated by an on-chip WSM. Once a valid program/erase command sequence is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally to accomplish the requested operation. A command is valid only if the exact sequence of WRITEs is completed. After the WSM completes its task, the WSM status bit (SR7) is set to a logic HIGH level (1), allowing the CSM to respond to the full command set again.

OPERATION

Device operations are selected by entering standard JEDEC 8-bit command codes with conventional microprocessor timings into an on-chip CSM through I/Os DQ0–DQ7. When the device is powered up, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. The on-chip status register allows the progress of various operations to be monitored. The status register is interrogated by entering a READ STATUS REGISTER command onto the CSM (cycle 1) and reading the register data on I/Os DQ0–DQ7 (cycle 2). Status register bits SR0-SR7 correspond to DQ0–DQ7 (see Table 4).

Table 2
Command State Machine Codes for Device Mode Selection

COMMAND DQ0–DQ7	CODE ON DEVICE MODE
10h/40h	Write setup/alternate write setup
20h	Block erase setup
50h	Clear status register
70h	Read status register
90h	Identify device
0Fh	Soft protection
B0h	Program/erase suspend
D0h	Program/erase resume Erase confirm
FFh	Read array/OTP exit
AFh	OTP entry
60h	Reserved

COMMAND DEFINITIONS

Once a specific command code has been entered, the WSM executes an internal algorithm generating the necessary timing signals to program, erase, and verify data.

See Table 3 for the CSM command definitions and data for each of the bus cycles.

Table 3
Command Definitions

	FIRST CYCLE			SECOND CYCLE		
COMMAND	OPERATION	ADDRESS	CSM/INPUT	OPERATION	ADDRESS	DATA
READ ARRAY	WRITE	X	FFh	READ	WA	AD
IDENTIFY DEVICE	WRITE	X	90h	READ	IA	ID
READ STATUS REGISTER	WRITE	X	70h	READ	BA	SRD
WORD PROGRAM	WRITE	X	10h/40h	WRITE	WA	PD
BLOCK ERASE	WRITE	X	20h	WRITE	BA	D0h
PROGRAM/ERASE SUSPEND	WRITE	X	B0h			
PROGRAM/ERASE RESUME	WRITE	X	D0h			
CLEAR STATUS REGISTER	WRITE	X	50h			
SOFT PROTECTION	WRITE	X	0Fh	WRITE	BA	SPC
OTP ENTRY	WRITE	X	AFh	WRITE	X	AFh
OTP EXIT	WRITE	X	FFh	WRITE	X	FFh

NOTE: 1. The command data is written through DQ0–DQ7
2. ID = Manufacturer ID: 002Ch; Device ID (Top Boot): 4492h; Device ID (Bottom Boot): 4493h
3. IA = Identify address: 00000h for manufacturer code and 00001h for device code
4. BA = Any address within the block to be selected
5. WA = Word address
6. AD = Array data
7. SRD = Data read from status register
8. PD = Data to be written at location WA
9. SPC = Soft protect command:
   00h = Clear all soft protection
   FFh = Set all soft protection
   F0h = Clear addressed block soft protection
   0Fh = Set addressed block soft protection
10. X = Don't Care

STATUS REGISTER

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete. The status register is monitored by toggling OE# and CE# and by reading the resulting status code on I/O pins DQ0–DQ7. The high-order I/Os (DQ8–DQ15) are set to 00h internally, so only the low-order I/Os (DQ0–DQ7) need interpreting.

Register data is updated on the falling edge of OE# or CE#. The latest falling edge of either of these two signals updates the latch within a given READ cycle. Latching the data prevents errors from occurring if the register input changes during a status register monitoring. To ensure that the status register output contains updated status data, CE# or OE# must be toggled for each subsequent STATUS READ.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 4 defines the status register bits.

After monitoring the status register during a PROGRAM/ERASE, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

COMMAND STATE MACHINE OPERATIONS

The CSM decodes instructions for read, read device identification code, read status register, clear status register, program, erase, erase suspend, erase resume, program suspend, program resume, soft protection, and OTP entry/exit. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 2 for CSM codes). During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested.

During a PROGRAM cycle, the WSM controls the program sequences and the CSM responds to a PROGRAM SUSPEND command only. During an ERASE cycle, the CSM responds to an ERASE SUSPEND command only. When the WSM has completed its task, the WSM status bit (SR7) is set to a logic HIGH level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an ERASE or PROGRAM operation only when V_{PP} is within its correct voltage range. For data protection, it is required that RP# be held at a logic LOW level during a CPU reset.

CLEAR STATUS REGISTER

The WSM can set to "1" the block lock status bit (SR1), the V_{PP} status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to internal operations. After issuing this command, the status bits are cleared and the device returns to the read array mode.

READ OPERATIONS

Three READ operations are available: READ ARRAY, READ DEVICE IDENTIFICATION CODE, and READ STATUS REGISTER.

READ ARRAY

The array is read by entering the command code FFh on DQ0–DQ7. Control signals CE# and OE# must be at a logic LOW level (V_{IL}) and WE# and RP# must be at a logic HIGH level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15. Any valid address within any of the blocks selects that address and allows data to be read from that address. Upon initial power-up, the device defaults to the read array mode.

READ DEVICE IDENTIFICATION CODE

Device identification codes are read by entering command code 90h on DQ0–DQ7. Two bus cycles are required for this operation, the first to enter the command code and the second to read the selected code. Control signals CE# and OE# must be at a logic LOW level (V_{IL}) and WE# and RP# must be at a logic HIGH level (V_{IH}). The manufacturer code is obtained on DQ0–DQ15 in the second cycle, after the identify address 00000h is latched. The device code is obtained on DQ0–DQ15 in the second cycle, after the identify address 00001h is latched (see Table 3).

READ STATUS REGISTER

The status register is read by entering the command code 70h on DQ0–DQ7. Control signals CE# and OE# must be at a logic LOW level (V_{IL}), and WE# and RP# must be at a logic HIGH level (V_{IH}). Two bus cycles are required for this operation: one to enter the command code, and one to read the status register. The status register contents are updated on the falling edge of CE# or OE#, whichever occurs last within the cycle.

Table 4
Status Register

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS (WSM) 1 = Ready 0 = Busy	If SR7 = 0 (busy), the WSM has not completed an ERASE or PROGRAM operation. If SR7 = 1 (ready), other operations can be performed.
SR6	ERASE SUSPEND STATUS 1 = ERASE SUSPEND 0 = ERASE in progress or ERASE complete	If SR6 = 1, WSM halts execution, indicating that the ERASE operation has been suspended. SR6 remains "1" until an ERASE RESUME command is issued.
SR5	ERASE STATUS 1 = BLOCK ERASE error 0 = BLOCK ERASE successful	SR5 = 0 indicates that a BLOCK ERASE has been successful. SR5 = 1 indicates that an erase has failed; therefore, the WSM has completed the maximum allowable erase pulses determined by the internal algorithm but which were insufficient to completely erase the device.
SR4	PROGRAM STATUS 1 = PROGRAM error 0 = PROGRAM successful	SR4 = 0 indicates successful programming has occurred at the address location. SR4 = 1 indicates the WSM was unable to correctly program the addressed location.
SR3	V_{PP} STATUS 1 = Program abort V_{PP} range error 0 = V_{PP} good	SR3 provides status of V_{PP} during programming.
SR2	PROGRAM SUSPEND STATUS 1 = PROGRAM suspended 0 = PROGRAM in progress or PROGRAM complete	If SR2 = 1, WSM halts execution, indicating the PROGRAM operation has been suspended. SR2 stays "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS 1 = Block locked 0 = Block not locked	SR1 = 1 indicates that the address block is locked when WP# = V_{IL}. Any attempt to program/erase this block aborts the operation and the device returns to read status mode.
SR0	RESERVED	

NOTE:
1. After a PROGRAM/ERASE command is issued and confirmed, status bit SR7 goes LOW to indicate that the operation is in progress. If SR7 = 1 (ready), other polling operations can be performed. Until this occurs, the other status bits are not valid. SR7 is not updated automatically at the completion of a WSM task; therefore, if the WSM status bit shows busy (0), OE# and CE# must be toggled periodically to determine when the WSM has completed an operation (SR7 = 1).
2. When an ERASE SUSPEND command is issued, the WSM halts execution and sets SR6 = 1, indicating that the ERASE operation has been suspended. The WSM status bit is also set to HIGH (SR7 = 1), indicating that the ERASE SUSPEND operation has been completed successfully.
3. During an ERASE error, the SR5 bit is set (SR5 = 1), while SR5 = 0 indicates that a successful block erasure has occurred.
4. If the WSM is unable to program the addressed location correctly, the SR4 bit is set (SR4 = 1) and SR4 = 0 indicates that a successful programming operation has occurred at the addressed block location. Information concerning the status of V_{PP} during programming/erasure is provided by SR3. If V_{PP} is lower than V_{PPLK} after a PROGRAM/ERASE command has been issued, SR3 is set to a "1," indicating that the PROGRAM/ERASE operation has aborted due to a low V_{PP}.
5. During a PROGRAM SUSPEND command, the WSM halts execution and the SR2 bit is set, indicating that the PROGRAM operation has been suspended. This bit remains "1" until a PROGRAM RESUME command is issued. The WSM status bit is also set to HIGH (SR7 = 1), indicating that the PROGRAM SUSPEND operation has been completed successfully.
6. A proper block address must be provided in an ERASE operation. If that addressed block is protected, then the SR1 bit is set (SR1 = 1) when WP# = V_{IL}. If that block is not protected, then SR1 = 0.

PROGRAMMING OPERATIONS

There are two CSM commands for programming: program setup and alternate program setup (see Table 2). After the desired command code is entered, the WSM takes over and correctly sequences the device to complete the program operation. Monitoring of the WRITE operation is possible through the status register (see the Status Register section). During this time, the CSM responds only to a PROGRAM SUSPEND command until the PROGRAM operation has been completed, after which all commands to the CSM become valid again. (See Figure 4 for programming operation.)

During programming, V_{PP} must remain in the appropriate V_{PP} voltage range as shown in the recommended operating conditions table. Different combinations of RP#, WP#, and V_{PP} voltage levels ensure that data in certain blocks are secure and therefore cannot be programmed (see Table 5 for a list of combinations). Only "0s" are written and compared during a PROGRAM operation. If "1s" are programmed, the memory cell contents do not change and no error occurs.

PROGRAM SUSPENSION

The PROGRAM operation can be suspended by issuing a PROGRAM SUSPEND command (B0h). The PROGRAM SUSPEND command typically takes 1µs to execute, and the device is then in program suspend mode. Once the WSM has reached the suspend state, it allows the CSM to respond only to READ ARRAY, READ STATUS REGISTER, and PROGRAM RESUME commands. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the PROGRAM operation, a PROGRAM RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set. (See Figure 7 for PROGRAM SUSPEND and PROGRAM RESUME.)

ERASE OPERATIONS

An ERASE operation must be used to initialize all bits in an array block to "1s." After BLOCK ERASE CONFIRM is issued, the CSM responds only to an ERASE SUSPEND command until the WSM completes its task.

Block erasure inside the memory array sets all bits within the addressed block to logic 1s. Erase is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Note that different combinations of RP#, WP# and V_{PP} voltage levels ensure that data in certain blocks are secure and therefore cannot be erased (see Table 5 for a list of combinations). Block erasure is initiated by a command sequence to the CSM: block erase setup (20h) followed by block erase confirm (D0h) (see Figure 5). A two-command erase sequence protects against accidental erasure of memory contents.

When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally verification is performed to ensure that all bits are correctly erased. Monitoring of the ERASE operation is possible through the status register (see the Status Register section).

ERASE SUSPENSION

During the execution of an ERASE operation, the ERASE SUSPEND command (B0h) can be entered to direct the WSM to suspend the ERASE operation. The ERASE SUSPEND command typically takes 1µs to execute, and the device is then in erase suspend mode. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, ERASE RESUME and PROGRAM commands. During the ERASE SUSPEND operation, array data must

Table 5
Data Protection Combinations

DATA PROTECTION PROVIDED	V_{PP}	RP#	WP#
All blocks locked	≤ V_{PPLK}	X	X
All blocks locked	X	V_{IL}	X
All blocks unlocked	≥ V_{PPLK}	V_{IH}	V_{IH}
Soft-protected blocks locked	≥ V_{PPLK}	V_{IH}	V_{IL}

be read from a block other than the one being erased. To resume the ERASE operation, an ERASE RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set. It is also possible that an ERASE in any block can be suspended and a WRITE to another block can be initiated. After the completion of WRITE, the ERASE can be resumed by writing an ERASE RESUME command (see Figure 6). It is also possible to suspend the WRITE operation and read from another block.

AUTOMATIC POWER-SAVING MODE

Substantial power savings are realized during periods when the device is not accessed while in the active mode. During this time, the device switches to the automatic power saving (APS) mode. When the device switches to this mode, I_{CC} is reduced to 1µA typically. This mode is entered automatically if no address or control lines toggle within approximately a 300ns time-out period. At least one transition on CE# must occur after power-up to activate this mode's availability. The device remains in this mode and the I/O lines retain the data from the last access until a new read address is issued or another operation is initiated.

RESET/ DEEP POWER-DOWN MODE

Very low levels of power consumption can be attained by using a special ball, RP#, to disable internal device circuitry. When RP# is at a logic LOW level of 0.0V ±0.2V, a much lower I_{CC} current consumption is achieved, typically 1µA. This is important in portable applications where extended battery life is a major concern.

A recovery time is required when exiting from deep power-down mode. A minimum of t_{RS} is required before a CSM command can be recognized. With RP# at ground, the WSM is reset and the status register is cleared, effectively eliminating accidental programming to the array during system reset. After restoration of power, the device will be disabled until RP# is returned to V_{IH}.

If RP# goes LOW during a PROGRAM or ERASE operation, the device powers down and becomes nonfunctional. Data being written or erased at that time becomes invalid or indeterminate, requiring that the operation be performed again after power restoration. When RP# is set at logic LOW, all internal circuits will be reset. Setting RP# LOW during a PROGRAM or ERASE operation is not recommended.

OTP MODE

The device has 128 bits of OTP (one time programmable) area. There are 64 bits that are programmed at the factory with a unique 64-bit code that is not modifiable. The other 64-bit OTP area is left blank to program for customer design requirements if needed. Protection of the user-programmable, 64-bit contents is provided, after the area is programmed, by programming the lock bit.

To program the OTP area, two "AFh" commands must be written, followed by two WRITE cycles of the normal program sequences. When in the OTP mode, the WSM programs the OTP area and not the array. During programming, a read can acquire only the WSM status (status register output). When the programming is complete, the device remains in the OTP mode and only the status can be read in the OTP area. Writing two "FFh" commands exits the OTP mode and causes the device to go into the read array mode. To read the OTP area after programming, the OTP mode must be re-entered.

To read the OTP area contents, two "AFh" commands must be written, followed by a READ. Writing two "FFh" commands exits the OTP mode and causes the device to go into the read array mode.

After programming the 64-bit OTP area, the lock bit can be programmed. The lock bit is at address 00040h and is on DQ15. Once the lock bit is programmed to a "0," the 64-bit, user-programmable area is permanently protected (see Figure 3). The lock bit can be read in OTP mode, as described above.

STANDBY MODE

I_{CC} supply current is reduced by applying a logic HIGH level on CE# and RP# to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a logic HIGH level ($V_{CC}Q$) on CE# and RP# reduces the current to 1µA typically. If the device is deselected during an ERASE operation or during programming, the device continues to draw active current until the operation is complete.

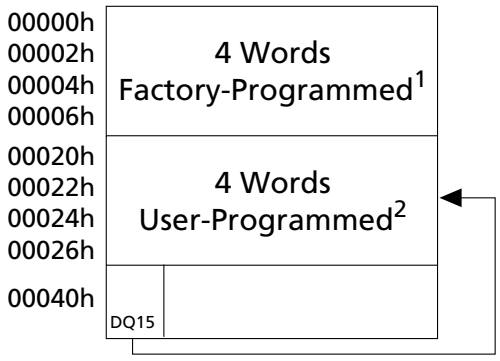


Figure 3
OTP Area Map

NOTE: 1. Always locked.
2. Locked by programming DQ15 at address 00040h.

SOFT BLOCK DATA PROTECTION

Soft protection is available with CSM command 0Fh (see Table 3). The protection bit for each block can be set and cleared individually, or all at once. After the soft protection bit of a block is set, the block is protected when $V_{PP} \geq V_{PPLK}$, RP# is HIGH, and WP# is LOW. When $V_{PP} \leq V_{PPLK}$ the block is protected (locked) as well. A block is unlocked when WP# is HIGH, even if its soft protection bit is set (see Table 5).

When the device is powered down or reset, the soft protection bits will be set to the protected state. If WP# goes LOW after first power-up, reset, or power-down, all blocks are protected. The CSM command 0Fh is needed to clear the soft protected blocks. When WP# goes LOW, the cleared blocks are unprotected.

The block lock status bit SR1 is used to monitor the individual block lock status after the second WRITE cycle of the soft protection CSM command. Additionally, to monitor the block lock status of any block, the read status register command 70h can be used. On the command's second cycle, any address within a block is issued and SR1 indicates the block lock status for that block. When monitoring the block lock status bit SR1, the correct status can only be obtained with WP# LOW.

POWER-UP

During a power-up, it is not necessary to sequence V_{CC} Q, V_{CC}, and V_{PP}. However, it is recommended that RP# be held LOW during power-up for additional protection while V_{CC} is ramping above V_{LKO} to a stable operative level. After a power-up or RESET, the status register is reset, and the device will enter the array read mode.

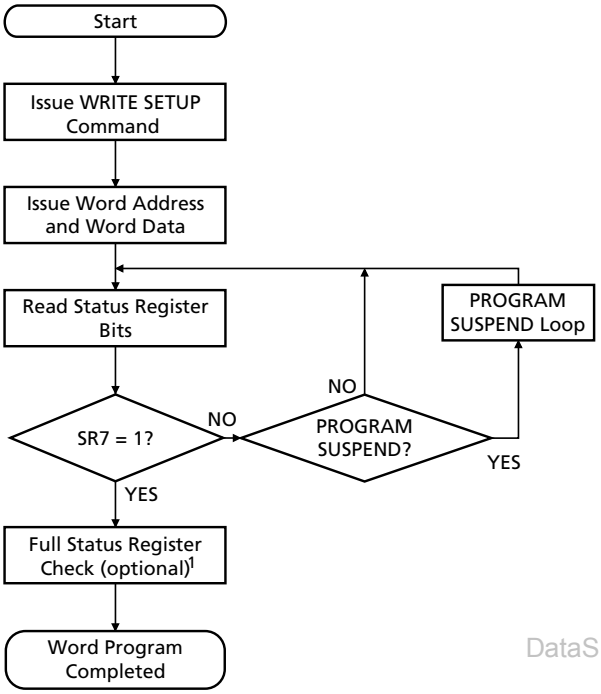
POWER-UP PROTECTION

The likelihood of unwanted WRITE or ERASE operations is minimized since two consecutive cycles are required to execute either operation. When $V_{CC} < V_{LKO}$, the device does not accept any WRITE cycles, and noise pulses < 5ns on CE# or WE# do not initiate a WRITE cycle.

POWER SUPPLY DECOUPLING

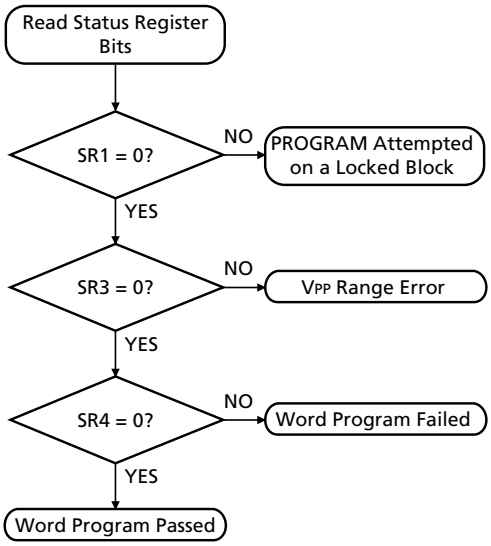
For decoupling purposes, each device should have a 0.1µF ceramic capacitor connected between V_{CC} and V_{SS}, V_{PP} and V_{SS}, and between $V_{CC}Q$ and V_{SS}. The capacitor should be as close as possible to the device balls.

Figure 4
Automated Word Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE SETUP	Data = 40h or 10h Addr = Don't Care
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word programming operation to reset the device to read array mode.		

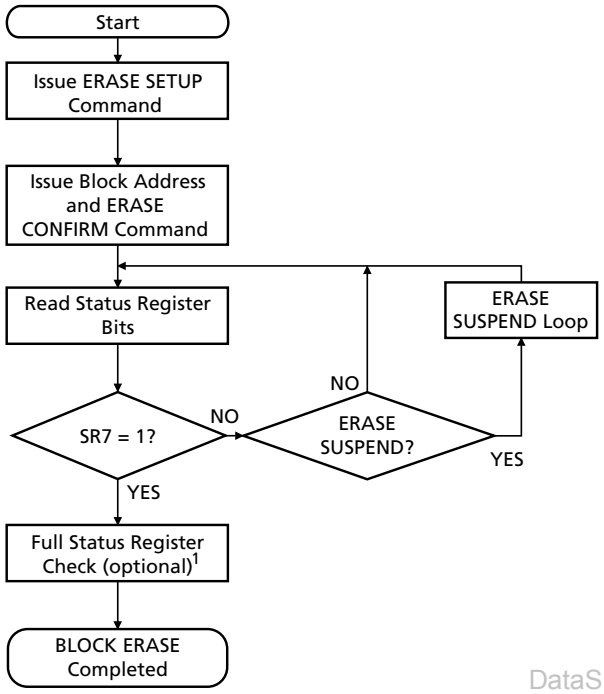
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect V_{PP} low
Standby		Check SR4[3] 1 = Word program error

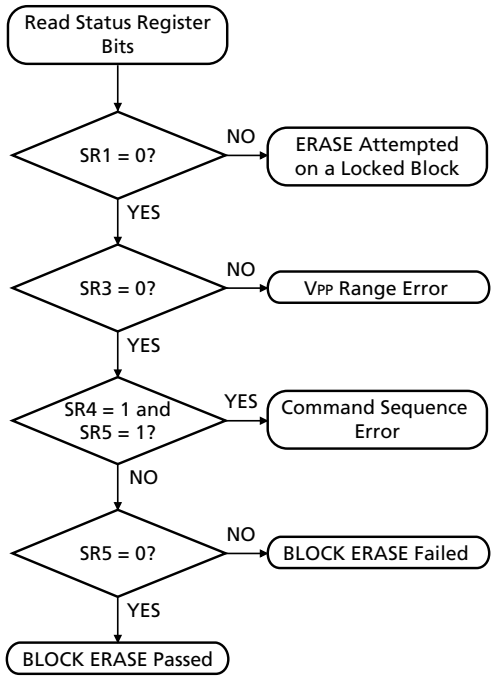
NOTE: 1. Full status register check can be done after each word or after a sequence of words.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR4 is cleared only by the CLEAR STATUS REGISTER command, but it does not prevent additional program operation attempts.

Figure 5
Automated BLOCK ERASE Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Addr = Don't Care
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last BLOCK ERASE operation to reset the device to read array mode.		

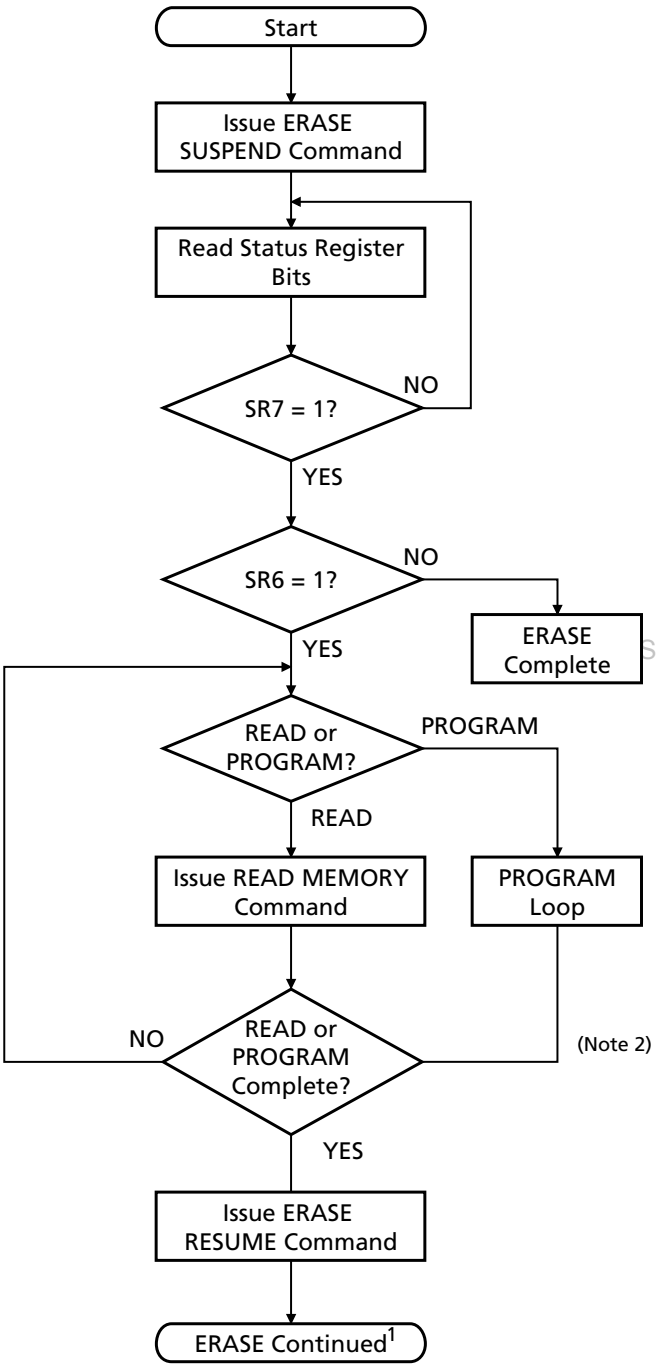
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect VPP low
Standby		Check SR4 and SR5 1 = BLOCK ERASE command error
Standby		Check SR5[3] 1 = BLOCK ERASE error

NOTE: 1. Full status register check can be done after each block or after a sequence of blocks.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

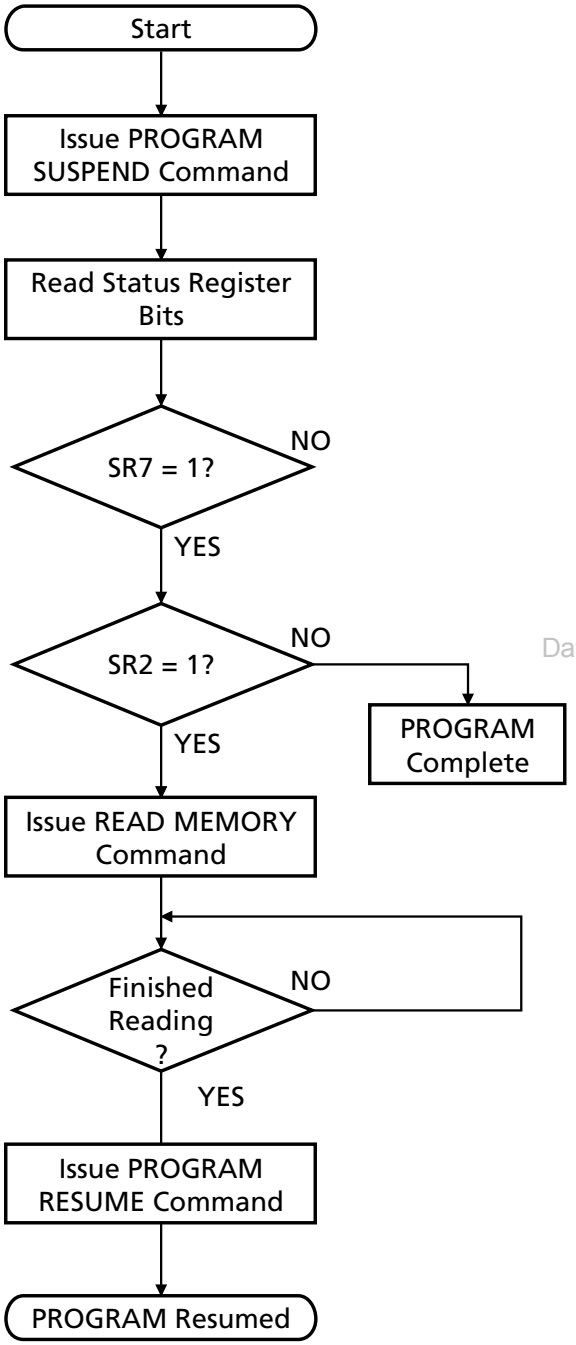
Figure 6
ERASE SUSPEND/ERASE RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h
READ		Status register data Toggle OE# or CE# to update status register
Standby		Check SR7 1 = Ready
Standby		Check SR6 1 = Suspended
WRITE or WRITE	READ MEMORY WRITE SETUP	Data = FFh Data = 40h or 10h Addr = Don't Care
READ or WRITE	 WRITE DATA	Read data from block other than that being erased Data = Word to be programmed Addr = Address of word to be programmed
WRITE	ERASE RESUME	Data = D0h Addr = Don't Care

NOTE: 1. See BLOCK ERASE Flowchart for complete erasure procedure.
2. See Word Programming Flowchart for complete programming procedure.

Figure 7
PROGRAM SUSPEND/ PROGRAM RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
READ		Status register data Toggle OE# or CE# to update status register
Standby		Check SR7 1 = Ready
Standby		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed
WRITE	PROGRAM RESUME	Data = D0h Addr = Don't Care

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage Range, V_{CC} ..... -0.6V to +4.0V[3]
Supply Voltage Range, V_{PP} ..... -0.6V to +13.0V[3]
Input Voltage Range ..... -0.6V to +4.0V
Output Voltage Range ..... -0.6V to +4.0V[4]
Storage Temperature Range, T_{STG} ..... -65°C to +150°C

[1]Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
[2]All voltage values are with respect to V_{SS}.
[3]The voltage can undershoot to -1V for periods < 20ns.
[4]The voltage on any output can overshoot to 4.6V for periods < 20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ +85°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (during program/read/erase/suspend)	V_{CC}	3.135	3.465	V	5
I/O Supply Voltage	V_{CCQ}	3.135	3.465	V	5, 6
Supply Voltage (during program/erase operations)	V_{PP1}	1.65	3.465	V	5
	V_{PP2}	11.4	12.6	V	5, 7
Input High (Logic 1) Voltage, all inputs	V_{IH}	V_{CCQ} - 0.2	V_{CCQ} + 0.2	V	5
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.2	0.2	V	5
OUTPUT VOLTAGE LEVELS V_{CC} = V_{CC} (MIN), V_{CCQ} = V_{CCQ} (MIN) Output High Voltage (I_{OH} = -0.1mA)	V_{OH}	V_{CCQ} - 0.1	–	V	5
Output Low Voltage (I_{OL} = 0.1mA)	V_{OL}	–	0.1	V	
INPUT LEAKAGE CURRENT V_{CC} = V_{CC} (MAX), V_{CCQ} = V_{CCQ} (MAX) Any input (0V ≤ V_{IN} ≤ V_{CCQ}); All other balls not under test = 0V	I_L	-1	1	µA	
OUTPUT LEAKAGE CURRENT V_{CC} = V_{CC} (MAX), V_{CCQ} = V_{CCQ} (MAX) (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CCQ})	I_{OZ}	-10	10	µA	
BLOCK ERASE cycling	–	100,000	–	Cyc	

NOTE: 5. All voltages referenced to V_{SS}.
6. V_{CCQ} must be less than or equal to V_{CC}.
7. 12V V_{PP} is allowable for production only.

CAPACITANCE

(T_A = +25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

READ, STANDBY AND DEEP POWER-DOWN CURRENT DRAIN

(-40°C ≤ T_A ≤ +85°C; V_{CC} = 3.3V ±5%)

PARAMETER/CONDITION		SYMBOL	TYP	MAX	UNITS	NOTES
READ CURRENT: V_{CC} = V_{CC} (MAX), V_{CCQ} = V_{CCQ} (MAX) (CE# = V_{IL}; OE# = V_{IH}; RP# = V_{IH}; f = 5 MHz; Other inputs V_{IH} or V_{IL})		I_{CC1}	–	30	mA	1, 2
STANDBY CURRENT: V_{CC} SUPPLY V_{CC} = V_{CC} (MAX); (CE# = RP# = V_{CCQ})		I_{CC2}	1	10	µA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY V_{CC} = V_{CC} (MAX); V_{CCQ} = V_{CCQ} (MAX) (RP# = V_{IL}; Other inputs V_{CCQ} or V_{SS})		I_{CC3}	1	10	µA	
READ CURRENT: V_{PP} SUPPLY	$V_{PP} \le V_{CC}$	I_{PP1}	2	±15	µA	
	$V_{PP} > V_{CC}$	I_{PP2}	50	200	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY (RP# = V_{IL}; $V_{PP} \le V_{CC}$)		I_{PP3}	1	10	µA	
STANDBY CURRENT: V_{PP} SUPPLY ($V_{PP} \le V_{CC}$)		I_{PP4}	1	10	µA	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. Automatic power savings (APS) mode reduces I_{CC1} to standby current level I_{CC2} for static operation.

AC TEST CONDITIONS

Input pulse levels	0V to $V_{CC}Q$
Input rise and fall times	<10ns
Input timing reference level	$V_{CC}Q/2$
Output timing reference level	$V_{CC}Q/2$
Output load	C_L = 30pF

Figure 8
AC Test Output and Load Circuit

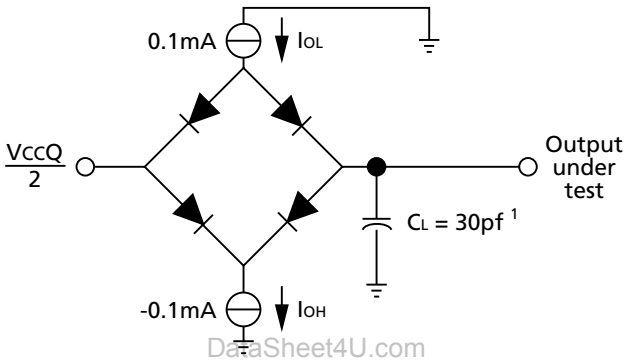
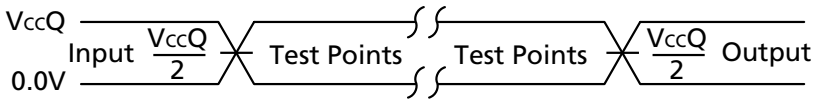


Figure 9
AC Input/Output Reference Waveform



NOTE: 1. C_L includes probe and fixture capacitance.

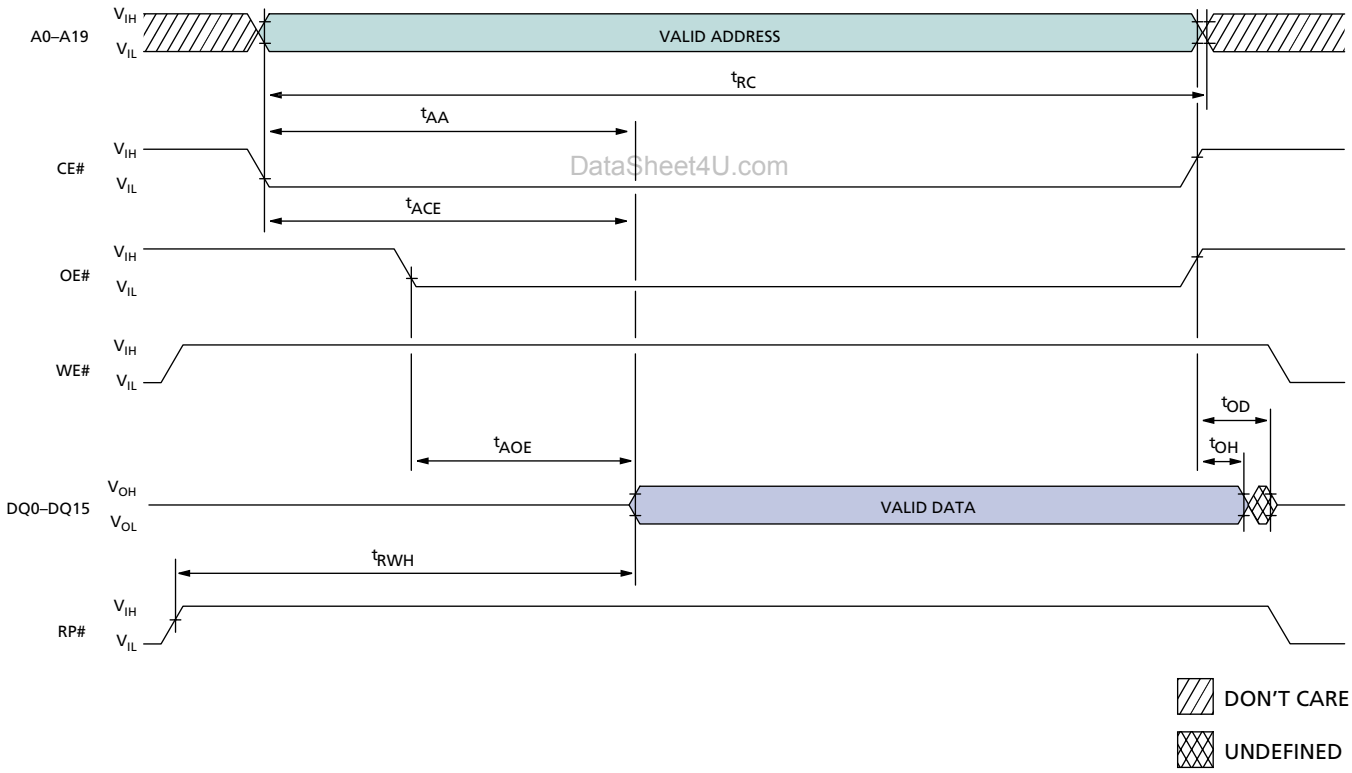
READ AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ +85°C; Vcc = 3.3V ±5%)

AC CHARACTERISTICS		-9			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ cycle time	^tRC	90		ns	
Access time from CE#	^tACE		90	ns	1
Access time from OE#	^tAOE		30	ns	1
Access time from address	^tAA		90	ns	
RP# HIGH to output valid delay	^tRWH		600	ns	
RP# LOW pulse width	^tRP	100		ns	
OE# or CE# HIGH to output in High-Z	^tOD		25	ns	
Output hold time from OE#, CE# or address change	^tOH	0		ns	

NOTE: 1. OE# may be delayed by ^tACE minus ^tAOE after CE# falls before ^tACE is affected.

READ CYCLE



TIMING PARAMETERS

SYMBOL	-9 MIN	-9 MAX	UNITS
^tRC	90		ns
^tACE		90	ns
^tAOE		30	ns
^tAA		90	ns

SYMBOL	-9 MIN	-9 MAX	UNITS
^tRWH		600	ns
^tOD		25	ns
^tOH	0		ns

RECOMMENDED DC WRITE/ERASE CONDITIONS

(-40°C ≤ T_A ≤ +85°C; V_{CC} = 3.3V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{PP} WRITE/ERASE lockout voltage	V_{PPLK}	–	–	1	V	1
V_{PP} voltage during WRITE/ERASE operation	V_{PPH1}	1.65	–	3.465	V	
	V_{PPH2}	11.4	–	12.6	V	2
V_{CC} WRITE/ERASE lockout operation	V_{LKO}	–	1.5	–	V	

WRITE/ERASE CURRENT DRAIN

(-40°C ≤ T_A ≤ +85°C; V_{CC} = 3.3V ±5%)

PARAMETER/CONDITION		SYMBOL	TYP	MAX	UNITS	NOTES
WRITE CURRENT: V_{CC} SUPPLY		I_{CC4}	–	55	mA	
ERASE CURRENT: V_{CC} SUPPLY		I_{CC5}	–	45	mA	
ERASE/PROGRAM SUSPEND CURRENT: V_{CC} SUPPLY (ERASE/PROGRAM suspended)		I_{CC6}	10	25	µA	3
WRITE/ERASE CURRENT: V_{PP} SUPPLY	$V_{PP} = V_{PP1}$	I_{PP5}	–	0.1	mA	
	$V_{PP} = V_{PP2}$	I_{PP6}	–	3	mA	
ERASE/PROGRAM SUSPEND CURRENT: V_{PP} SUPPLY (ERASE/PROGRAM suspended)	$V_{PP} = V_{PP1}$	I_{PP7}	1	10	µA	
	$V_{PP} = V_{PP2}$	I_{PP8}	50	200	µA	

WORD WRITE AND ERASE DURATION CHARACTERISTICS

	3.3V ±5% Vcc					
	1.65V–3.465V V_{PP}		12V V_{PP}			
PARAMETER	TYP	MAX	TYP	MAX	UNITS	NOTES
Boot/parameter BLOCK ERASE time	0.5	4	0.5	4	s	4, 5
Main BLOCK ERASE time	1	5	1	5	s	4, 5
Boot/parameter BLOCK WRITE time	0.1	–	0.1	–	s	4, 5, 6, 7
Main BLOCK WRITE time	0.3	–	0.3	–	s	4, 5, 6, 7
Program/erase suspend latency	1	3	1	3	µs	

NOTE:
1. Absolute WRITE/ERASE protection when $V_{PP} \le V_{PPLK}$.
2. 12V V_{PP} is allowable for production only. Write timings are identical to 1.65V–3.465V V_{PP} operation.
3. Parameter is specified when device is not accessed. Actual current draw will be I_{CC6} plus current of operation being executed while the device is in suspend mode.
4. The 12V V_{PP} is for production only.
5. Typical values measured at T_A = +25°C.
6. Assumes no system overhead.
7. Typical write times tested with checkerboard data pattern.

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE# (CE#)-CONTROLLED WRITES

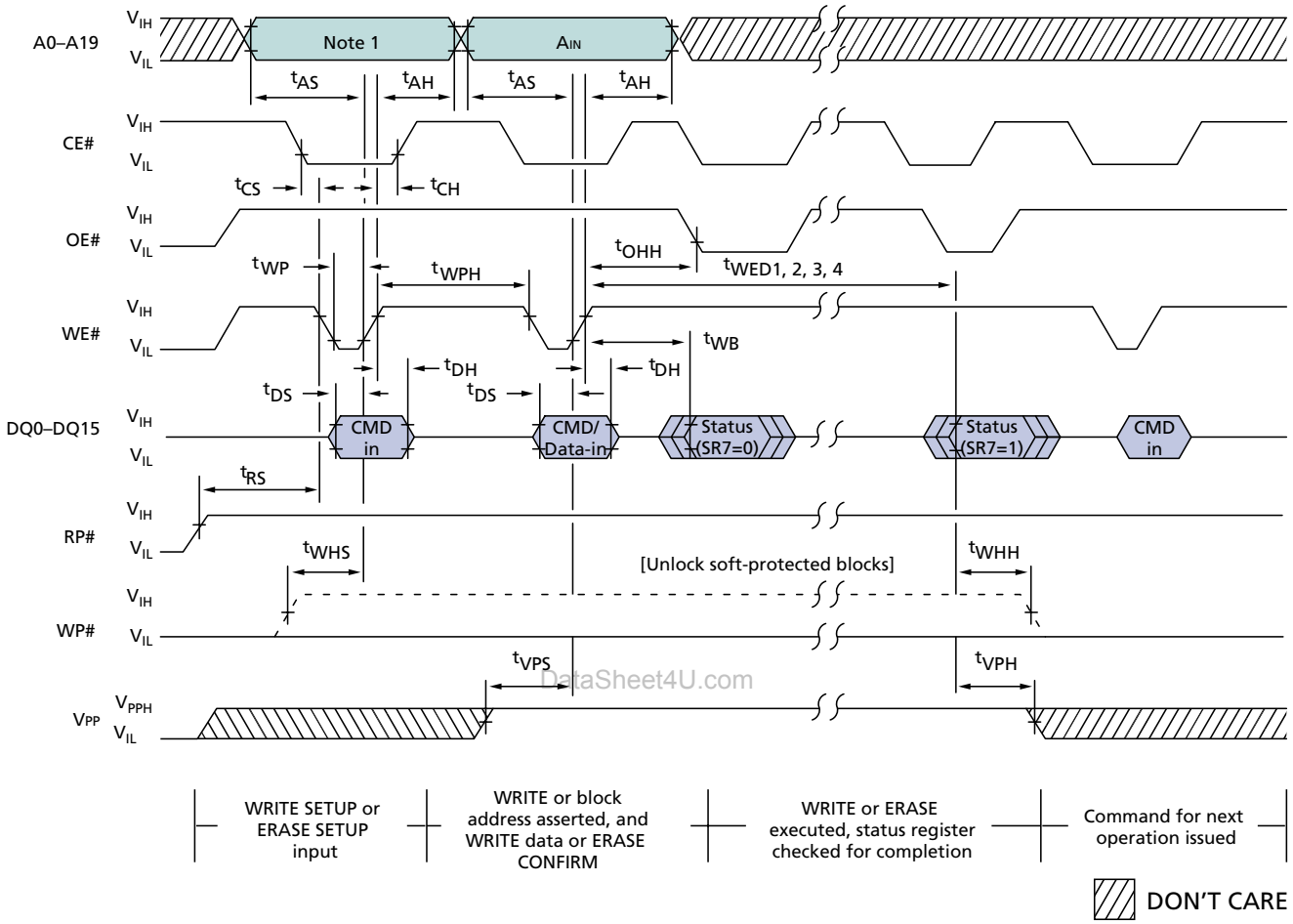
(-40°C ≤ T_A ≤ +85°C; V_{CC} = 3.3V ±5%)

AC CHARACTERISTICS		-9		
PARAMETER	**SYMBOL**	**MIN**	**UNITS**	**NOTES**
WE# (CE#) HIGH pulse width	^tWPH (^tCPH)	30	ns	
WE# (CE#) pulse width	^tWP (^tCP)	70	ns	
Address setup time to WE# (CE#) HIGH	^tAS	70	ns	
Address hold time from WE# (CE#) HIGH	^tAH	0	ns	
Data setup time to WE# (CE#) HIGH	^tDS	50	ns	
Data hold time from WE# (CE#) HIGH	^tDH	0	ns	
CE# (WE#) setup time to WE# (CE#) LOW	^tCS (^tWS)	0	ns	
CE# (WE#) hold time from WE# (CE#) HIGH	^tCH (^tWH)	0	ns	
V_{PP} setup time to WE# (CE#) HIGH	^tVPS	200	ns	
RP# HIGH to WE# (CE#) LOW delay	^tRS	150	ns	
WRITE duration	$^tWED1$	6	µs	
Boot BLOCK ERASE duration	$^tWED2$	0.5	s	
Parameter BLOCK ERASE duration	$^tWED3$	0.5	s	
Main BLOCK ERASE duration	$^tWED4$	1	s	
V_{PP} hold time from status data valid	^tVPH	0	ns	
WE# (CE#) HIGH to busy status (SR7 = 0)	^tWB	200	ns	1, 2
WP# HIGH setup time to WE# (CE#) HIGH	^tWHS	0	ns	
WP# HIGH hold time from status data valid	^tWHH	0	ns	
OE# HIGH hold time from WE# HIGH	^tOHH	30	ns	

NOTE: 1. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
2. ^tWB = 800ns (MAX).

WRITE/ERASE CYCLE

WE#-CONTROLLED WRITE/ERASE



TIMING PARAMETERS

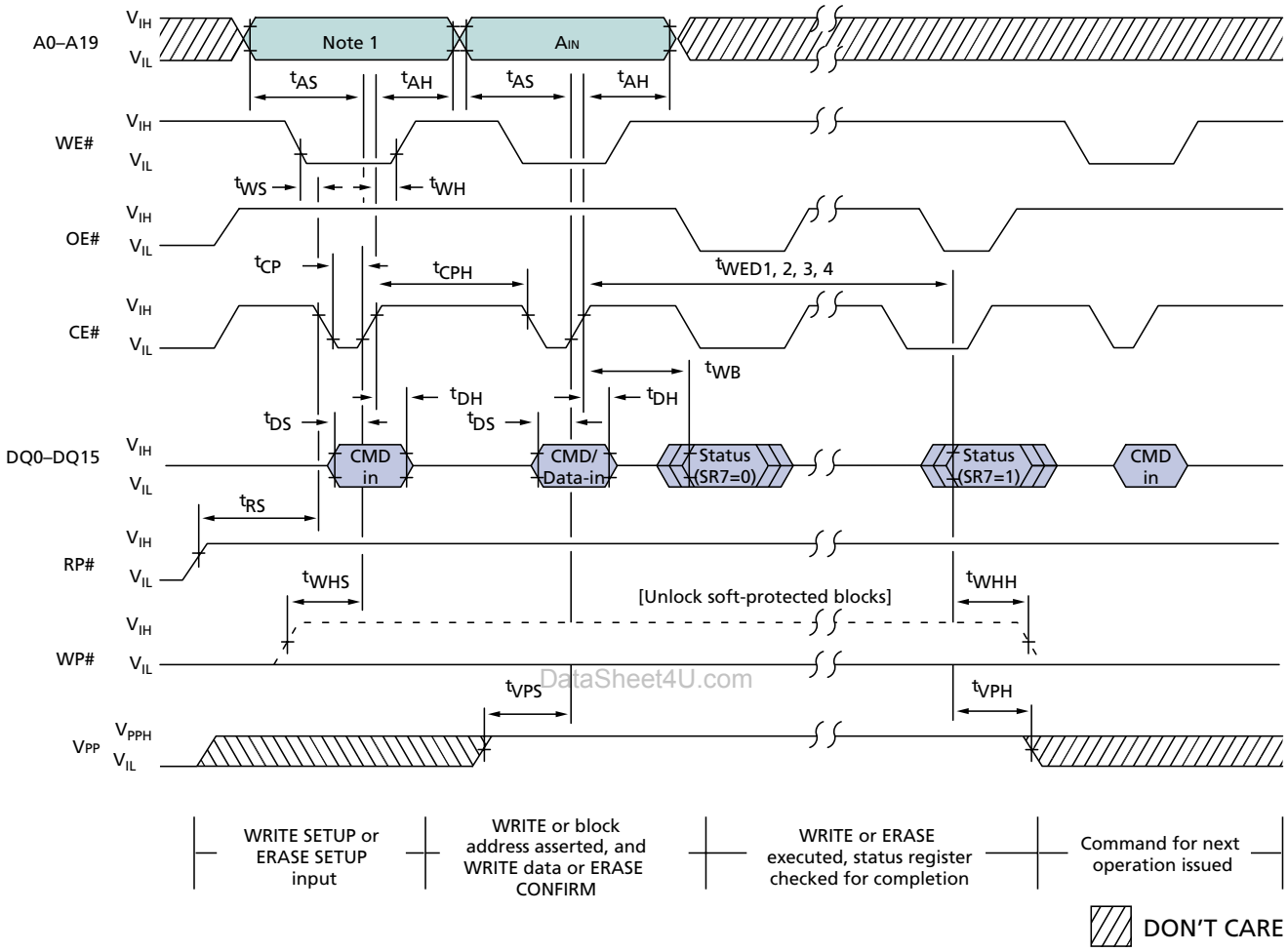
SYMBOL	-9 MIN	UNITS
tWPH	30	ns
tWP	70	ns
tAS	70	ns
tAH	0	ns
tDS	50	ns
tDH	0	ns
tCS	0	ns
tCH	0	ns
tVPS	200	ns
tRS	150	ns

SYMBOL	-9 MIN	UNITS
tWED1	6	µs
tWED2	0.5	s
tWED3	0.5	s
tWED4	1	s
tVPH	0	ns
tWB[2]	200	ns
tWHS	0	ns
tWHH	0	ns
tOHH	30	ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. tWB = 800ns (MAX).

WRITE/ERASE CYCLE

CE#-CONTROLLED WRITE/ERASE



TIMING PARAMETERS

SYMBOL	-9 MIN	UNITS
tCPH	30	ns
tCP	70	ns
tAS	70	ns
tAH	0	ns
tDS	50	ns
tDH	0	ns
tWS	0	ns
tWH	0	ns
tVPS	200	ns

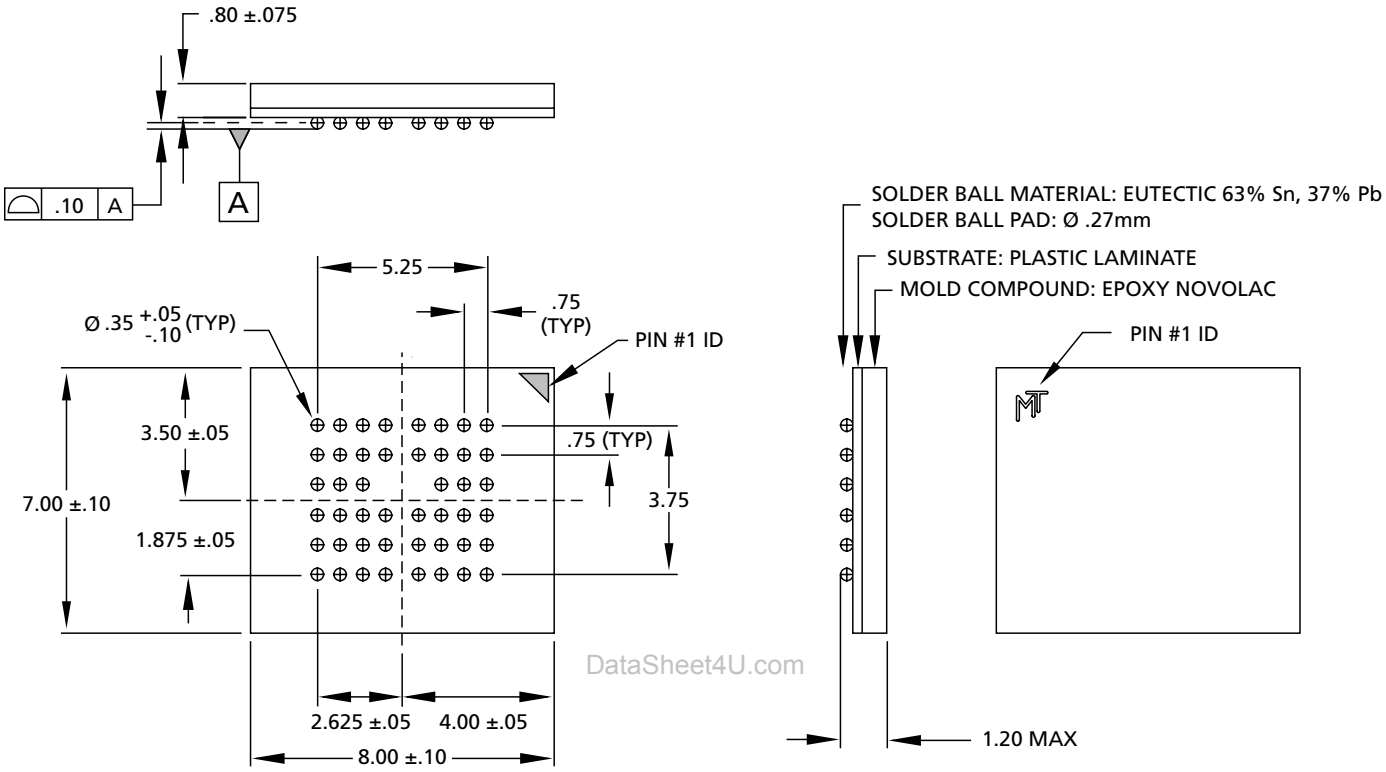
SYMBOL	-9 MIN	UNITS
tRS	150	ns
tWED1	6	µs
tWED2	0.5	s
tWED3	0.5	s
tWED4	1	s
tVPH	0	ns
tWB[2]	200	ns
tWHS	0	ns
tWHH	0	ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. tWB = 800ns (MAX).

Table 6
Command State Machine Current/Next States

	COMMAND INPUTS (and next state)													
Current State	SR7	Data when Read	Read Array (FFh)	Write setup (10h/ 40h)	Block erase setup (20h)	Erase confirm (D0h)	Prog./ erase susp. (B0h)	Prog./ erase resume (D0h)	Read SR (70h)	Clear SR (50h)	Identify device (90h)	Soft prot. setup (0Fh)	Soft prot. (SPC)	Otp entry (AFh)
Read Array	1	Array	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Read Status	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Identify Device	1	ID	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Soft Prot. Setup	1	Status	Soft prot. all	Read array								Soft prot. block	Soft prot.	Read array
Soft Protection Complete	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Write Setup	1	Status	Program											
Program Not Complete	0	Status	Program (not complete)				Prog. susp. status		Program (not complete)					
Program Suspend Status	1	Status	Program susp. read array	Program suspend read array		Program	Program susp. read array	Program	Program susp. status	Program suspend read array				
Program Suspend Read Array	1	Array	Program susp. read array	Program suspend read array		Program	Program susp. read array	Program	Program susp. status	Program suspend read array				
Program Complete	1	Status	Read Array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Erase Setup	1	Status	Erase command error			Erase	Erase	Erase	Erase command error					
Erase Comd. Error	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ Read array	Otp entry
Erase Not Complete	0	Status	Erase (not complete)				Erase susp. to status		Erase (not complete)					
Erase Suspend Status	1	Status	Erase susp. read array	Write setup	Erase susp. read array	Erase	Erase susp. read array	Erase	Erase susp. status	Erase suspend read array				
Erase Suspend Array	1	Array	Erase susp. read array	Write setup	Erase susp. read array	Erase	Erase susp. read array	Erase	Erase susp. status	Erase suspend read array				
Erase Complete	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry

46-BALL FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

DATA SHEET DESIGNATION

Advance This data sheet contains initial descriptions of products still under development.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

REVISION HISTORY

Rev. 3 ..... 8/01
- Added ^{t}WB maximum specification
- Corrected WRITE/ERASE Cycle timing diagram (CE#-Controlled)

Rev. 2, ADVANCE 3/01
- Added a bottom boot block starting address
- Updated package drawing

Original document, ADVANCE 2/01