NAND Flash Memory

Serial Peripheral Interface (SPI)

MT29F1G01AAADD

Features

- Single-level cell (SLC) technology
- Organization
  - Page size x1: 2112 bytes (2048 + 64 bytes)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes x 512 blocks per plane
  - Device size: 1Gb: 1024 blocks
- Data retention: 10 years
- New commands
  - PAGE READ in x2 mode
  - PAGE READ in x4 mode

Options

- Density: 1Gb (single die)
- Operating temperature
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)
- Package
  - 63-ball VFBGA, lead-free, (9mm x 11mm)

Table 1: NAND Flash SPI Parameters

Parameters	Value
V_{CC} range	2.7–3.6V
Frequency	50 MHz
Transfer rate	20ns
Loading throughput	50 MT/s
^{t}BERS (BLOCK ERASE)	4ms (TYP)
^{t}PROG (PAGE PROGRAM)	400µs (TYP)
^{t}RD (PAGE READ)	100µs (MAX)
Internal ECC correction	4-bit
Width	x1, x2, x4

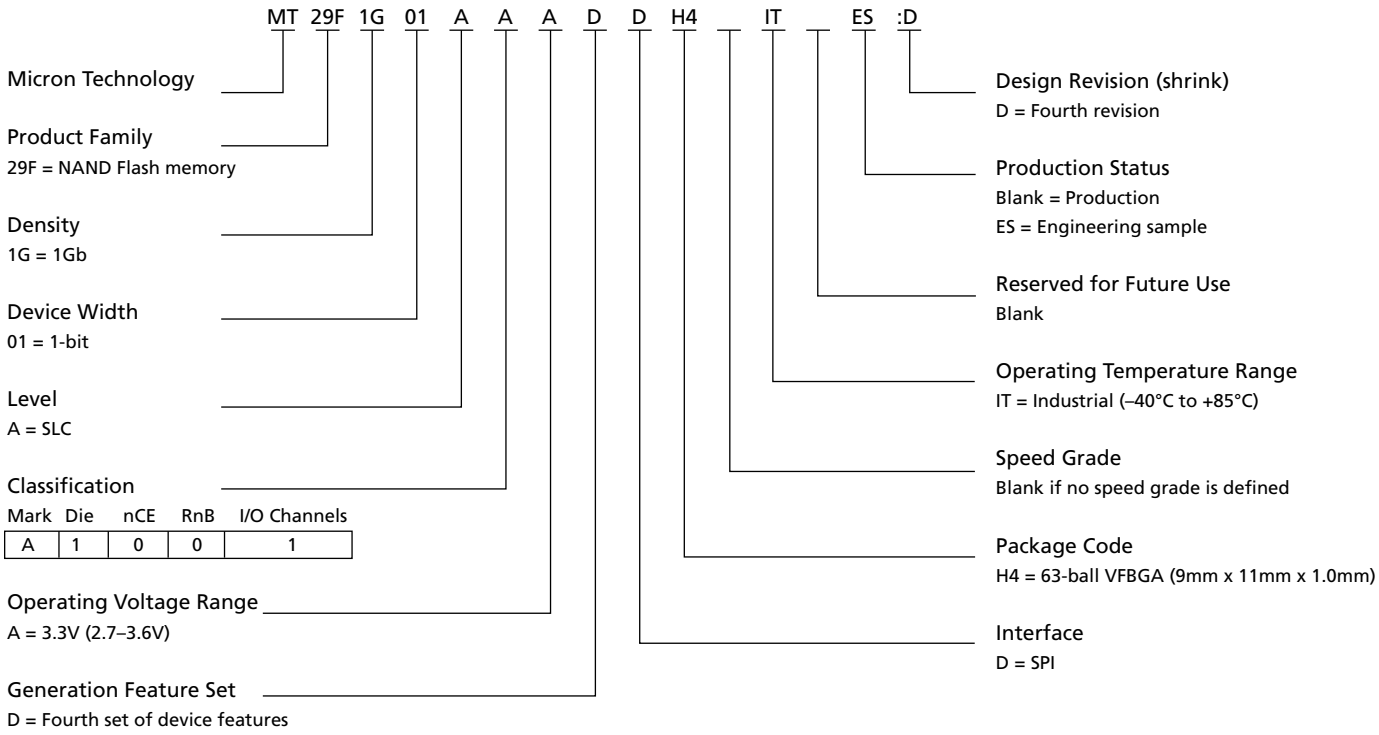
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Contents

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

List of Figures

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

List of Tables

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

General Description

The serial peripheral interface (SPI) provides NAND Flash with a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

SPI NAND Flash is an SLC NAND Flash memory device based on the standard parallel NAND Flash. The serial electrical interface follows the industry-standard serial peripheral interface. New command protocols and registers are defined for SPI operation. The command set resembles common SPI-NOR command sets, modified to handle NAND-specific functions and added new features. New features include user-selectable internal ECC. SPI NAND Flash devices have six signal lines plus VCC and ground (GND). The signal lines are SCK (serial clock), SI, SO (for command/response and data input/output), and control signals CS, HOLD#, WP#. This hardware interface creates a low-pin-count device with a standard pinout that remains the same from one density to another, supporting future upgrades to higher densities without board redesign.

Each block of the serial NAND Flash device is subdivided into 64 programmable pages. Each page consists of 2112 bytes. The pages are further divided into a 2048-byte data storage region with a separate 64-byte spare area. The 64-byte area is typically used for memory and error management functions. See Table 10 on page 32 for available user area when ECC is enabled.

With internal ECC enabled, ECC code is generated internally when a page is written to the memory core. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

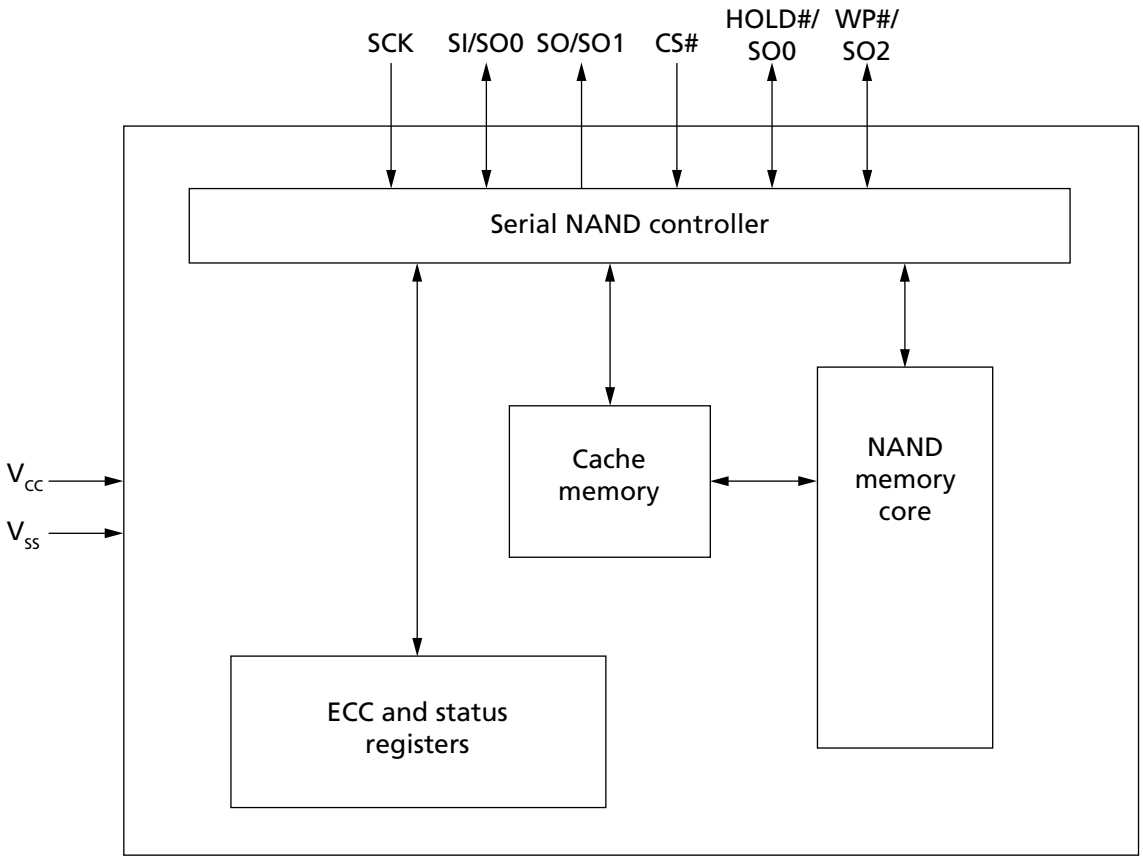
Architecture

These devices use an industry-standard NAND Flash memory core organized by page/block. The standard parallel NAND Flash electrical interface and I/O logic are replaced by an SPI interface. The new command protocol set is a modification of the SPI-NOR command set common in the industry. The modifications are specifically to handle functions related to NAND Flash architecture. The interface supports page and random read/write and copy-back functions. The device also includes an internal ECC feature.

Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

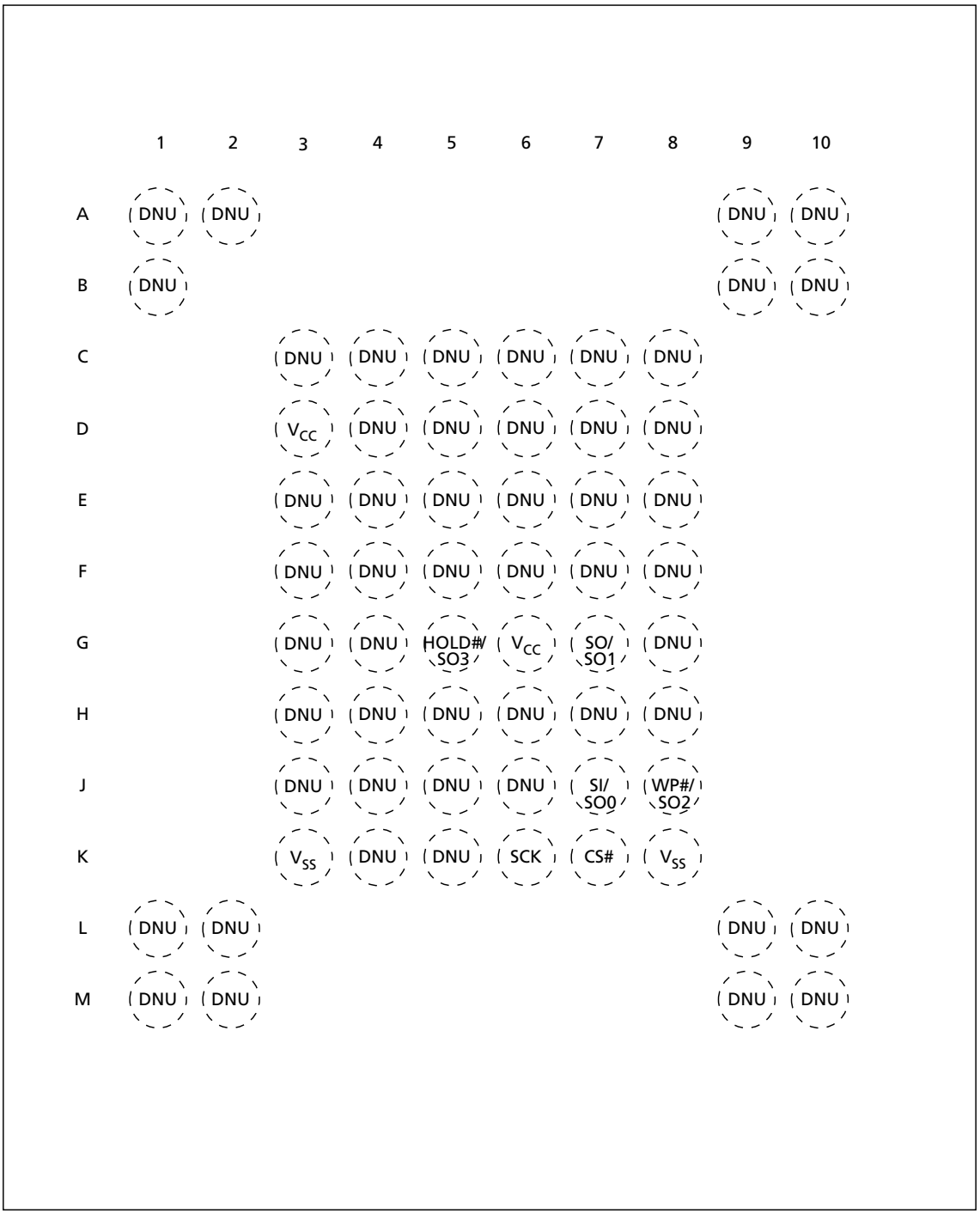
Figure 2: Functional Block Diagram



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Ball Assignments and Descriptions

Figure 3: 63-Ball VFBGA (SPI only) Ball Assignments



Top View, Ball Down

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

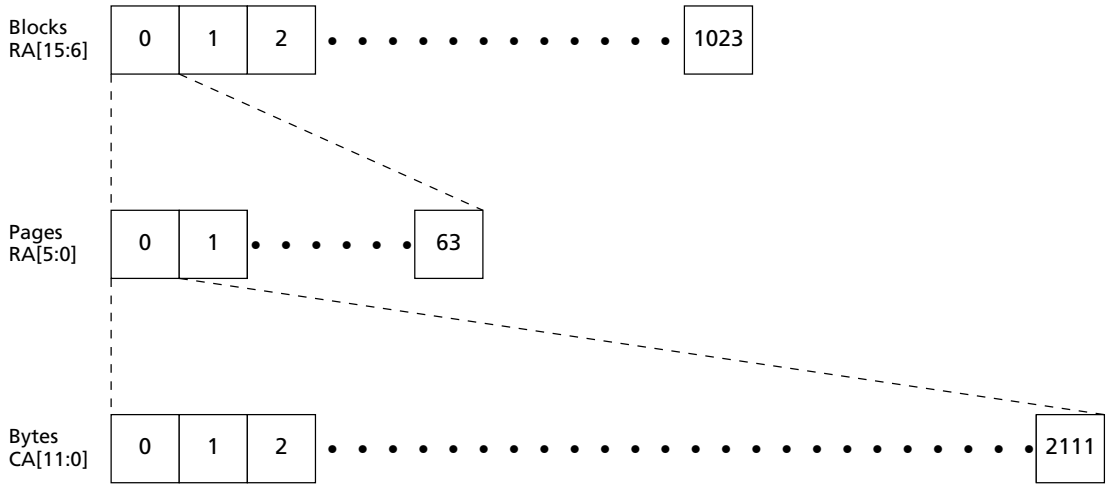
Table 2: SPI Ball Descriptions

Symbol	Type	Description
CS#	Input	**Chip select:** Places the device in active power mode when driven LOW. Deselects the device and places SO at High-Z when HIGH. After power-up, the device requires a falling edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. Single command and address sequences and array-based operations are registered on CS#.
SCK	Input	**Serial clock:** Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK.
HOLD#/SO3	I/O	**Hold:** Pauses any serial communication with the device without deselecting it. When driven LOW, SO is at High-Z, and all inputs at SI and SCK are ignored. Requires that CS# also be driven LOW. HOLD# must not be driven by the host during x4 read operations.
SI/SO0	I/O	**Serial data input:** Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. SI must not be driven by the host during x2 or x4 read operations.
WP#/SO2	I/O	**Write protect:** When LOW, prevents overwriting block-lock bits if the block register write disable (BRWD) bit is set. WP# must not be driven by the host during x4 read operations.
SO/SO1	Output	**Serial data output:** Transfers data serially out of the device on the falling edge of SCK.
V_{CC}	Supply	**V_{CC}:** Supply voltage
V_{SS}	Supply	**V_{SS}:** Ground
DNU	–	**Do not use:** DNUs must be left unconnected.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Memory Mapping

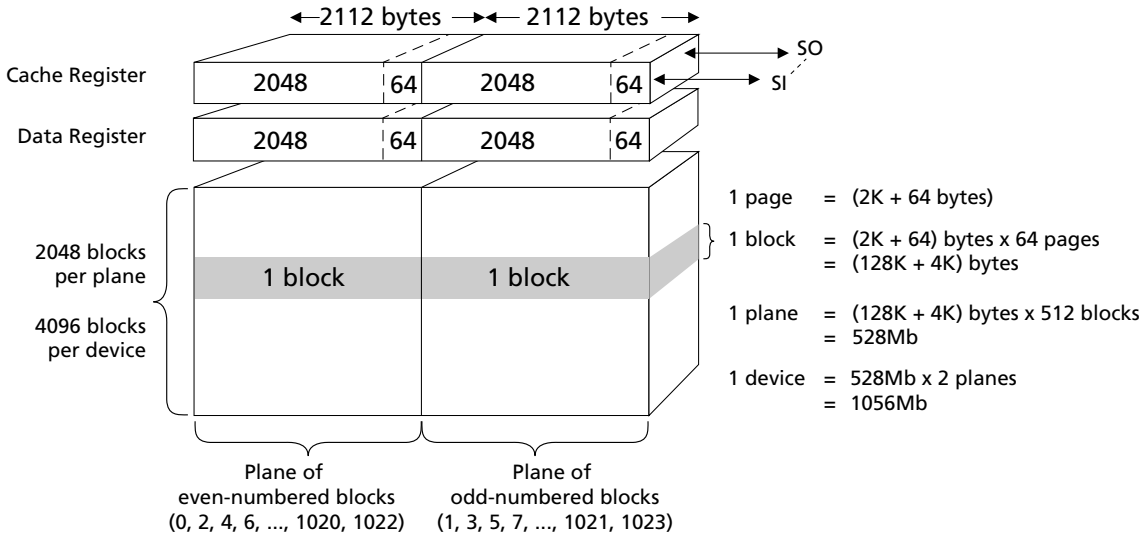
Figure 4: Memory Map



Notes:
1. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are "out of bounds," do not exist in the device, and cannot be addressed.
2. BA6 controls plane selection.

Array Organization

Figure 5: Array Organization



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Bus Operation

SPI Modes

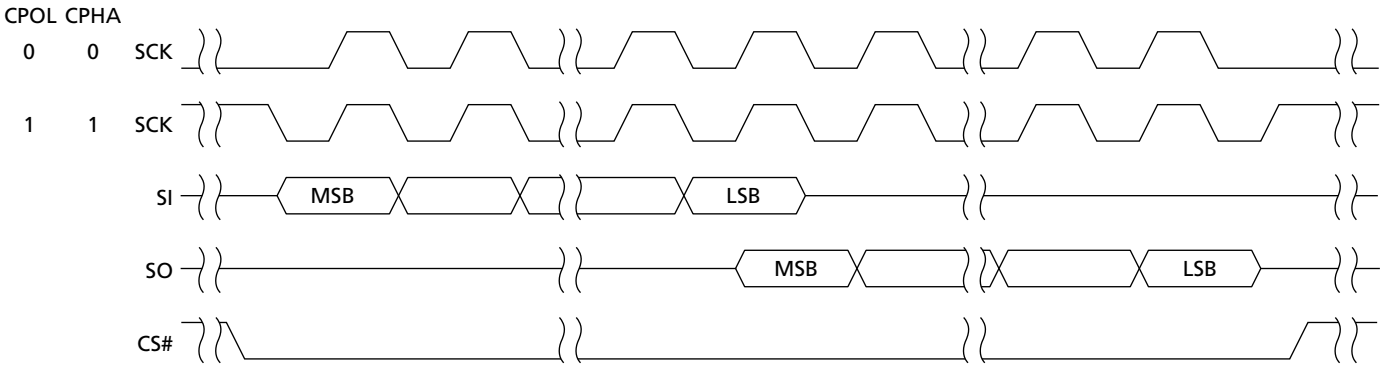
SPI NAND supports two SPI modes:
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode:
- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

All timing diagrams shown in this data sheet are mode 0.

Figure 6: SPI Modes Timing



Note: 1. While CS# is HIGH, keep SCK at V_{CC} or GND (determined by mode 0 or mode 3). Do not begin toggling SCK until after CS# is driven LOW.

CS#

Chip select (CS#) activates or deactivates the device. When CS goes LOW, the device is placed in active mode. When CS is HIGH, the device is placed in inactive mode and SO is High-Z.

SCK

Serial clock (SCK) provides interface timing for SPI NAND. Addresses, data, and commands are latched on the rising edge of SCK. Data is placed on SO at the falling edge of SCK. When CS# is HIGH, SCK must return either HIGH or LOW.

HOLD#/SO3

HOLD# input provides a method to pause serial communication with the device but does not terminate any ERASE, READ, or WRITE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCK.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK.

During hold mode, SO is High-Z, and SI and SCK inputs are ignored.

SO3 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK. During this time the host must wait until the READ FROM CACHE x4 command is complete before driving HOLD#.

SI/SO0

Writes use serial data in (SI). Data, commands, and addresses are transferred on SI in x1 mode at the rising edge of SCK. SI must not be driven by the host during x2 or x4 read operations.

SO0 operation is enabled by issuing a READ FROM CACHE x2 or x4 command with data being clocked out of the device at the falling edge of SCK. During this time the host must wait until the READ FROM CACHE x2 or x4 command is complete before driving SI.

WP#/SO2

Write protect (WP#) prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered. WP# must not be driven by the host during READ FROM CACHE x4 operations.

SO2 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK. During this time the host must wait until the READ FROM CACHE x4 command is complete before driving WP#.

SO/SO1

Reads use serial data out (SO). Device reads are performed in x1, or x2, or x4 modes. SO acts as the only output in x1 READ operations, and as SO1 in x2 and x4 read operations.

Data is clocked out of the device on SO at the falling edge of SCK control signals.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

SPI NAND Command Definitions

Table 3: SPI NAND Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
BLOCK ERASE	D8h	3	0	0	Block erase
GET FEATURE	0Fh	1	0	1	Get features
PAGE READ	13h	3	0	0	Array read
PROGRAM EXECUTE	10h	3	0	0	Enter block/page address, no data, execute
PROGRAM LOAD RANDOM DATA	02h	2	0	1 to 2112	Load program data—2kB MAX
PROGRAM LOAD	84h	2	0	1 to 2112	Enter cache address/data
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112	Output cache data at addr
READ FROM CACHE x2	3Bh	2	1	1 to 2112	Output cache data on SI and SO
READ FROM CACHE x4	6Bh	2	1	1 to 2112	Output cache data on SI, SO, WP#, HOLD#
READ ID	9Fh	0	1	2	Read device ID
RESET	FFh	0	0	0	Reset the device
SET FEATURE	1Fh	1	0	1	Set features
WRITE DISABLE	04h	0	0	0	
WRITE ENABLE	06h	0	0	0	

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

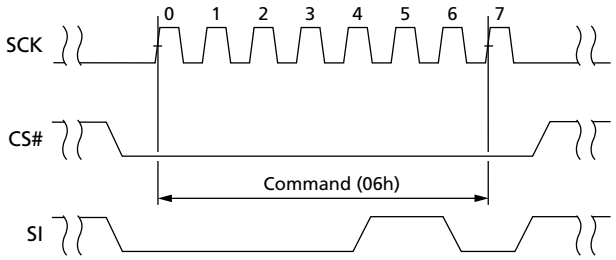
WRITE Operations

WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. WRITE ENABLE is required in the following operations that change the contents of the memory array:

- Page program
- OTP program
- BLOCK ERASE

Figure 7: WRITE ENABLE (06h) Timing

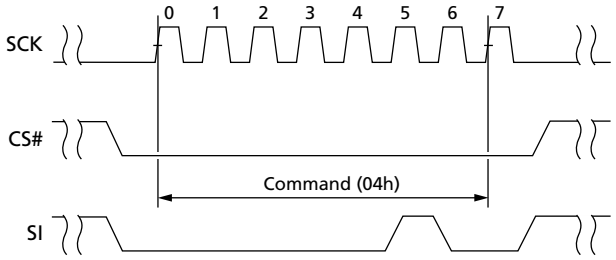


WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0. This disables the following operations:

- Page program
- OTP program
- BLOCK ERASE

Figure 8: WRITE DISABLE (04h) Timing



Features Operations

GET FEATURES (0Fh) and SET FEATURES (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 4: Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block lock	A0h	BRWD[1]	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	ECC Enable	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	ECC Status	ECC Status	P_Fail	E_Fail	WEL	OIP

Note: 1. If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 9: GET FEATURES (0Fh) Timing

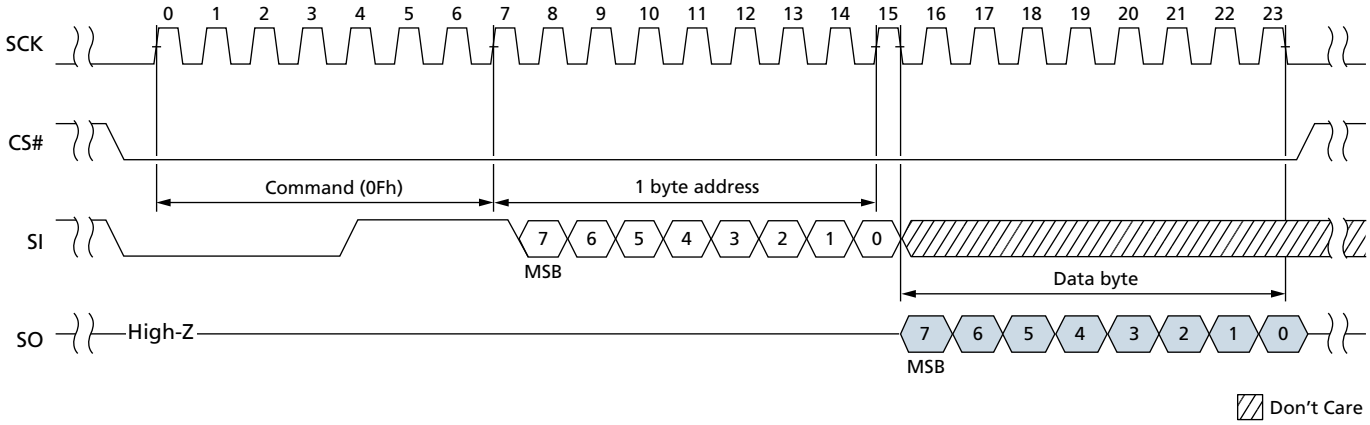
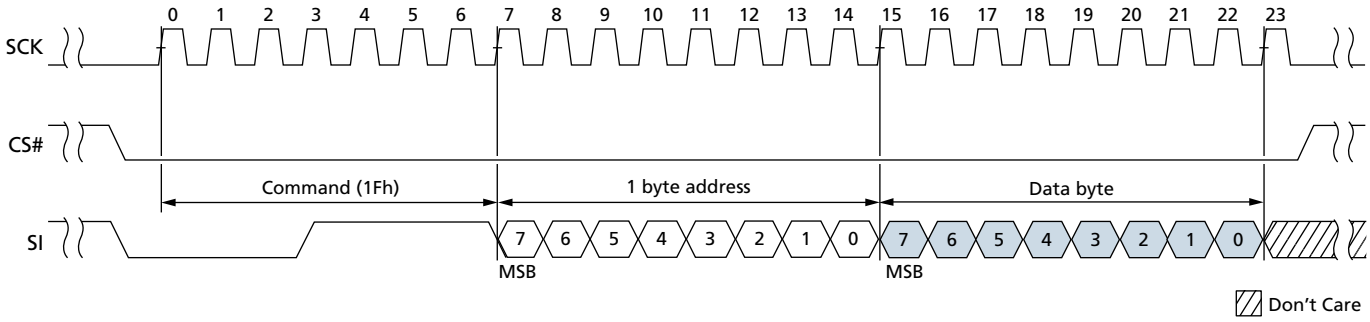


Figure 10: SET FEATURES (1Fh) Timing



READ Operations

PAGE READ (13h)

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

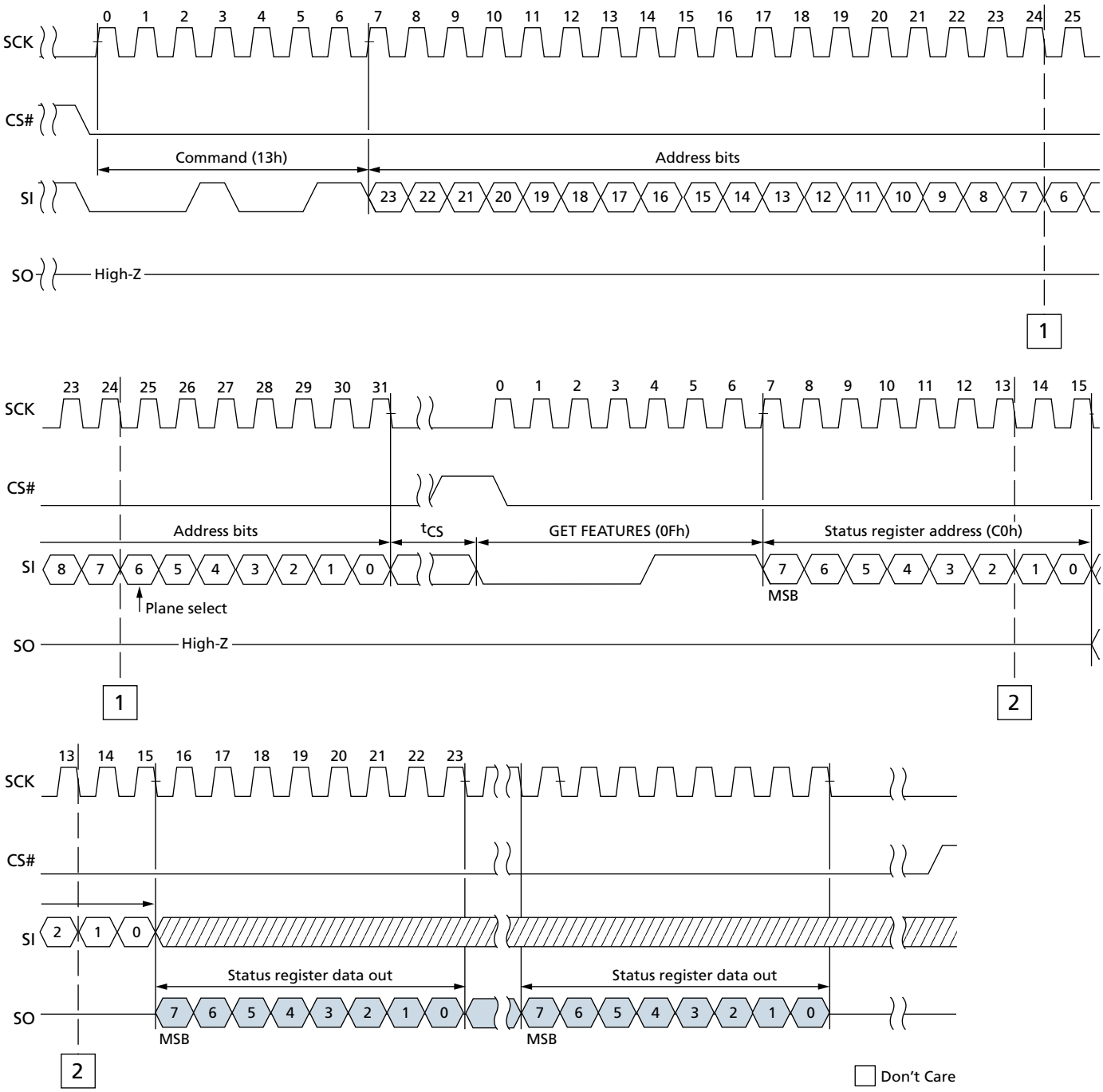
- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status)
- 0Bh or 03h (Random data read)

The PAGE READ command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for ^{t}RD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation. Following a status of successful completion, the RANDOM DATA READ (03h or 0Bh) command must be issued in order to read the data out of the cache. The RANDOM DATA READ command requires 3 dummy bits, followed by a plane select and a 12-bit column address for the starting byte address. The starting byte address can be 0 to 2111, but after the end of the cache register is reached, the data does

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

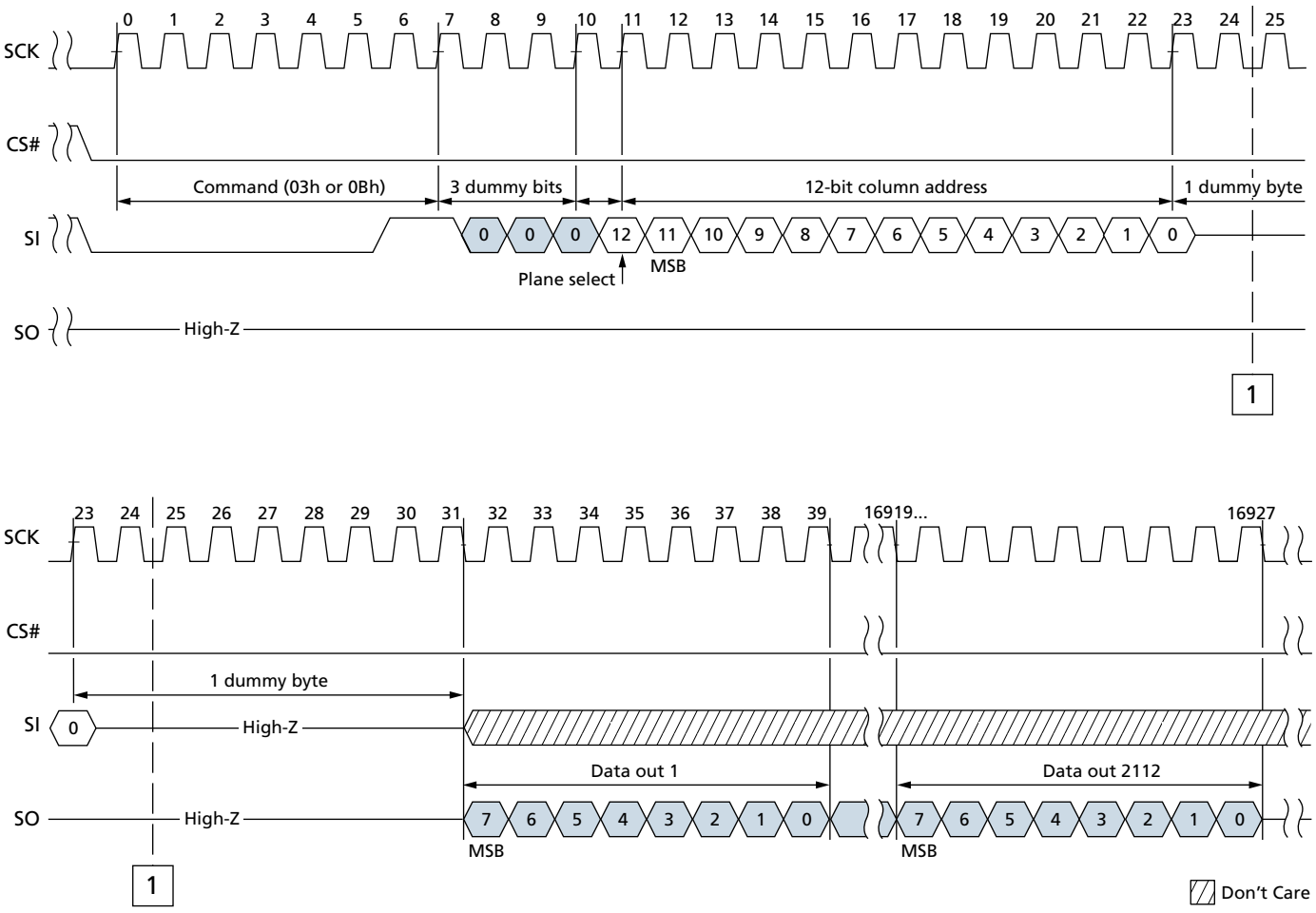
not wrap around and SO goes to a High-Z state. Refer to Figure 11 (page 17) and Figure 12 (page 18) to view the entire READ operation.

Figure 11: PAGE READ (13h) Timing x1



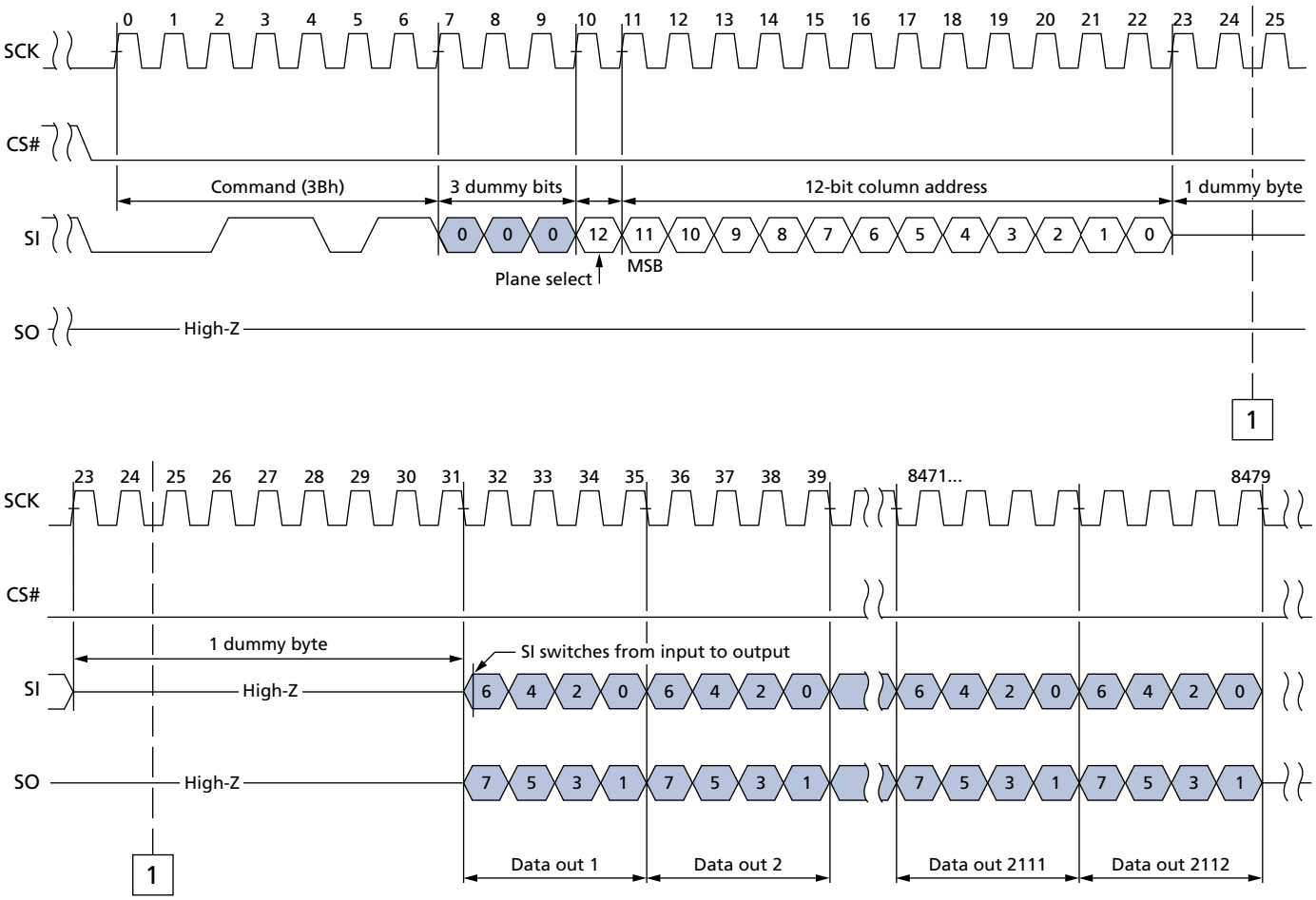
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 12: RANDOM DATA READ (03h or 0Bh) Timing



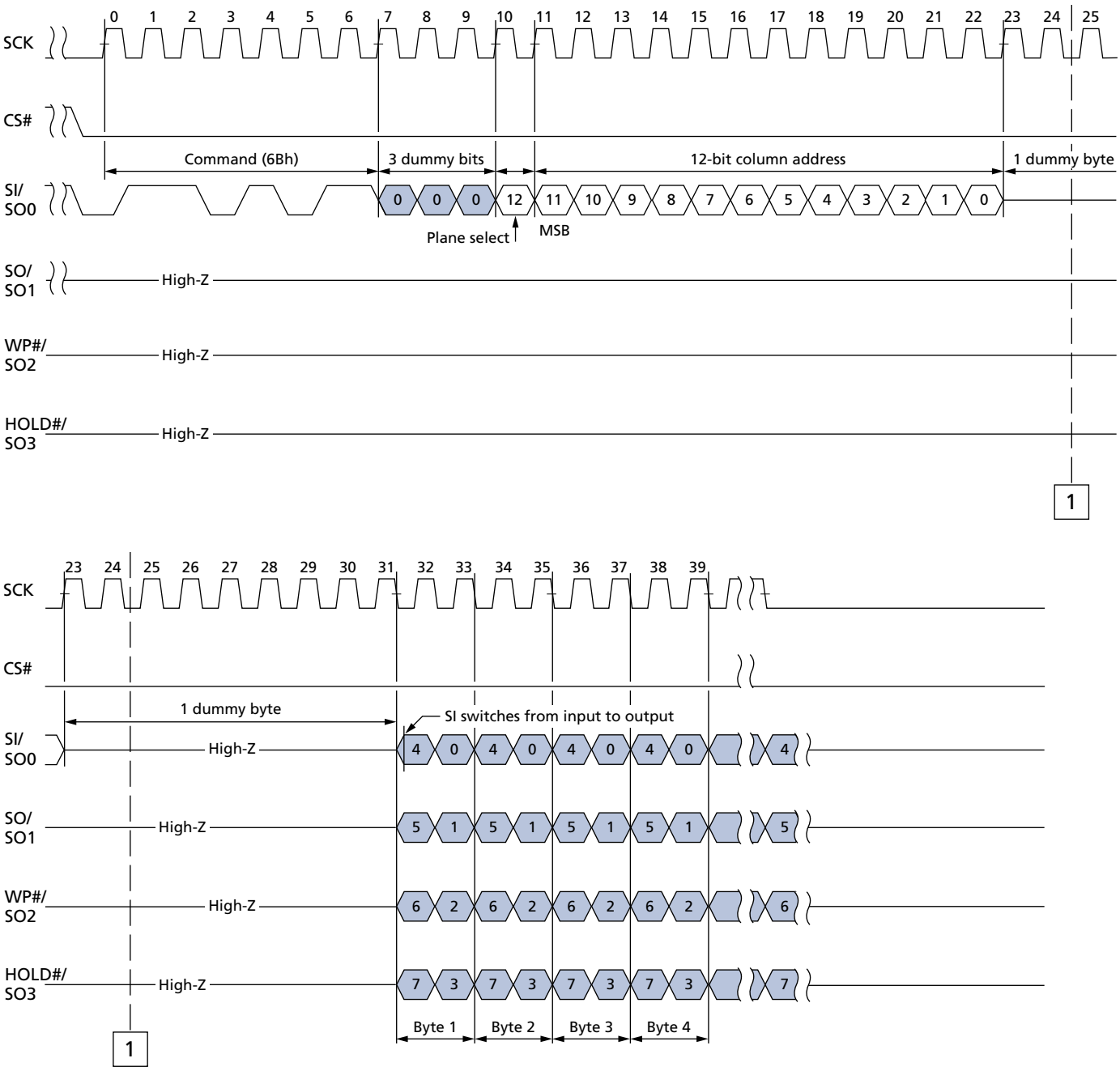
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 13: READ FROM CACHE x2



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 14: READ FROM CACHE x 4



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

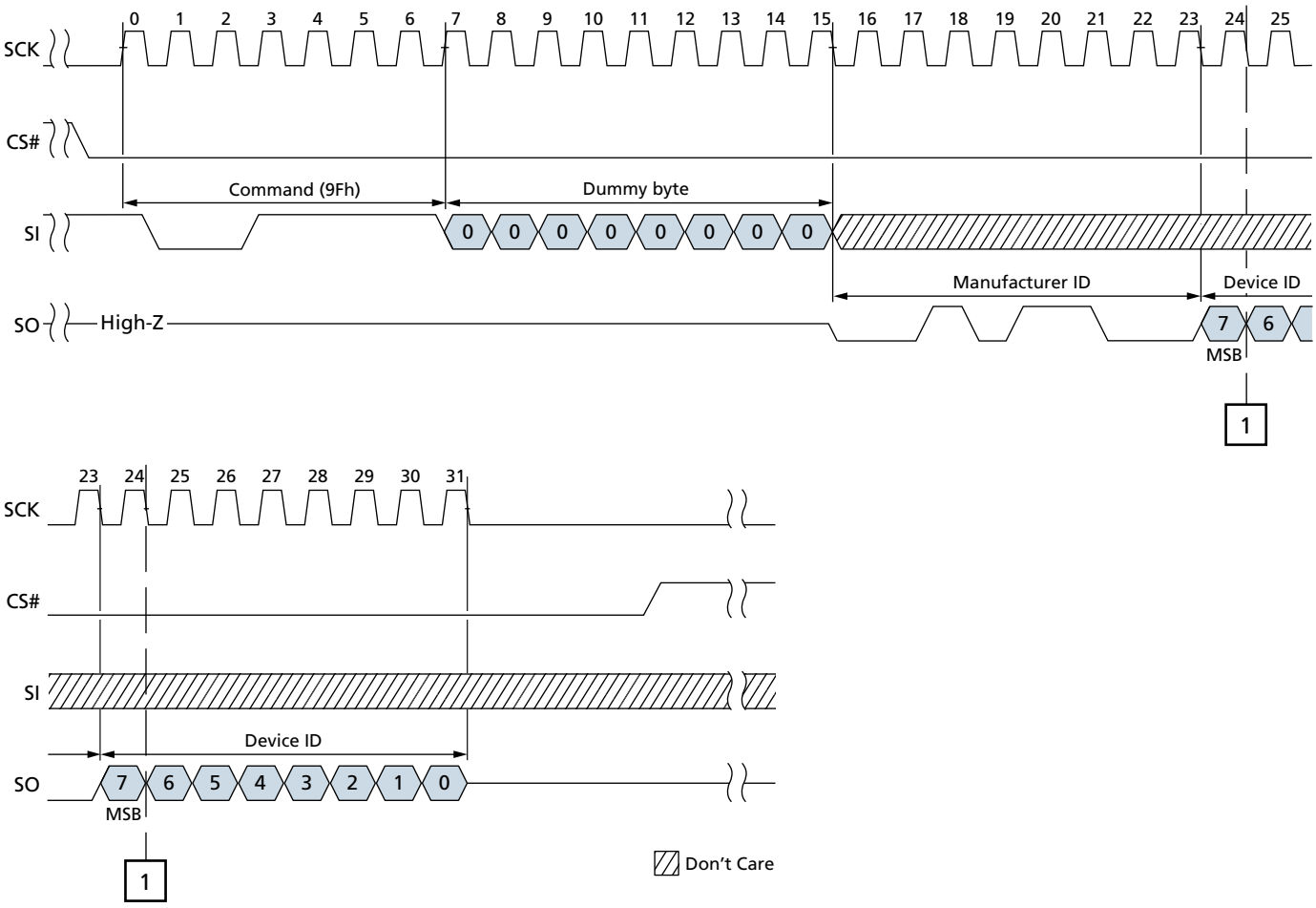
READ ID (9Fh)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the device configuration.

Table 5: READ ID Table

Byte	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Micron)	0	0	1	0	1	1	0	0	2Ch
Byte 1	Device ID (SPI)	0	0	0	1	0	0	1	0	12h

Figure 15: READ ID (9Fh) Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Parameter Page

The following command flow must be issued by the memory controller to access the parameter page contained within Micron SPI devices:

1. Issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 40h (OTP enable, ECC disable).
2. Issue a PAGE READ (13h) command with a block/page address of 0x01h, and then check the status of the read completion using the GET FEATURES (0Fh) command with a feature address of C0h.
3. Issue a READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device (see the following Parameter Page Data Structure table for a description of the contents of the parameter page.)
4. To exit reading the parameter page, issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 10h (main array READ, ECC enable).

UniqueID Page

The following command flow must be issued by the memory controller to access the uniqueID page contained within Micron SPI devices:

1. Issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 40h (OTP enable, ECC disable).
2. Issue a PAGE READ (13h) command with a block/page address of 0x00h, and then check the status of the read completion using the GET FEATURES (0Fh) command with a feature address of C0h.
3. Issue a READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device. (The contents of the uniqueID page are described in the following note.)

   Note: The device stores 16 copies of the unique ID data. Each copy is 32 bytes; the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data.
4. To exit reading the uniqueID page, issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 10h (main array READ, ECC enable).

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Parameter Page Data Structure Table

Table 6: Parameter Page Data Structure

Byte	Description		Value[1]
0–3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4–5	Revision number		00h, 00h (n/a)
6–7	Features supported	MT29F1G01AAADDH4	00h, 00h (n/a)
8–9	Optional commands supported		06h, 00h
10–31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32–43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model	MT29F1G01AAADDH4	4Dh, 54h, 32h, 39h, 46h, 31h, 47h, 30h, 31h, 41h, 41h, 41h, 44h, 44h, 48h, 34h, 20h, 20h, 20h, 20h
64	Manufacturer ID		2Ch
65–66	Date code		00h, 00h
67–79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80–83	Number of data bytes per page		00h, 08h, 00h, 00h
84–85	Number of spare bytes per page		40h, 00h
86–89	Number of data bytes per partial page		00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page		10h, 00h
92–95	Number of pages per block		40h, 00h, 00h, 00h
96–99	Number of blocks per unit		00h, 04h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		00h (n/a)
102	Number of bits per cell		01h
103–104	Bad blocks maximum per unit		14h, 00h
105–106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		00h (n/a)
108–109	Block endurance for guaranteed valid blocks		00h (n/a)
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of ECC bits		00h
113	Number of interleaved address bits		00h (n/a)
114	Interleaved operation attributes		00h (n/a)
115–127	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance	MT29F1G01AAADDH4	0Ah
129–130	Timing mode support		00h, 00h (n/a)
131–132	Program cache timing		00h, 00h (n/a)
133–134	^{t}PROG maximum page program time		84h, 03h
135–136	^{t}BERS maximum block erase time		10h, 27h

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Table 6: Parameter Page Data Structure (Continued)

Byte	Description	Value[1]
137–138	^{t}R maximum page read time	64h, 00h
139–140	^{t}CCS minimum	00h, 00h (n/a)
141–163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164–165	Vendor-specific revision number	01h, 00h (n/a)
166–253	Vendor specific	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 02h, 02h, B0h, 0Ah, B0h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 01h
254–255	Integrity CRC	Set at test
256–511	Value of bytes 0–255	
512–767	Value of bytes 0–255	
768+	Additional redundant parameter pages	

Note: 1. h = hexadecimal.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Program Operations

PAGE PROGRAM

The PAGE PROGRAM operation sequence programs 1 byte to 2112 bytes of data within a page. The page program sequence is as follows:

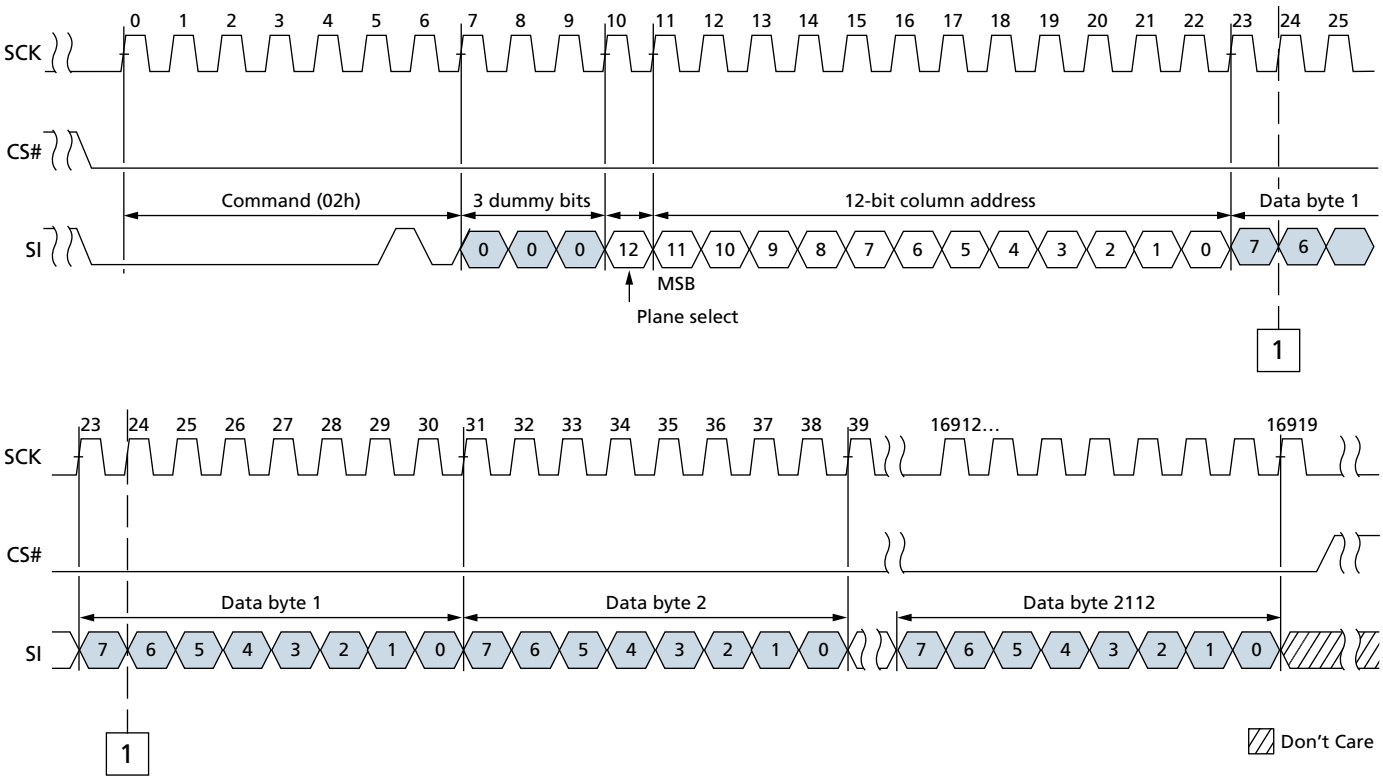
- 06h (WRITE ENABLE
- 02h (PROGRAM LOAD)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored. WRITE ENABLE must be followed by a PROGRAM LOAD (02h) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 3 dummy bits, a plane select and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2112 bytes long. Only four partial-page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS goes from LOW to HIGH. Figure 16 shows the PROGRAM LOAD operation.

After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for ^{t}PROG time. This operation is shown in Figure 17. During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

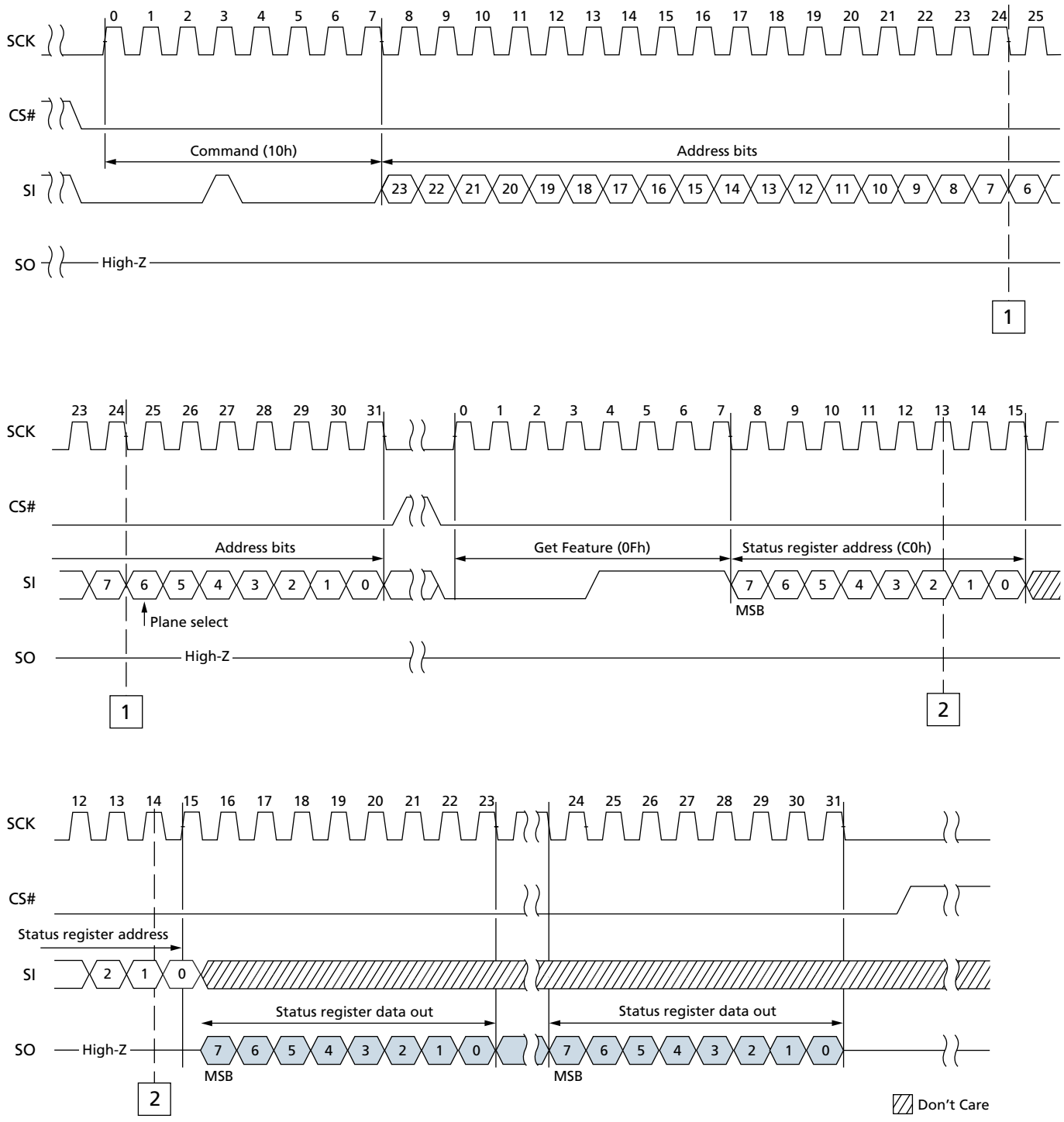
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 16: PROGRAM LOAD (02h) Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 17: PROGRAM EXECUTE (10h) Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

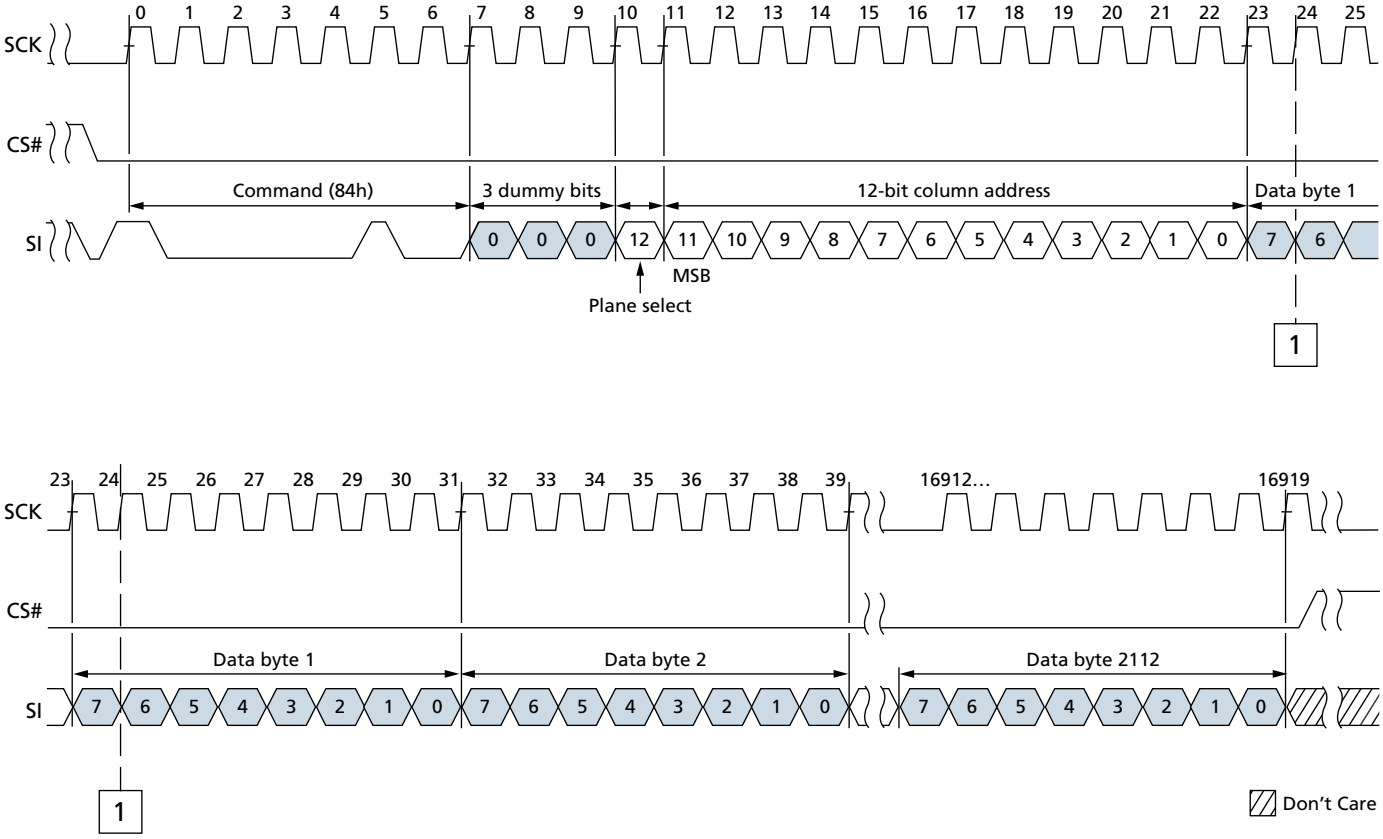
RANDOM DATA PROGRAM

The RANDOM DATA PROGRAM sequence programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE
- 84h (PROGRAM LOAD RANDOM DATA)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing a PROGRAM LOAD RANDOM DATA operation, a WRITE ENABLE (06h) command must be issued to change the contents of the memory array. Following a WRITE ENABLE (06) command, a PROGRAM LOAD RANDOM DATA (84h) command must be issued. This command consists of an 8-bit Op code, followed by 3 dummy bits, a plane select bit, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Figure 18: PROGRAM LOAD RANDOM DATA (84h) Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

INTERNAL DATA MOVE

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:
- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE
- 84h (PROGRAM LOAD RANDOM DATA)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command (see Figure 11). The PAGE READ command must be followed with a WRITE ENABLE (06h) command in order to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h) command can be issued. This command consists of an 8-bit Op code, followed by 3 dummy bits, a plane select, and a 12-bit column address. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h) command must be issued with the new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

INTERNAL DATA MOVE is not supported across internal planes.

Block Operations

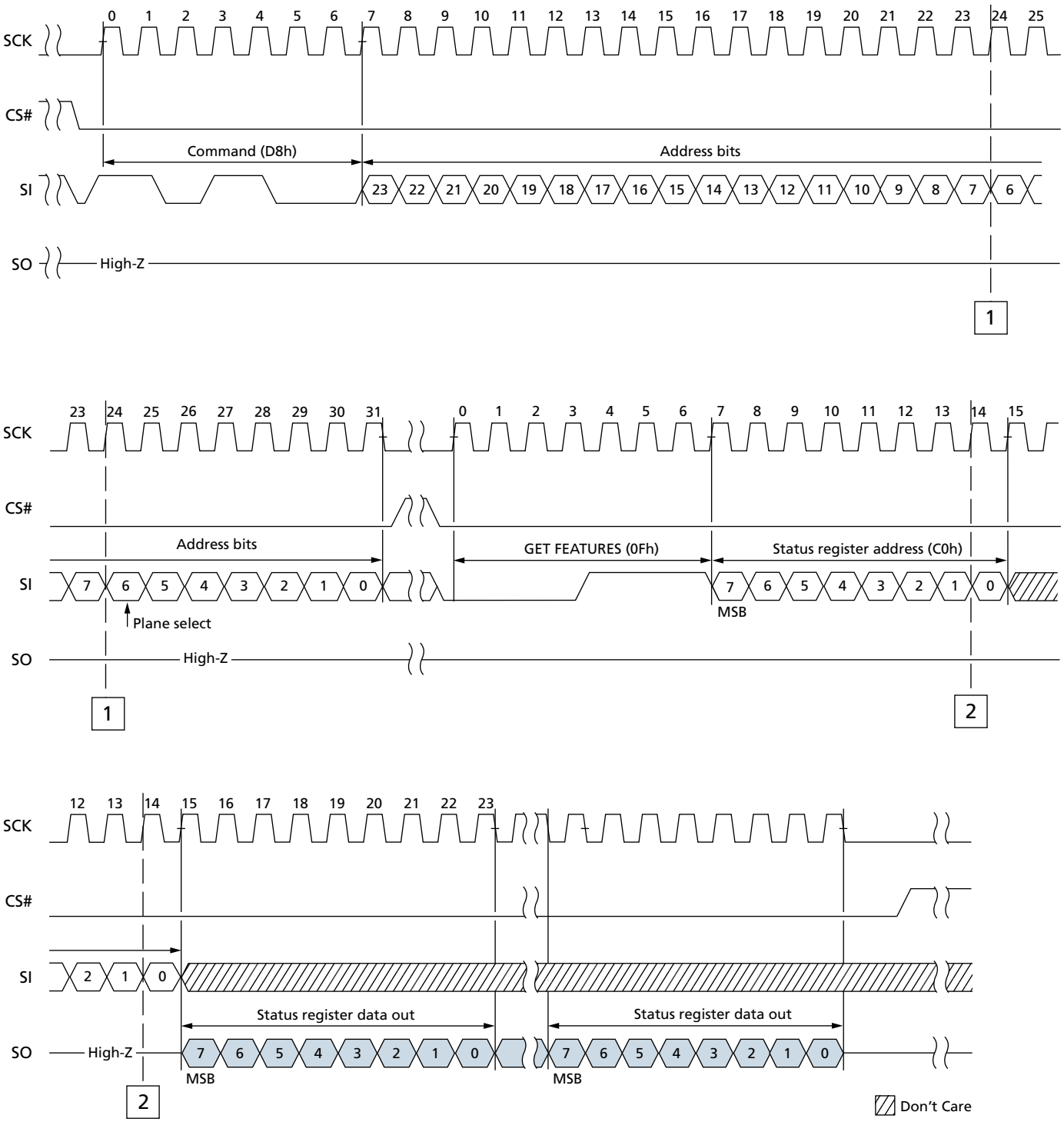
BLOCK ERASE (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2112 bytes per page (2048 + 64 bytes). Each block is 132 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:
- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 8 dummy bits followed by an 16-bit row address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation (see Figure 19).

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 19: BLOCK ERASE (D8h) Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Block Lock Feature

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the "locked" state, i.e., bits 3, 4, and 5 of the block lock register are set to 1. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued with the A0h feature address, including the data bits shown in Table 6. The operation for the SET FEATURES command is shown in Figure 10 on page 15. When BRWD is set and WP is LOW, none of the writable bits (3, 4, 5, and 7) in the block lock register can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, a status of 00h is returned. When an ERASE command is issued to a locked block, the erase failure, 04h, is returned. When a PROGRAM command is issued to a locked block, program failure, 08h, is returned.

Table 7: Block Lock Register Block Protect Bits

BP2	BP1	BP0	Protected Rows
0	0	0	None—all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

For example, if all the blocks need to be unlocked after power-up, the following sequence should be performed:

- Issue SET FEATURES register write (1Fh)
- Issue the feature address to unlock the block (A0h)
- Issue 00h on data bits to unlock all blocks

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

One-Time Programmable (OTP) Feature

The serial device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2112 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want; typical uses include programming serial numbers, or other data, for permanent storage. To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 02h–0Bh can be programmed in sequential order. The PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands can be used to program the pages. Also, the PAGE READ (13h) command can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

OTP Access

To access OTP, perform the following command sequence:
- Issue the SET FEATURES register write (1Fh)
- Issue the OTP feature address (B0h)
- Issue the PAGE PROGRAM or PAGE READ command

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see the following table.

Table 8: OTP States

OTP Protect Bit	OTP Enable Bit	State
0	0	Normal operation
0	1	Access OTP space
1	0	Not applicable
1	1	Use PROGRAM EXECUTE (10h) to lock OTP

Note: 1. The OTP space cannot be erased and after it has been protected, it cannot be programmed again.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Status Register

The NAND Flash device has an 8-bit status register that software can read during the device operation. The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address C0h (see Figure 9 (page 16)).

The status register will output the status of the operation. The description of data bits from status register are shown in the following table.

Table 9: Status Register Bit Descriptions

Bit	Bit Name	Description
P_Fail	Program fail	This bit indicates that a program failure has occurred (P_Fail set to 1). This bit will also be set if the user attempts to program an invalid address or a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_Fail = 0).
E_Fail	Erase fail	This bit indicates that an erase failure has occurred (E_Fail set to 1). This bit will also be set if the user attempts to erase a locked region, or if the ERASE operation fails. This bit is cleared (E_Fail = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write enable latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation in progress	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing; the device is busy. When the bit is 0, the interface is in the ready state.
ECC_Status	N/A	ECC_Status provides ECC status as follows: 00b = No bit errors were detected during the previous read algorithm. 01b = A bit error was detected and corrected. 10b = Multiple bit errors were detected and not corrected. 11b = Reserved ECC_Status is set to 00b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC_Status is invalid if ECC is disabled (via a SET FEATURES command to the OTP feature address). After power-up RESET, ECC status is set to reflect the contents of block 0, page 0.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (N_{VB}) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 10: Error Management Details

Description	Requirement
Minimum number of valid blocks (N_{VB})	1004
Total available blocks per die	1024
First spare area location	Byte 2048
Bad-block mark	00h

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

ECC Protection

The serial device offers data corruption protection by offering 4-bit internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting the ECC bit in the OTP register. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state.

To enable/disable ECC, perform the following command sequence:
- Issue the SET FEATURES register write (1Fh).
- Issue the OTP feature address (B0h).
- Then:
  - To enable ECC Set Bit 4, ECC Enable, to 1.
  - To disable ECC Clear Bit 4, ECC Enable, to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a 1- to 4-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:
- Spare area definitions provided in the ECC Protection table below.
- WRITEs to ECC are supported for main and spare areas 0, and 1. WRITEs to the ECC area are prohibited (see the ECC Protection table below).
- When using partial-page programming, the following conditions must both be met:
  - In the main user area and in user meta data area I, single partial-page programming operations must be used (see the ECC Protection table below).
  - Within a page, the user can perform a maximum of four partial-page programming operations.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Table 11: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
801h	800h	No		Reserved (bad block data)
803h	802h	No		User meta data II
807h	804h	Yes	Spare 0	User meta data I
80Fh	808h	Yes	Spare 0	ECC for main/spare 0
811h	810h	No		Reserved
813h	812h	No		User meta data II
817h	814h	Yes	Spare 1	User meta data I
81Fh	818h	Yes	Spare 1	ECC for main/spare 1
821h	820h	No		Reserved
823h	822h	No		User meta data II
827h	824h	Yes	Spare 2	User meta data I
82Fh	828h	Yes	Spare 2	ECC for main/spare 2
831h	830h	No		Reserved
833h	832h	No		User meta data II
837h	834h	Yes	Spare 3	User meta data I
83Fh	838h	Yes	Spare 3	ECC for main/spare 3

Table 12: ECC Status

Bit 1	Bit 0	Description
0	0	No errors
0	1	1- to 4-bit error detected and corrected
1	0	Bit errors greater than four bits detected and not corrected
1	1	Reserved

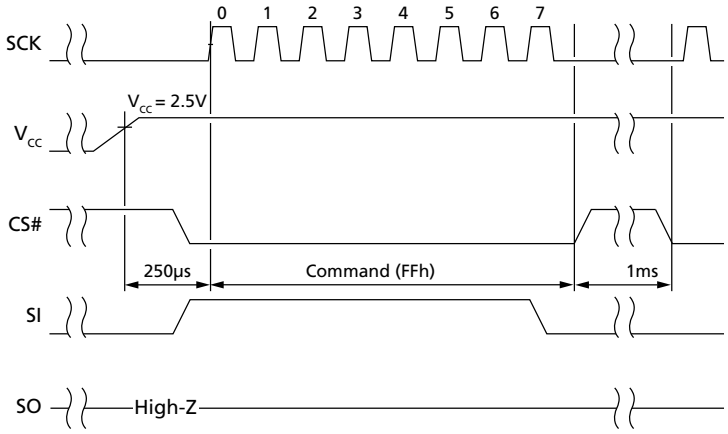
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Power-Up

SPI Power-Up

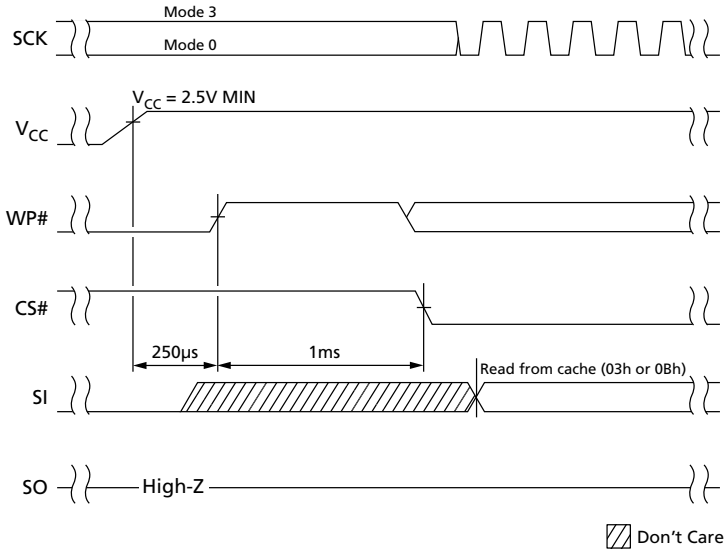
Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored and when V_{CC} reaches 2.5V, a minimum of 250µs must elapse before issuing a RESET (FFh) command. After issuing the RESET command, 1ms must elapse before issuing any other command (see Figure 20).

Figure 20: SPI Power-Up Timing



Micron has developed an alternative SPI NAND sequence that does not require issuing an explicit RESET (FFh) command upon power-up. When WP# is taken HIGH 250µs after V_{CC} has reached 2.5V, the device automatically performs the RESET command. The first access to the SPI NAND device can occur 1ms after WP# goes HIGH, and then CS# can be driven LOW, SCK can start, and the required command can be issued to the SPI NAND device (see Figure 21).

Figure 21: Alternative SPI Power-Up Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 13: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage (SPI)	V_{CC}	2.7	3.6	V
Operating temperature (ambient)	T_A	–40	85	°C
Junction temperature[1]	T_J	–	110	°C
Storage temperature	T_S	–40	125	°C

Note: 1. T_J is calculated based on $T_J = R_{th} \times P + T_A$ with R_{th} = 180K/W.

Table 14: SPI Mode Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (SPI)	V_{CC}	2.7	3	3.6	V
Supply current (READ/PROGRAM/ERASE, MAX ROOT MEAN SQUARE)	I_{CC}	–	25	35	mA
Standby	I_{SB}	–	10	50	mA

Table 15: DC Characteristics

Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH},	0.7 × V_{CC}	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	- 0.3	0.2 × V_{CC}	V	
Output high voltage	V_{OH},	0.7 × V_{CC}	V_{CC} + 0.3	V	I_{OH} = –20µA
Output low voltage	V_{OL}	–	0.15 × V_{CC}	V	I_{OL} = –1mA
Input leakage current	I_{LI}	–	±10	µA	
Output leakage current	I_{LO}	–	±10	µA	

Table 16: General Timing Characteristics (SPI)

Parameter	Symbol	Min	Max	Units
Clock frequency	^{f}C	–	50	MHz
Hold# non-active hold time relative to SCK	^{t}CD	5	–	ns
HOLD# holding time relative to SCK	^{t}CH	5	–	ns
Command deselect time	^{t}CS	100	–	ns
Chip select# hold time	^{t}CSH	5	–	ns

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Table 16: General Timing Characteristics (SPI) (Continued)

Parameter	Symbol	Min	Max	Units
Chip select# setup time	^{t}CSS	5	–	ns
Output disable time	^{t}DIS	–	20	ns
Hold# non-active setup time relative to SCK	^{t}HC	5	–	ns
Hold# setup time relative to SCK	^{t}HD	5	–	ns
Data input hold time	^{t}HDDAT	5	–	ns
Output hold time	^{t}HO	0	–	ns
Hold to output High-Z	^{t}HZ	–	15	ns
Hold# to output Low-Z	^{t}LZ	–	15	ns
Rise/fall time	^{t}R, ^{t}F	–	2	ns
Data input setup time	^{t}SUDAT	5	–	ns
Clock LOW to output valid	^{t}V	–	15	ns
Clock HIGH time	^{t}WH	8	–	ns
Clock LOW time	^{t}WL	8	–	ns
WP# hold time	^{t}WPH	100	–	ns
WP# setup time	^{t}WPS	20	–	ns

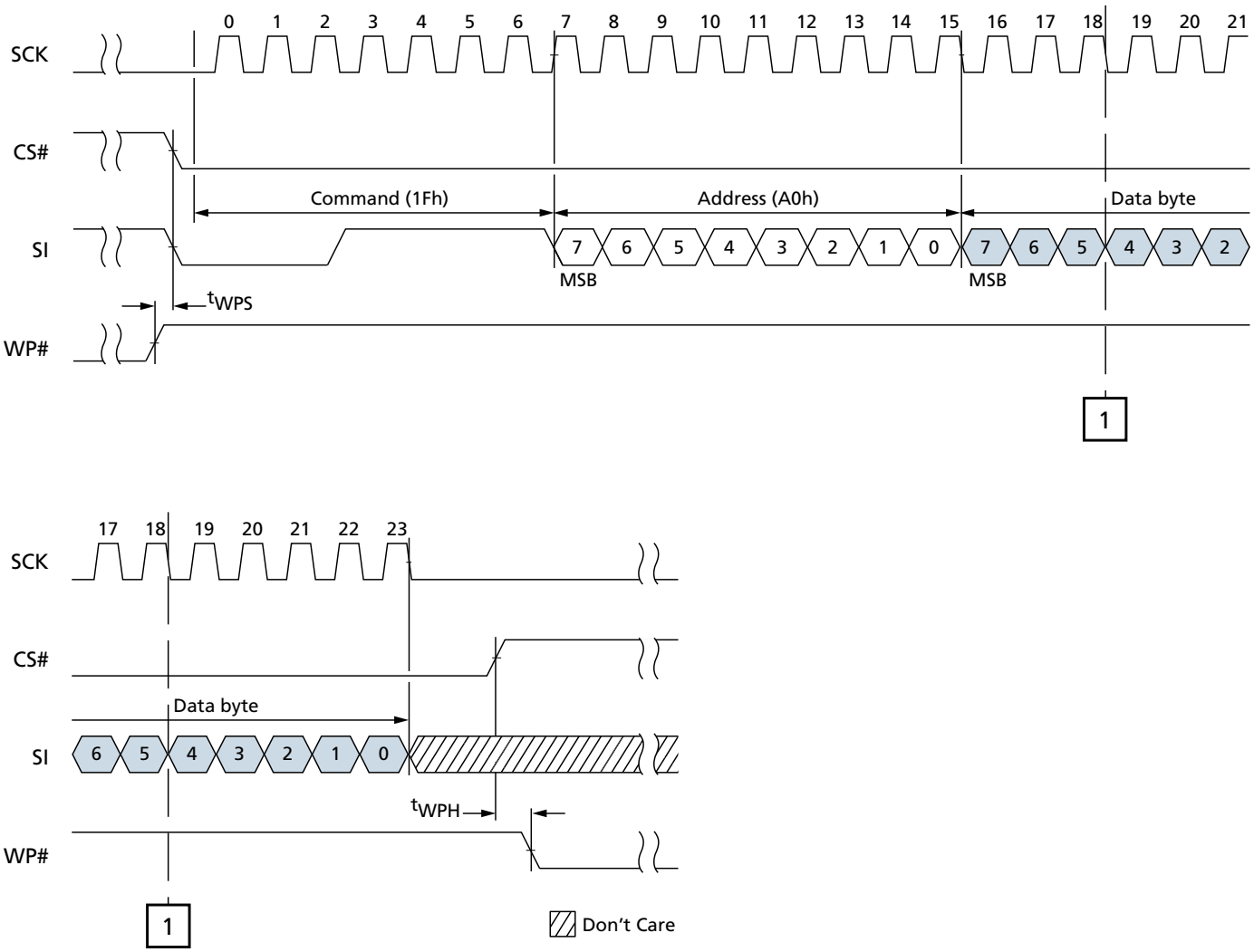
Table 17: PROGRAM/READ/ERASE Timing Characteristics (SPI)

Parameter	Typ	Max	Description
NOP	–	4[1]	Number of partial-page programming operations supported.
^{t}ERS	4ms	10ms[2]	BLOCK ERASE operation time.
^{t}PROG	400µs	900µs	PROGRAM PAGE operation time (ECC enabled).
^{t}RD	–	100µs	Data transfer time from NAND Flash array to data register with internal ECC enabled.
^{t}RST (RD/PGM/ERS)	–	5µs/10µs/500µs[2]	Resetting time for READ, PROGRAM, and ERASE operations.

Notes:
1. Four total partial-page programs to the same page. If ECC is enabled, the device is limited to one partial-page program per ECC user area, not exceeding four partial-page programs per page.
2. 100,000 cycles.
3. For first RESET condition after power up, tRST will be 1ms maximum.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 22: WP# Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Figure 23: Serial Input Timing

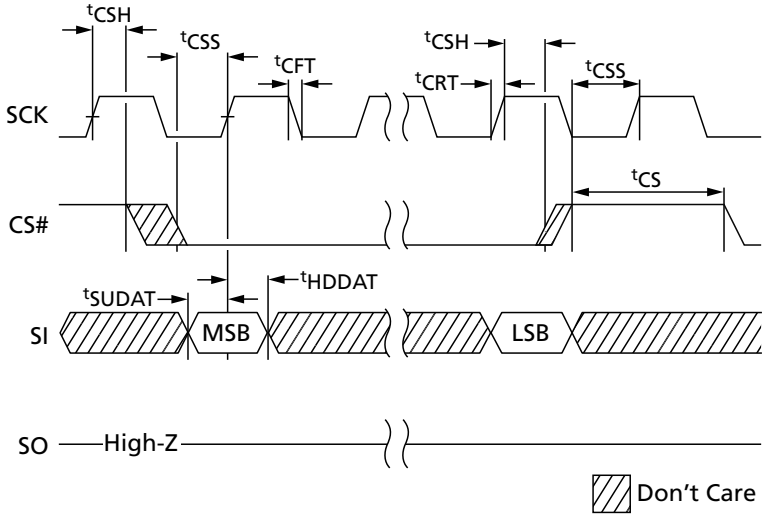


Figure 24: Serial Output Timing

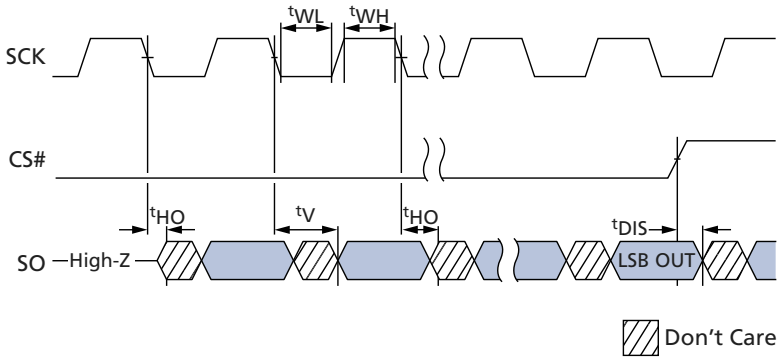
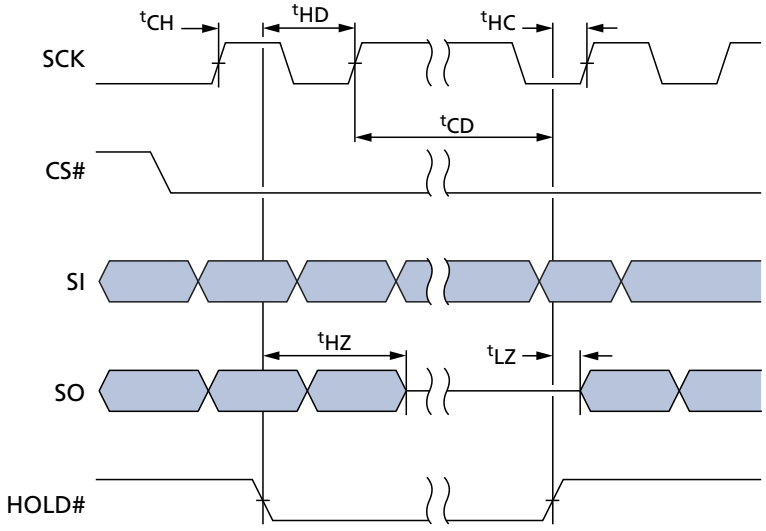


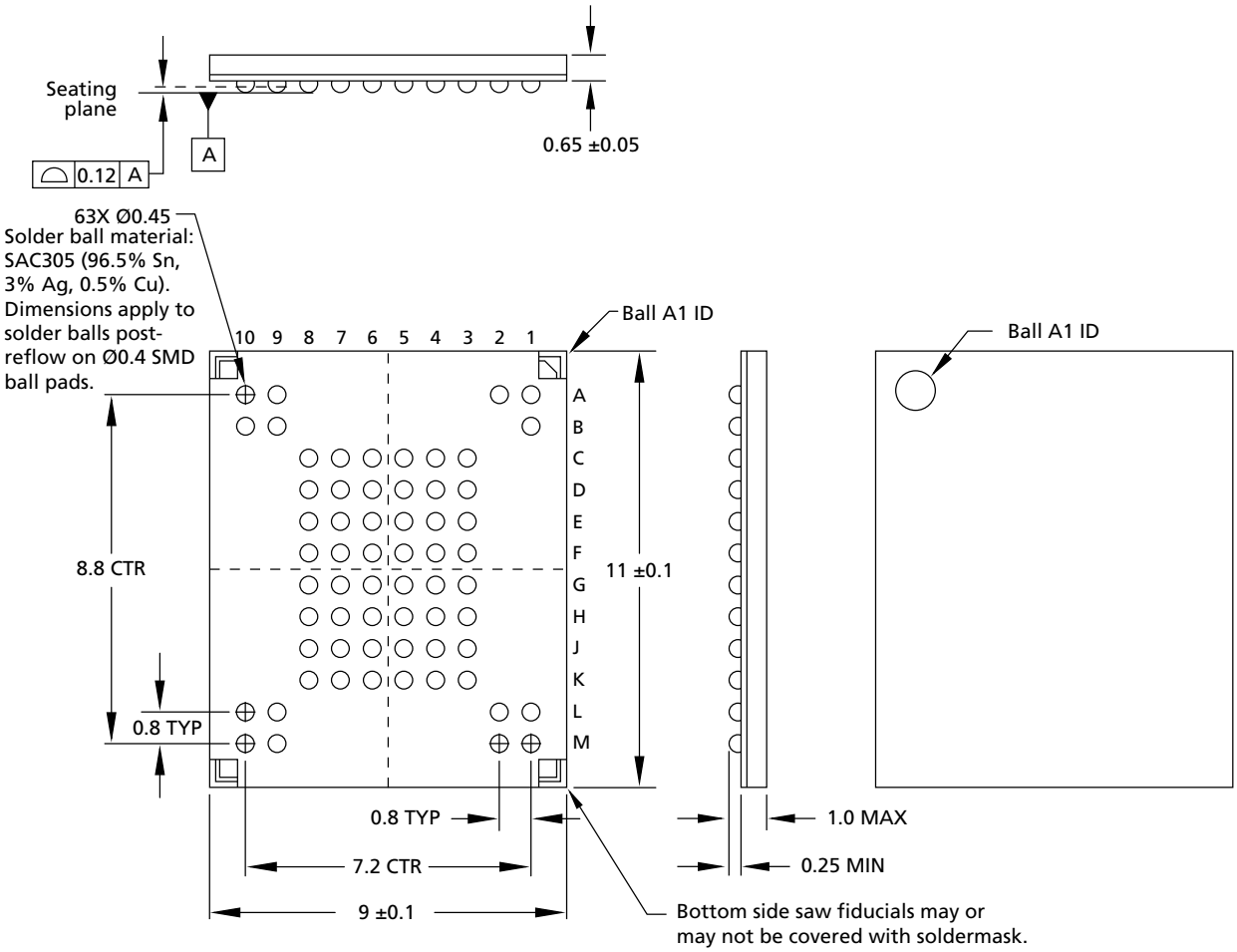
Figure 25: Hold# Timing



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Package Dimensions

Figure 26: 63-Ball VFBGA, Package Code H4



Note: 1. All dimensions are in millimeters.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.

Revision History

Rev. B, Advance – 2/11

- Added Parameter Page Data Structure Table

Rev. A, Advance – 7/10

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992
Micron and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.
This data sheet contains initial descriptions of products still under development.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2010 Micron Technology, Inc. All rights reserved.