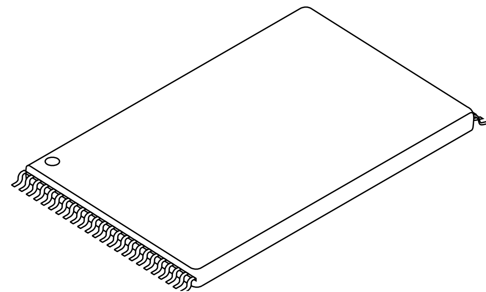
NAND Flash Memory

MT29F32G08MAA ES, MT29F32G08CBAAA, MT29F64G08CFAAA, MT29F64G08CEAAA, MT29F128G08TAA ES, MT29F128G08CJAAA, MT29F128G08CKAAA

Features

- Open NAND Flash Interface (ONFI) 2.0-compliant
- Multilevel cell (MLC) technology
- Organization
  Page size: x8: 4314 bytes (4096 + 218 bytes)
  - Block size: 128 pages (512K + 27K bytes)
  - Plane size: 4096 blocks
  - Device size: 32Gb, 8192 blocks; 64Gb, 16,384 blocks; 128Gb, 32,768 blocks
- READ performance
  - Random read: 50µs
  - Sequential read: 20ns
- PROGRAM performance
  - Page program: 900µs (TYP)
  - Block erase: 3ms (TYP)
- Endurance: 10,000 PROGRAM/ERASE cycles[1]
- First block (block address 00h) guaranteed to be valid with ECC when shipped from factory[1]
- Industry-standard basic NAND Flash command set
- Advanced command set
  - PROGRAM PAGE CACHE MODE
  - PAGE READ CACHE MODE
  - Two-plane commands
  - Interleaved die operations
  - READ UNIQUE ID
- Operation status byte provides a software method of detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting PROGRAM and ERASE cycle completion
- WP# signal: entire-device hardware write protect
- RESET required as first command after power-up
- INTERNAL DATA MOVE operations supported within the plane from which data is read

Figure 1: 48-Pin TSOP Type 1



Options

- Density[2]: 32Gb, 64Gb, 128Gb
- Device width: x8
- Configuration:

	# of die	# of CE#	# of R/B#	I/O
TSOP	1	1	1	Common
TSOP	2	2	2	Common
TSOP	4	2	2	Common
LGA	2	2	2	Separate
LGA	4	2	2	Separate

- Vcc: 2.7V–3.6 V
- Package: 48-pin TSOP type I (lead-free plating), 52-pad LGA
- Operating temperature:
  – Commercial temperature (0°C to +70°C)
  – Extended temperature (–40°C to +85°C)

Notes: 1. For details, see “Error Management” on page 89.
2. For part numbering and markings, see Figure 2 on page 2.

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Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities (see Figure 2).

Figure 2: Part Number Chart for 32Gb, 64Gb TSOP Engineering Samples

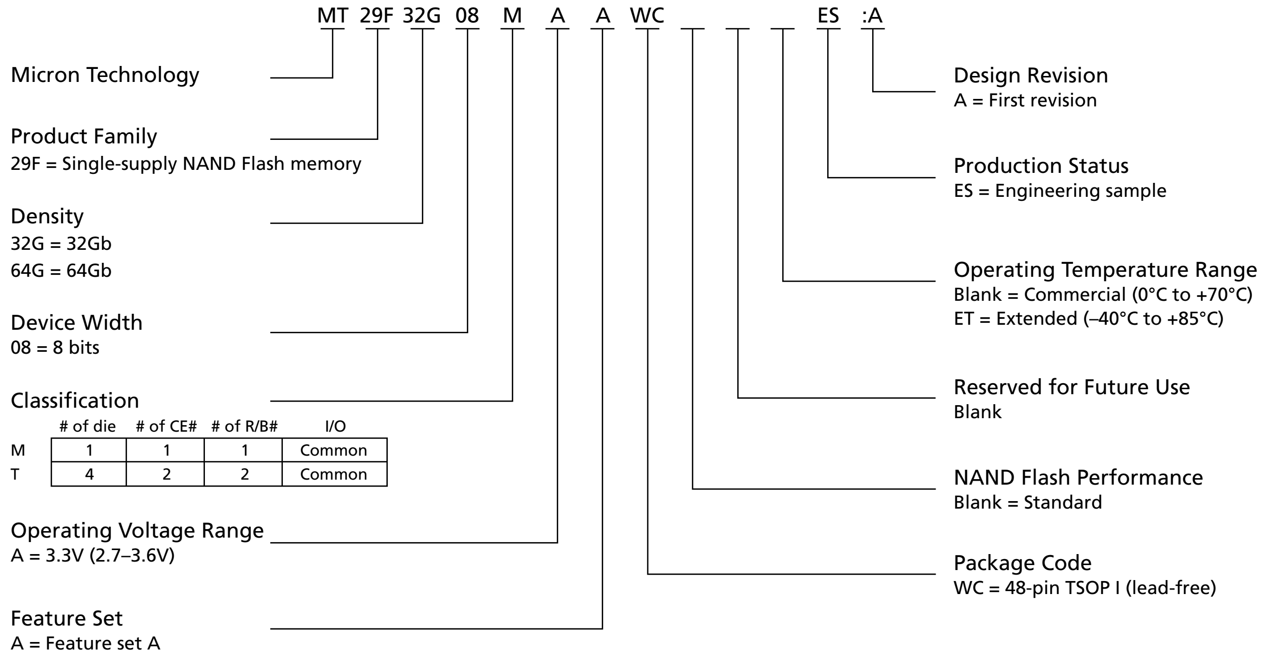

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Figure 3: Part Number Chart

MT 29F 32G 08 C B A A A WC _ _ _ _ :A

Micron Technology — MT

Product Family — 29F
29F = Single-supply NAND Flash memory

Density
32G = 32Gb
64G = 64Gb
128G = 128Gb

Device Width
08 = 8 bits

Cell Type
C = MLC-2

Classification

	# of die	# of CE#	# of R/B#	I/O
B	1	1	1	1
E	2	2	2	2
F	2	2	2	1
J	4	2	2	1
K	4	2	2	2

Operating Voltage Range
A = 3.3V (2.7–3.6V)

Feature Set
A = Feature set A

Interface
A = Async only

Package Code
WC = 48-pin OCPL TSOP I (lead-free)
WP = 48-pin CPL TSOP I (lead-free)
C5 = 52-pad VLGA
14mm x 18mm x 1mm (lead-free)

Speed Grade
Blank (if no grade defined)

Operating Temperature Range
Blank = Commercial (0°C to +70°C)
ET = Extended (–40°C to +85°C)
WT = Wireless (–25°C to +85°C)

Reserved for Future Use
Blank

Production Status
Blank = Production

Design Revision
A = First revision

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site at www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

Micron® NAND Flash technology provides a cost-effective solution for applications requiring high-density solid-state storage. The MT29F32G is a 32Gb NAND Flash memory device. The MT29F64G is a two-die stack that operates as two independent 32Gb devices. The MT29F128G is a four-die stacks that operates as two independent 64Gb devices, providing a total storage capacity of 128Gb. Each stack provides the noted density in a single, space-saving package. Micron NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

Micron NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Two additional pins control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, supporting future upgrades to higher densities without board redesign.

The MT29F32G and MT29F64G devices contain two planes per die for each CE#. The MT29F128G device contains two planes per die, with two die per CE#, for a total of four planes per CE#. Each plane consists of 4096 blocks. Each block is subdivided into 128 programmable pages. Each page consists of 4314 bytes. The pages are further divided into a 4096-byte data storage region with a separate 218-byte spare area. The 218-byte area is typically used for error management functions.

The contents of each 4314-byte page can be programmed in ^{t}PROG, and an entire block can be erased in ^{t}BERS. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 10,000 cycles when using appropriate error correction code (ECC) and error management.

The MT29F32G, MT29F64G, and MT29F128G are ONFI 2.0-compliant devices. The ONFI 2.0 specification can be found at www.onfi.org.

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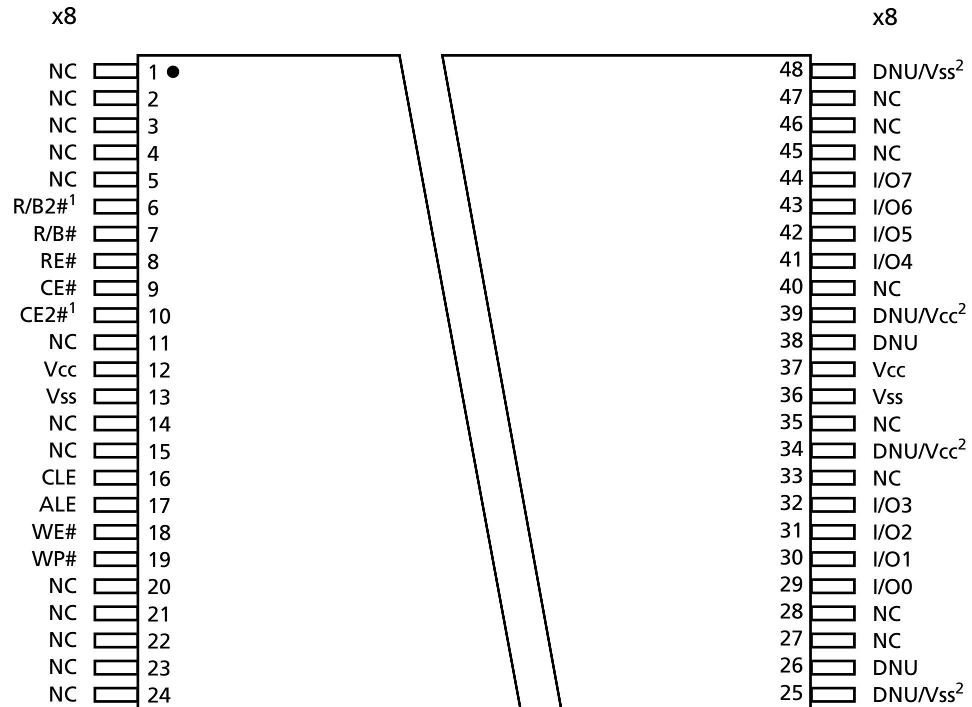
Figure 4: Pin Assignment (Top View) 48-Pin TSOP Type 1



Notes:
1. CE2# and R/B2# are available on 64Gb and 128Gb devices only. These pins are NC for other configurations.
2. These Vcc and Vss pins are for compatibility with ONFI 2.0. If not supplying Vcc or Vss to these pins, do not use them.

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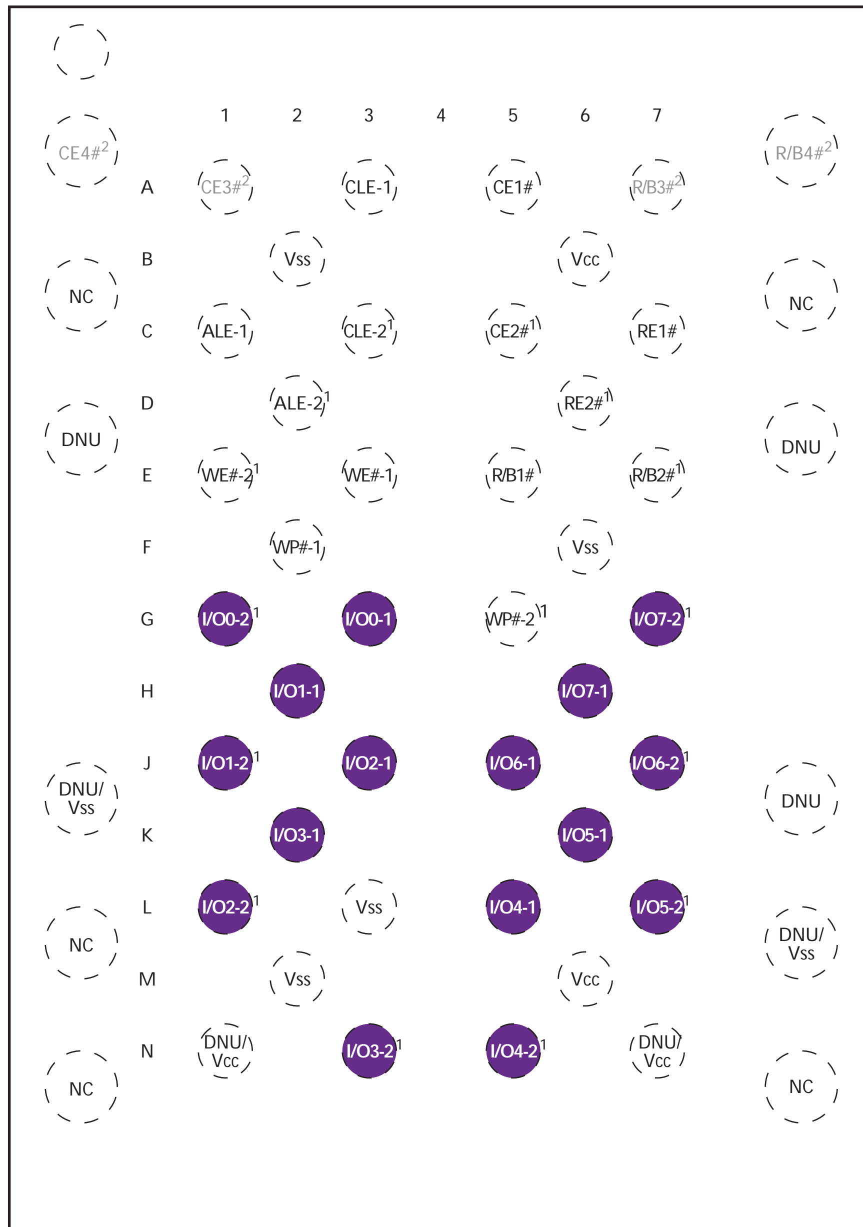
Figure 5: Pad Assignment (Top View) 52-Pad LGA



Top View, Pads Down

Notes: 1. These pads are available only on the 64Gb and 128Gb devices. These pads are NC for other configurations.
2. These pads are currently NC and are shown for future placement.

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Table 1: Signal Descriptions (TSOP/LGA)

Symbol	Type	Description
ALE, ALE-1, ALE-2	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2# (CE3#, CE4#)	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be deasserted. For the 32Gb configuration, CE# controls the first 16Gb of memory; CE2# controls the second 16Gb of memory. For the 64Gb configuration, CE# controls the first 32Gb of memory; CE2# controls the second 32Gb of memory. For the 128Gb configuration, CE# controls the first 64Gb of memory; CE2# controls the second 64Gb of memory. See "Bus Operation" on page 17 for additional operational details.
CLE, CLE-1, CLE-2	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#, RE#-1, RE#-2	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#, WE#-1, WE#-2	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#, WP#-1, WP#-2	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0], I/O[7:0]-1, I/O[7:0]-2	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, RB2# (R/B3#, R/B4#)	Output	Ready/busy: This is an open-drain, active-LOW output that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during READ operations to indicate when data is being transferred from the array into the serial data register. After these operations have completed, R/B# returns to the high-impedance state. In the 64Gb configuration, R/B# is for the 32Gb of memory enabled by CE#; R/B2# is for the 32Gb of memory enabled by CE2#. In the 128Gb configuration, R/B# is for the 64Gb of memory enabled by CE#; R/B2# is for the 64Gb of memory enabled by CE2#.
Vcc	Supply	Vcc: Power supply pin.
Vss	Supply	Vss: Ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left disconnected.
DNU/Vss	–	If not supplying Vss to these pins/pads, do not use them.
DNU/Vcc	–	If not supplying Vcc to these pins/pads, do not use them.

Note: CE3#, CE4#, R/B3#, and R/B4# are currently NC and are shown for future placement.

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Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

The data is transferred to or from the NAND Flash memory array, byte by byte (x8), through a data register and a cache register. The cache register is closest to the I/O control circuits and acts as a data buffer for I/O data, whereas the data register is closest to the memory array and acts as a data buffer for NAND Flash memory array operation.

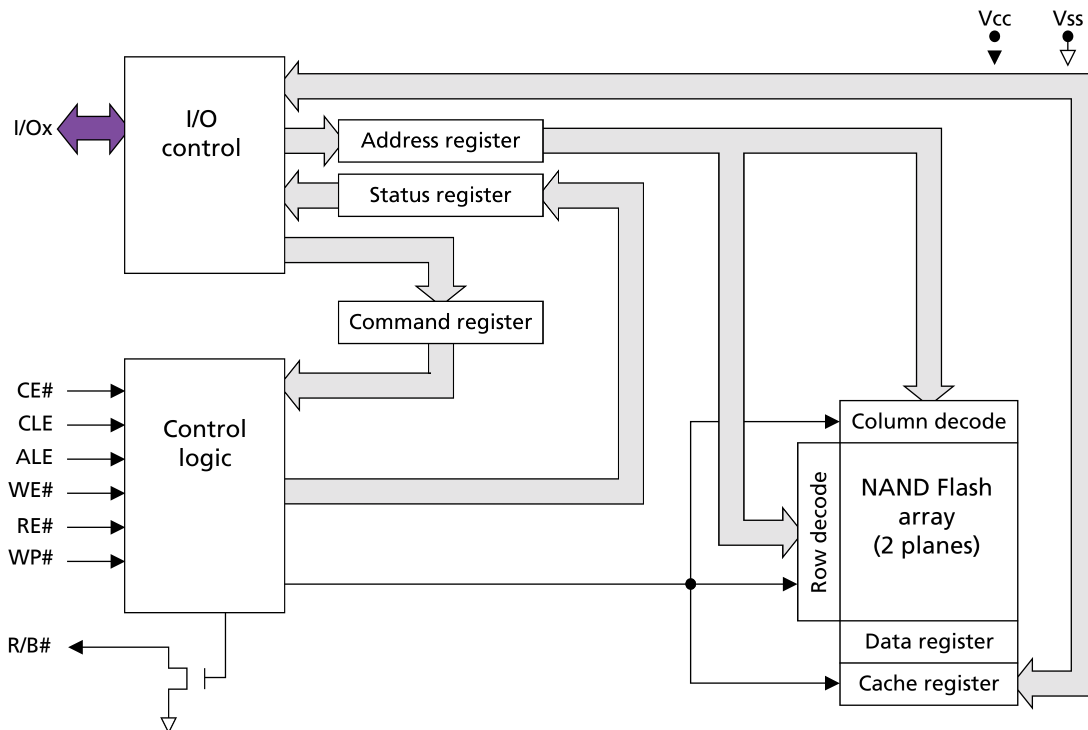
The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operations.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence as shown in Tables 3 and 4, on pages 15 and 16. See Figure 7 on page 14 for additional memory mapping and addressing details.

Figure 6: NAND Flash Functional Block Diagram



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Memory Mapping

Figure 7: Memory Map

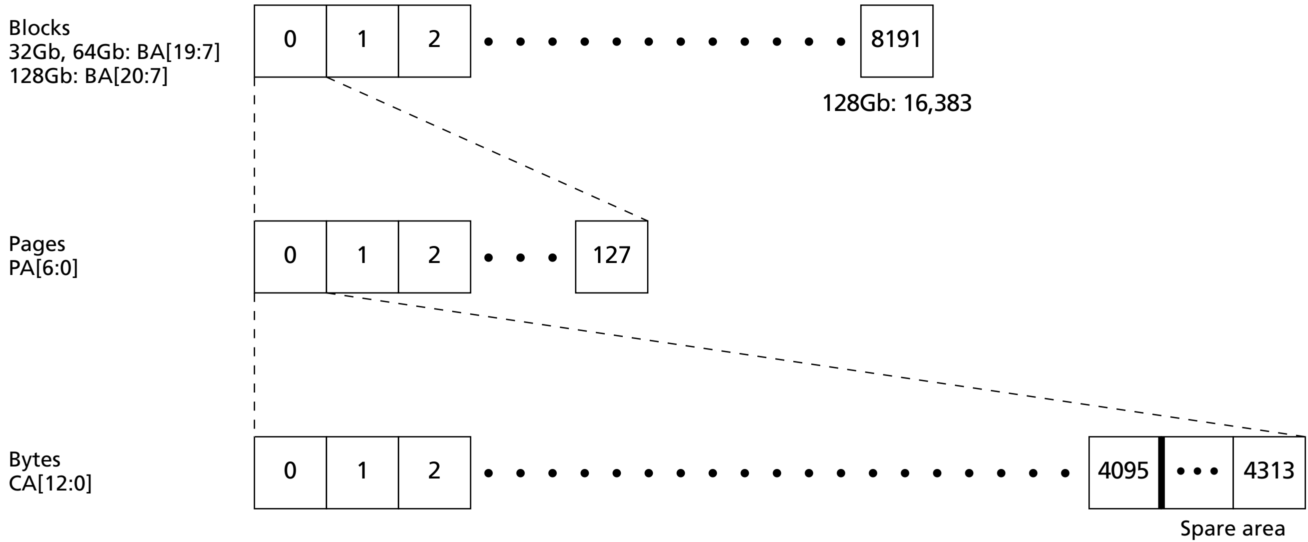

Table 2: Operational Example

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x00000010D9	0x00000010DA–0x0000001FFF
0	1	0x0000010000	0x00000110D9	0x00000110DA–0x0000011FFF
0	2	0x0000020000	0x00000210D9	0x00000210DA–0x0000021FFF
…	…	…	…	
16,383	126	0x1FFFFE0000	0x1FFFFE10D9	0x1FFFFE10DA–0x1FFFFEFFFF
16,383	127	0x1FFFFF0000	0x1FFFFF10D9	0x1FFFFF10DA–0x1FFFFFFFFF

Note: As shown in Table 3 on page 15, the three most significant bits in the high nibble of address cycle 2 are not assigned; however, these 3 bits must be held LOW during the address cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in address cycle 2 even though they do not have address bits assigned to them.

The 13-bit column address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4313 are valid. Bytes 4314 through 8191 of each page are out of bounds, do not exist in the device, and cannot be addressed.

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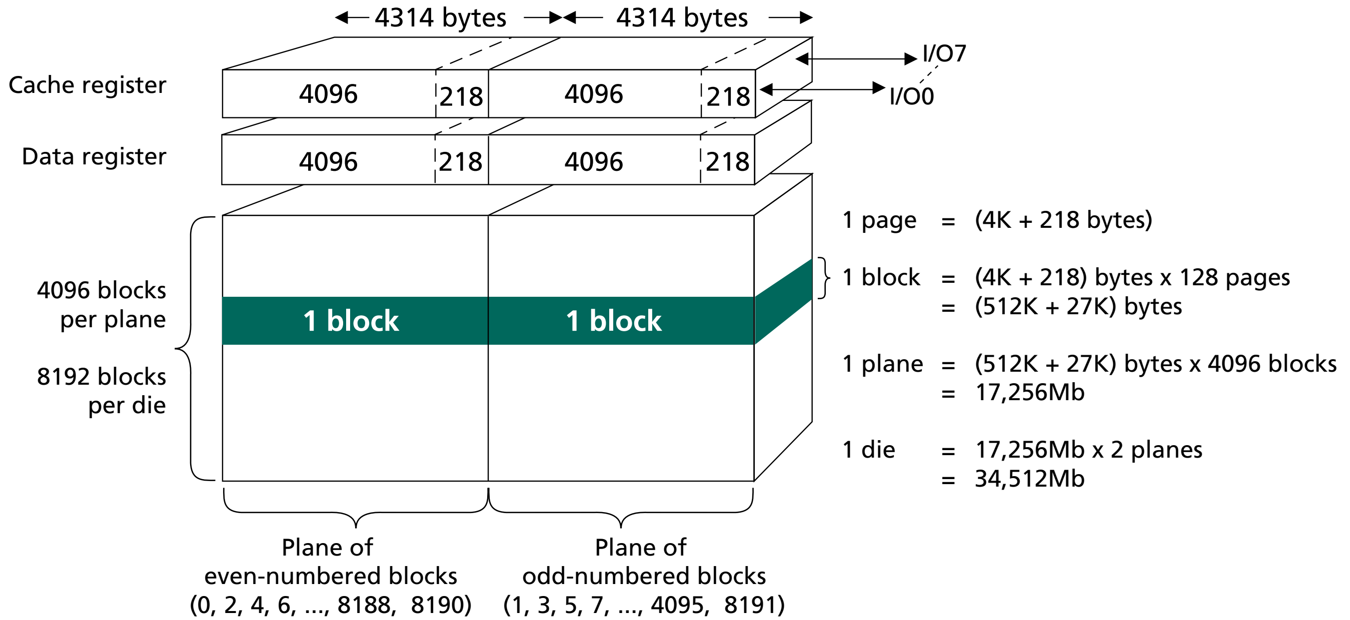
Array Organization

Figure 8: Array Organization: 32Gb and 64Gb Devices



Note: For 64Gb devices, the 32Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 3: Array Addressing: 32Gb and 64Gb

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7[3]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	BA19	BA18	BA17	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. Column address 4313 (10D9h) is the maximum valid column address.
3. Plane select bit:
   0 = plane of even-numbered blocks
   1 = plane of odd-numbered blocks

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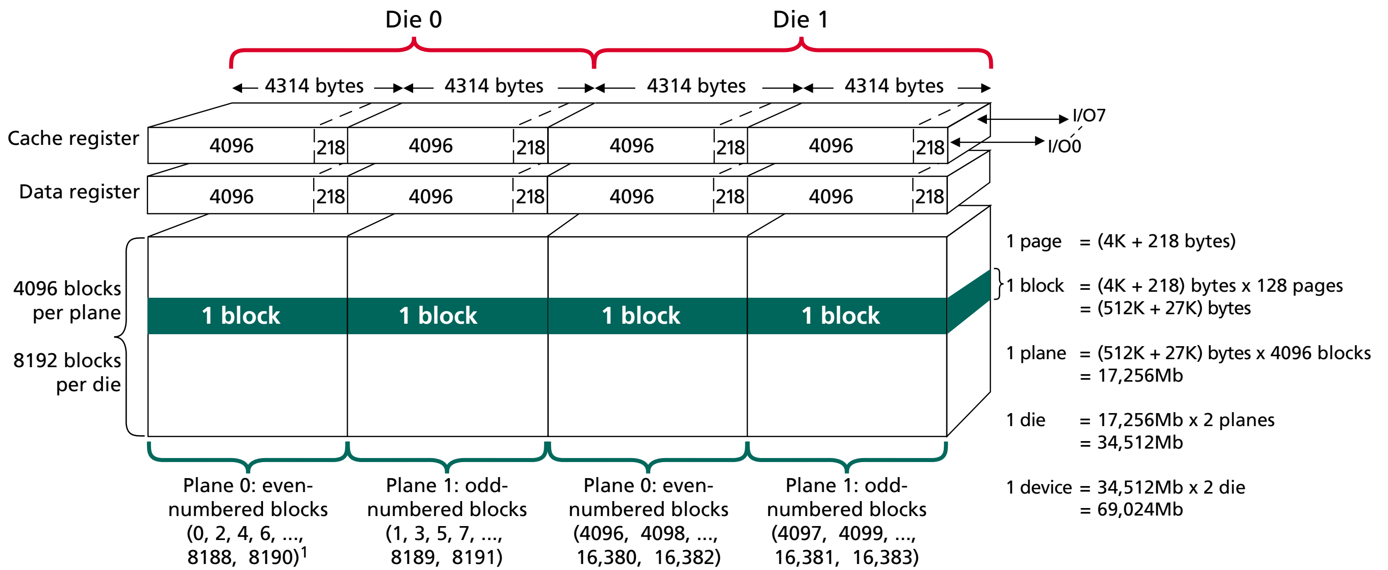
Figure 9: Array Organization: 128Gb Devices



Notes:
1. Die 0, Plane 0: BA20 = 0; BA7 = 0
   Die 0, Plane 1: BA20 = 0; BA7 = 1
   Die 1, Plane 0: BA20 = 1; BA7 = 0
   Die 1, Plane 1: BA20 = 1; BA7 = 1
2. For 128Gb devices, the 64Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 4: Array Addressing: 128Gb

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7[3]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	BA20[4]	BA19	BA18	BA17	BA16

Notes:
1. CAx = column address; PAx = page address; BAx = block address.
2. Column address 4313 (10D9h) is the maximum valid column address.
3. Plane select bit:
   0 = plane of even-numbered blocks
   1 = plane of odd-numbered blocks
4. Die select bit:
   0 = 0–32Gb
   1 = 32Gb–64Gb

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Bus Operation

The bus on NAND Flash devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0]. The 64Gb and 128Gb LGA packaged devices each have two independent data I/O and command pads. These are I/O[7:0], CE#, WE#, RE#, CLE, ALE, WP#, and I/O[7-2:0-2], CE2#, WE#-2, RE#-2, CLE-2, ALE-2, WP#-2. This enables independent data I/O, address, and command control for each half of a 64Gb or 128Gb device.

The command sequence normally consists of a command latch cycle, address input cycles, and one or more data cycles—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE, and WP# control NAND Flash device READ and WRITE operations. On the 64Gb MT29F64G, CE#, and CE2# each control independent 32Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#. On 128Gb devices, CE# and CE2# each control independent 64Gb arrays. CE2# functions the same as CE# for its own arrays; all operations described for CE# also apply to CE2#..

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the NAND Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH, and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred, and the device is not busy. This helps reduce power consumption. See Figure 81 on page 101 and Figure 89 on page 108 for examples of CE# “Don’t Care” operations.

The CE# “Don’t Care” operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

As exceptions, the device accepts the READ STATUS, TWO-PLANE/MULTIPLE-DIE READ STATUS, and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 73 on page 97).

Commands are input on I/O[7:0] only.

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are low, and
- ALE is high.

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Addresses are input on I/O[7:0] only. Bits not part of the address space must be LOW (see Figure 74 on page 97).

The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. See Table 6 on page 22 and Table 7 on page 23.

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0] for x8 devices. See Figure 75 on page 98 for additional data input details.

READs

After a READ command is issued, data is transferred from the memory array to the data register from the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. R/B# returns to HIGH at this time. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 80 on page 101 for detailed timing information.

The READ STATUS (70h) command, TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command, or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 76 on page 99 for proper timing. If ^{t}RC is less than 30ns, use Figure 77 on page 99 for extended data output (EDO) timing.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. R/B# is typically connected to an interrupt pin on the system controller (see Figure 12 on page 19).

On the 64Gb device, R/B# provides a status indication for the 32Gb section enabled by CE#, and R/B2# does the same for the 32Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indicators for each 32Gb section.

On 128Gb devices, R/B# provides a status indicator for the 64Gb section enabled by CE#; R/B2# provides this status indicator for the 64Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indicators for each 64Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10%–90% points on the R/B# waveform, rise time is approximately two time constants (TC), as shown in Figure 10.

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Figure 10: Time Constants

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined primarily by the output impedance of the R/B# pin and the total load capacitance. Refer to Figure 13 and Figure 14 on page 20, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and Vcc.

Figure 11: Minimum Rp

$$Rp(\mathrm{MIN}) = \frac{V_{CC}(MAX) - V_{OL}(MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 12: READY/BUSY# Open-Drain

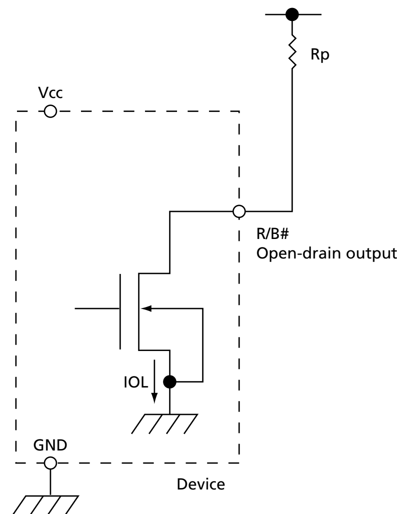

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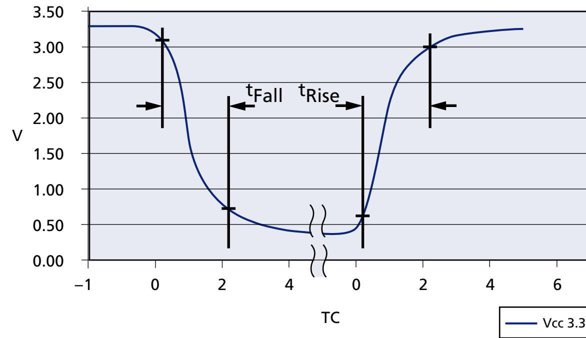
Figure 13: ^{t}Fall and ^{t}Rise



Notes:
1. ^{t}Fall and ^{t}Rise are calculated at 10%–90% points.
2. ^{t}Rise is primarily dependent on the external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 10ns at 3.3V.
4. See TC values in Table 15 on page 20 for approximate Rp value and TC.

Figure 14: IOL vs. Rp

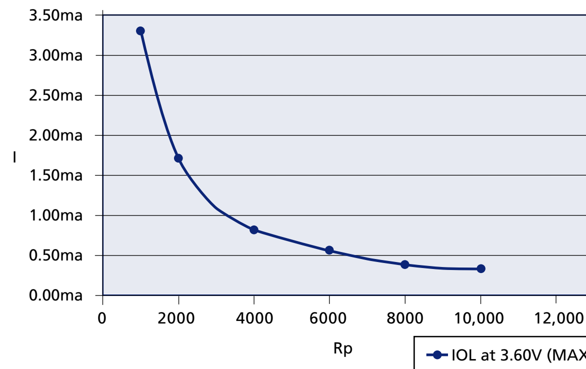


Figure 15: TC vs. Rp

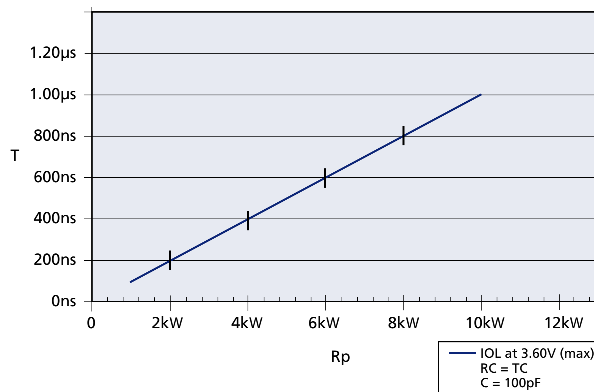


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Table 5: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read mode	Command input
L	H	L	↑	H	X		Address input
H	L	L	↑	H	H	Write mode	Command input
L	H	L	↑	H	H		Address input
L	L	L	↑	H	H	Data input	
L	L	L	H	↓	X	Sequential read and data output	
X	X	X	H	H	X	During READ (busy)	
X	X	X	X	X	H	During PROGRAM (busy)	
X	X	X	X	X	H	During ERASE (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/Vcc[1]	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = Vih or Vil.

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Command Definitions

Table 6: Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	5
PAGE READ CACHE MODE SEQUENTIAL	31h	–	No	–	No	
PAGE READ CACHE MODE RANDOM	00h	5	No	31h	No	
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	2, 5
RANDOM DATA READ	05h	2	No	E0h	No	3, 5
READ ID	90h	1	No	–	No	
READ UNIQUE ID	EDh	1	No	--	No	
READ PARAMETER PAGE	ECh	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	5
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	5
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	2, 5
RANDOM DATA INPUT	85h	2/5	Yes/optional	–	No	4, 5
BLOCK ERASE	60h	3	No	D0h	No	5
RESET	FFh	–	No	–	Yes	5
SET FEATURES	EFh	1	4	–	No	
GET FEATURES	EEh	1	No	–	No	

Notes:
1. Indicates required data cycles between command cycle 1 and command cycle 2.
2. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE or PROGRAM for INTERNAL DATA MOVE. See Figure 8 on page 15 and Figure 9 on page 16 for plane address boundary definitions.
3. RANDOM DATA READ command limited to use within a single page.
4. RANDOM DATA INPUT command will support 2 address cycles or 5 address cycles.
5. These commands are valid during busy when an interleaved die operation is being performed (see "Interleaved Die Operations" on page 69).

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Table 7: Two-Plane Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	2
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h	5	10h	No	2
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h	5	15h	No	2
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-85h	5	10h	No	1,2
TWO-PLANE BLOCK ERASE	60h	3	D1h-60h	3	D0h	No	2

Notes:
1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE or TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Figure 8 on page 15 and Figure 9 on page 16 for plane address boundary definitions.
2. These commands are valid during busy when interleaved die operations are being performed.

READ Operations

PAGE READ 00h–30h

At power-on the device defaults to read mode. To enter read mode while in operation, write the 00h command to the command register, then write 5 address cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal; or alternatively, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must reissue the READ (00h) command to receive data output from the data register. (See Figure 85 on page 105 and Figure 86 on page 106 for examples.) After the READ command has been reissued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial PAGE READ sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 16 on page 24).

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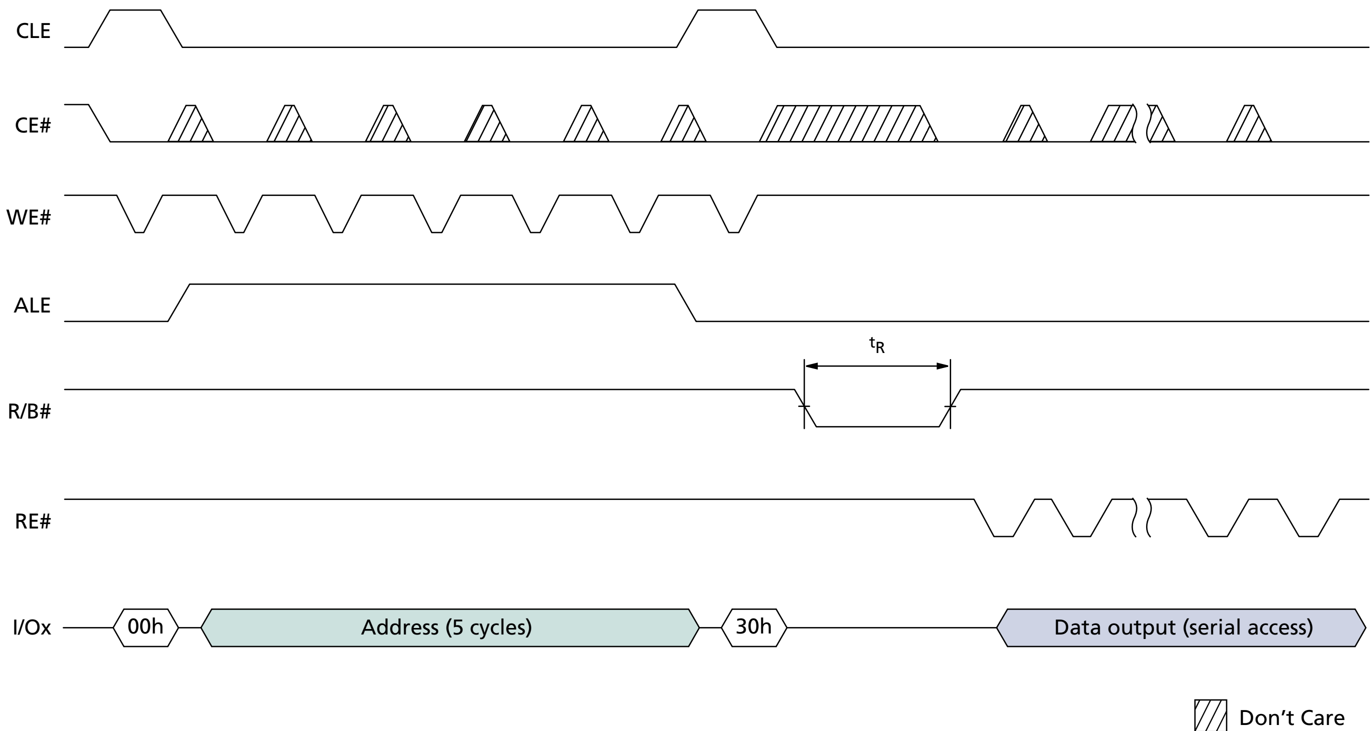
Figure 16: PAGE READ Operation



RANDOM DATA READ 05h–E0h

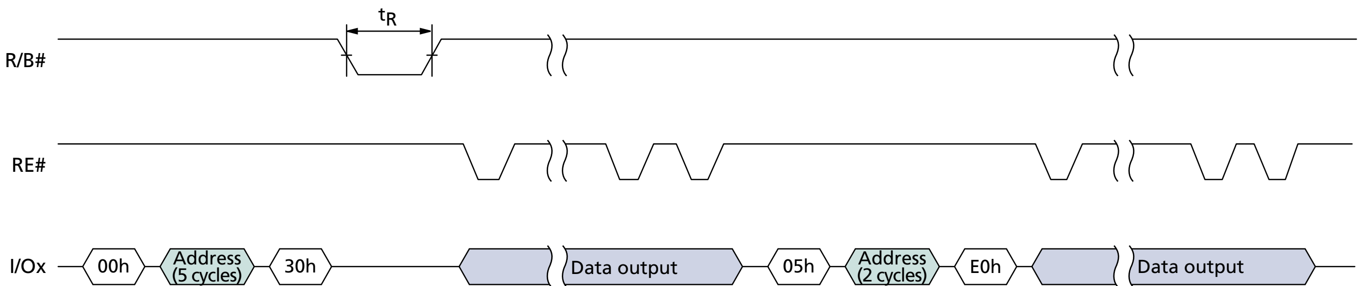
The RANDOM DATA READ command enables the user to specify a new column address so data at single or multiple addresses can be read. The random read mode is enabled after any PAGE READ operation sequence (PAGE READ, PAGE READ CACHE MODE, and TWO-PLANE PAGE READ).

Random data can be output after the initial PAGE READ by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 17).

Figure 17: RANDOM DATA READ Operation



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PAGE READ CACHE MODE Operations

Micron NAND Flash devices have a cache register that can be used to increase READ operation speed. Data can be output from the device's cache register while concurrently moving a page from the NAND Flash array to the data register.

To begin a PAGE READ CACHE MODE sequence, begin by reading a page from the NAND Flash array to the cache register using the PAGE READ (00h-30h) command (see “PAGE READ 00h–30h” on page 23). R/B# goes LOW during ^{t}R (status register bits 6 and 5 = 00). After ^{t}R (R/B# is HIGH and status register bits 6 and 5 = 11), issue one of these commands:

- PAGE READ CACHE MODE SEQUENTIAL (31h) command to begin copying the next sequential page from the NAND Flash array to the data register.
- PAGE READ CACHE MODE RANDOM (00h-31h) command to begin copying the page specified in this command from the NAND Flash array to the data register.

PAGE READ CACHE MODE RANDOM (00h-31h) can cross block and plane address boundaries, but not die address boundaries.

After the PAGE READ CACHE MODE SEQUENTIAL or PAGE READ CACHE MODE RANDOM command has been issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR1 while the next page begins copying into the data register. After ^{t}RCBSYR1, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that a page is being copied from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

After outputting the desired number of bytes from the cache register, it is possible to begin an additional PAGE READ CACHE MODE (31h or 00h-31h) operation or to issue the PAGE READ CACHE MODE LAST (3Fh) command.

If an additional PAGE READ CACHE MODE (31h or 00h-31h) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR2 while the data register is copied to the cache register, then the next page begins copying into the data register. After ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

If the PAGE READ CACHE MODE LAST (3Fh) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR2 while the data register is copied into the cache register. After ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

During device busy times, ^{t}RCBSYR1 and ^{t}RCBSYR2, the only valid commands are READ STATUS (70h 78h) and RESET (FFh). Until status register bit 5 = 1, the only valid commands during PAGE READ CACHE MODE operations are READ STATUS (70h 78h), READ (00h), PAGE READ CACHE MODE (31h and 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

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PAGE READ CACHE MODE SEQUENTIAL 31h

The PAGE READ CACHE MODE SEQUENTIAL (31h) command reads the next sequential page into the data register while the previous page is output from the cache register. To issue this command, write 31h to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSYR1 or ^{t}RCBSYR2. After ^{t}RCBSYR1 or ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register by toggling RE#, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Do not issue the 31h command after reading the last page of the block into the data register. Instead, issue the 3Fh command. Crossing block boundaries with the PAGE READ CACHE MODE SEQUENTIAL (31h) command is prohibited.

PAGE READ CACHE MODE RANDOM 00h-31h

The PAGE READ CACHE MODE RANDOM (00h-31h) command reads the specified page into the data register while the previous page is output from the cache register. To issue this command, write 00h to the command register, then write 5 address cycles to the address register. Conclude the sequence by writing 31h to the command register. The column address in the specified address is ignored.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSYR1 or ^{t}RCBSYR2. After ^{t}RCBSYR1 or ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

PAGE READ CACHE MODE LAST 3Fh

The PAGE READ CACHE MODE LAST (3Fh) command copies a page from the data register to the cache register without beginning a new PAGE READ CACHE MODE operation. To issue the PAGE READ CACHE MODE LAST command, write 3Fh to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR2. After ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11 to indicate that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

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Figure 18: PAGE READ CACHE MODE

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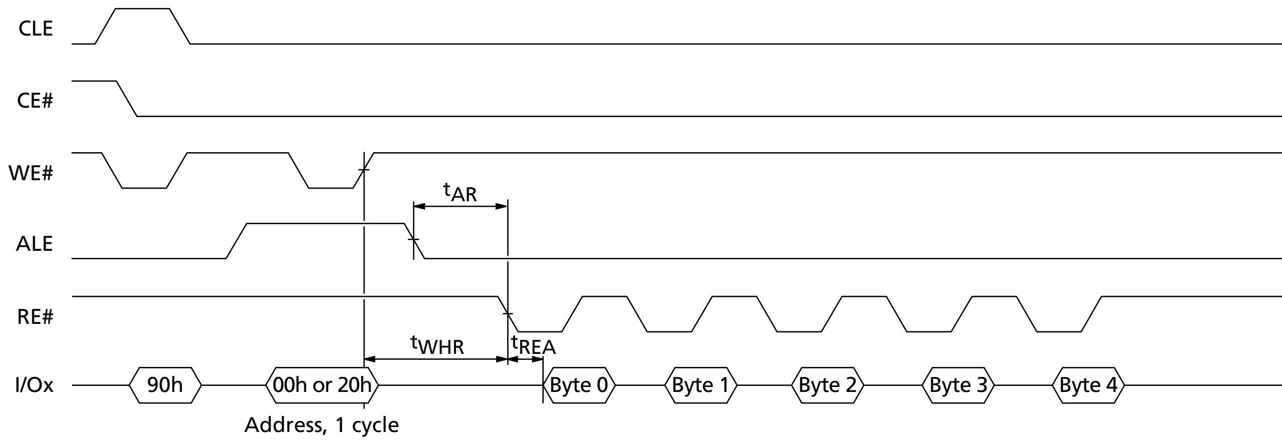
READ ID 90h

The READ ID command is used to read the 5 bytes of identifier code programmed into the device. The READ ID command reads a 5-byte table that includes Manufacturer ID, device configuration, and part-specific information (see Table 8 on page 29 and Table 9 on page 30).

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see Figure 19). For address 00h, bytes 5 to 7 are unknown reserved bytes. The device will repeatedly output the same 8 bytes of data if the host continues to toggle RE#. For address 20h, the device will repeatedly output the same 4 bytes of data if the host continues to toggle RE#.

Figure 19: READ ID Operation



Notes:
1. See Table 8 on page 29 for byte definitions with address 00h.
2. See Table 9 on page 30 for byte definitions with address 20h.

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Table 8: Device ID and Configuration Codes for Address 00h

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	**Manufacturer ID**										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	**Device ID**										
MT29F32G	32Gb, ×8, 3V	1	1	0	1	0	1	1	1	D7h	
MT29F64G	64Gb, ×8, 3V	1	1	0	1	0	1	1	1	D7h	2
MT29F128G	128Gb, ×8, 3V	1	1	0	1	1	0	0	1	D9h	3
Byte 2											
Number of die per CE#	1							0	0	00b	
	2							0	1	01b	
Cell type	MLC					0	1			01b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	MT29F32G	1	0	0	1	0	1	0	0	94h	
	MT29F64G	1	0	0	1	0	1	0	0	94h	
	MT29F128G	1	1	0	1	0	1	0	1	D5h	
Byte 3											
Page Size	4KB							1	0	10b	
Spare area size (bytes)	218B						1			1b	
Block size (w/o spare)	512KB			1	1					11b	
Organization	×8		0							0b	
Serial access (MIN)	20nS	0				1				0xxx1b	
Byte value	–	0	0	1	1	1	1	1	0	3Eh	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane Size	16Gb	1	0	0	0					1000b	
Byte value	MT29F32G	1	0	0	0	0	1	0	0	84h	
	MT29F64G	1	0	0	0	0	1	0	0	84h	
	MT29F128G	1	0	0	0	1	0	0	0	88h	

Notes:
1. b = binary, h = hex
2. MT29F64G reflects the configuration of each 32Gb section.
3. MT29F128G reflects the configuration of each 64Gb section.

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Table 9: Device ID and Configuration Codes for ONFI Address (20h)

Address = 20h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	O	0b	1b	0b	0b	1b	1b	1b	1b	4Fh	
Byte 1	N	0b	1b	0b	0b	1b	1b	1b	0b	4Eh	
Byte 2	F	0b	1b	0b	0b	0b	1b	1b	0b	46h	
Byte 3	I	0b	1b	0b	0b	1b	0b	0b	1b	49h	

Notes: 1. b = binary, h = hex

READ PARAMETER PAGE ECh

When issued, the READ PARAMETER PAGE (ECh) command returns device configuration information. RANDOM DATA READ (05h-E0h) is supported during data output. READ STATUS (70h) can be used to check the status of the READ PARAMETER PAGE command. After reading status, issue 00h to resume reading the parameter page. Refer to the ONFI specification for parameter page data structure definition. The data structure is defined at least five times. Reading bytes beyond the final parameter page copy returns indeterminate values.

Figure 20: READ PARAMETER PAGE (ECh)

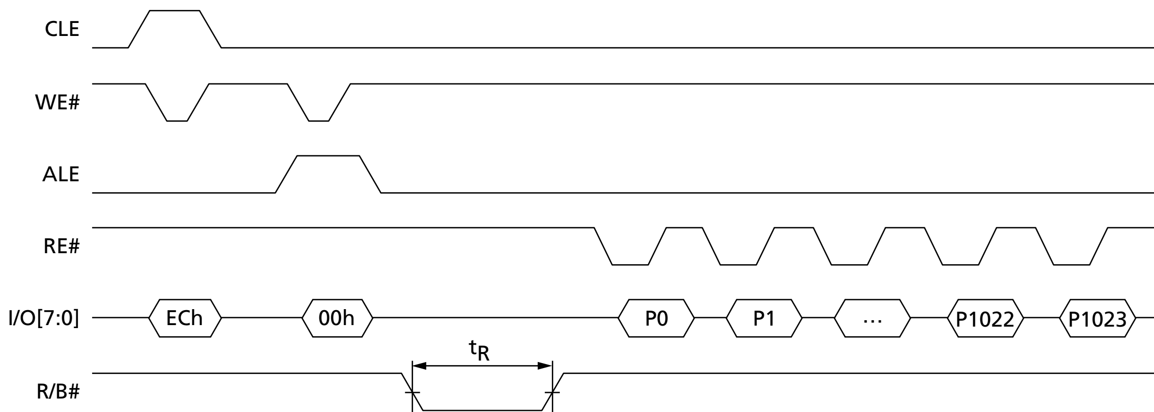

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Table 10: Parameter Page Data Structure

Byte	Description	Device	Values
Revision Information and Features Block			
0–3	Parameter page signature Byte 0: 4Fh, O Byte 1: 4Eh, N Byte 2: 46h, F Byte 3: 49h, I	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	06h, 00h
6–7	Features supported Bit[15:6]: Reserved (0) Bit 5: 0 = does not support synchronous interface Bit 4: 1 = supports odd to even page copyback Bit 3: 1 = supports interleaved operations Bit 2: 1 = supports nonsequential page programming Bit 1: 1 = supports multiple logical unit (LUN) operations Bit 0: 1 = supports 16-bit data bus width	MT29F32G	18h, 00h
		MT29F64G	18h, 00h
		MT29F128G	1Ah, 00h
8–9	Optional commands supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports INTERNAL DATA MOVE Bit 3: 1 = supports TWO-PLANE/MULTIPLE-DIE READ STATUS Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE MODE command	–	3Eh, 00h
10–31	Reserved (0)	–	All 00h
Manufacturer Information Block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

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Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F32G08MAA	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 4Dh, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F32G08CBAAA	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 43h, 42h, 41h, 41h, 41h, 20h, 20h, 20h, 20h, 20h
		MT29F64G08CFAAA	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 43h, 46h, 41h, 41h, 41h, 20h, 20h, 20h, 20h, 20h
		MT29F64G08CEAAA	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 43h, 45h, 41h, 41h, 41h, 20h, 20h, 20h, 20h, 20h
		MT29F128G08TAA	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 54h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F128G0CJAAA	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 4Ah, 41h, 41h, 41h, 20h, 20h, 20h, 20h
		MT29F128G08CKAAA	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 4Bh, 41h, 41h, 41h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory Organization Block			
80–83	Number of data bytes per page	–	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	–	DAh, 00h
86–89	Number of data bytes per partial page	–	00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page	–	1Bh, 00h
92–95	Number of pages per block	–	80h, 00h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 20h, 00h, 00h
100	Number of LUNs per CE#	MT29F32G	01h
		MT29F64G	01h
		MT29F128G	02h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	02h
103–104	Bad blocks maximum per LUN	–	C8h, 00h
105–106	Block endurance	–	01h, 04h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h

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Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
110	Number of programs per page	–	01h
111	Partial programming attributes Bit[7:5]: Reserved (0) Bit 4: 1 = partial page layout is partial page data followed by partial page spare Bits [3:1]: Reserved (0) Bit 0: 1 = partial page programming has constraints	–	00h
112	Number of bits ECC correctability	–	0Ch
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	01h
114	Interleaved operation attributes Bit[7:4]: Reserved (0) Bit 3: Address restrictions for program cache Bit 2: 1 = program cache supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	02h
115–127	Reserved (0)	–	All 00h
Electrical Parameters Block			
128	I/O pin capacitance per CE#	MT29F32G	05h
		MT29F64G	05h
		MT29F128G	0Ah
129–130	Timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	3Fh, 00h
131–132	Program cache timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h, 00h
133–134	^{t}PROG maximum PROGRAM PAGE time (µs)	–	98h, 08h
135–136	^{t}BERS maximum BLOCK ERASE time (µs)	–	10h, 27h
137–138	^{t}R maximum PAGE READ time (µs)	–	32h, 00h
139–140	^{t}CCS minimum change column setup time (ns)	–	FAh, 00h
141–149	Reserved (0)	–	All 00h
150	Input pin capacitance, maximum	MT29F32G	0Ah
		MT29F64G	0Ah
		MT29F128G	14h
151	Driver strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Supports driver strength settings	–	01h
152-163	Reserved (0)	–	All 00h

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Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
Vendor Block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = supports TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = does not support Micron-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable I/O drive strength support Bit[7:1]: Reserved (0) Bit 0: 0 = no support for programmable I/O drive strength by B8h command	–	00h
170	Number of programmable I/O drive strength settings Bit[7:3]: Reserved (0) Bit [2:0] = number of programmable I/O drive strength settings	–	04h
171	Programmable I/O drive strength feature address Bit[7:0] = programmable I/O drive strength feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = supports programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:1]: Reserved (0) Bit 0: 0 = does not support OTP mode	–	00h
176	OTP page start Bit[7:0] = page where OTP page space begins	–	00h
177	OTP DATA PROTECT address Bit[7:0] = page address to use when issuing OTP DATA PROTECT command	–	00h
178	Number of OTP pages Bit[15:4]: Reserved (0) Bit[3:0] = number of OTP pages	–	00h
179–252	Reserved (0)	–	All 00h
253	Parameter page revision	–	01h

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Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
254–255	Integrity cyclical redundancy check (CRC)	MT29F32G08MAA	76h, CAh
		MT29F32G08CBAAA	02h, F7h
		MT29F64G08CFAAA	90h, 75h
		MT29F64G08CEAAA	86h, 33h
		MT29F128G08TAA	E5h, E0h
		MT29F128G08CJAAA	7Ah, 42h
		MT29F128G08CKAAA	46h, 15h
Redundant Parameter Pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
768–1023	Value of bytes 0–255	–	See bytes 0–255
1024–1279	Value of bytes 0–255	–	See bytes 0–255
1278–1535	Value of bytes 0–255	–	See bytes 0–255
1536–1791	Value of bytes 0–255	–	See bytes 0–255
1792–2047	Value of bytes 0–255	–	See bytes 0–255
2048–2303	Value of bytes 0–255	–	See bytes 0–255
2304–2559	Value of bytes 0–255	–	See bytes 0–255
2560–2815	Value of bytes 0–255	–	See bytes 0–255
2816–3071	Value of bytes 0–255	–	See bytes 0–255
3072–3327	Value of bytes 0–255	–	See bytes 0–255
3328–3583	Value of bytes 0–255	–	See bytes 0–255
3584–4095	Value of bytes 0–255	–	See bytes 0–255
4096–4313	Reserved (FFh)	–	All FFh

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READ STATUS 70h

These NAND Flash devices have an 8-bit status register that the software can read during device operation. Table 11 on page 37 describes the status register.

Following a READ STATUS command, all READ cycles will originate from the status register until a new command is issued. Changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

In devices that have more than one die sharing a common CE# pin, the READ STATUS (70h) command reports the status of the die that was last addressed. If concurrent operations are started on both die, then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will continue to respond until the next operation is issued.

While monitoring the status register to determine when ^{t}R is complete, the user must reissue the READ (00h) command to make the change from status output to data output. After the READ command has been reissued, pulsing the RE# line will result in outputting data, starting from the initial column address.

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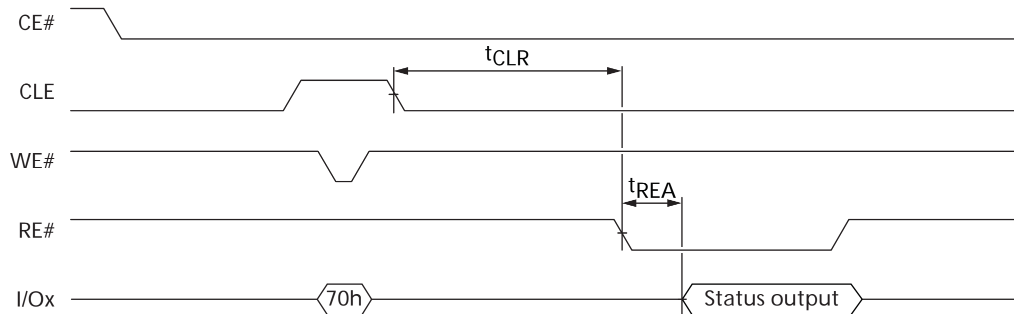
Table 11: Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0[1]	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	0 = Successful PROGRAM 1 = Error in PROGRAM
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy[2]	Ready/busy	Ready/busy[2]	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	0 = Busy 1 = Ready
7[4]	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected
[15:8]	–	–	–	–	–	0

Notes:
1. Status register bit 0 reports a 1 if a TWO-PLANE PROGRAM/ERASE operation fails on one or both planes. Status register bit 1 reports a 1 if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) to determine the plane to which the operation failed.
2. Status register bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.
3. Status register bit 6 is 1 when the cache register is ready to accept new data. R/B# follows bit 6.
4. Status register bit 7 typically mirrors the status of the WP# pin.

Figure 21: Status Register Operation



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READ UNIQUE ID EDh

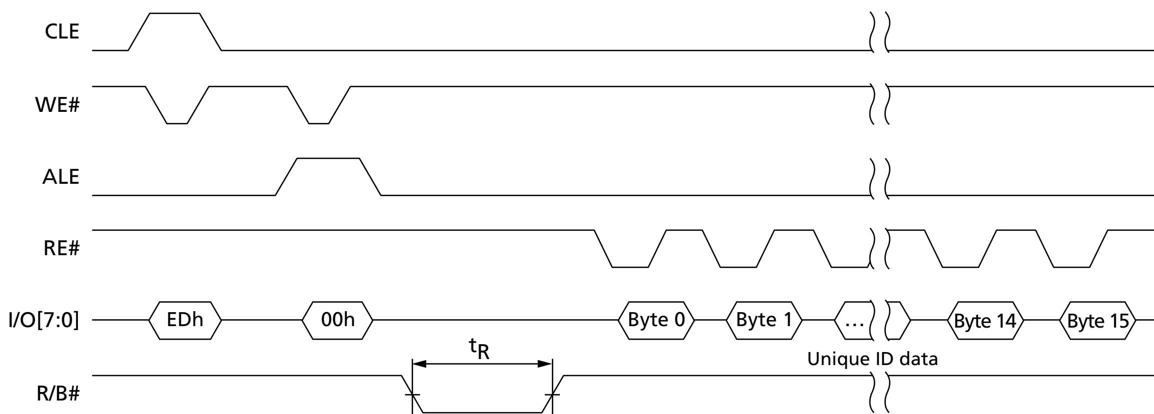
Micron offers the READ UNIQUE ID (EDh) command feature to provide a method for uniquely identifying a NAND Flash device. READ UNIQUE ID operation uses standard command and address timing. The format of the ID is arbitrary; however, this ID is guaranteed to be unique for every NAND Flash device manufactured.

Many controllers use proprietary error correction code (ECC) schemes; thus, it is not possible for Micron to protect unique ID data (UID) with factory-programmed ECC. However, to ensure data integrity, Micron programs the NAND Flash devices with a 16-byte unique ID, beginning at byte 0 of the page, then follows with a 16-byte ID complement. These 32 bytes of data are then repeated a total of 16 times, such that the last byte of the last copy of the unique ID complement resides at byte 511 in the page. The user can simply XOR the first copy of the unique ID and its complement. If all the bits in the results are 1, then the unique ID is good. In the unlikely event that any of the bits in the result are non-zero, the user can repeat the XOR operation on a subsequent copy of the unique ID data.

READ UNIQUE ID command timing is shown in Figure 22 on page 38. Unique ID data is stored on consecutive bytes for x8 devices. Normal page read timings apply for READ UNIQUE ID operations. To exit READ UNIQUE ID, cycle the power on the NAND Flash device or issue a RESET command.

READ STATUS (70h) commands and RESET (FFh) commands are the only commands supported during READ UNIQUE ID operation. Do not use MULTIPLE-DIE READ STATUS (78h) commands during READ UNIQUE ID command sequences. After reading status, issue 00h to resume reading the unique ID. RANDOM DATA READ is also supported during the READ UNIQUE ID command sequence. Reading bytes beyond the final UID copy returns indeterminate values.

Figure 22: READ UNIQUE ID



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PROGRAM Operations

PROGRAM PAGE 80h-10h

NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, from the least significant page address to the most significant page address (i.e., 0, 1, 2, … 127). Random page address programming is prohibited.

This NAND Flash device does not support partial-page programming operations.

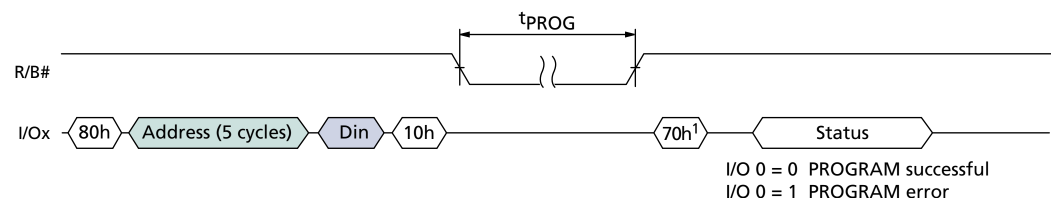
If a RESET (FFh) command is issued during a PROGRAM PAGE operation while R/B# is LOW, the data in the shared-memory cells being programmed could become invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by 5 address cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the specified address. The PROGRAM (10h) command is written after data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. WRITE verification detects only 1s that are not successfully written to 0s.

R/B# goes low for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h or 78h) command and the RESET (FFh) command are the only commands valid during programming operations. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the programming operation passed or failed (see Figure 23). The command register stays in read status register mode until another valid command is issued.

Figure 23: PROGRAM and READ STATUS Operation



Notes: 1. Command can be 70h or 78h.

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RANDOM DATA INPUT 85h

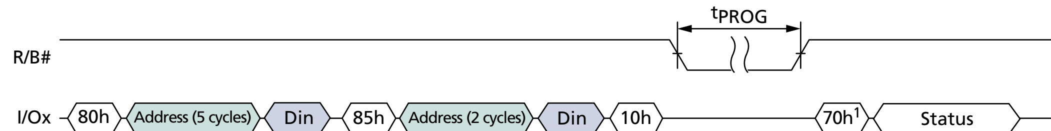
After the initial data set is input, additional data can be written with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 24 for the proper command sequence.

The RANDOM DATA INPUT command supposes 2 and 5 address cycles. The NAND Flash device exhibits the following behavior:

- If there are only 2 address input cycles, those addresses are identified as column addresses.
- If there are 5 address input cycles, the first 2 cycles are identified as column addresses and the last 3 cycles as row addresses.

Changing the plane address from the initial address is prohibited.

Figure 24: RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h.
2. This waveform shows only 2 address cycles; 85h also supports 5 address cycles.

PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by 5 address cycles, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE PROGRAM (15h) command is latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another PROGRAM PAGE CACHE MODE command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is delayed until current data register content has been programmed into the array.

RANDOM DATA INPUT commands are supported during PROGRAM PAGE CACHE MODE operations.

Bit 6 (cache R/B#) of the status register can be read by issuing the READ STATUS (70h, 78h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

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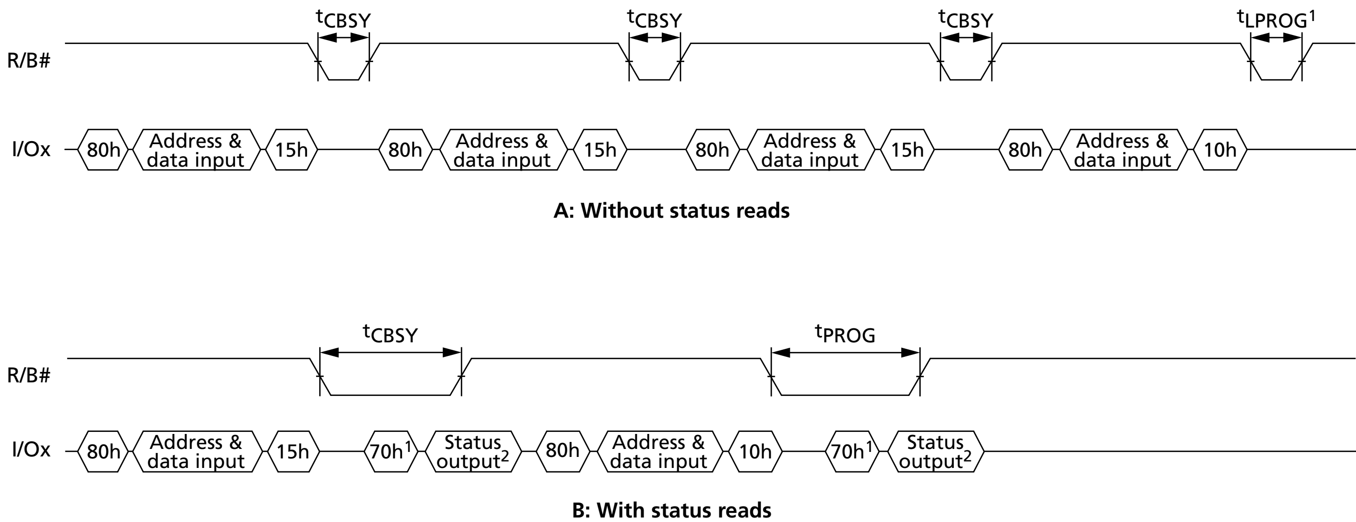
If the R/B# pin alone is used to determine programming completion, the last page of the programming sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 25).

Bit 1 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a 1 (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a 1 (ready state) (see Figure 25.)

If a RESET (FFh) command is issued during a PROGRAM PAGE CACHE MODE operation while R/B#, bit 5, or bit 6 of the status register is LOW, the data in the shared memory cells being programmed could become invalid. Interruption of a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 25: PROGRAM PAGE CACHE MODE Example



Notes:
1. Command can be 70h or 78h.
2. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h or 78h command.

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Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. Data moves are supported only within the plane from which data is read.

READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (5 cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

All 5 address cycles are required when a READ for INTERNAL DATA MOVE command is issued.

After a READ for INTERNAL DATA MOVE (00h-35h) command is issued and R/B# returns HIGH, signifying operation completion, the data transferred from the source page into the cache register can be read out by toggling RE#. Data is output sequentially from the column address originally specified with the READ FOR INTERNAL DATA MOVE (00h-35h) command, and the device can accept the PROGRAM for INTERNAL DATA MOVE command. RANDOM DATA READ (05h-E0h) commands can be issued without limit after the READ FOR INTERNAL DATA MOVE command. (See “PROGRAM for INTERNAL DATA MOVE 85h-10h” on page 42).

The PAGE READ (00h-30h) command can be used in place of the READ for INTERNAL DATA MOVE (00h-35h) command.

PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued, and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register, and the programming sequence for the new destination page begins, writing the 85h command, the destination address (5 cycles), and then the 10h command to the command register. After 10h is written, R/B# goes LOW, while the control logic automatically programs the new page. The READ STATUS command and bit 6 of the status register can be used instead of the R/B# line to determine when the WRITE is complete. Bit 0 of the status register indicates whether the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written, along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figure 26 on page 44 and Figure 27 on page 44).

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Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that exceeds the minimum required ECC.

If a RESET (FFh) command is issued during a PROGRAM for INTERNAL DATA MOVE (85h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed could become invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

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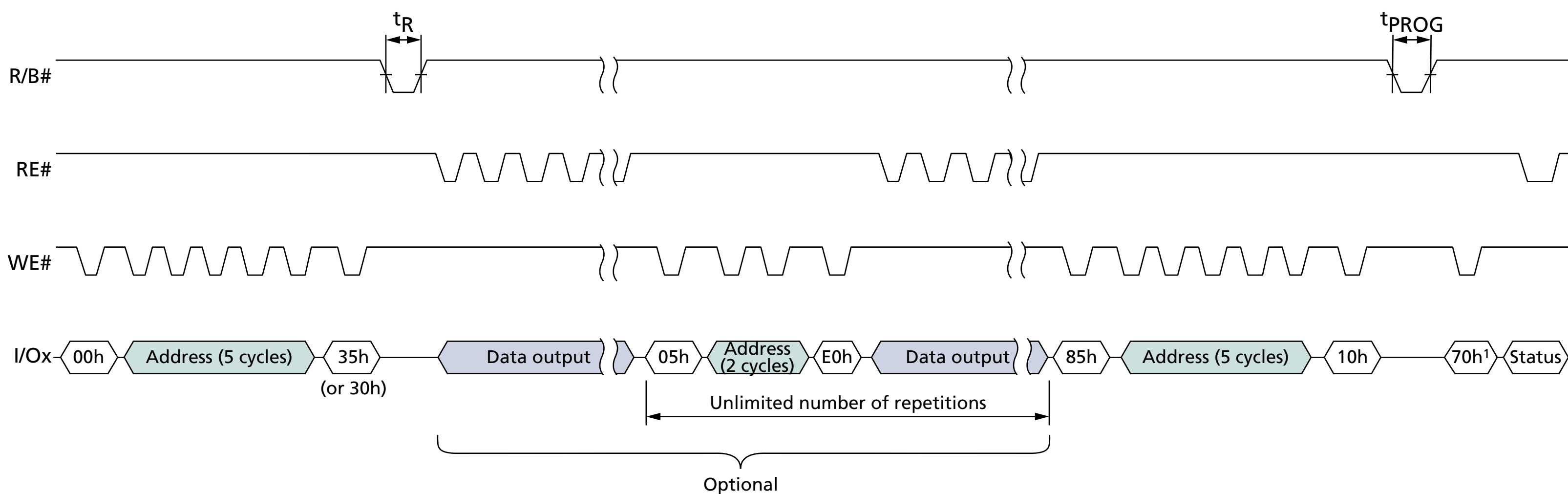
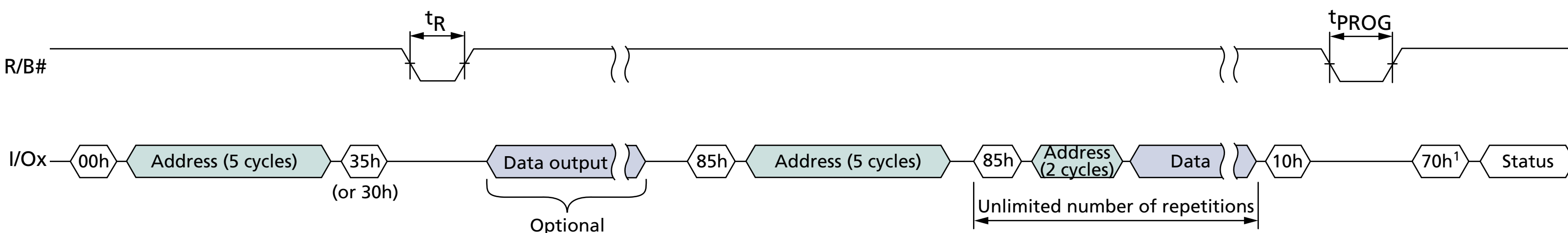
Figure 26: INTERNAL DATA MOVE



Notes: 1. Command can be 70h or 78h
2. The RANDOM DATA INPUT (85h) command supports 2 or 5 address cycles.

Figure 27: INTERNAL DATA MOVE with Optional Data Output and RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h
2. The RANDOM DATA INPUT (85h) command supports 2 or 5 address cycles.

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BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

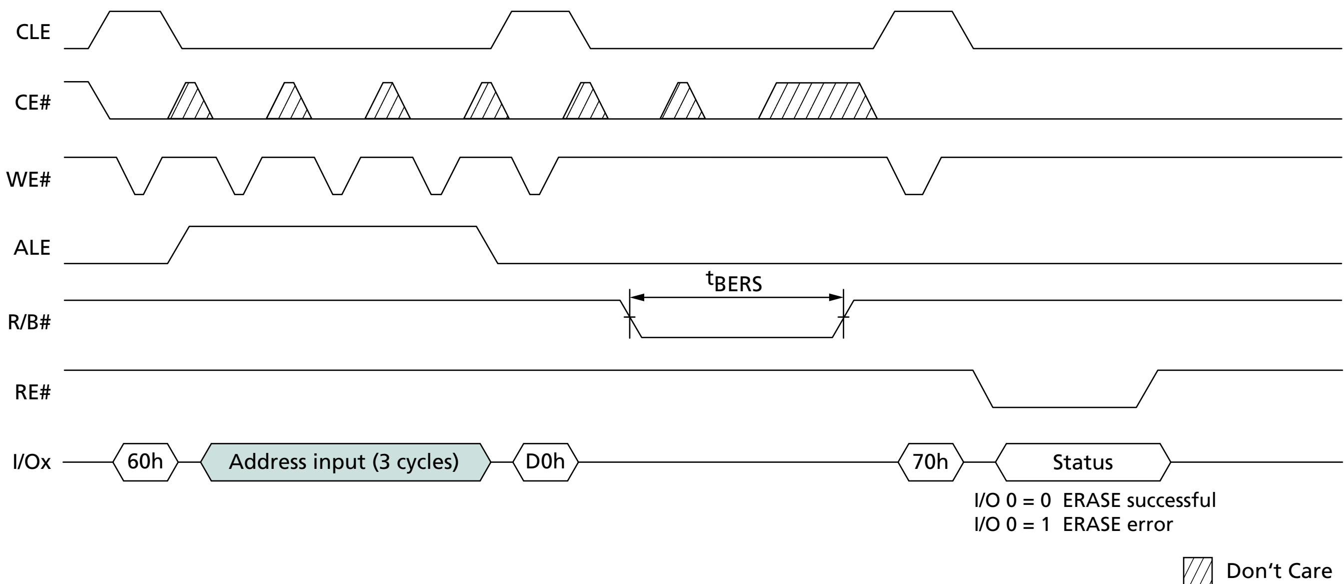
Erasing occurs at the block level. For example, the MT29F32G device has 8192 erase blocks, organized into 128 pages per block and 4314 bytes per page (4096 + 218 bytes). Each block is 539K bytes (512K + 27K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 28).

To erase a block, write 60h to the command register. Then write 3 address cycles containing the row address; the page address is ignored. Finish by writing D0h to the command register.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then 3 address cycles are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW, and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h) command can be used to check error status. When bit 6 = 1, the ERASE operation is complete. Bit 0 indicates a pass/fail condition where 0 = pass (see Figure 28, and Table 11 on page 37).

Figure 28: BLOCK ERASE Operation



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Features Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to alter default NAND Flash device power-on behaviors. These commands use a 1-byte feature address to determine which subfeature parameters are to be read or modified. Each feature address (in the range of 00h to FFh) is defined in Table 12 on page 47.

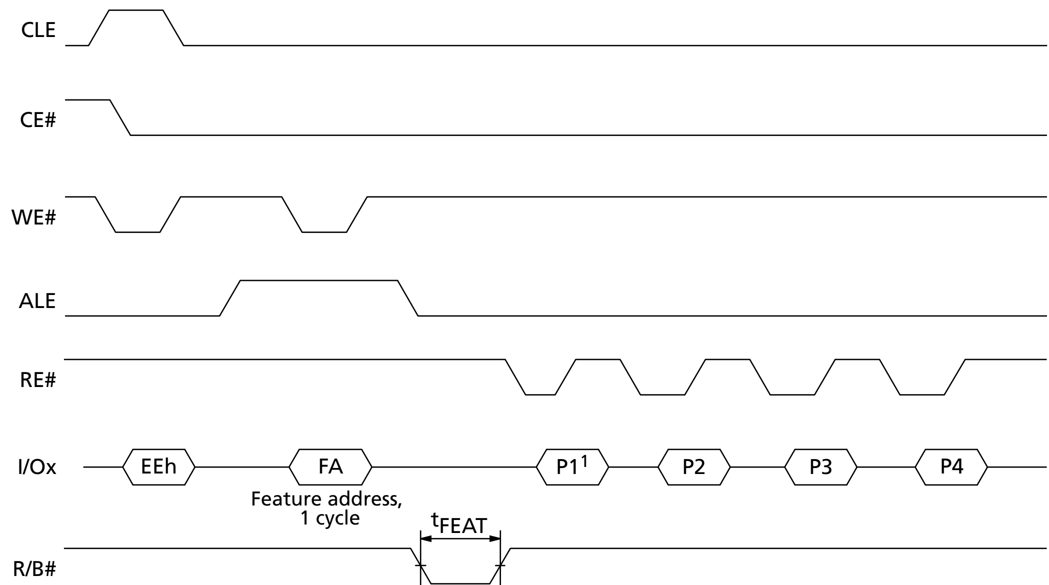
The GET FEATURES command reads the subfeature parameters (P1–P4) at the specified feature address. The SET FEATURES (EFh) command places subfeature parameters (P1-P4) at the specified feature address. Feature settings are volatile and by default persist until the device is power-cycled. It is volatile. Unless otherwise specified in the features table, after a device feature is set, the feature remains set, even if a RESET (FFh) command is issued.

GET FEATURES EEh

The GET FEATURES command is used to retrieve a stored feature. P1–P4 are the parameters for the specified feature address (FA). If a P1–P4 parameter has values defined as reserved, the device must return a 0 for all bits in the parameters so defined.

R/B# goes LOW while the subfeature parameters are being loaded from the specified feature address (^{t}FEAT). The READ STATUS (70h) command is available during the busy time and before data output. Bits 6 and 5 of the status register will reflect the state of R/B#. After reading the status, issue the 00h command to resume reading from the feature address. The 70h command is prohibited while reading subfeature parameters. The device will repeatedly output the same 4 bytes of data if the host continues to toggle RE#.

Figure 29: GET FEATURES (EEh)



Notes: 1. P1–P4 are the subfeature parameters read from the specified feature address (FA).

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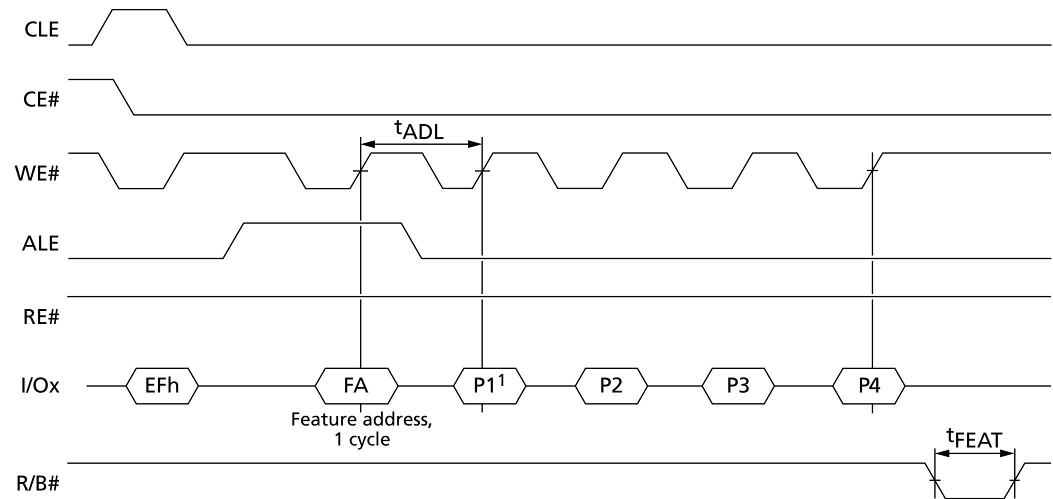
SET FEATURES EFh

The SET FEATURES command is used to set the subfeature parameters at a specified feature address. These parameters are stored in the device until the device is powered down. The subfeature parameters are applied to all die on the CE# to which this command is issued. Figure 30 depicts SET FEATURES behavior and timing.

R/B# goes LOW for ^{t}FEAT, while the subfeature parameters are written to the specified feature address. All four subfeature parameters must be issued to the device for the SET FEATURES command to work. The READ STATUS (70h) command and the RESET (FFh) command are the only valid commands during SET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Figure 30: Set Features (EFh)



Notes: 1. P1–P4 are the subfeature parameters written to the specified feature address (FA).

Table 12: Features Table

Feature Address	Description
00h	Reserved
01h	Timing mode
02h–0Fh	Reserved
10h	Programmable I/O drive strength
11h–7Fh	Reserved
80h	Programmable I/O drive strength
81h	Programmable R/B# pull-down strength
82h-FFh	Reserved

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Table 13: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing Mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1
	Mode 1	Reserved (0)					0	0	1	01h	
	Mode 2	Reserved (0)					0	1	0	02h	
	Mode 3	Reserved (0)					0	1	1	03h	
	Mode 4	Reserved (0)					1	0	0	04h	
	Mode 5	Reserved (0)					1	0	1	05h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Notes: 1. The timing-mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands as well as address and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power-cycled. Supported timing modes are reported in the parameter page.

Table 14: Feature Address 10h and 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarter	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Notes: 1. The programmable drive strength is used to change the default I/O strength. Drive strength should be selected based on the expected loading of the memory bus. This table shows the four supported output drive-strength settings. The default drive strength is full strength. The device returns to the default setting when power-cycled. AC timing parameters must be relaxed if the I/O drive strength is not set to full.

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Table 15: Feature Address 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarter	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Notes: 1. The programmable R/B# pull-down strength is used to change the R/B# pull-down strength. Pull-down strength should be selected based on the expected loading of R/B#. This table shows the four supported pull-down settings. The default setting is full strength. The device returns to the default setting when power-cycled.

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TWO-PLANE Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 4314-byte data register, a 4314-byte cache register, and a 4096-block NAND Flash array. Two-plane commands make better use of the NAND Flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, thus significantly improving system performance.

Two-Plane Addressing

Two-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit, BA7, must be different for each address.
- The most significant block address bit, BA20, for 128Gb devices, must be identical for both addresses.
- The page address bits, PA[6:0], must be identical for both addresses.

TWO-PLANE PAGE READ 00h-00h-30h

TWO-PLANE PAGE READ (00h-00h-30h) command is similar to PAGE READ (00h-30h) command. It transfers two pages of data from the NAND Flash array to the data registers. Each page must be from a different plane on the same die.

To enter TWO-PLANE PAGE READ mode, write the 00h command to the command register, then write 5 address cycles for plane 0 (BA7 = 0). Next, write the 00h command to the command register, then write 5 address cycles for plane 1 (BA7 = 1). Finally, issue the 30h command. The first-plane and second-plane addresses must meet the two-plane addressing requirements; they must also have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# returns HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternatively, the READ STATUS (70h) command can monitor the data transfers. When the transfers are complete, status register bit 6 is set to 1. To read data from one of the two planes, the user must first issue the TWO-PLANE RANDOM DATA READ (06h-E0h) command followed by 5 address cycles (see “TWO-PLANE RANDOM DATA READ 06h-E0h” on page 51). To read out data from the plane and column address specified with the TWO-PLANE RANDOM DATA READ command, pulse RE# repeatedly. When the data cycle is complete, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the other plane. To output data beginning at the specified column address, pulse RE# repeatedly.

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is supported during and following a TWO-PLANE PAGE READ operation. The same die to which the TWO-PLANE PAGE READ command was issued must remain selected when data is read out from the NAND Flash device. Otherwise, the data read out will be invalid data for the TWO-PLANE PAGE READ command issued. A die can be selected by issuing a TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command to any valid address location on a die.

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TWO-PLANE RANDOM DATA READ 06h-E0h

The TWO-PLANE RANDOM DATA READ (06h-E0h) command selects a plane and column address from which to read data after a TWO-PLANE PAGE READ (00h-00h-30h) command.

To issue a TWO-PLANE RANDOM DATA READ command, issue the 06h command, then 5 address cycles, followed by the E0h command. Pulse RE# repeatedly to read data from the new plane beginning at the specified column address.

The primary purpose of the TWO-PLANE RANDOM DATA READ command is to select a new plane and column address within that plane. If a new plane does not need to be selected, then it is possible to use the RANDOM DATA READ (05h-E0h) command instead (see “RANDOM DATA READ 05h–E0h” on page 24).

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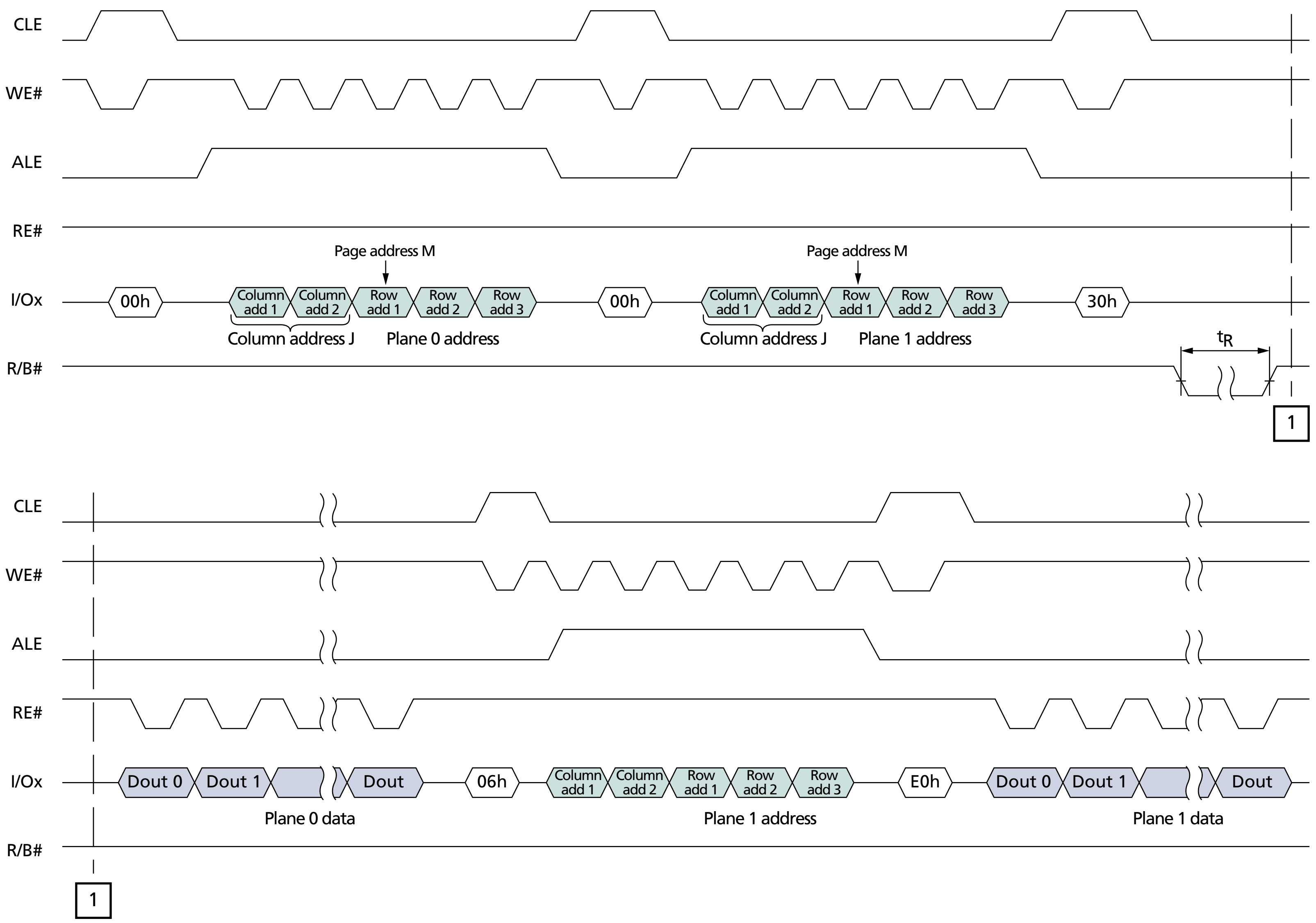
Figure 31: TWO-PLANE PAGE READ



Notes: 1. Column and page addresses must be the same.
2. The least-significant block address bit must be different for the first and second-plane addresses.

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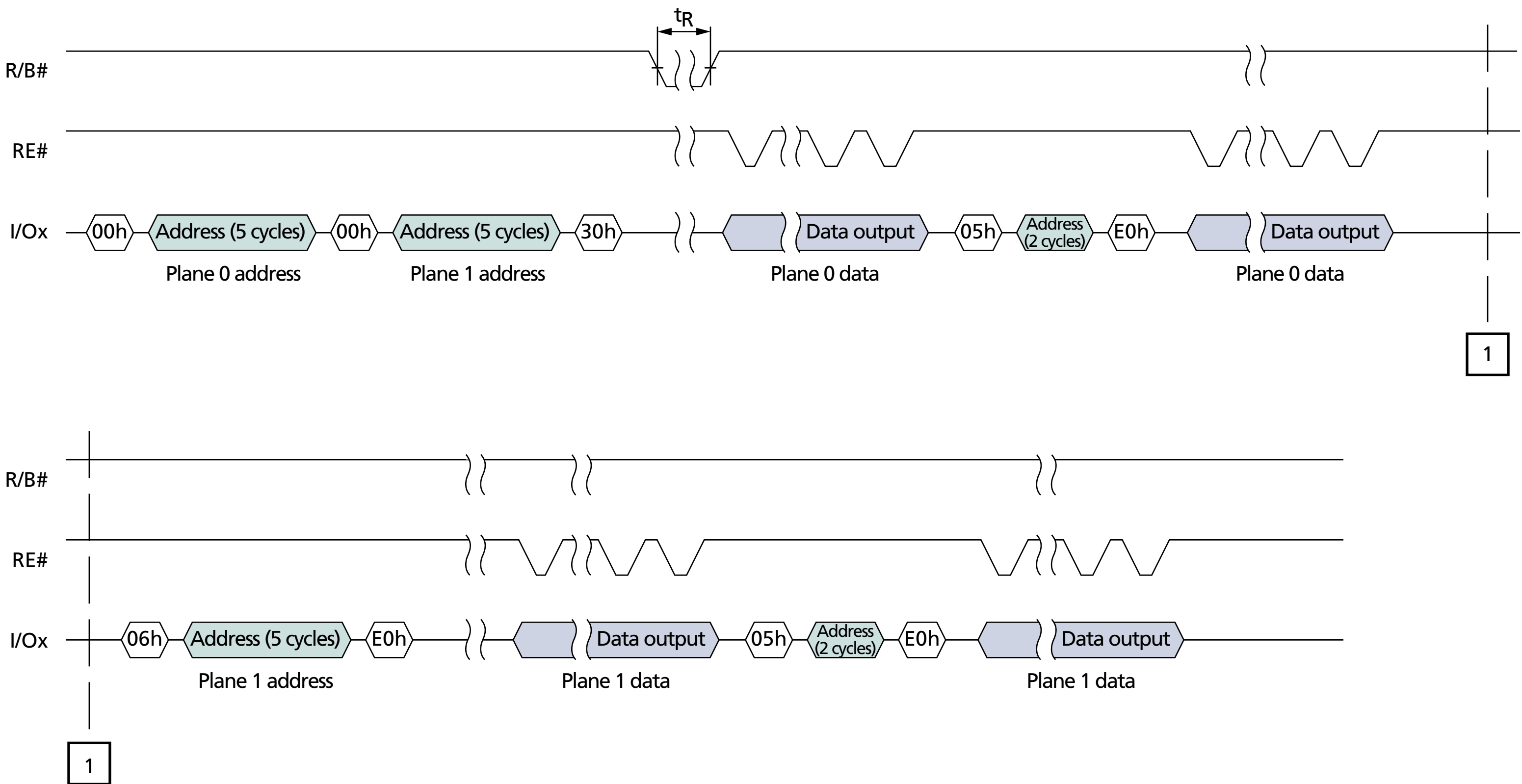
Figure 32: TWO-PLANE PAGE READ with RANDOM DATA READ



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TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h

The TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command is similar to the PROGRAM PAGE (80h-10h) command. It programs two pages of data from the data registers to the NAND Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first-plane address and the second-plane address must meet the two-plane addressing requirements (see “Two-Plane Addressing” on page 50).

To begin the TWO-PLANE PROGRAM PAGE operation, write the 80h command to the command register; write 5 address cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a dummy command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, and then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register; write 5 address cycles to the second plane; then write the data. The PROGRAM (10h) command is written after the second-plane data input is complete.

After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. WRITE verification detects only 1s that are not successfully written to 0s.

R/B# goes LOW for the duration of the array programming time (^{t}PROG). When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}PROG are READ STATUS (70h), TWO-PLANE/MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed could become invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

When the device is ready, if the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = 1), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operation failed.

During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane. Figure 33 on page 55 shows TWO-PLANE PROGRAM PAGE operation.

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Figure 33: TWO-PLANE PROGRAM PAGE

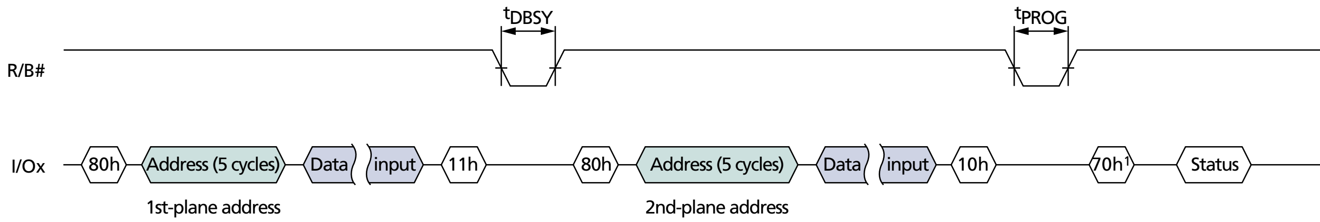
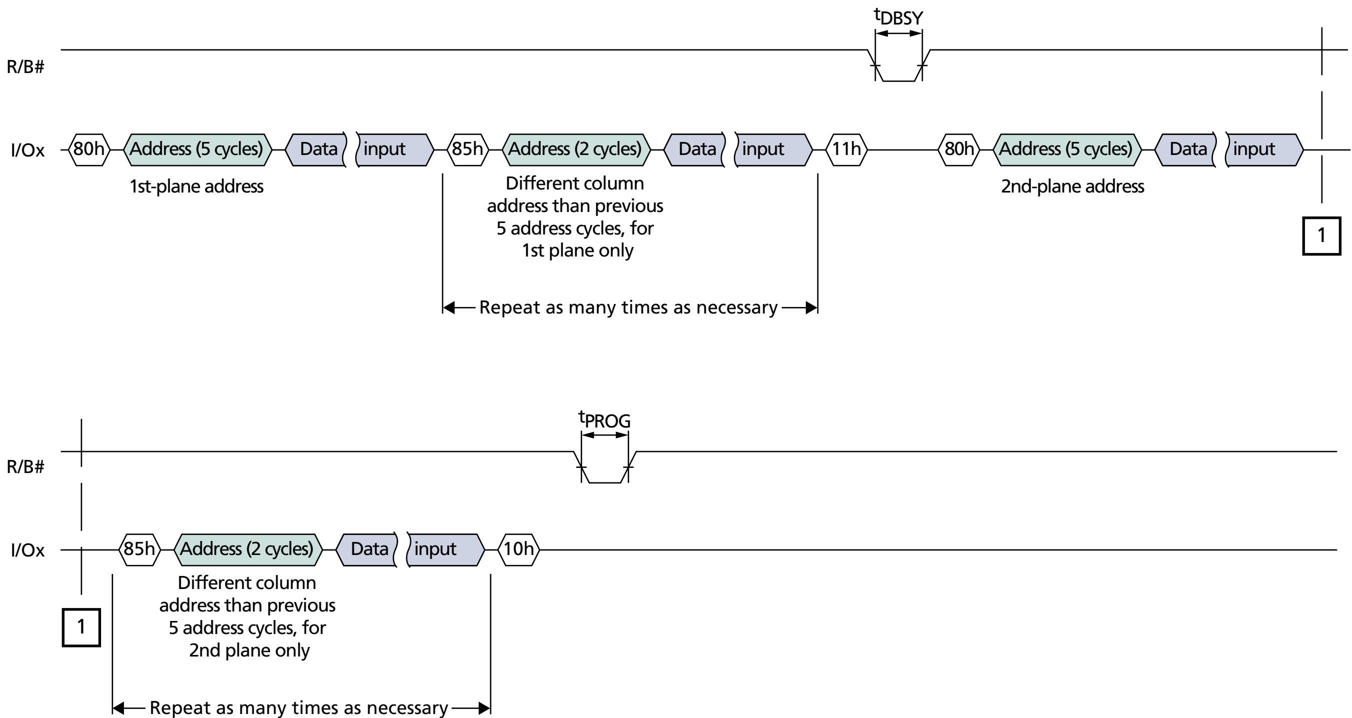


Figure 34: TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT



Notes: 1. The RANDOM DATA INPUT (85h) command supports 2 or 5 address cycles.

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TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h

TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command is similar to the PROGRAM PAGE CACHE MODE (80h-15h) command. It cache-programs two pages of data from the data registers to the NAND Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first-plane and second-plane addresses must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 50).

To begin TWO-PLANE PROGRAM PAGE CACHE MODE, write the 80h command to the command register, write 5 address cycles for the first plane, and then write the data. Serial data is loaded on consecutive WE# cycles starting at the specified address. Next, write the 11h command. The 11h command is a dummy command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register, write 5 address cycles for the second plane, then write the data. The CACHE PROGRAM (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers, and R/B# returns HIGH, memory array programming to both planes begins.

When R/B# returns HIGH, new data can be written to the cache registers by issuing another TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) sequence. The time that R/B# stays LOW (^{t}CBSY) is determined by the actual programming time of the previous operation. For the first cache operation, the duration of ^{t}CBSY is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent TWO-PLANE PROGRAM PAGE CACHE MODE operations, transfer from the cache registers to the data registers is delayed until the current data registers' contents have been programmed into the arrays.

If the R/B# pin is used to determine programming completion, the last operation of the program sequence must use the TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command instead of the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command. If the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command is used for the last operation, then use READ STATUS (70h) to monitor the operation's progress. Status register bit 5 indicates when programming is complete. See Table 11 on page 37 for status register details.

To determine when the current TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) operation has completed, issue the READ STATUS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 or bit 1 = 1, indicating a failed operation, then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which current or previous plane operation failed. For more information on status register bit definitions, see Table 11 on page 37.

During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane.

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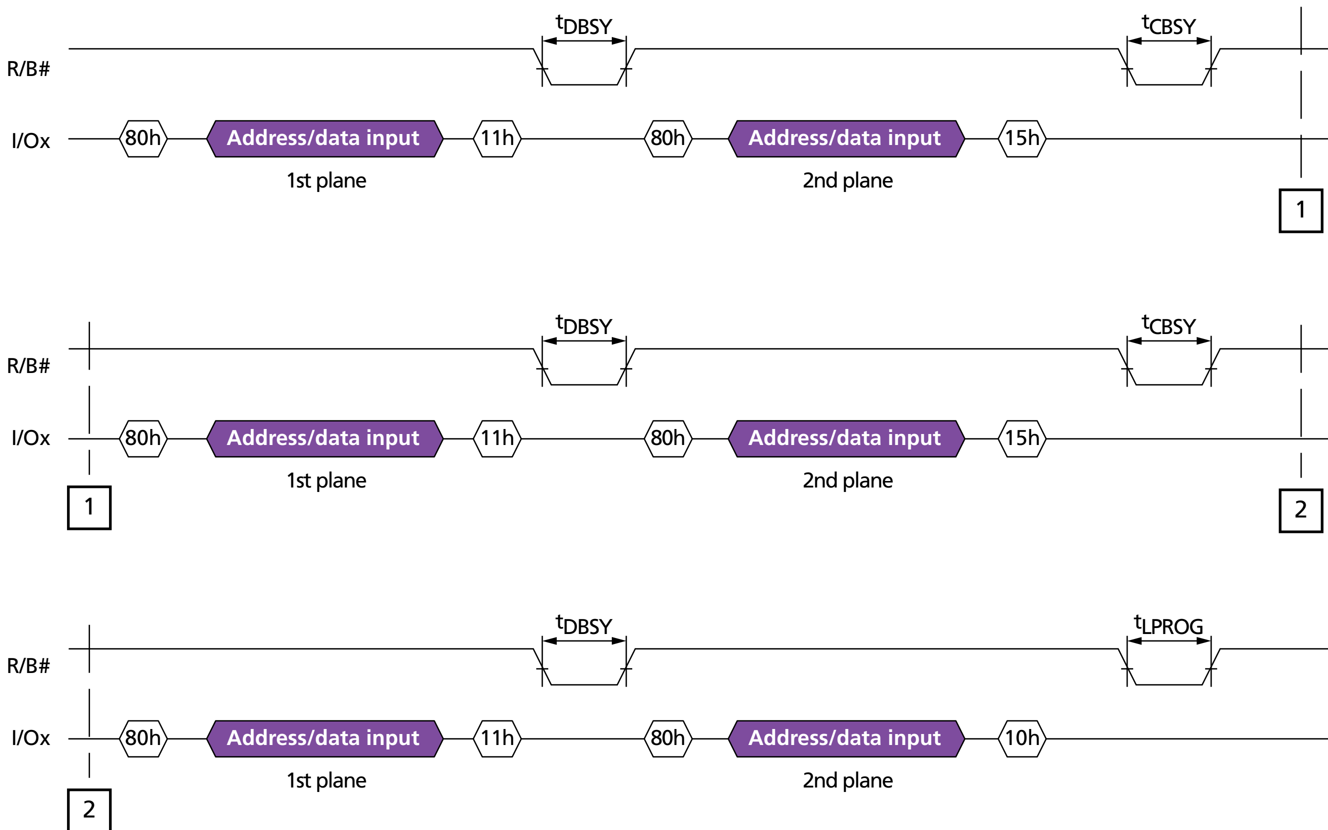
If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE CACHE MODE operation while R/B# is LOW or bit 5 or bit 6 of the status register is LOW, the data in the shared memory cells being programmed could become invalid. Interruption of a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 35: TWO-PLANE PROGRAM PAGE CACHE MODE



TWO-PLANE INTERNAL DATA MOVE 00h-00h-35h/85h-11h-85h-10h

A TWO-PLANE INTERNAL DATA MOVE command is similar to the INTERNAL DATA MOVE command, and requires two sequences. Issue a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command first, then the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. Data moves are supported only within the planes from which data is read. The first-plane and second-plane addresses must meet the two-plane addressing requirements for both the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) and TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) commands (see "Two-Plane Addressing" on page 50).

TWO-PLANE READ for INTERNAL DATA MOVE 00h-00h-35h

The TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is used in conjunction with the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. First, write 00h to the command register, and then write the first-

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plane internal source address (5 cycles). Again, write 00h to the command register, followed by the second-plane internal source address (5 cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for ^{t}R, while two pages are read into their respective cache registers.

After a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is issued, the data transferred from the source pages into the cache registers can be read out by toggling RE#. Data is output sequentially from the column address originally specified by the TWO-PLANE READ FOR INTERNAL DATA MOVE (00h-00h-35h) command, starting with plane 0.

A TWO-PLANE RANDOM DATA READ (06h-E0h) command can be used to select the data transferred from the source pages of each plane. This command will change the starting column address only on the selected plane. The column address on the plane from which data is moved will remain unchanged from its previous location.

To read out data after the TWO-PLANE READ for INTERNAL DATA MOVE command, issue either TWO-PLANE RANDOM DATA READ (06h-E0h) commands without limit or a combination of TWO-PLANE/MULTIPLE-DIE READ STATUS and RANDOM DATA READ (05h-E0h) commands.

The memory device is now ready to accept the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

Alternatively, two READ for INTERNAL DATA MOVE (00h-35h) commands can be issued, each addressing different planes on the same die, prior to issuing the TWO PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

Alternatively, a TWO-PLANE PAGE READ (00h-00h-30h) command can be issued, prior to issuing the TWO PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-85h-10h

After the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command has been issued, and R/B# goes HIGH (or the status register bit 6 is 1), the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first-plane destination address (5 cycles), and then write 11h to the command register. The 11h command is a dummy command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, and then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 85h command to the command register, then write the second-plane destination address (5 cycles), and then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

R/B# goes LOW for the duration of array programming time, ^{t}PROG. When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}PROG are READ STATUS (70h), TWO-PLANE/MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

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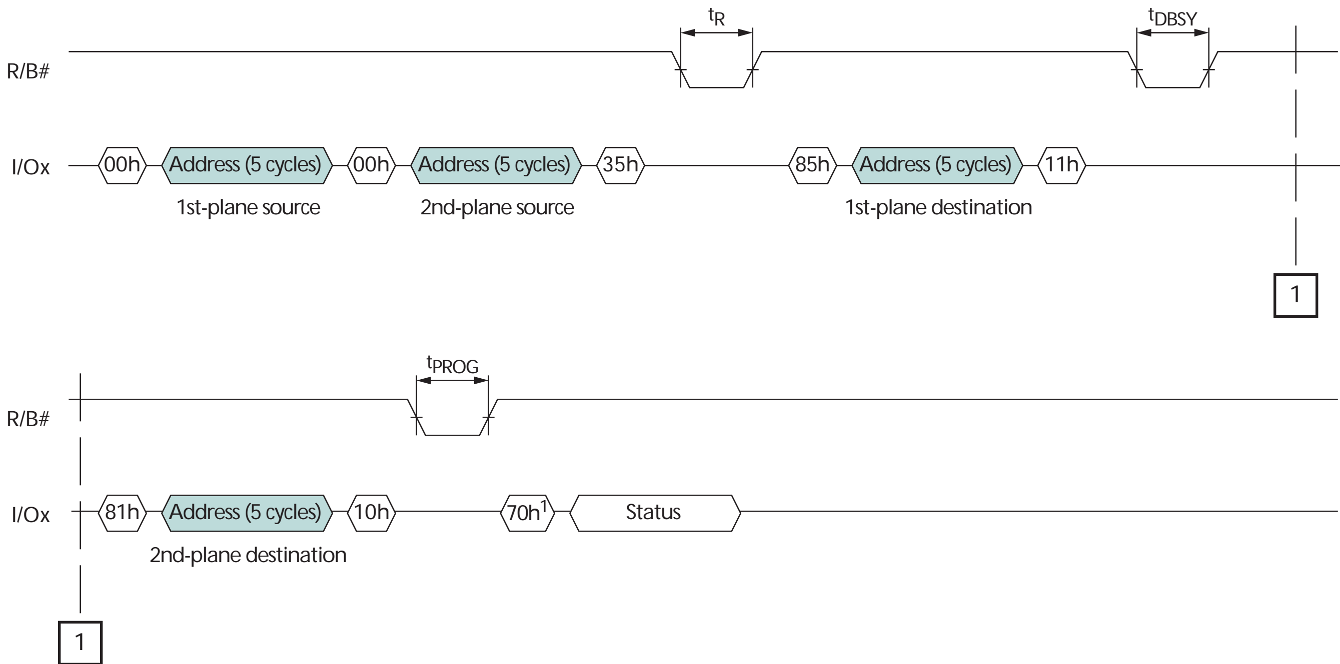
If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) operation while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = 1), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operation failed.

During the serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane (see Figure 38 on page 61).

Figure 36: TWO-PLANE INTERNAL DATA MOVE



Notes: 1. Command can be 70h or 78h.

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Figure 37: TWO-PLANE INTERNAL DATA MOVE with TWO-PLANE RANDOM DATA READ

R/B#
RE#
I/Ox
tR
00h
Address (5 cycles)
00h
Address (5 cycles)
35h
Data output
06h
Address (5 cycles)
E0h
1st-plane source
2nd-plane source
(or 30h)
Data from 1st-plane source
2nd-plane source address
1

R/B#
RE#
I/Ox
Data output
05h
Address (2 cycles)
E0h
Data output
1
Data from
2nd-plane source
2nd-plane
source column address
Data from 2nd-plane source
from new column address
2
Optional

R/B#
RE#
I/Ox
tDBSY
tPROG
85h
Address (5 cycles)
11h
85h
Address (5 cycles)
10h
70h[1]
Status
2
1st-plane destination
2nd-plane destination

Notes: 1. Command can be 70h or 78h.

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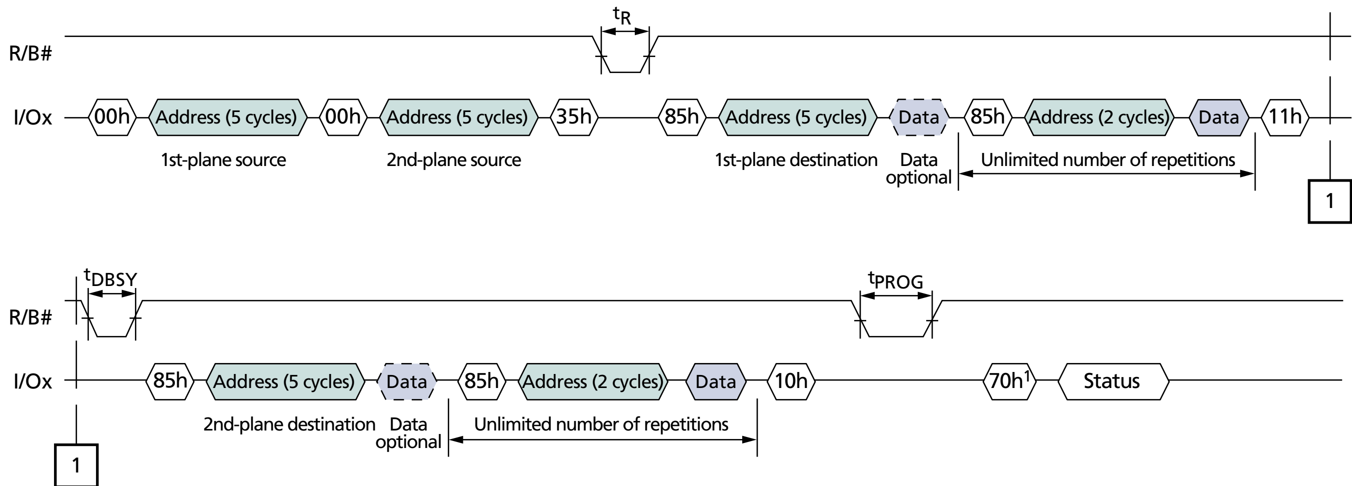
Figure 38: TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT



Notes:
1. Command can be 70h or 78h.
2. The RANDOM DATA INPUT (85h) command supports 2 or 5 address cycles.

TWO-PLANE BLOCK ERASE 60h-D1h-60h-D0h

The TWO-PLANE BLOCK ERASE (60h-D1h-60h-D0h) command is similar to the BLOCK ERASE (60h-D0h) command. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first-plane and second-plane addresses must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 50).

Begin a TWO-PLANE BLOCK ERASE operation by writing 60h to the command register, followed by 3 address cycles of the first-plane block address. Next, write the D1h command. The D1h command is a dummy command. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command indicates that the device is ready when the status register bit 6 is set to 1. The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 60h command to the command register, followed by 3 address cycles for the second plane. Finally, issue the D0h command.

R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erasure is complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}BERS are READ STATUS (70h), TWO-PLANE/MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = 1), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operation failed.

Alternatively, the D1h command can be omitted. In this case, there is no ^{t}DBSY time.

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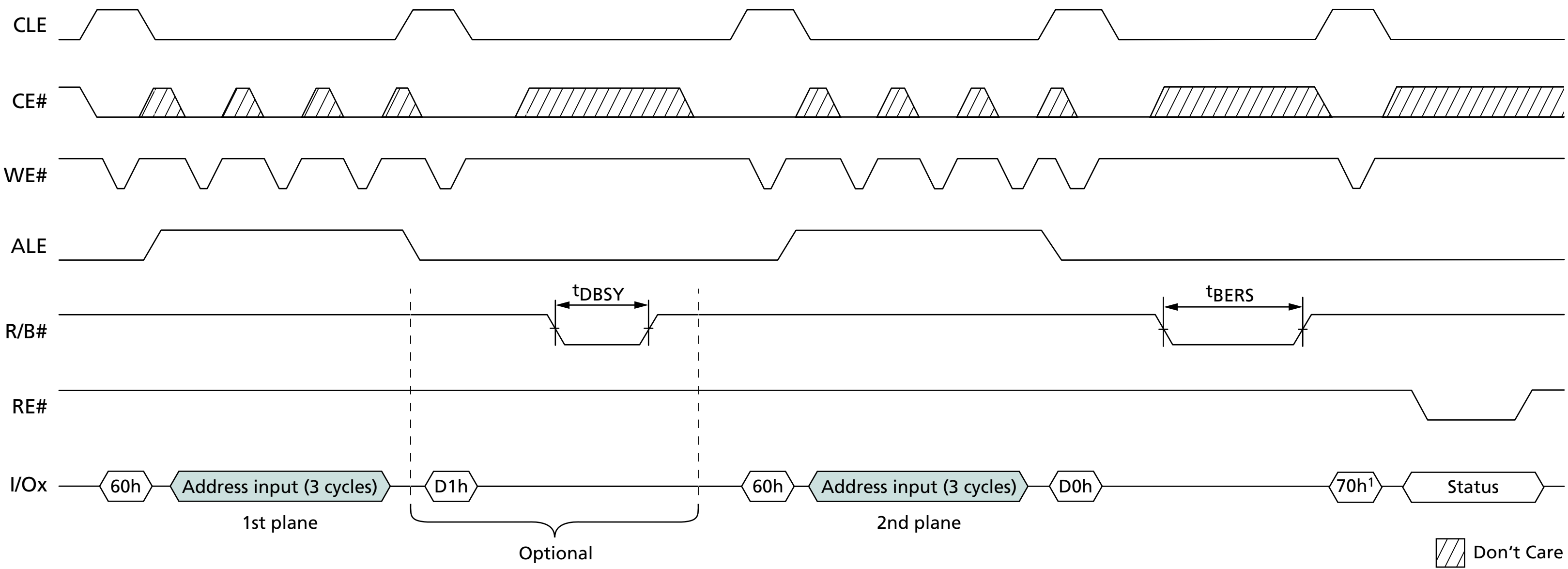
Figure 39: TWO-PLANE BLOCK ERASE Operation



Note: Command can be 70h or 78h.

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TWO-PLANE/MULTIPLE-DIE READ STATUS 78h

In Micron two-plane NAND Flash devices where one or more die in a package share the same CE# pin, it is possible to poll the status register of a particular plane and die independently using the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. This feature operates regardless of device size, organization, or status. This command can be used to check status during and after two-plane operations and to check the status of PROGRAM and ERASE operations interleaved between two die sharing the same CE# pin.

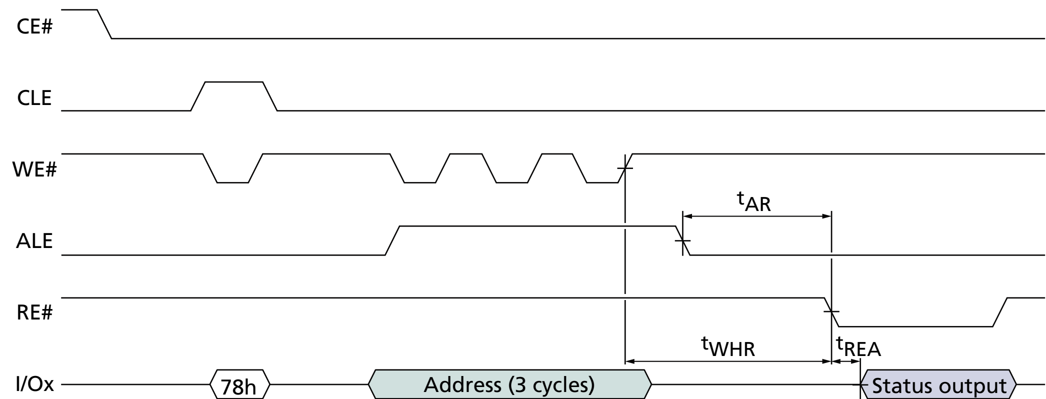
After the 78h command is issued, the device requires 3 address cycles containing the block and page addresses BA[20:7] and PA[6:0]. The most significant block address bit in the third address cycle (BA20) selects the proper die, and the least significant block address bit in the first address cycle (BA7) selects the proper plane within that die.

After the 78h command and the 3 address cycles, the status register is output on I/O[7:0] when RE# is LOW. Changes in the status register will be indicated on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to issue a new READ STATUS command to indicate these changes. The status register bit definitions are identical to those reported by the READ STATUS command (see Table 11 on page 37).

In devices with more than one die sharing a common CE# pin, when one die is not busy (status register bit 5 is 1), it is possible to initiate a new operation to that die even if the other die is busy. Operations can overlap and occur concurrently on the two die (see "Interleaved Die Operations" on page 69).

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and immediately following power-on and during the first RESET command.

Figure 40: TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



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RESET Operation

RESET FFh

The RESET (FFh) command is used to put the memory device into a known condition and to abort any command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data can be partially erased or programmed, and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are marked invalid.

If a RESET (FFh) command is issued during any type of programming operation (PROGRAM PAGE, PROGRAM PAGE CACHE MODE, PROGRAM for INTERNAL DATA MOVE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, or TWO-PLANE PROGRAM for INTERNAL DATA MOVE) while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting any programming operation on one page could corrupt the data in another page within the block being programmed.

The status register contains the value E0h when WP# is HIGH; otherwise, it is written with a 60h value. R/B# goes low for ^{t}RST after the RESET command is written to the command register (see Figure 41 and Table 16 on page 64).

The RESET command must be issued as the first command to all CE#s after power-on. The device will be busy for a maximum of 1ms. During and following the initial RESET command, and prior to issuing the next command, use of the TWO PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited.

If the RESET command is issued during or following an interleaved-die operation, then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be issued, one time per die, to determine completion of the RESET operation. Use of the READ STATUS (70h) command is not supported until the 78h command is issued.

Figure 41: RESET Operation

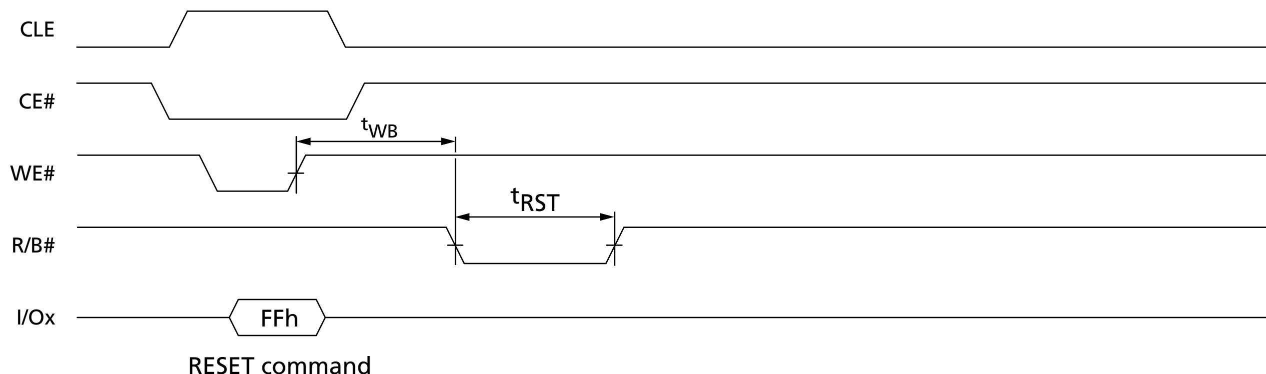

Table 16: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

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WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using the WP# pin. Figures 42 through 53 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, the WP# pin must not be toggled until the command is complete and the device is ready (status register bit 5 is 1).

Figure 42: ERASE Enable

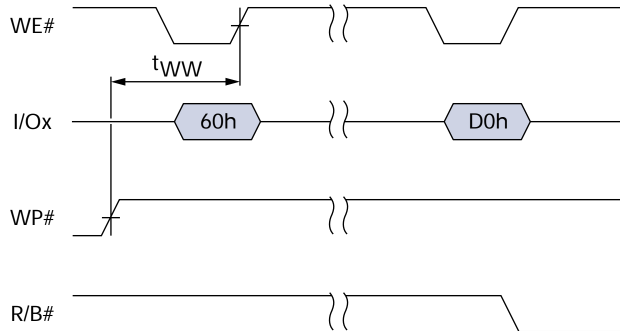

Figure 43: ERASE Disable

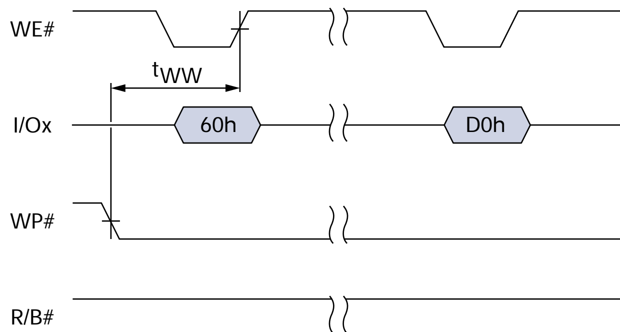

Figure 44: PROGRAM Enable

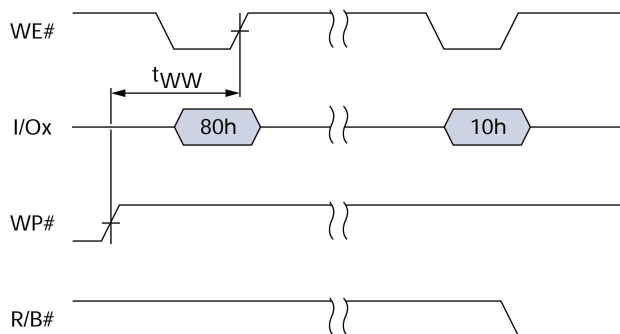

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Figure 45: PROGRAM Disable

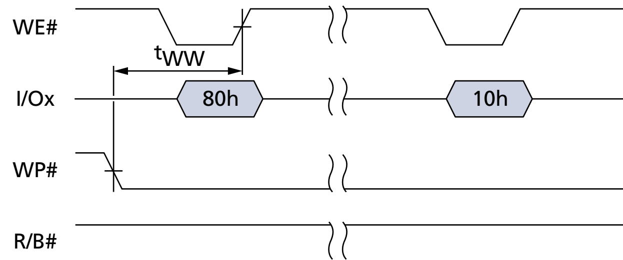

Figure 46: PROGRAM IDM Enable

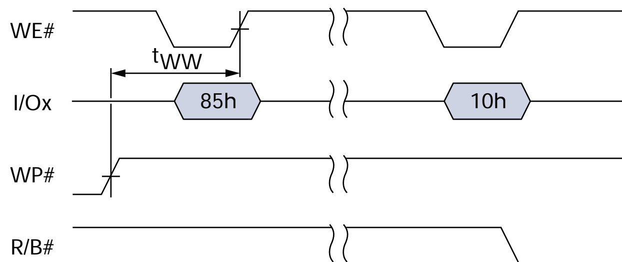

Figure 47: PROGRAM IDM Disable

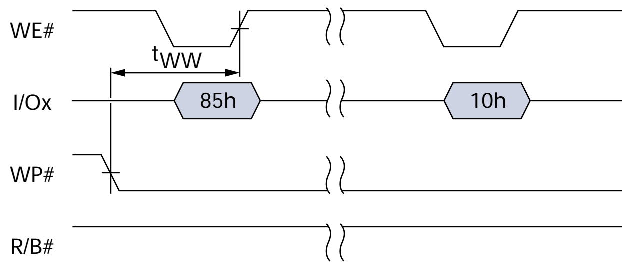

Figure 48: Two PLANE ERASE Enable

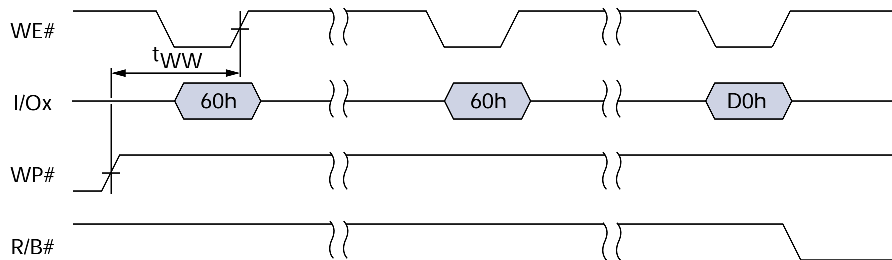

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Figure 49: Two PLANE ERASE Disable

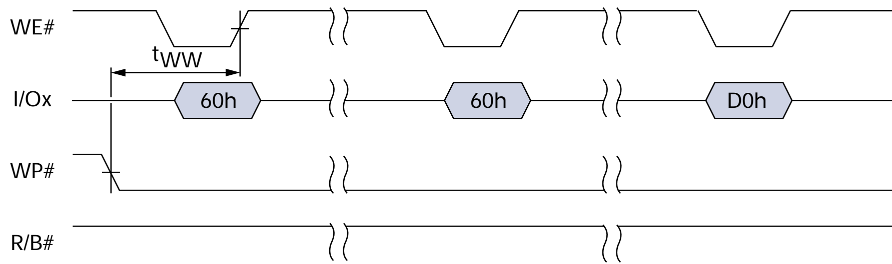

Figure 50: Two PLANE PROGRAM Enable

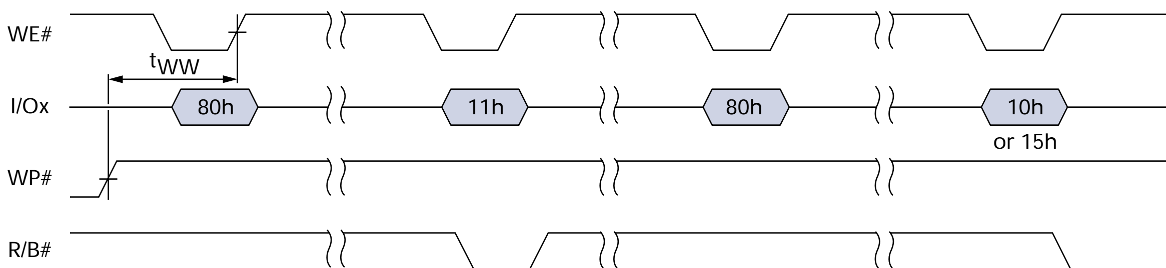

Figure 51: Two PLANE PROGRAM Disable

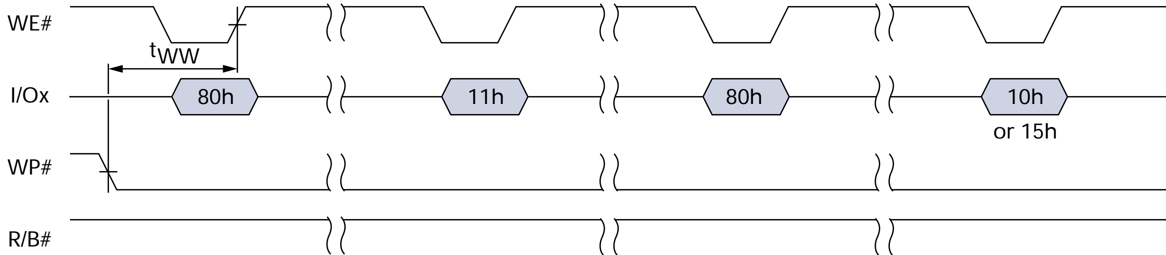

Figure 52: Two PLANE PROGRAM IDM Enable

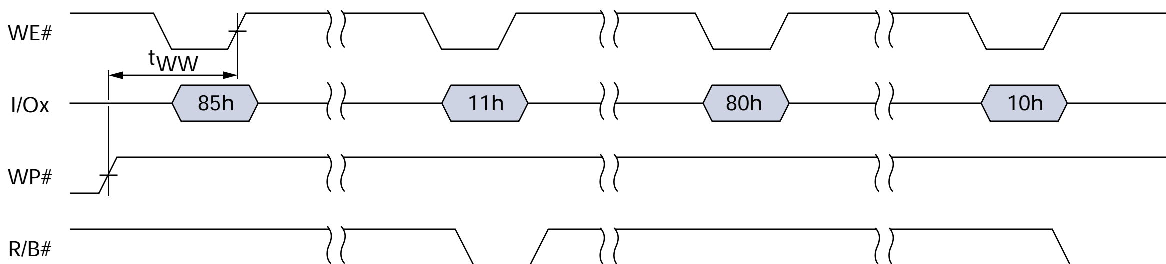

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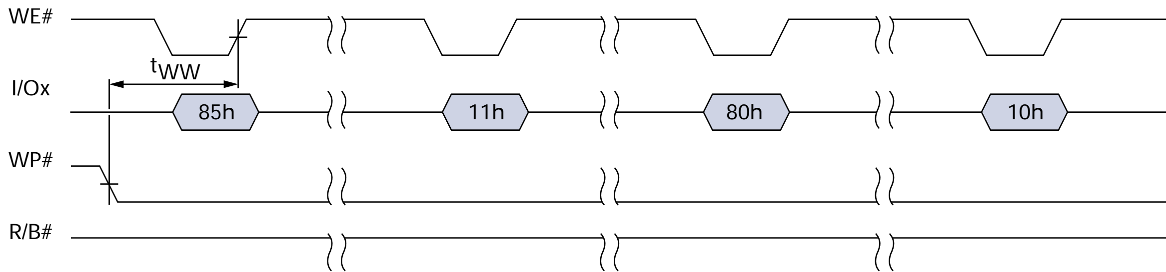
Figure 53: Two PLANE PROGRAM IDM Disable



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Interleaved Die Operations

In devices with more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is 1), issue a command to the first die. Then, while the first die is busy (R/B# is LOW), issue a command to the other die.

There are two methods to determine operation completion. The R/B# signal indicates when both die have finished their operations. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command can report the status of each die individually. If a die is performing a cache operation, such as PROGRAM PAGE CACHE MODE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h), that die can accept data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

During and following interleaved die operations, the READ STATUS (70h) command is prohibited. Instead, use the 78hcommand to monitor status. These commands select which die will report status. Interleaved two-plane commands must also meet the requirements in "Two-Plane Addressing" on page 50.

PAGE READ, TWO-PLANE PAGE READ, PROGRAM PAGE, PROGRAM PAGE CACHE MODE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, READ for INTERNAL DATA MOVE, TWO-PLANE READ for INTERNAL DATA MOVE, PROGRAM for INTERNAL DATA MOVE, TWO-PLANE PROGRAM for INTERNAL DATA MOVE, BLOCK ERASE, and TWO-PLANE BLOCK ERASE can be used in any combination as interleaved operations on separate die sharing a common CE#.

In interleaved PROGRAM and READ operations, the PROGRAM operation must be issued before the READ operation. The data from the READ operation must be read out before the next PROGRAM operation begins.

Interleaved PAGE READ Operations

Interleaved PAGE READ operations are shown in Figure 54 on page 70.

During interleaved PAGE READ operations, a TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is required before reading data from either die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h command. A TWO-PLANE RANDOM DATA OUPUT (06h-E0h) command can also be used to select a die after the die has finished its PAGE READ operation. This ensures that no bus contention occurs between any die.

RANDOM DATA OUTPUT (05h-E0h) commands are supported during interleaved PAGE READ operations.

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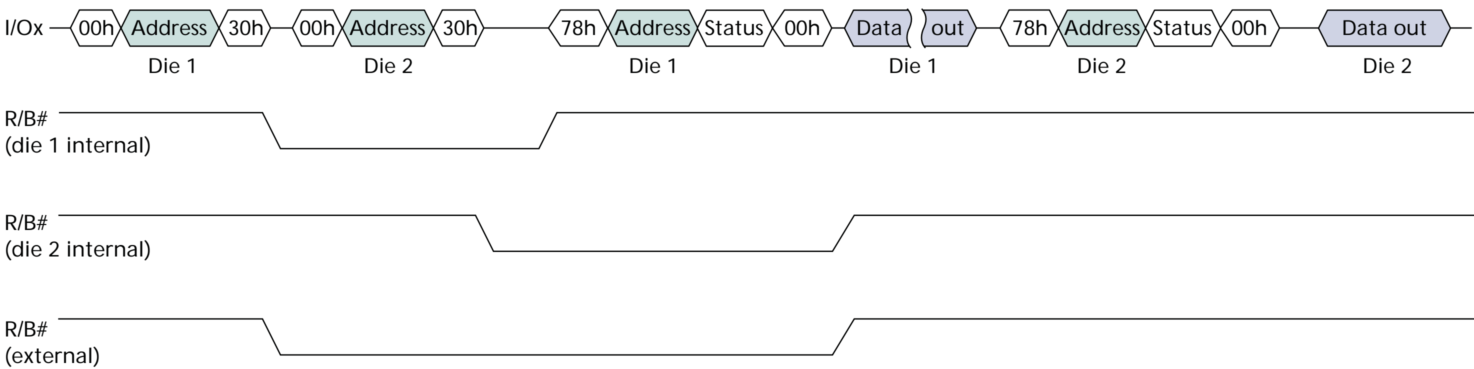
Figure 54: Interleaved PAGE READ with Status Register Monitoring



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Interleaved TWO-PLANE PAGE READ Operation

Interleaved TWO-PLANE PAGE READ operations are shown in Figure 55 on page 72. In the figure, the TWO-PLANE/MULITPLE DIE READ STATUS (78h) command is used to monitor the status register for operation completion. When the host has issued TWO-PLANE PAGE READ commands simultaneously to multiple die, the host must issue the TWO-PLANE/MULTIPLE DIE READ STATUS (78h) command before reading data from any die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h command. A TWO-PLANE RANDOM DATA OUPUT (06h-E0h) command can also be used to select a die after the die has finished its TWO-PLANE PAGE READ operation. This ensures that no bus contention occurs between any die.

The interleaved TWO-PLANE PAGE READ operation must meet two-plane addressing requirements (see “Two-Plane Addressing” on page 50).

RANDOM DATA OUTPUT (05h-E0h) is supported during interleaved TWO-PLANE PAGE READ operations to change the column address within a plane. TWO-PLANE RANDOM DATA OUTPUT (06h-E0h) is supported during interleaved TWO-PLANE PAGE READ operations to change planes and column addresses between the planes.

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Figure 55: Interleaved TWO-PLANE PAGE READ with Status Register Monitoring

Note: Two-plane addressing requirements apply.

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Interleaved PROGRAM PAGE Operations

Two types of interleaved PROGRAM PAGE operations are shown in Figures 56 and 57. In Figure 56, the R/B# signal is monitored for operation completion. In Figure 57, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is supported during interleaved PROGRAM PAGE operations.

Figure 56: Interleaved PROGRAM PAGE with R/B# Monitoring

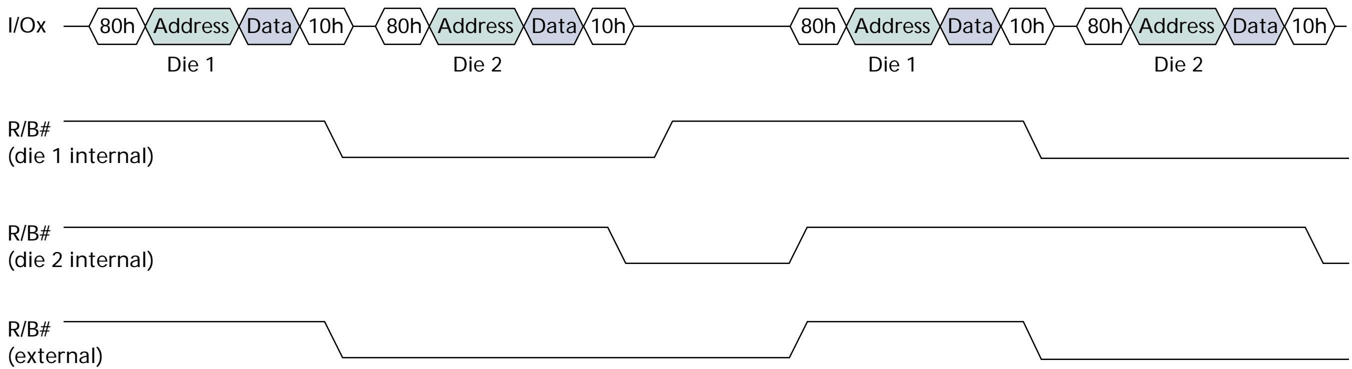
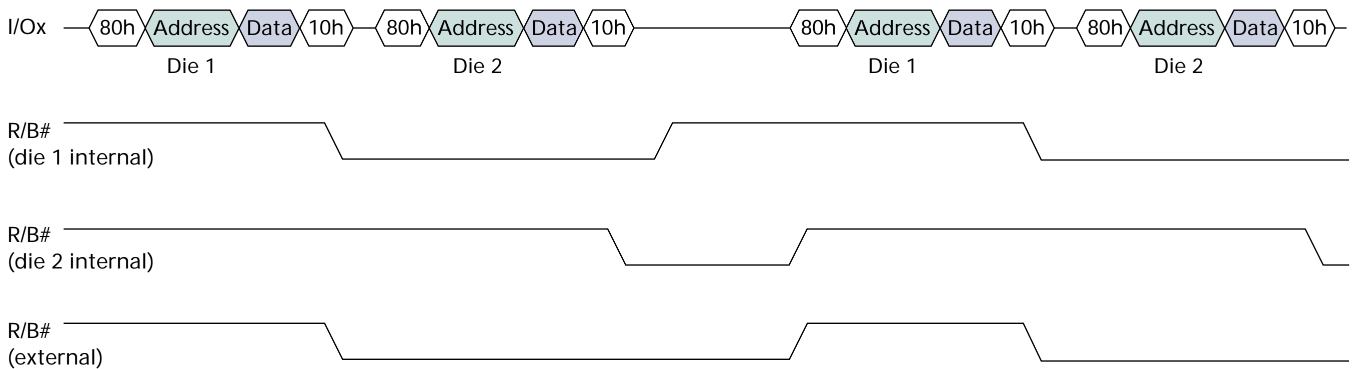


Figure 57: Interleaved PROGRAM PAGE with Status Register Monitoring



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Interleaved PROGRAM PAGE CACHE MODE Operations

Two types of interleaved PROGRAM PAGE CACHE MODE operations are shown in Figures 58 and 58. In Figure 58, the R/B# signal is monitored. In Figure 59, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command.

RANDOM DATA INPUT (85h) is supported during interleaved PROGRAM PAGE CACHE MODE operations.

Figure 58: Interleaved PROGRAM PAGE CACHE MODE with R/B# Monitoring

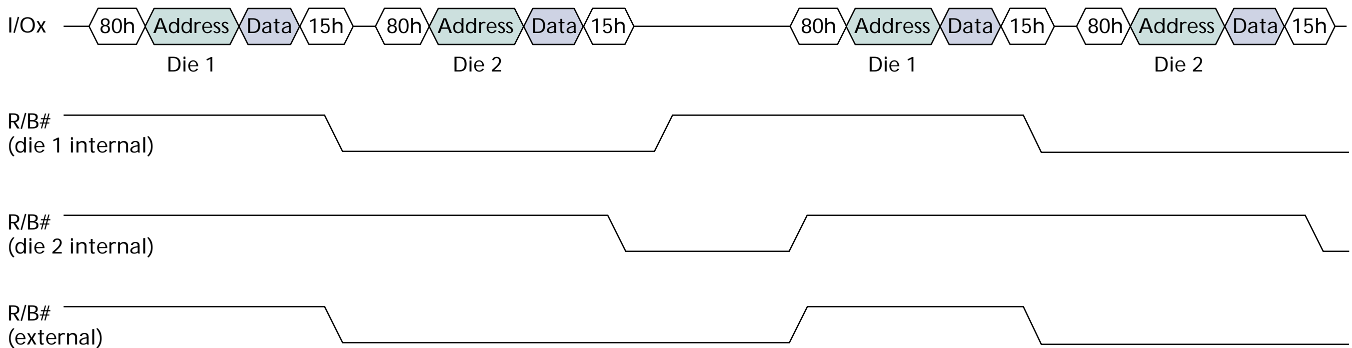
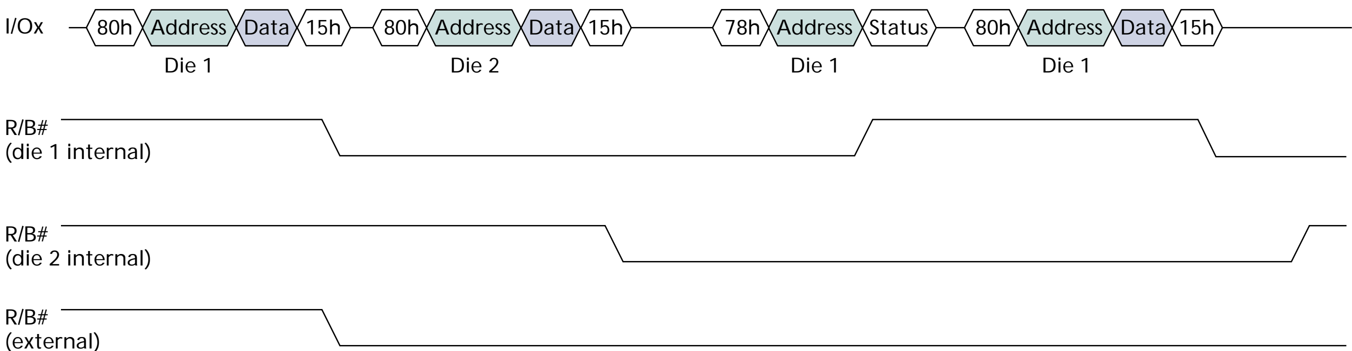


Figure 59: Interleaved PROGRAM PAGE CACHE MODE with Status Register Monitoring



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Interleaved TWO-PLANE PROGRAM PAGE Operation

Two types of interleaved TWO-PLANE PROGRAM PAGE operations are shown in Figure 60 and in Figure 61 on page 76. In Figure 60, the R/B# signal is monitored for operation completion. In Figure 61, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM PAGE operation must meet two-plane addressing requirements (see “Two-Plane Addressing” on page 50).

RANDOM DATA INPUT (85h) is supported during interleaved TWO-PLANE PROGRAM PAGE operations.

Figure 60: Interleaved TWO-PLANE PROGRAM PAGE with R/B# Monitoring

Note: Two-plane addressing requirements apply.

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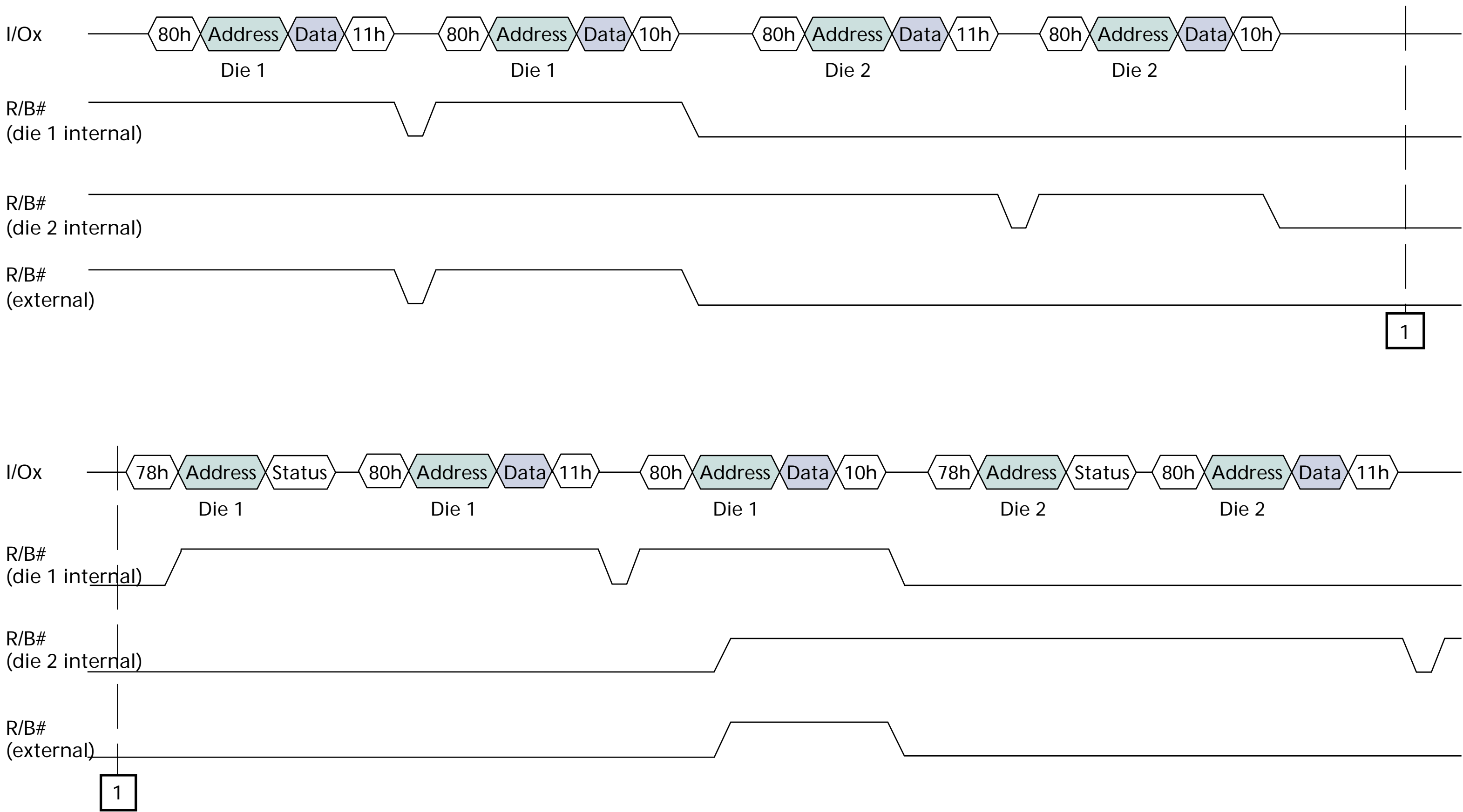
Figure 61: Interleaved TWO-PLANE PROGRAM PAGE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

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Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Operations

Two types of interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations are shown in Figure 62 on page 78, and in Figure 63 on page 79. In Figure 62, the R/B# signal is monitored. In Figure 63, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

The interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation must meet two-plane addressing requirements (see “Two-Plane Addressing” on page 50).

RANDOM DATA INPUT (85h) is supported during interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations.

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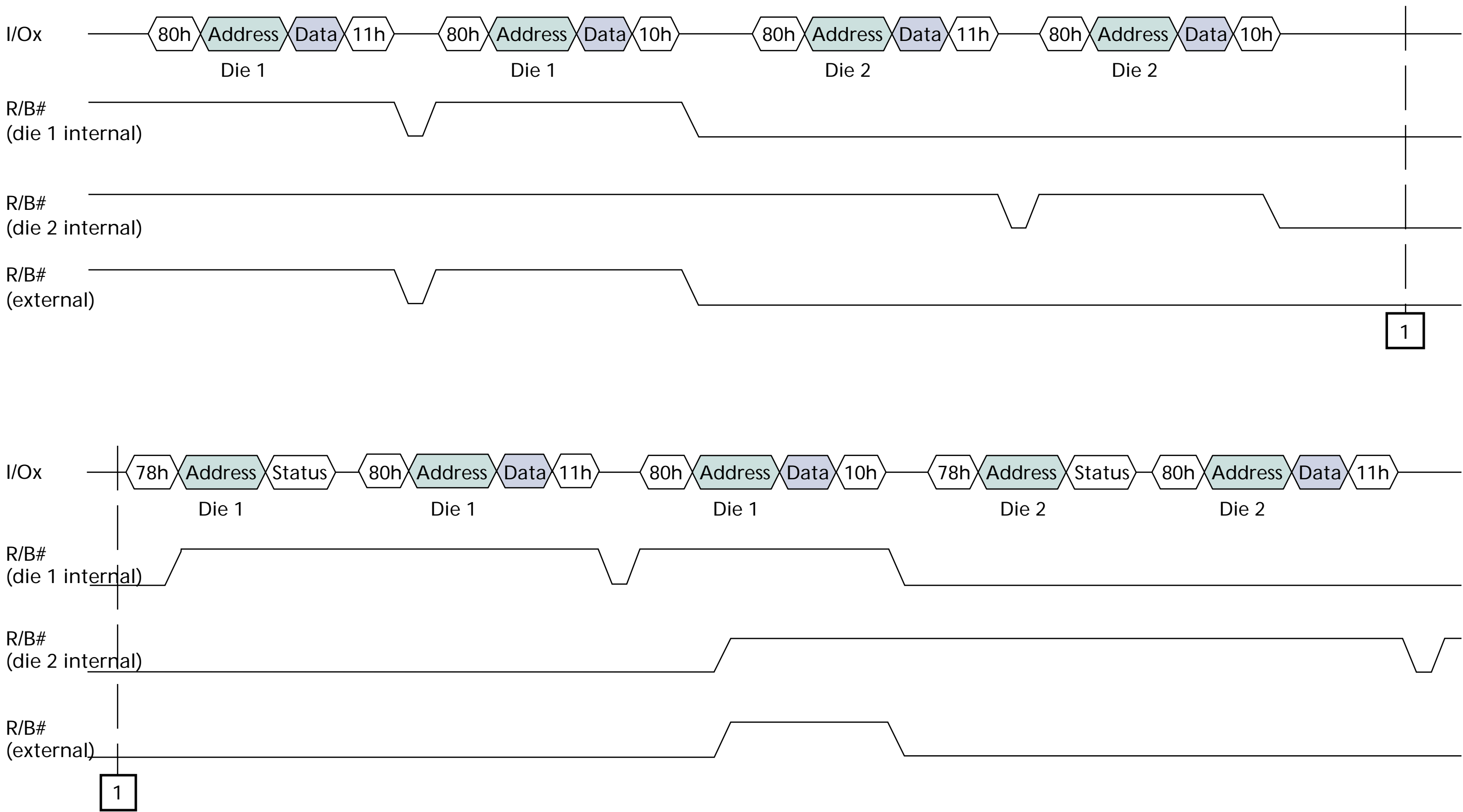
Figure 62: Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with R/B# Monitoring



Note: Two-plane addressing requirements apply.

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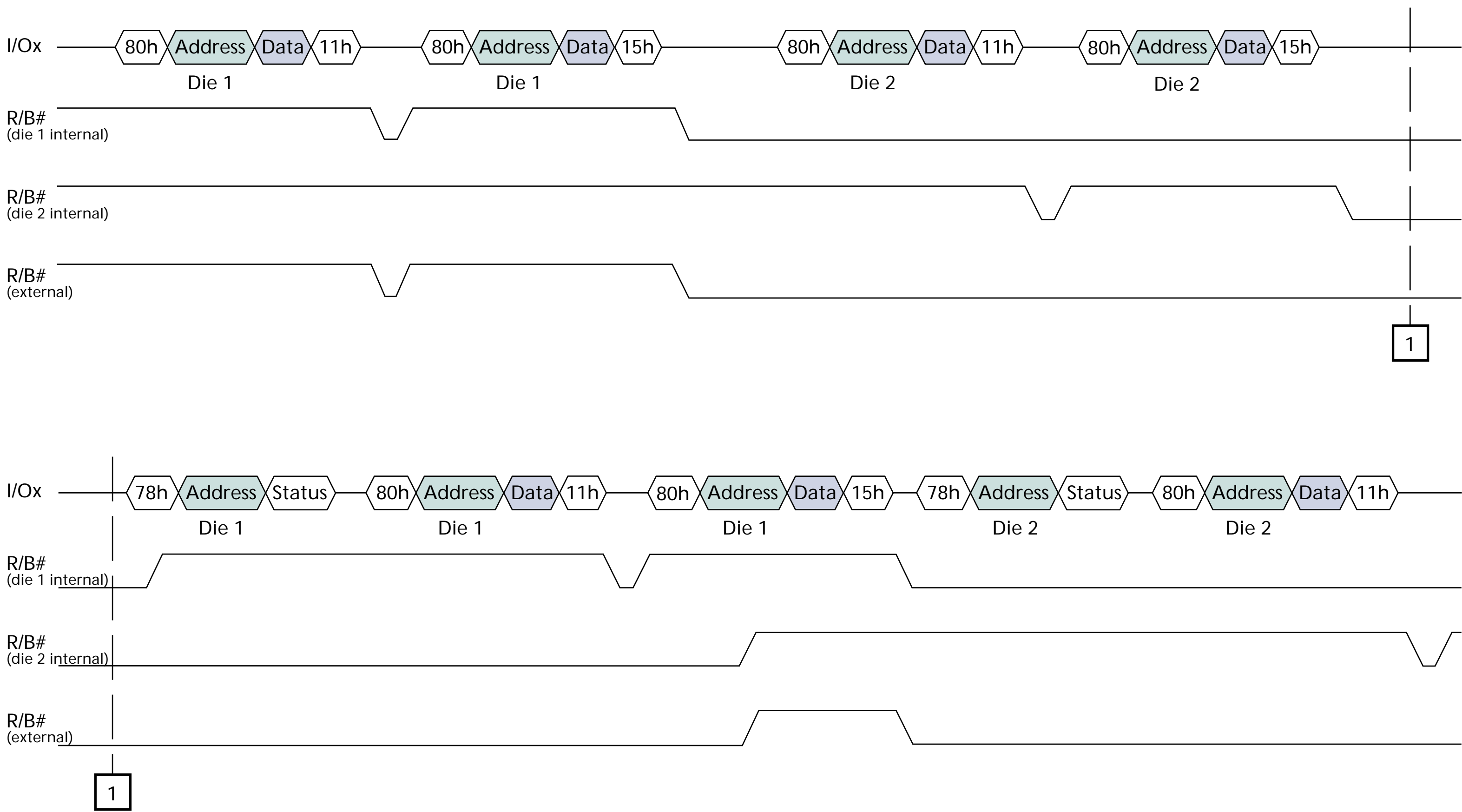
Figure 63: Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

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Interleaved READ for INTERNAL DATA MOVE Operations

Interleaved READ for INTERNAL DATA MOVE operations are shown in Figure 64 on page 81. In the figure, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. When the host has issued READ commands simultaneously to multiple die, the host must issue the TWO-PLANE/MULTIPLE DIE READ STATUS (78h) command before reading data from any die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h command. A TWO-PLANE RANDOM DATA OUPUT (06h-E0h) command can also be used to select a die after the die has finished its READ for INTERNAL DATA MOVE operation. This ensures that no bus contention occurs between any die.

READ for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA OUTPUT (05h-E0h) commands are supported during interleaved READ for INTERNAL DATA MOVE operations.

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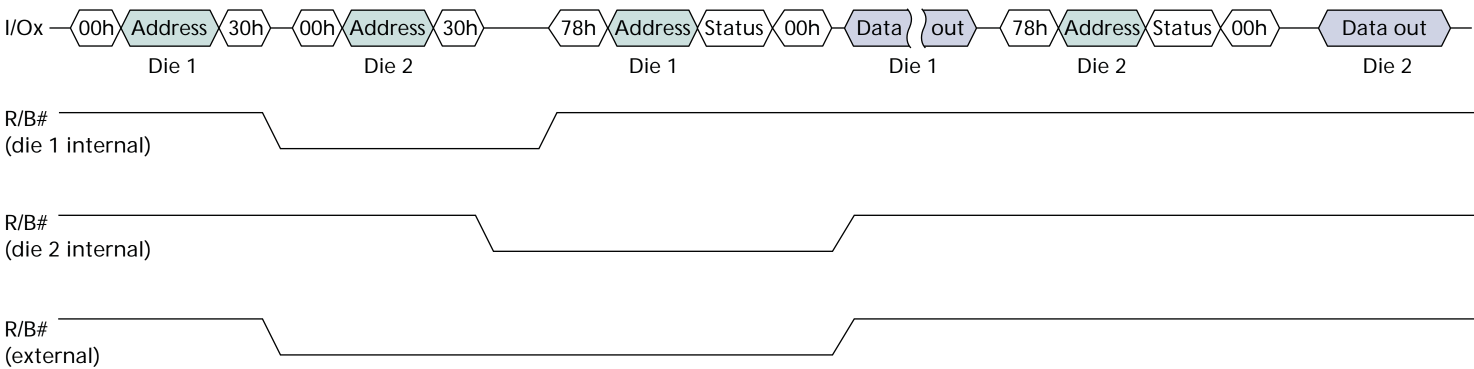
Figure 64: Interleaved READ for INTERNAL DATA MOVE with Status Register Monitoring



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Interleaved TWO-PLANE READ for INTERNAL DATA MOVE Operations

Interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations are shown in Figure 65 on page 83. In the figure, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion. When the host has issued READ commands to multiple die at the same time, the host must issue the TWO-PLANE/MULTIPLE DIE READ STATUS (78h) command before reading data from any die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h command. A TWO-PLANE RANDOM DATA OUPUT (06h-E0h) command can also be used to select a die after the die has finished its READ for INTERNAL DATA MOVE operation. This ensures that no bus contention occurs between any die.

The interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation must meet two-plane addressing requirements (see “Two-Plane Addressing” on page 50). TWO-PLANE READ for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA OUTPUT (05h-E0h) is supported during interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations to change the column address within a plane. TWO-PLANE RANDOM DATA OUTPUT (06h-E0h) is supported during interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations to change planes and column addresses between the planes.

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Figure 65: Interleaved TWO-PLANE READ for INTERNAL DATA MOVE w/Status Register Monitoring

I/Ox: 00h | Address (Die 1) | 00h | Address (Die 1) | 35h | 00h | Address (Die 2) | 00h | Address (Die 2) | 35h | 78h | Address (Die 1) | Status

R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

1

I/Ox: 06h | Address | E0h (Die 1, Plane 0) | Data output (Die 1, Plane 0) | 06h | Address | E0h (Die 1, Plane 1) | Data output (Die 1, Plane 1) | 78h | Address | Status (Die 2)

R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

1 2

I/Ox: 06h | Address | E0h (Die 2, Plane 0) | Data output (Die 2, Plane 0) | 06h | Address | E0h (Die 2, Plane 1) | Data output (Die 2, Plane 1) | 05h | Address | E0h (2 cycles) | Data output (Die 2, Plane 1)

R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

2

Note: Two-plane addressing requirements apply.

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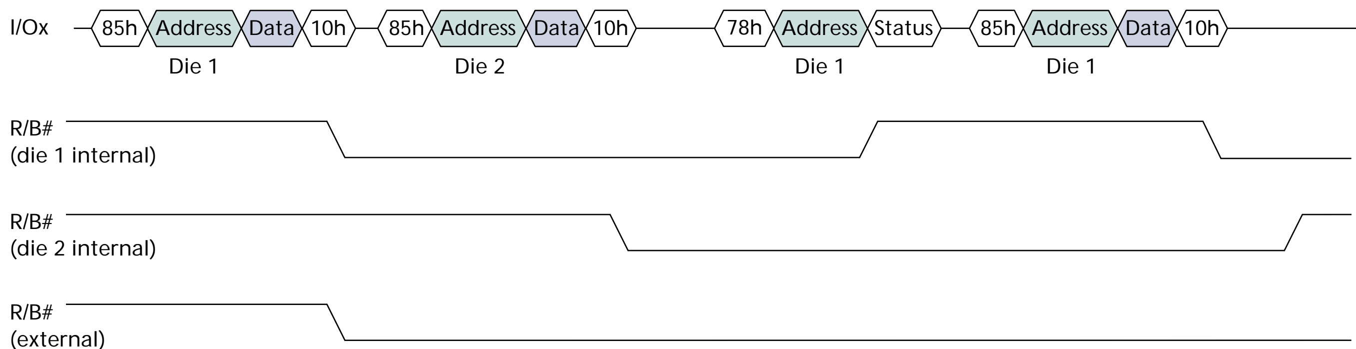
Interleaved PROGRAM for INTERNAL DATA MOVE Operations

Interleaved PROGRAM for INTERNAL DATA MOVE operations are shown in Figure 66. In the figure, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

An interleaved READ for INTERNAL DATA MOVE operation is required before a PROGRAM for INTERNAL DATA MOVE operation can be started (see "Interleaved READ for INTERNAL DATA MOVE Operations" on page 80). PROGRAM for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA INPUT (85h) commands are supported during interleaved PROGRAM for INTERNAL DATA MOVE operations.

Figure 66: Interleaved PROGRAM for INTERNAL DATA MOVE with Status Register Monitoring



Note: A previous interleaved READ for INTERNAL DATA MOVE operation is required.

Interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE Operations

Interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations are shown in Figure 67 on page 85. In the figure, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operation must meet two-plane addressing requirements (see "Two-Plane Addressing" on page 50). TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations must operate within the same plane.

An interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation is required before a TWO-PLANE PROGRAM for INTERNAL DATA MOVE operation can be started (see "Interleaved TWO-PLANE READ for INTERNAL DATA MOVE Operations" on page 82).

RANDOM DATA INPUT (85h) is supported during interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations.

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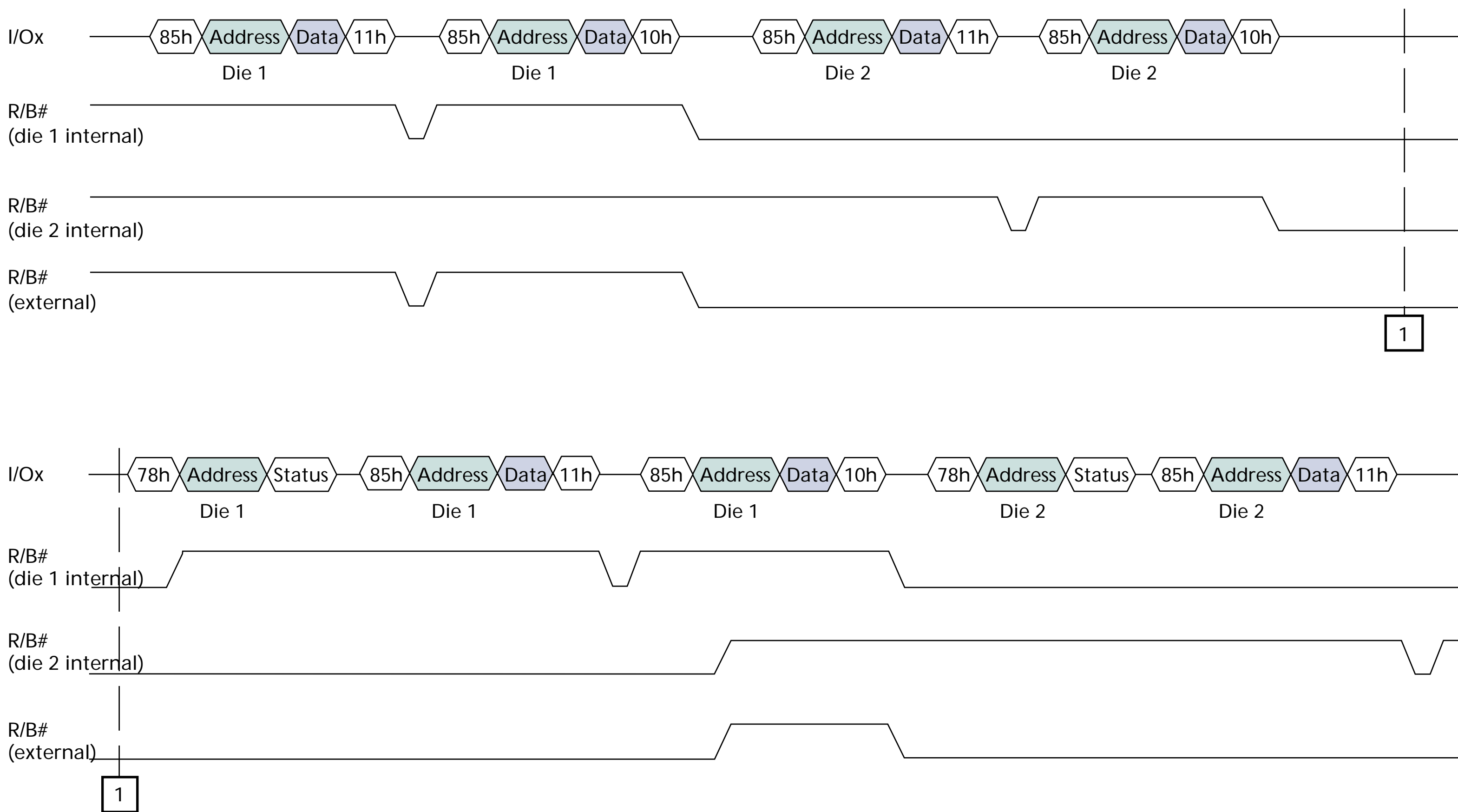
Figure 67: Interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE w/ Status Register Monitoring



Note: A previous interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation is required.

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Interleaved BLOCK ERASE Operations

Two types of interleaved BLOCK ERASE operations are shown in Figures 68 and 69. In Figure 68, the R/B# signal is monitored for operation completion. In Figure 69, theTWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

Figure 68: Interleaved BLOCK ERASE with R/B# Monitoring

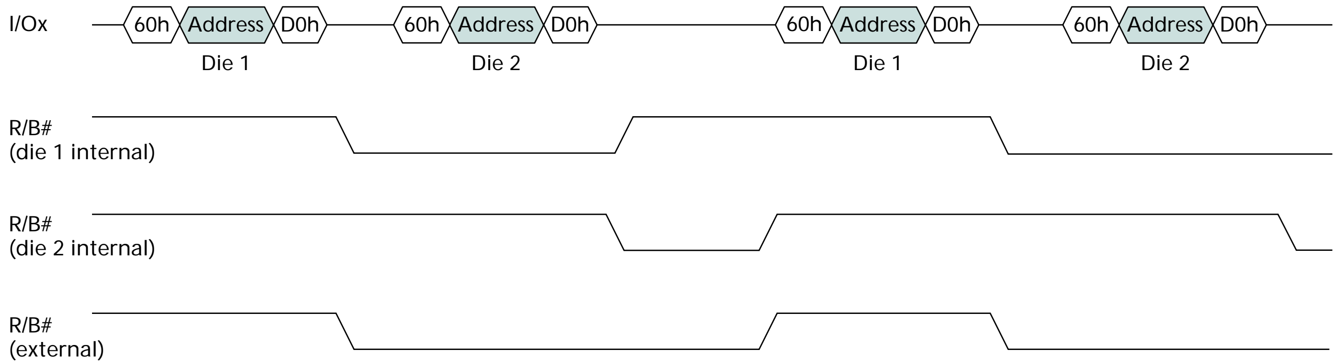
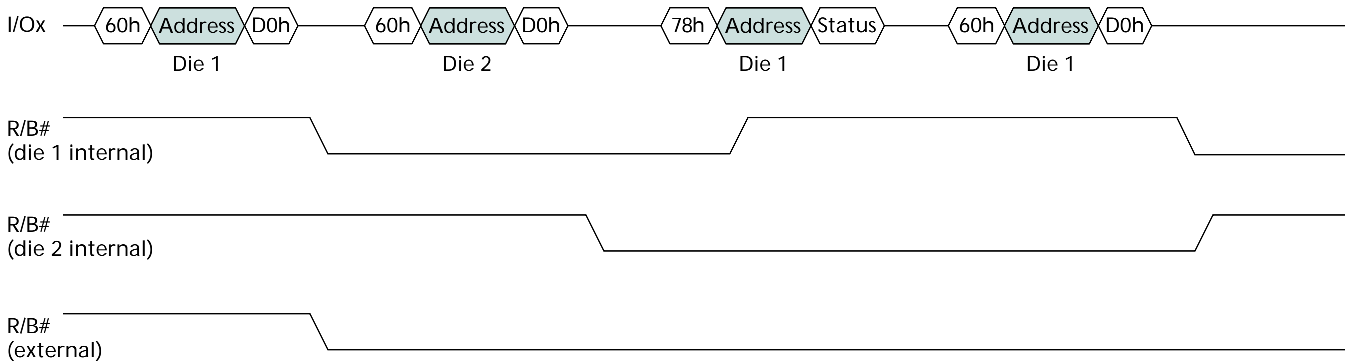


Figure 69: Interleaved BLOCK ERASE with Status Register Monitoring



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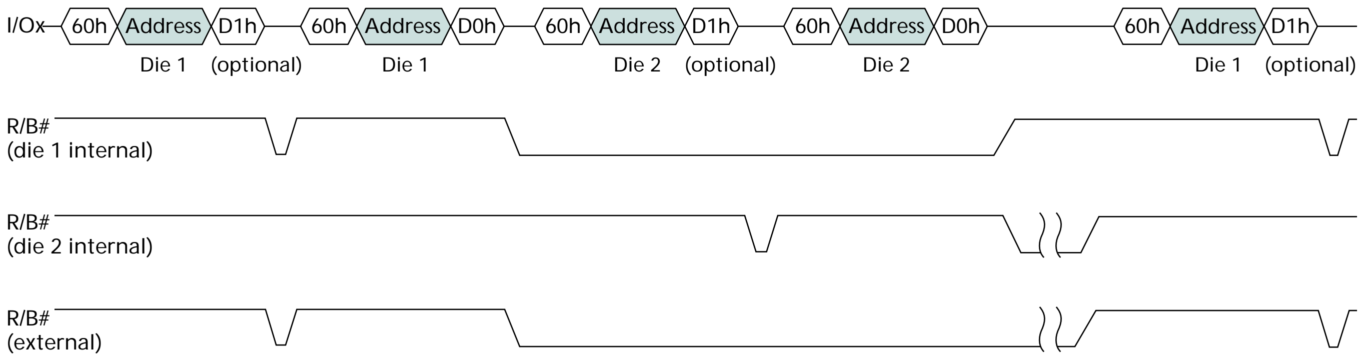
Interleaved TWO-PLANE BLOCK ERASE Operations

Two types of interleaved TWO-PLANE BLOCK ERASE operations are shown in Figure 70, and Figure 71 on page 88. In Figure 70, the R/B# signal is monitored for operation completion. In Figure 71, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE BLOCK ERASE operation must meet two-plane addressing requirements (see "Two-Plane Addressing" on page 50).

Figure 70: Interleaved TWO-PLANE BLOCK ERASE with R/B# Monitoring



Note: Two-plane addressing requirements apply.

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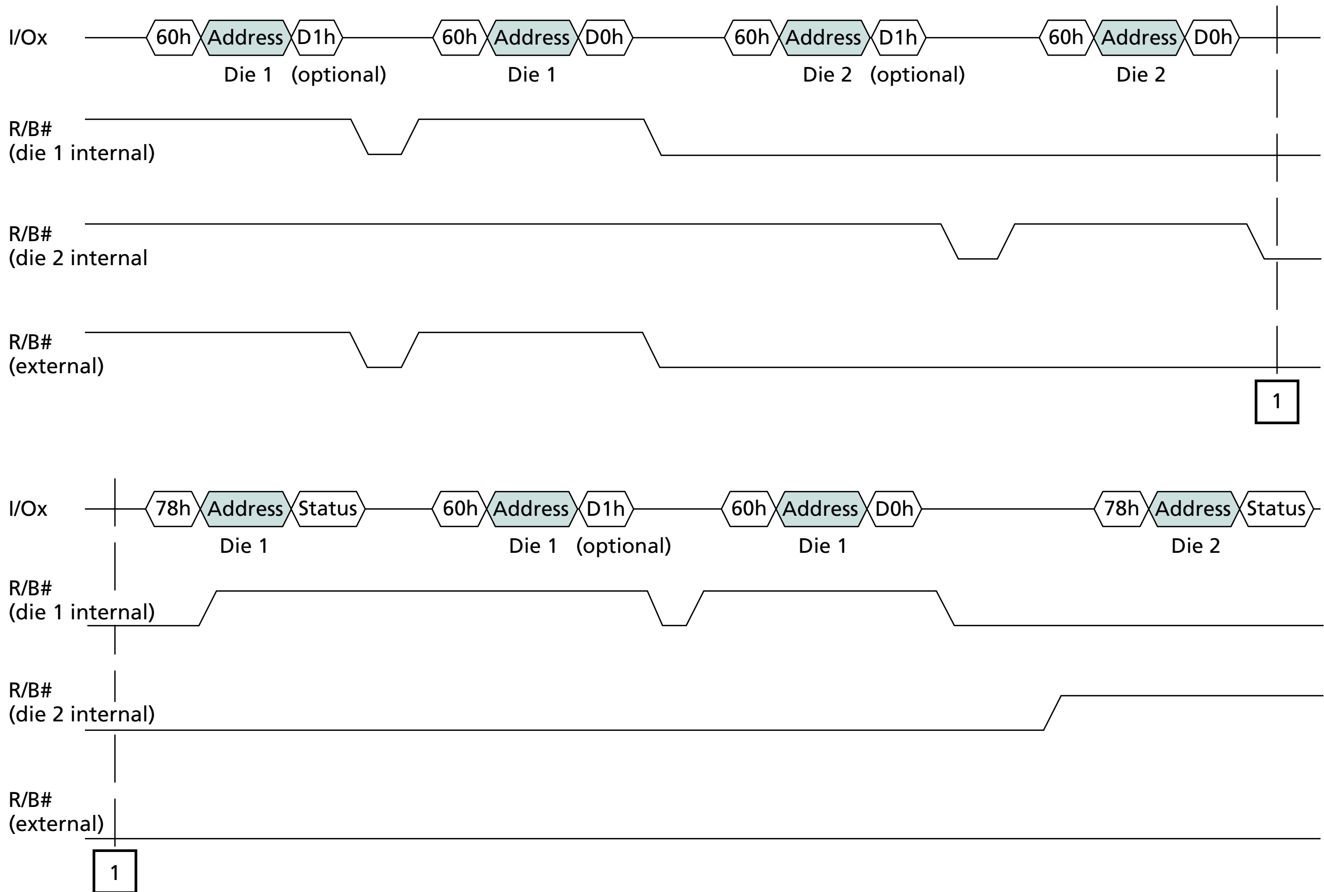
Figure 71: Interleaved TWO-PLANE BLOCK ERASE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

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Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in Table 21 on page 92. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page with more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms to ensure data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory-defect mapping requirements. See Table 17 for the bad-block mark.

System software should initially check the first spare area location on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after each PROGRAM and ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 17.
- Use bad-block management and wear-leveling algorithms.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 17: Error Management Details

Description	Requirement
Minimum NVB per die	7992
Total available blocks per die	8192
Minimum required ECC	12-bit ECC per 539 bytes of data
First spare area location	x8: byte 4096
Bad-block mark	x8: 00h

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Electrical Characteristics

Table 18: Absolute Maximum Ratings by Device
Voltage on any pin relative to Vss

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	Vin	–0.6	+4.6	V
Vcc supply voltage	Vcc	–0.6	+4.6	V
Storage temperature	T_{STG}	–65	+150	°C
Short circuit output current, I/Os		–	5	mA

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Extended		–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Ground supply voltage		Vss	0	0	0	V

Vcc Power-Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. Vcc is internally monitored. WP# provides additional hardware protection. WP# should be kept at Vil during power-cycling. When Vcc reaches 2.5V, a minimum of 100µs should be allowed for the NAND Flash to initialize before executing any commands (see Figure 72 on page 91).

Both of the following conditions must be satisfied before R/B# will be valid:

- Assuming a linear Vcc ramp rate, Vcc must reach its maximum value within 50µs of starting its ramp. This value for Vcc can be within the minimum and maximum values for Vcc as described in Table 21.
- No more than 10µs can elapse after Vcc reaches ≈ 2.5V.

The RESET command must be issued to all CE#s as the first command after the NAND Flash device is powered on. Each CE# will be busy for a maximum of 1ms after a RESET command is issued.

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Figure 72: AC Waveforms During Power Transitions

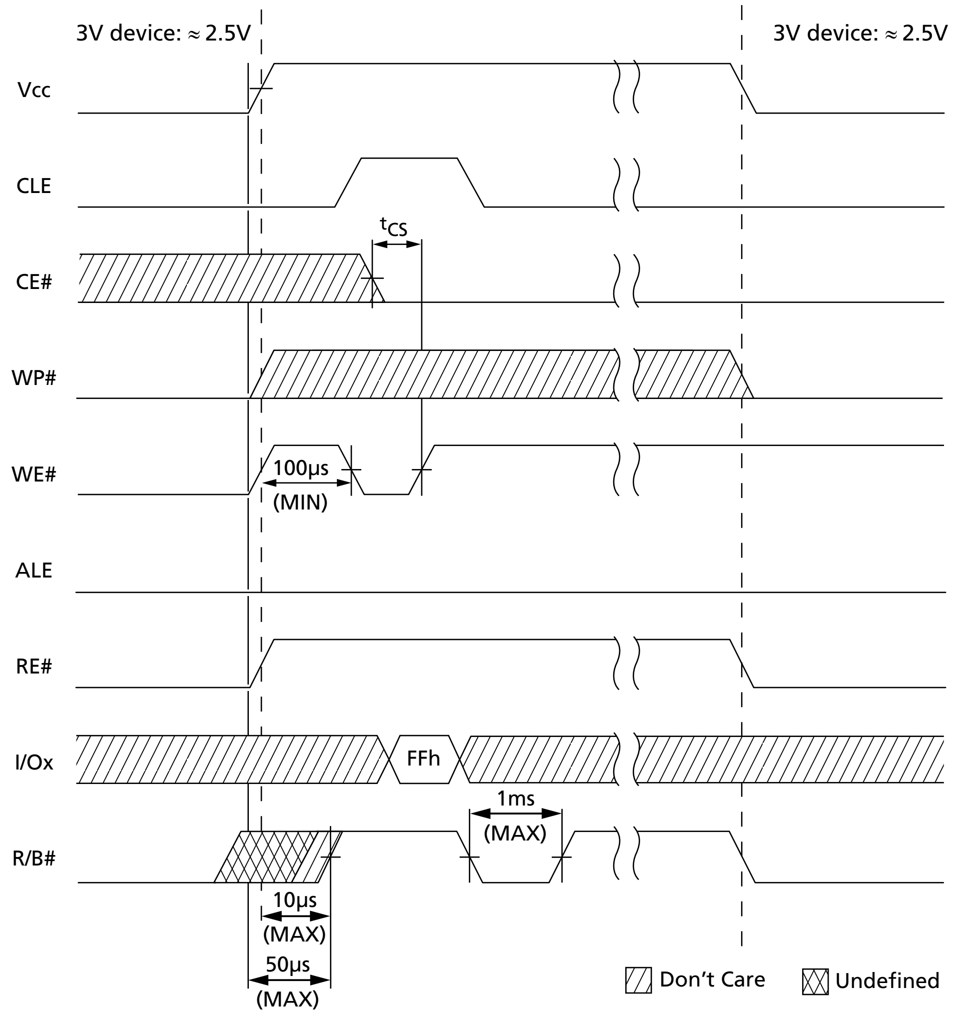

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Table 20: Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Array read current	–	Icc1_a	–	20	40	mA	1
Array program current	–	Icc2_a	–	20	40	mA	1
Array erase current	–	Icc3_a	–	20	40	mA	1
I/O burst read current	^{t}RC = ^{t}RC (MIN); Iout = 0mA	Icc4r_a	–	10	20	mA	1
I/O burst write current	^{t}WC = ^{t}WC (MIN)	Icc4w_a	–	10	20	mA	1
Bus idle current	–	Icc5_a	–	5	10	mA	1
Standby current (CMOS)	CE# = Vccq - 0.2V; WP# = 0V/Vccq	Isb_a	–	10	50	µA	1
Current during first RESET command after power-on	–	Icc5	–	–	10	mA	1
Input leakage current	Vin = 0V to Vcc	Ili	–	–	±10	µA	
Output leakage current	Vout = 0V to Vcc	Ilo	–	–	±10	µA	
Staggered power-up current	Rise time = 1ms, line capacitance = 0.1µF	Ist	–	–	10 per die	mA	2
Input high voltage	I/Ox, CE#, CLE, ALE, WE#, RE#, WP#	Vih	0.8 x Vcc	–	Vcc + 0.3	V	
Input low voltage (all inputs)	–	Vil	–0.3	–	0.2 x Vcc	V	
Output high voltage	IOH = –400µA	Voh	0.67 x Vcc	–	–	V	3
Output low voltage	IOL = 2.1mA	Vol	–	–	0.4	V	3

Notes:
1. This is for single-die operations. It can be greater for interleaved die operations.
2. Measurement is taken with 1ms averaging intervals and begins after Vcc reaches Vcc (MIN).
3. Test conditions for Voh and Vol.
4. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full (see Table 15 on page 49).

Table 21: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	MT29F32G	7992	8192	Blocks	1, 2,
		MT29F64G	15,984	16,384	Blocks	1, 2, 3
		MT29F128G	31,968	32,768	Blocks	1, 2, 4

Notes:
1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block of each CE#) is guaranteed to be valid with ECC when shipped from the factory.
3. Each 32Gb section has a maximum of 200 invalid blocks.
4. Each 64Gb section has a maximum of 400 invalid blocks.

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Table 22: Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input/output capacitance: ALE, CE#, CLE, RB#, RE#, WE#, WP#	Cin/Cout	MT29F32G	10	pF	1, 2
		MT29F64G	20		
		MT29F128G	40		
Input/output capacitance: I/O[7:0]	Cin/Cout	MT29F32G	5	pF	1, 2
		MT29F64G	10		
		MT29F128G	20		

Notes: 1. These parameters are verified in device characterization and are not 100% tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; Vin = 0V.

Table 23: Test Conditions

Parameter	Conditions	Value	Notes
Input pulse levels	—	0.0V to 3.3V	
Input rise and fall times	—	5ns	
Input and output timing levels	—	Vcc/2	
Output load	(Vcc = 3.0V ± 10%)	1 TTL GATE and CL = 50pF	1
	(Vcc = 3.3V ± 10%)	1 TTL GATE and CL = 100pF	1

Notes: 1. Verified in device characterization; not 100% tested.

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Table 24: AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	70	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	15	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	7	–	ns	
WRITE cycle time	^{t}WC	20	–	ns	
WE# pulse width HIGH	^{t}WH	7	–	ns	
WE# pulse width	^{t}WP	10	–	ns	
WP# setup time	^{t}WW	30	–	ns	

Notes:
1. Timing for ^{t}ADL begins in the address cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.
2. Timings meet ONFI timing mode 5 parameters.

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Table 25: AC Characteristics: Normal Operation

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	25	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	1
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15		ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
Data transfer from NAND Flash array to data register	^{t}R	–	50	µs	
READ cycle time	^{t}RC	20	–	ns	
RE# access time	^{t}REA	–	16	ns	2
RE# HIGH hold time	^{t}REH	7	–	ns	2
RE# HIGH to output hold	$^{t}RHOH$	15	–	ns	2
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	1, 2
RE# LOW to output hold	$^{t}RLOH$	5		ns	2
RE# pulse width	^{t}RP	10	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
RESET time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	

Notes:
1. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
2. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
3. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

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Table 26: PROGRAM/ERASE Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	1	Cycle	1
^{t}BERS	BLOCK ERASE operation time	3	10	ms	
^{t}CBSY	Busy time for PROGRAM CACHE operation	3	2200	µs	2
^{t}CCS	Change Column Setup time	250	–	ns	5
^{t}DBSY	Busy time for TWO-PLANE PROGRAM PAGE/TWO-PLANE PROGRAM PAGE CACHE/TWO-PLANE PROGRAM for IDM/TWO-PLANE BLOCK ERASE operation	0.5	1	µs	
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations		1	µs	
^{t}LPROG	LAST PAGE PROGRAM operation time	–	–	–	4
^{t}PROG	PAGE PROGRAM operation time	900	2200	µs	
^{t}RCBSY	Busy time for READ CACHE operation	3	50	µs	3

Notes:
1. One total to the same page.
2. ^{t}CBSY (MAX) time depends on timing between internal program completion and data in.
3. ^{t}RCBSY (MAX) time depends on timing between internal read completion.
4. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).
5. ^{t}CCS is a minimum spec. RANDOM DATA INPUT use this spec.

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Timing Diagrams

Figure 73: Command Latch Cycle

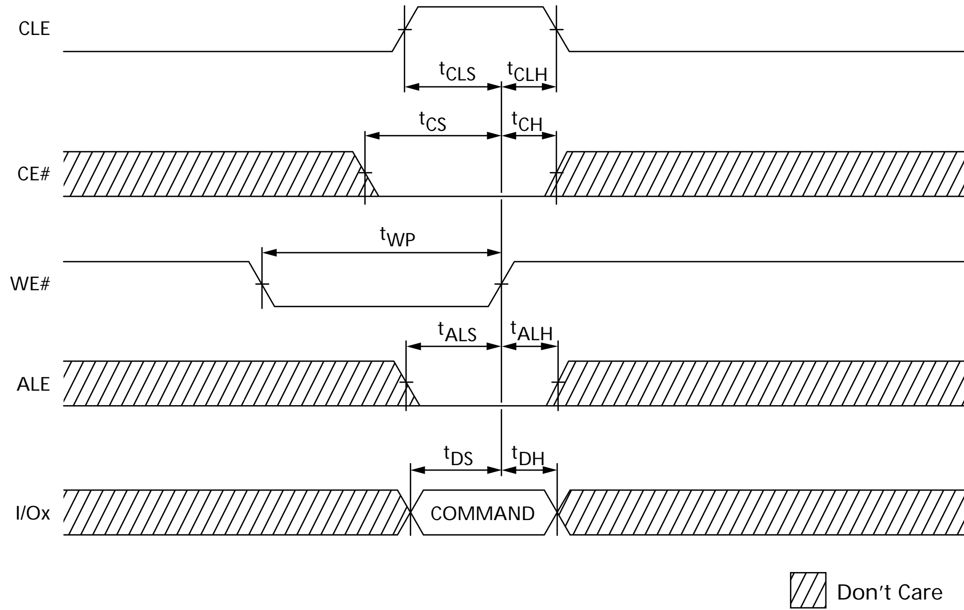

Figure 74: Address Latch Cycle

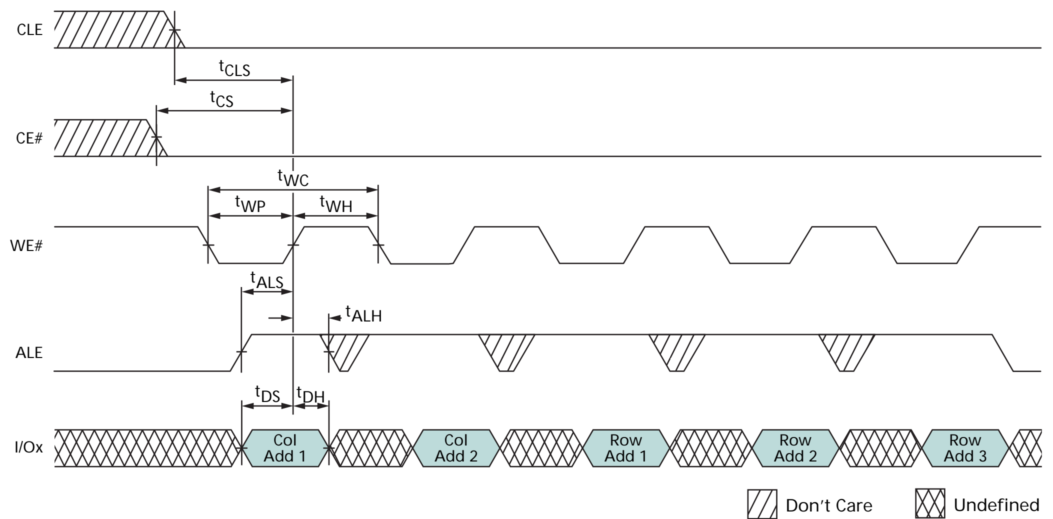

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Figure 75: Input Data Latch Cycle

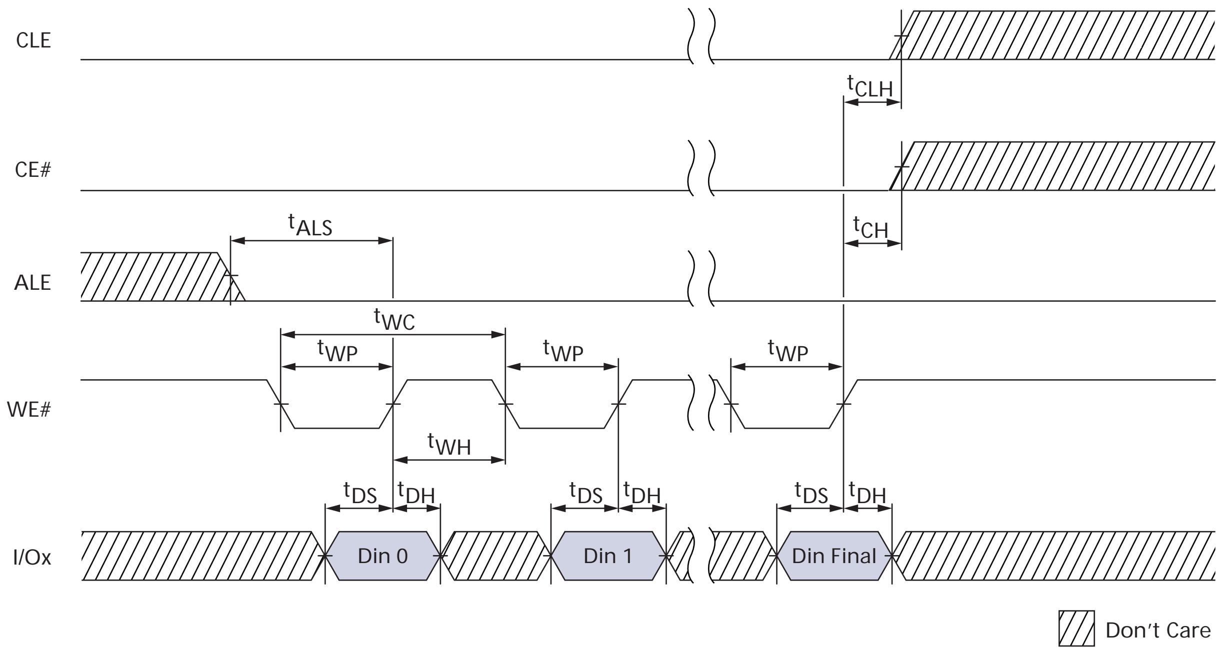

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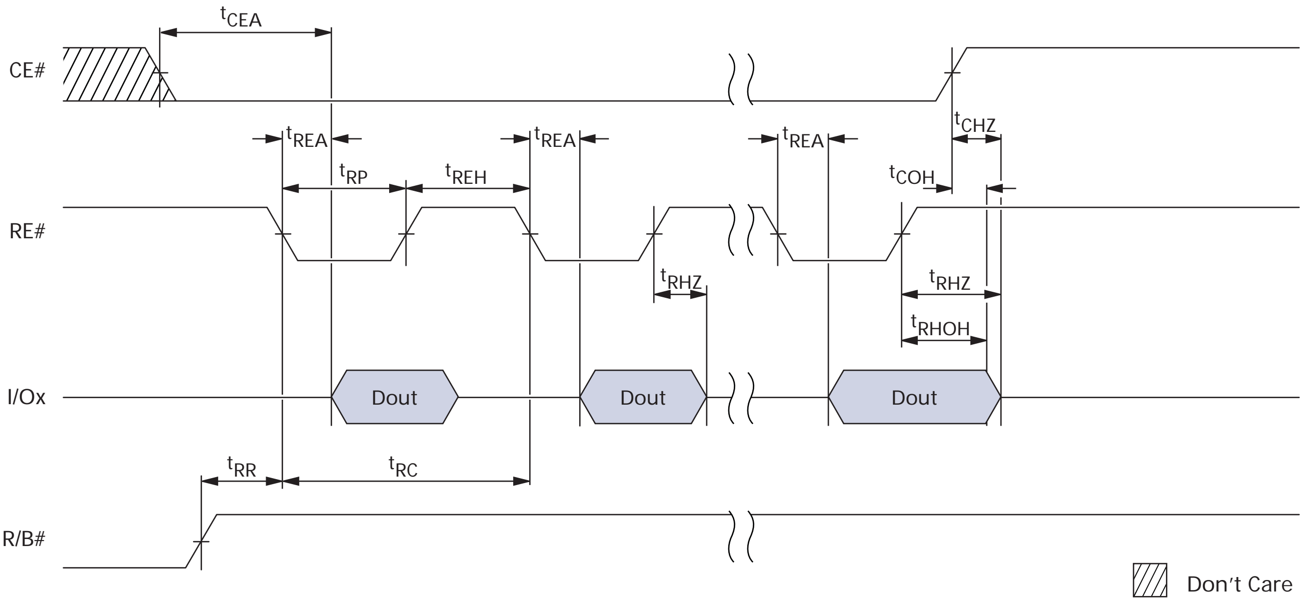
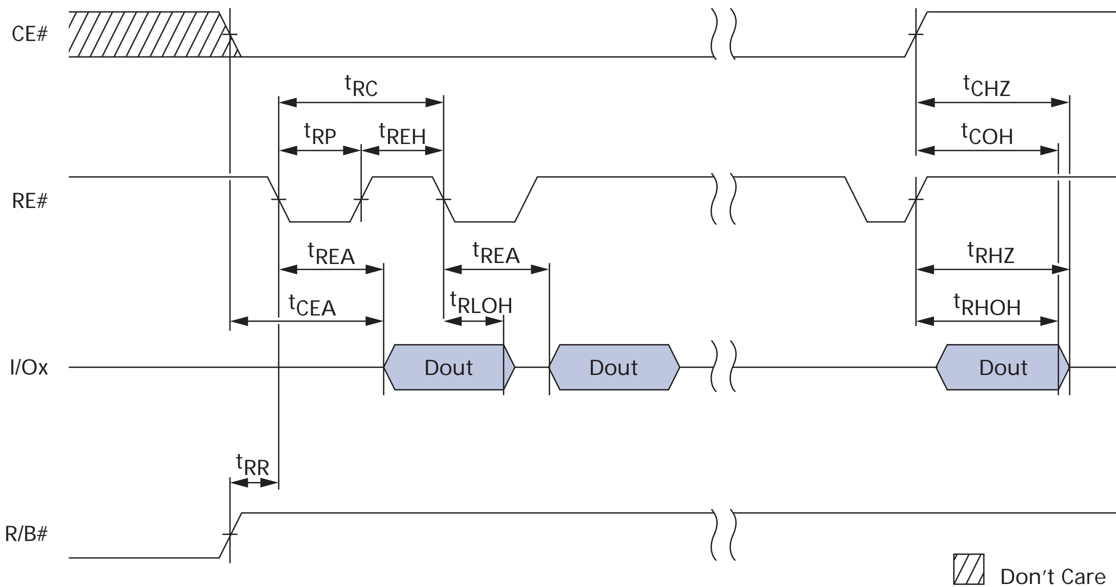
Figure 76: Serial Access Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30ns$.

Figure 77: Serial Access Cycle After READ (EDO Mode)



Note: Use this timing diagram for $^{t}RC < 30ns$.

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Figure 78: READ STATUS Cycle

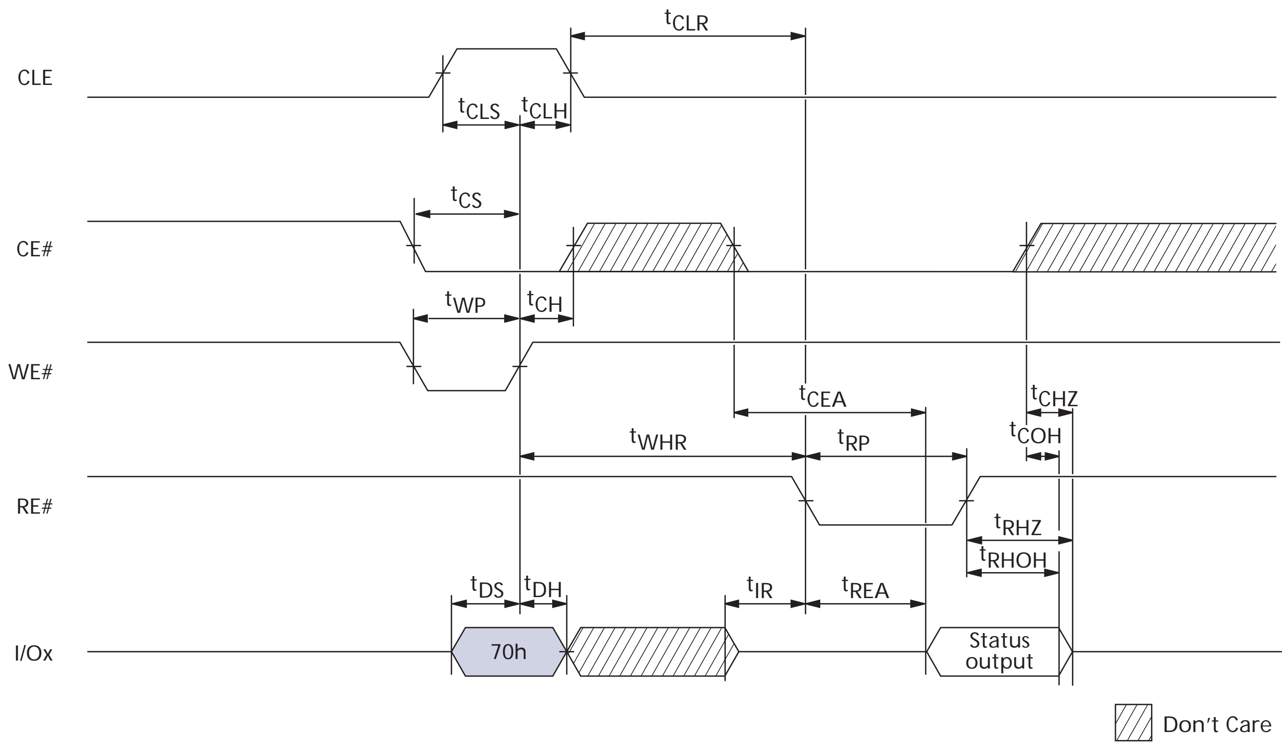

Figure 79: TWO-PLANE/MULTIPLE-DIE READ STATUS Operation

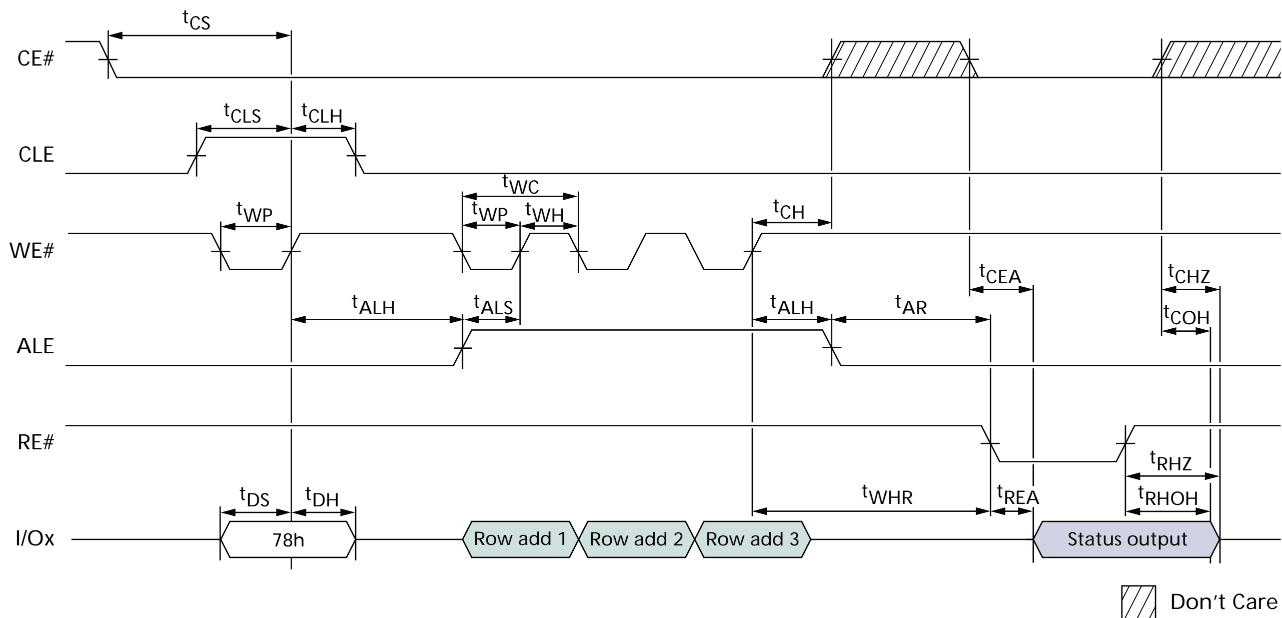

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Figure 80: PAGE READ

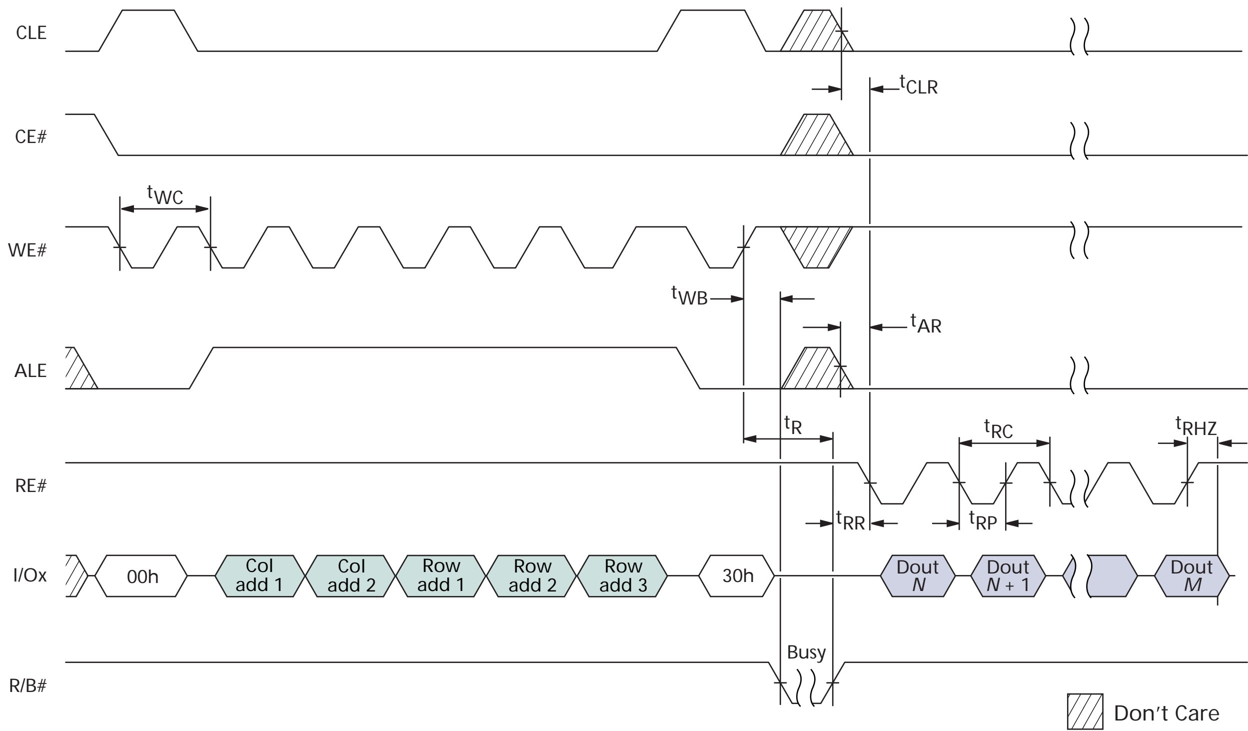

Figure 81: READ Operation with CE# "Don't Care"

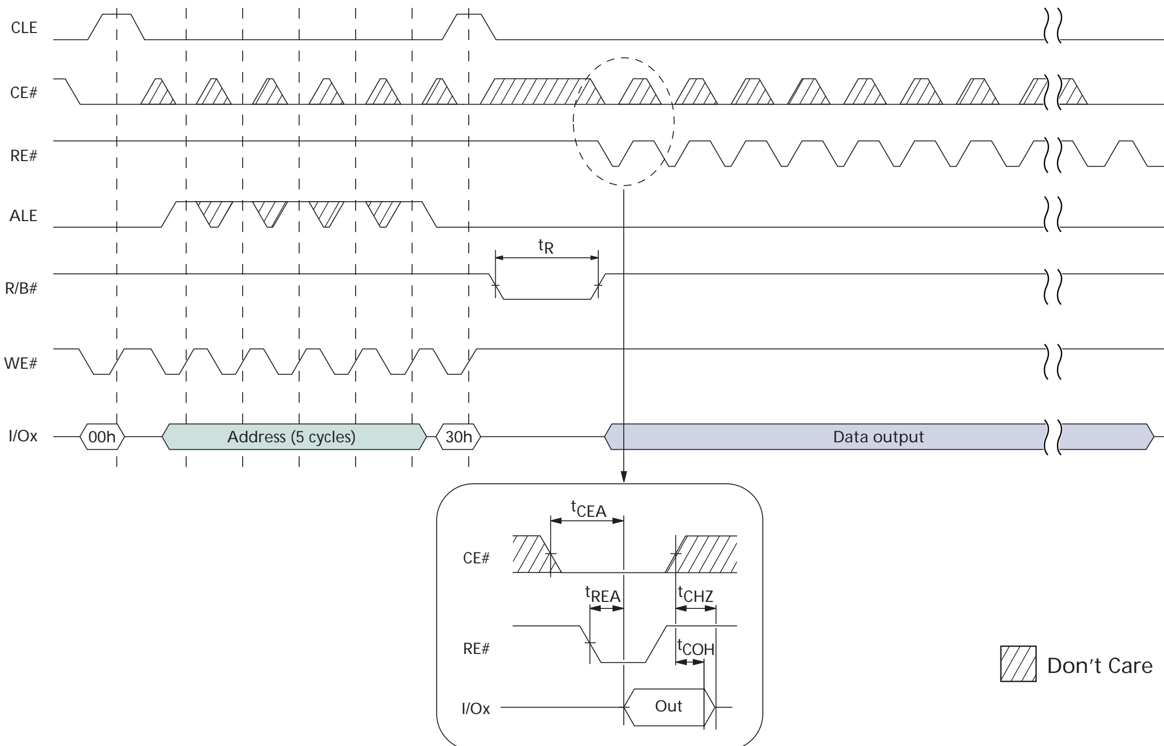

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Figure 82: RANDOM DATA READ

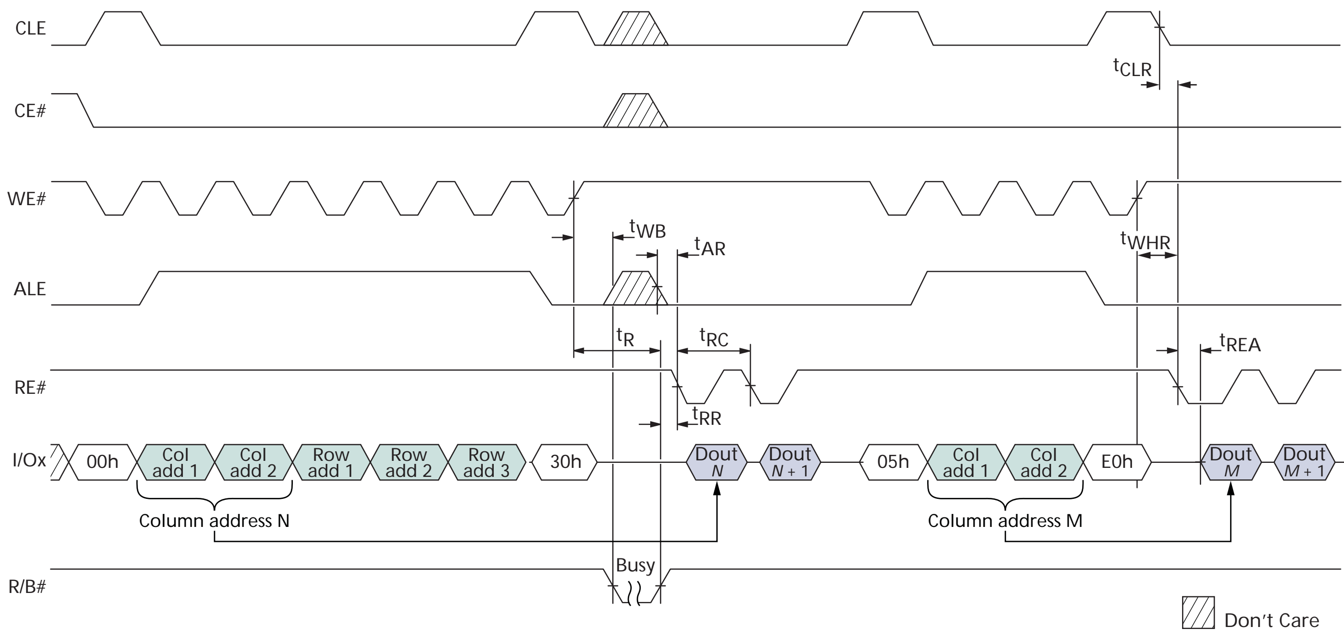

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Figure 83: PAGE READ CACHE MODE Timing Diagram, Part 1 of 2

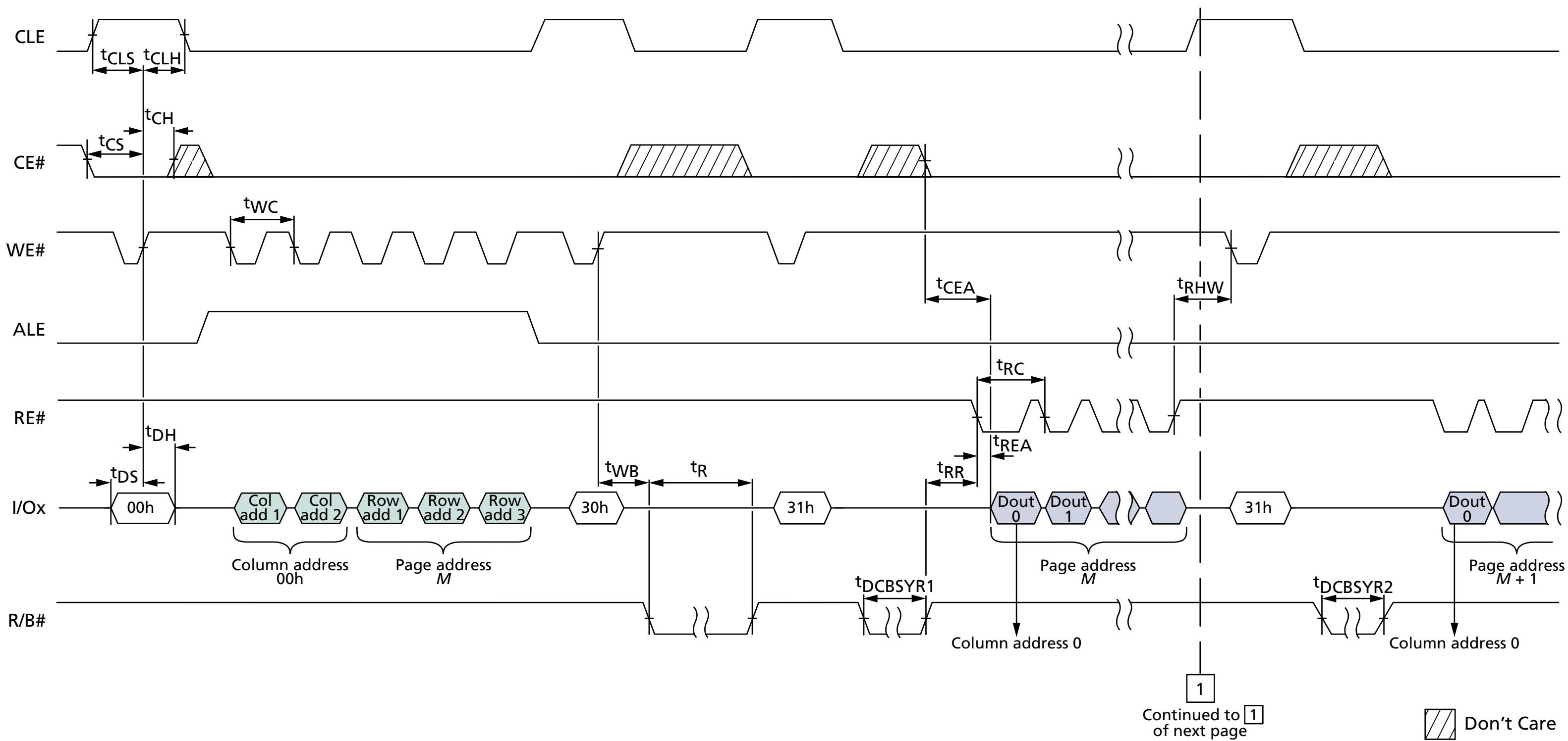

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Figure 84: PAGE READ CACHE MODE Timing Diagram, Part 2 of 2

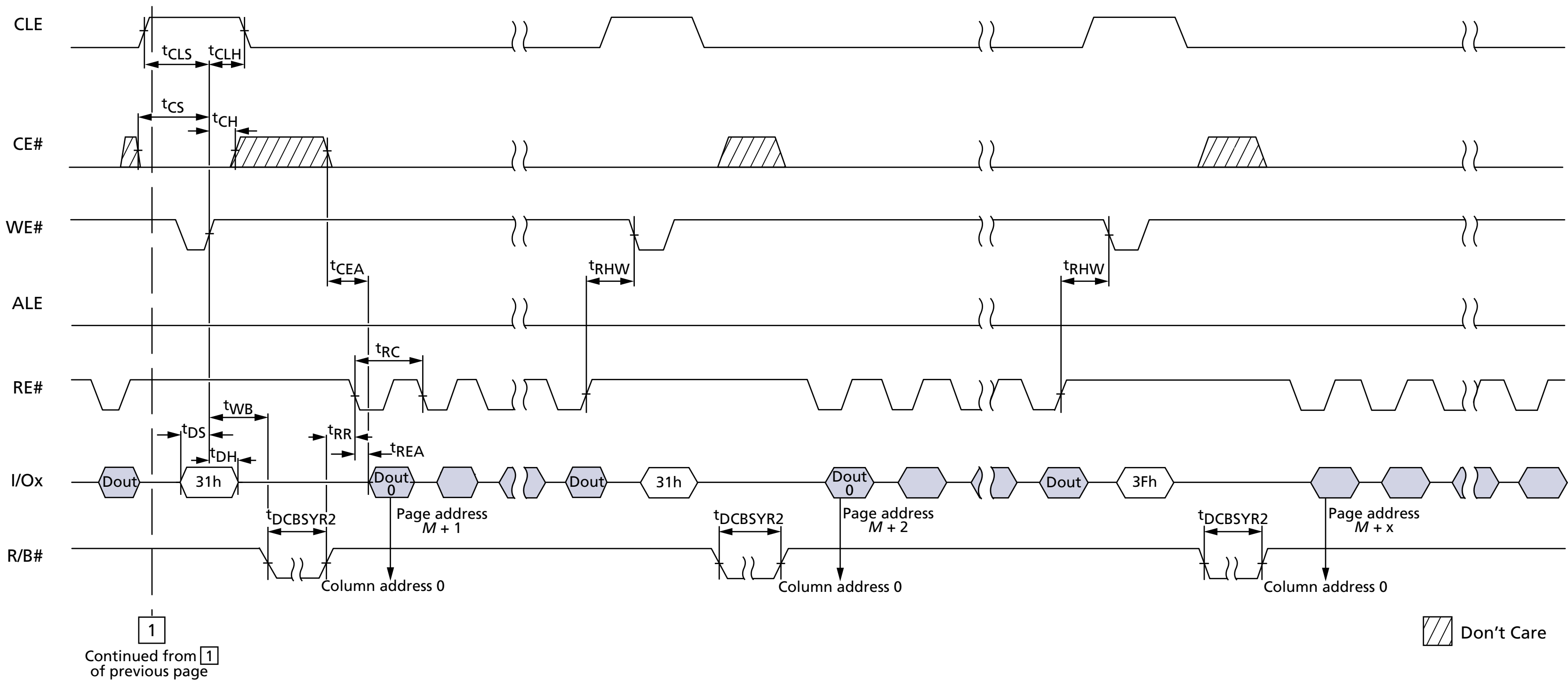

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Figure 85: PAGE READ CACHE MODE Timing without R/B#, Part 1 of 2

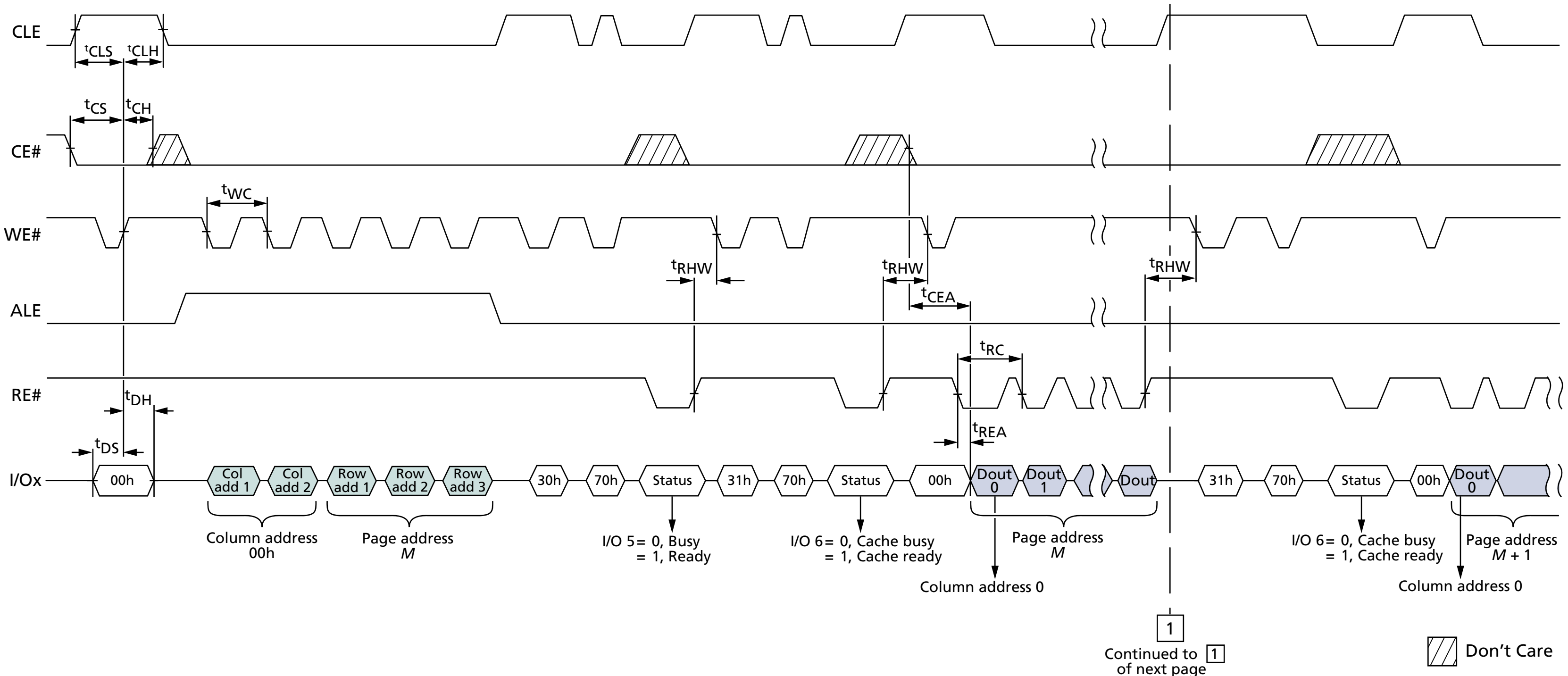

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Figure 86: PAGE READ CACHE MODE Timing without R/B#, Part 2 of 2

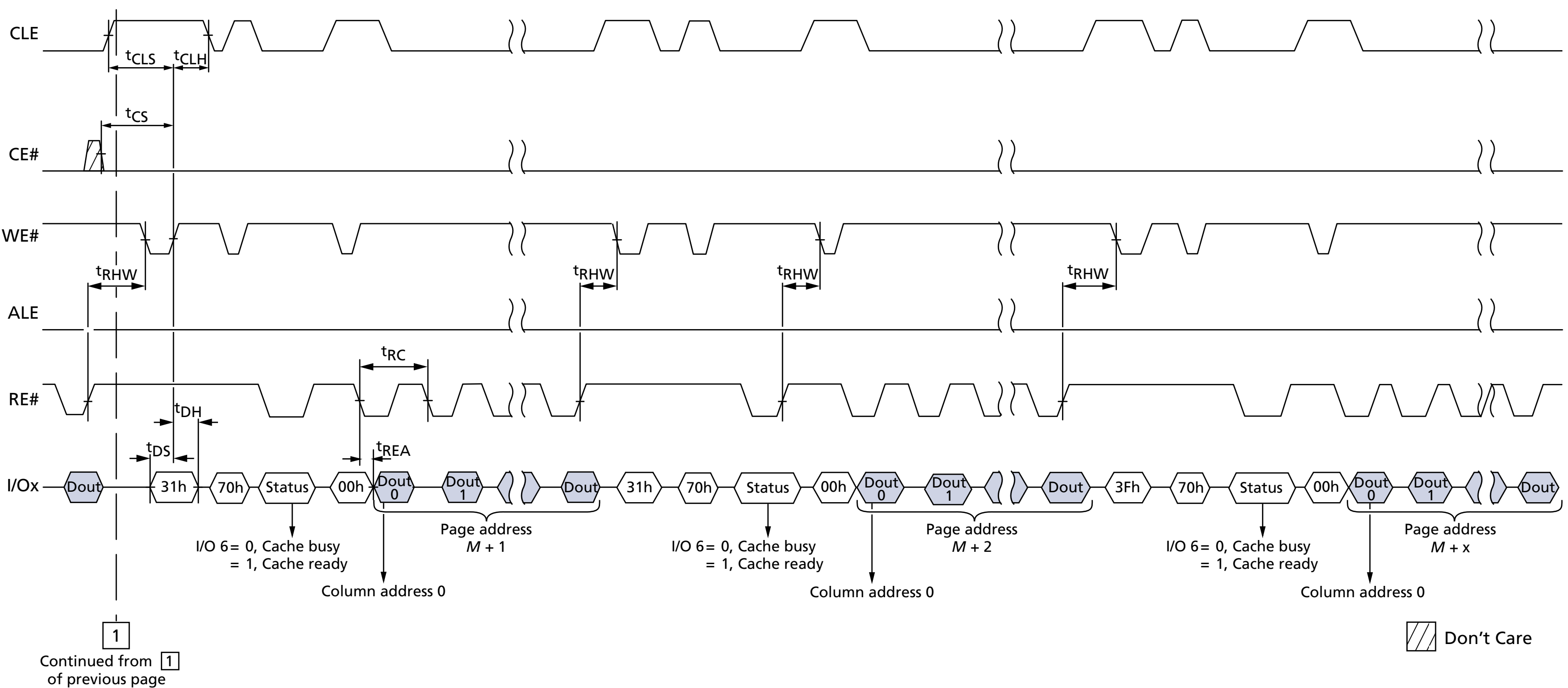

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Figure 87: READ ID Operation

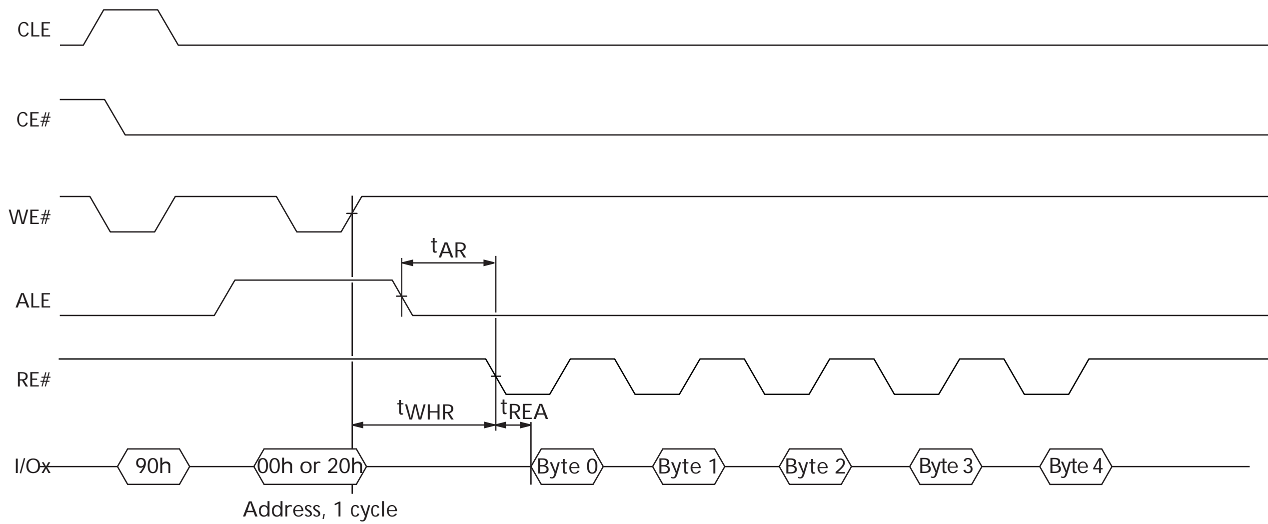

Figure 88: PROGRAM PAGE Operation

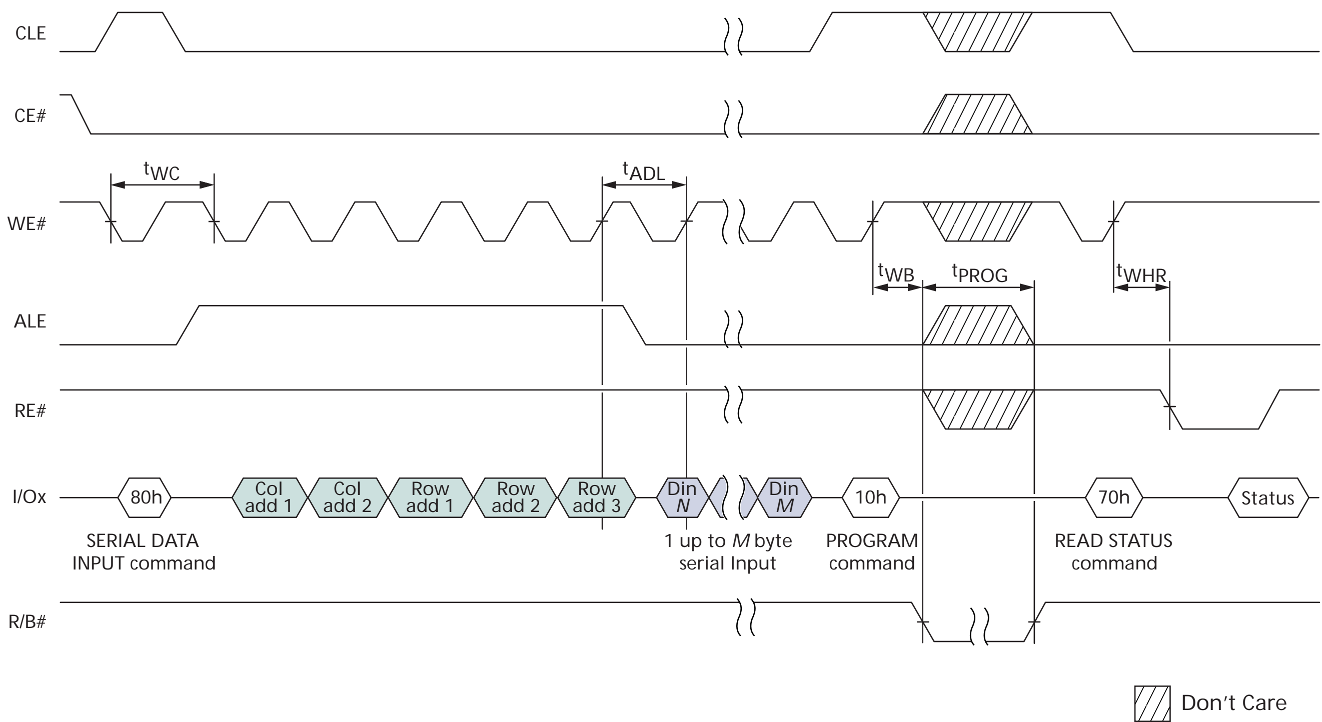

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Figure 89: Program Operation with CE# "Don't Care"

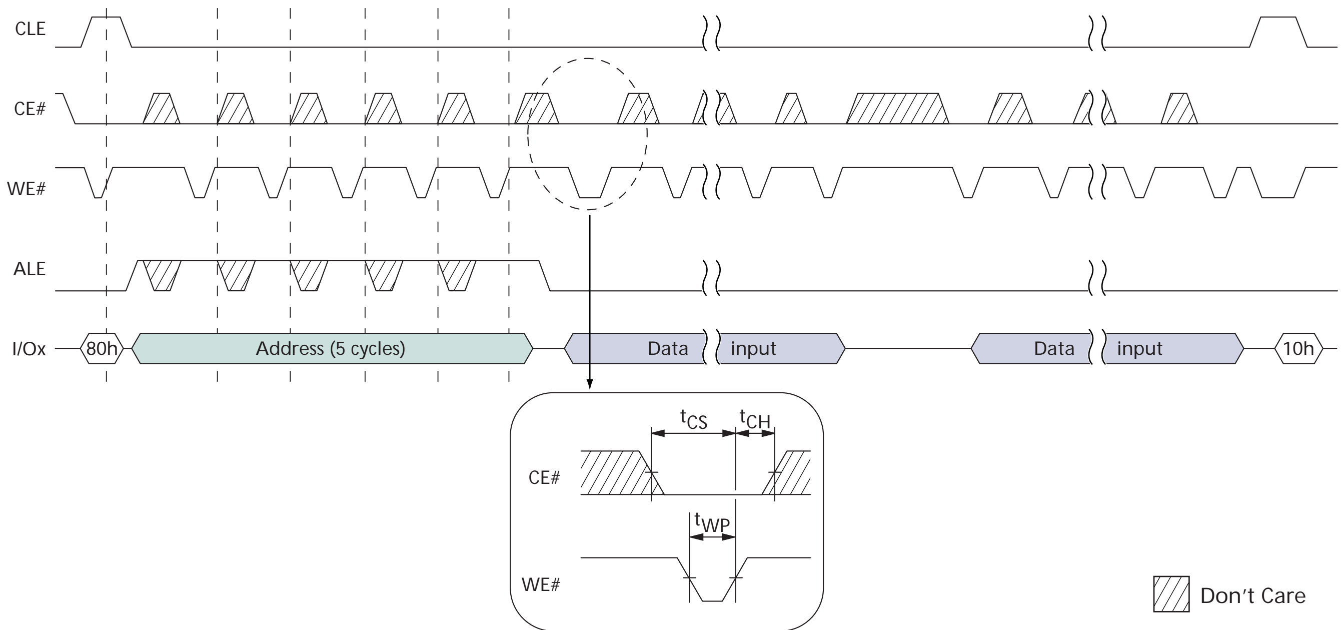

Figure 90: PROGRAM PAGE Operation with RANDOM DATA INPUT

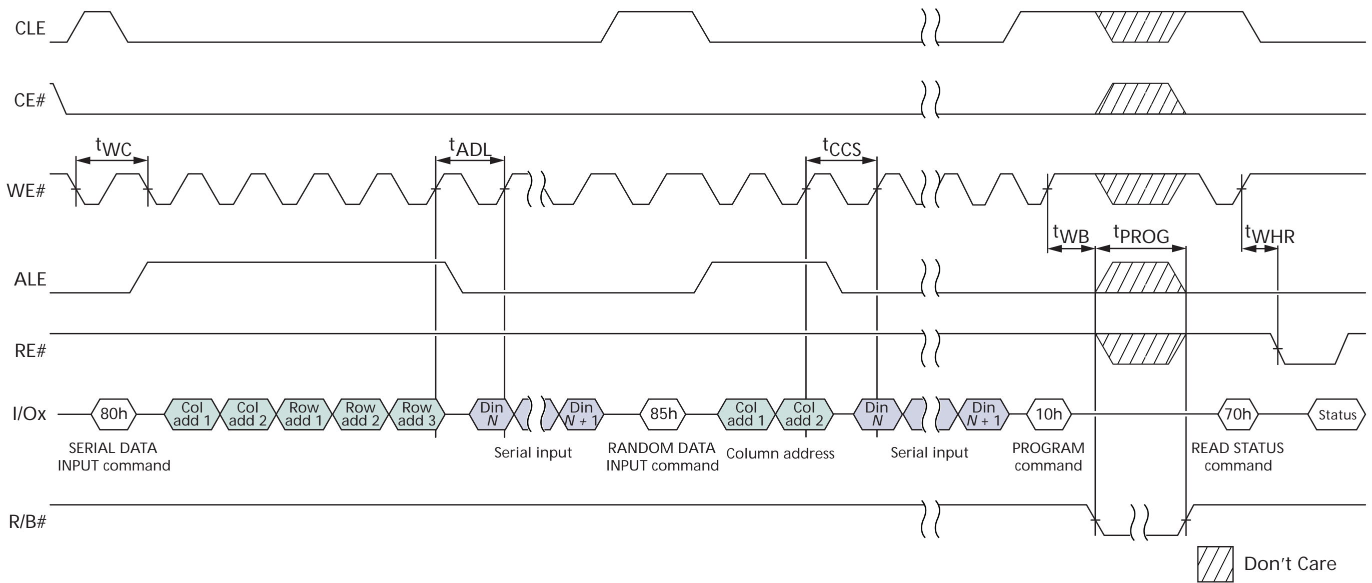

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Figure 91: INTERNAL DATA MOVE

CLE
CE#
WE#
ALE
RE#
I/Ox
R/B#
tWC
tADL
tWB
tR
tWB tPROG
tWHR
00h Col add 1 Col add 2 Row add 1 Row add 2 Row add 3 35h 85h Col add 1 Col add 2 Row add 1 Row add 2 Row add 3 Data 1 Data N 10h 70h Status
Busy
Busy
READ STATUS Command
INTERNAL DATA MOVE
Don't Care

Figure 92: PROGRAM PAGE CACHE MODE

CLE
CE#
WE#
ALE
RE#
I/Ox
R/B#
tWC
tWB tCBSY
tADL
tWB tLPROG
tWHR
80h Col add 1 Col add 2 Row add 1 Row add 2 Row add 3 Din N Din M 15h 80h Col add 1 Col add 2 Row add 1 Row add 2 Row add 3 Din N Din M 10h 70h Status
SERIAL DATA INPUT
Serial Input
PROGRAM
PROGRAM
Last Page - 1
Last Page
Don't Care

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Figure 93: PROGRAM PAGE CACHE MODE Ending on 15h

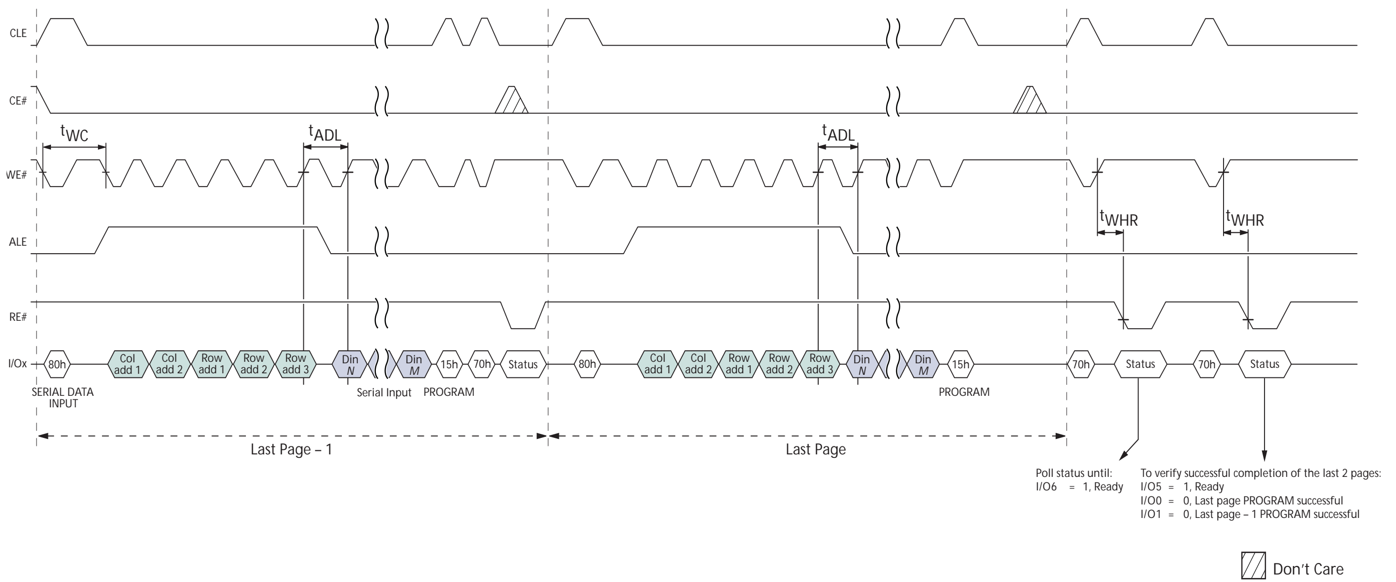

Figure 94: BLOCK ERASE Operation

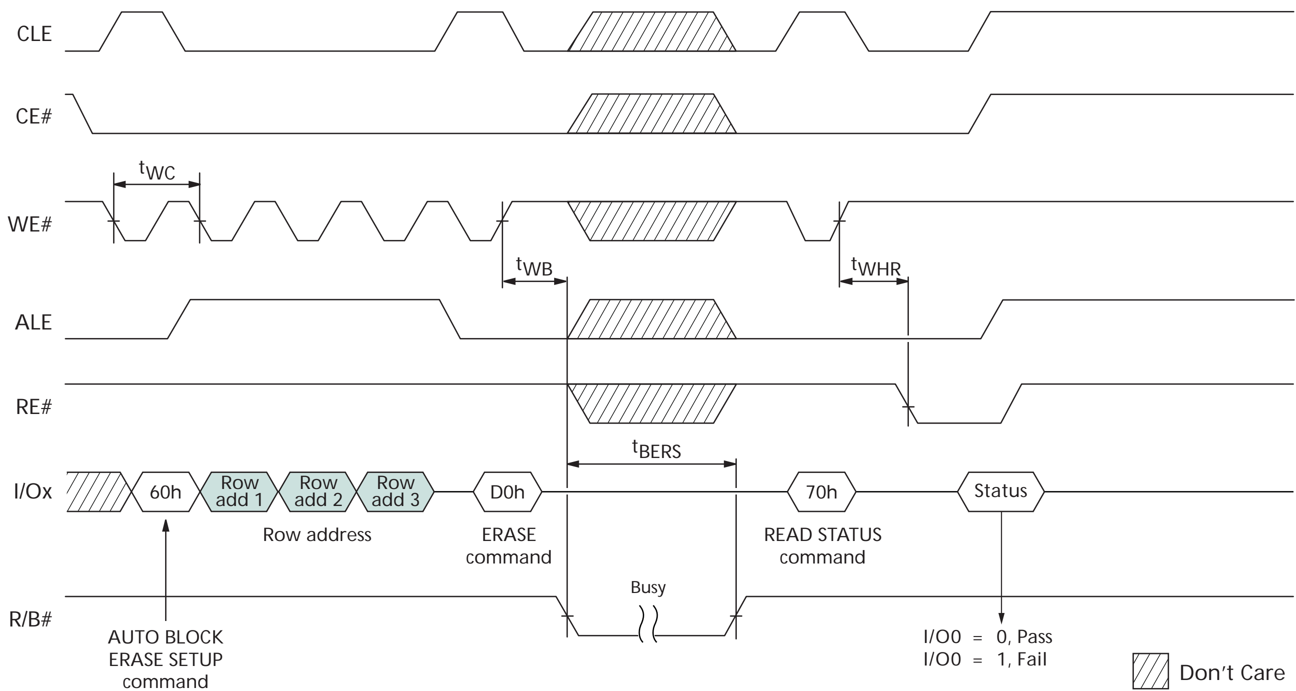

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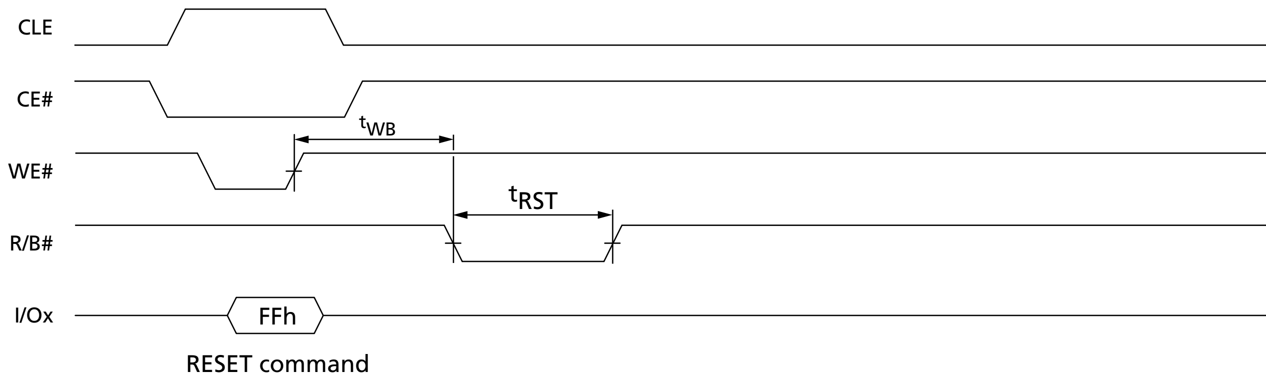
Figure 95: RESET Operation



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TSOP Package Information

Figure 96: 48-Pin TSOP Type 1 OCPL (WC Package Code)

20.00 ±0.25
18.40 ±0.08
0.25 for reference only
0.50 for reference only
48
1
24
25
12.00 ±0.08
Mold compound: Epoxy novolac
Plated lead finish: 100% Sn
Package width and length do not include mold protrusion. Allowable protrusion is 0.25 per side.
0.27 MAX
0.17 MIN
0.15 +0.03 -0.02
See detail A
1.20 MAX
0.10
0.25
Gage plane
0.10 +0.10 -0.05
0.50 ±0.1
0.80
Detail A

Notes: 1. All dimensions in millimeters; MIN/MAX, or typical, as noted.

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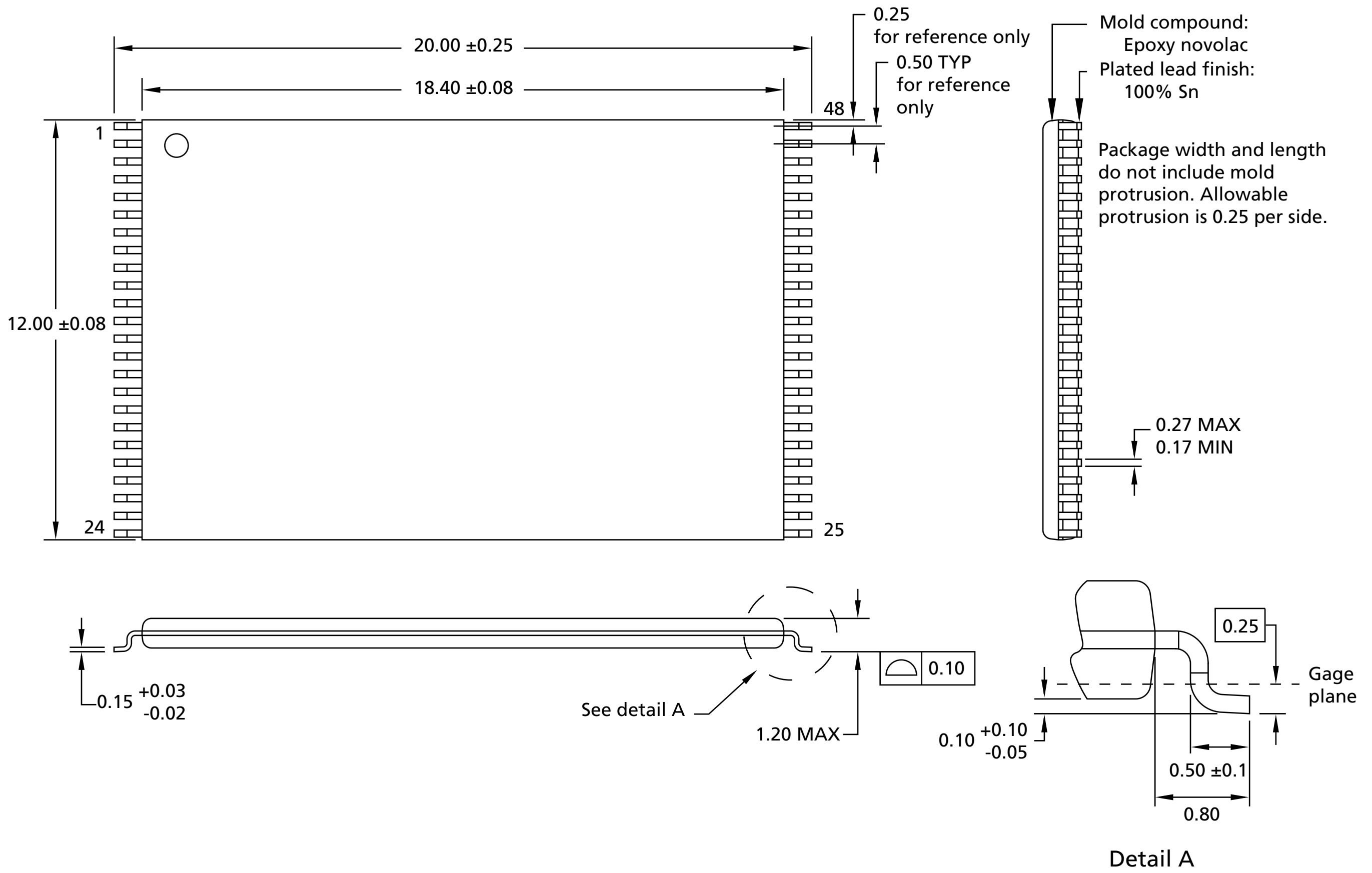
Figure 97: 48-Pin TSOP Type 1 (WP Package Code)



Notes: 1. All dimensions are in millimeters.

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VLGA Package Information

Figure 98: 52-Pad VLGA Package

Seating plane
0.08 A
A
See Note 3
Detail A
Not to scale[2]
See Detail A
40X Ø0.7[1]
12X Ø1[1]
6
4
2 3
8 7 6 5 4 3 2 1 0
Terminal A1 ID
Substrate material: plastic laminate
Mold compound: epoxy novolac
Terminal A1 ID
OA OB OC OD OE OF
A B C D E F G H J K L M N
7.8
9 ±0.08
18 ±0.15
6.5
2 TYP
13 12 10 5 6
2 TYP
2 TYP
7 ±0.08
5
10
14 ±0.15
1.0 MAX

Notes:
1. All dimensions are in millimeters.
2. Solder pads are nonsolder-mask defined (NSMD) and are plated with 3–15 microns of nickel followed by a minimum of 1.0 microns of soft wire bondable gold (99.99% pure).
3. Primary datum A (seating plane) is defined by the bottom terminal surface. Metallized test terminal lands or interconnect terminals need not extend below the package bottom surface.

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Advance: This data sheet contains initial descriptions of products still under development.

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Revision History

Rev. A, Advance 12/08

- Advance release.

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