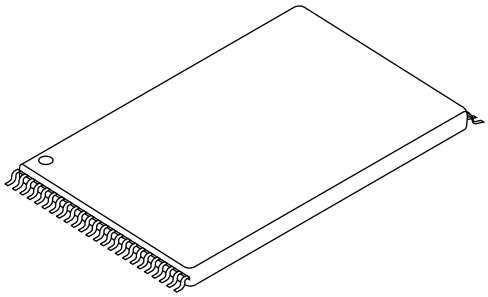
NAND Flash Memory MLC

MT29F8G08MAAWC, MT29F8G08MAAWP, MT29F16G08QAAWC,MT29F32G08TAAWC

Features

- Organization
  - Page size
    x8: 2,112 bytes (2,048 + 64 bytes)
    Block size: 128 pages (256K + 8K bytes)
  - Plane size: 2,048 blocks
  - Device size: 8Gb: 4,096 blocks; 16Gb: 8,192 blocks; 32Gb: 16,384 blocks
- READ performance
  - Random READ: 50µs
  - Sequential READ: 25ns
- WRITE performance
  - PROGRAM PAGE: 650µs (TYP)
  - BLOCK ERASE: 2ms (TYP)
- Endurance: 10,000 PROGRAM/ERASE cycles (with ECC and invalid block mapping)
- First block (block address 00h) guaranteed to be valid with ECC when shipped from factory
- Industry-standard basic NAND Flash command set
- New commands
  - PAGE READ CACHE MODE
  - TWO-PLANE/MULTIPLE-DIE READ STATUS
  - Two-plane commands for concurrent-plane operations
  - READ UNIQUE ID (contact factory)
  - READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - PROGRAM/ERASE/READ operation completion
  - PROGRAM/ERASE pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting PROGRAM, READ, or ERASE cycle completion
- WP# signal: Entire device hardware write protect
- Staggered power-up sequence: Issue RESET (FFh) command

Figure 1: 48-Pin TSOP Type 1



Options

- Density[1]
  - 8Gb (single-die stack)
  - 16Gb (dual-die stack)
  - 32Gb (quad-die stack)
- Device width: x8
- Configuration

# of die	# of CE#	# of R/B#	I/O
1	1	1	Common
2	2	2	Common
4	2	2	Common

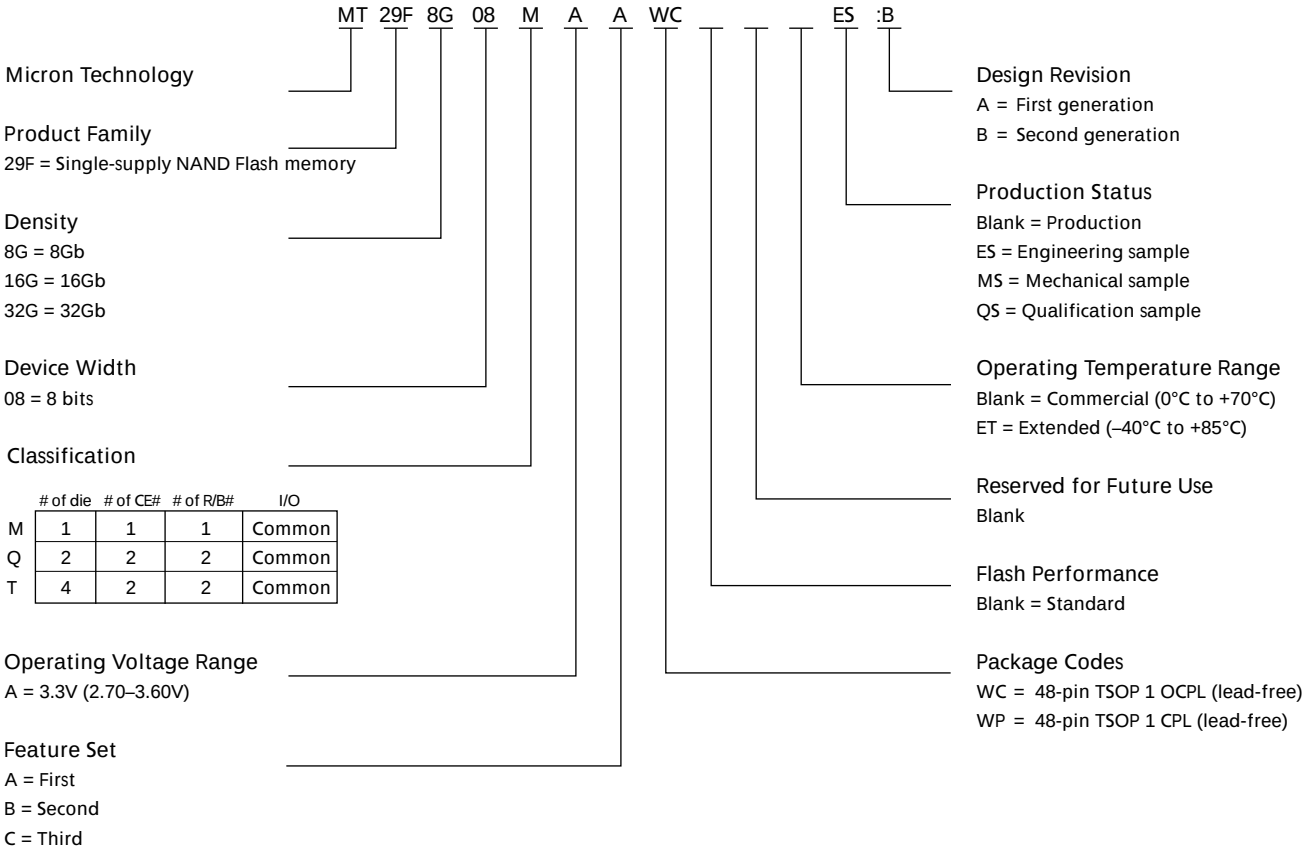
- V_{CC}: 2.7–3.6V
- First-generation die
- Package
  - 48-pin TSOP type I (lead-free plating)
  - 48-pin TSOP type I OCPL[2] (lead-free plating)
- Operating temperature
  - Commercial (0°C to 70°C)
  - Extended (–40°C to +85°C)[3]

Notes: 1. For part numbering and markings, see Figure 2 on page 2.
2. OCPL = off-center parting line.
3. For ET devices.

Part Numbering Information

Micron NAND Flash devices are available in several different configurations and densities (see Figure 2).

Figure 2: Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site: www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

NAND Flash technology provides a cost-effective solution for applications requiring high-density, solid-state storage. The MT29F8G08 is an 8Gb NAND Flash memory device. The MT29F16G08 is a two-die stack that operates as two independent 8Gb devices (MT29F8G08). The MT29F32G08 is a four-die stacked device that operates as two independent 16Gb devices (MT29F16G08), providing a total storage capacity of 32Gb in a single, space-saving package. Micron® NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

These NAND Flash devices utilize multilevel cell (MLC) technology. Each memory cell stores 2 bits of information.

Micron NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command signals (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Two additional signals control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The MT29FxG devices contain two planes per die. Each plane consists of 2,048 blocks. Each block is subdivided into 128 programmable pages. Each page consists of 2,112 bytes (x8). The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area on the x8 device. The 64-byte area is typically used for error management functions.

The contents of each 2,112-byte page can be programmed in ^{t}PROG (TYP), and an entire 264K-byte block can be erased in ^{t}BERS (TYP). On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. PROGRAM/ERASE endurance is specified at 10,000 cycles when appropriate error correction code (ECC) and error management are used.

Figure 3: NAND Flash Functional Block Diagram

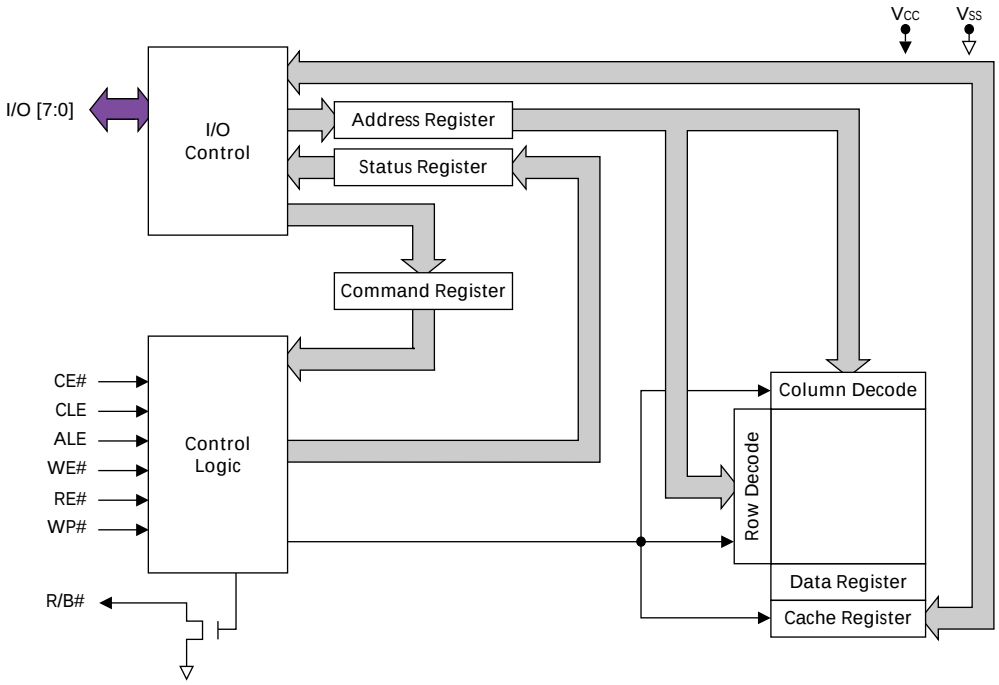
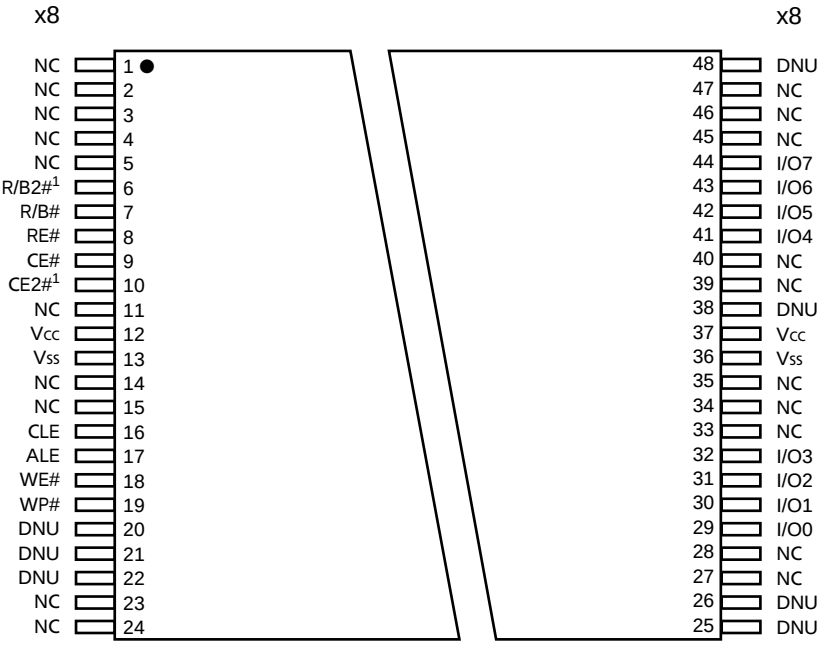


Figure 4: Pin Assignment (Top View) 48-Pin TSOP Type 1



Notes: 1. CE2# and R/B2# on 16Gb and 32Gb device only. These pins are NC for other configurations.

Table 1: Signal/Pin Descriptions

Symbol	Type	Function
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#	Input	Chip enable: CE# and CE2# are used to gate transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, chip enable(s) can be de-asserted. For the 16Gb configuration, CE# controls the first 8Gb of memory, and CE2E controls the second 8Gb. For the 32Gb configuration, CE# controls the first 16Gb of memory; CE2# controls the second 16Gb. See "Bus Operation" on page 15 for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#	Input	Read enable: RE# is used to gate transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: WE# is used to gate transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: WP# protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when the WP# is LOW.
I/O[7:0] MT29FxG08	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#	Output	Ready/busy: This is an open-drain, active-LOW output that uses an external pull-up resistor. R/B# and R/B2# are used to indicate when the chip is processing a PROGRAM or ERASE operation. R/B# and R/B2# are also used during READ operations to indicate when data is being transferred from the array into the serial data register. After these operations have completed, the R/B# returns to the high-impedance state. In the 16Gb configuration, R/B# is used for the 8Gb of memory enabled by CE#, and R/B2# is used for the 8Gb of memory enabled by CE2#. In the 32Gb configuration, R/B# used is for the 16Gb of memory enabled by CE#, and R/B2# is used for the 16Gb of memory enabled by CE2#.
V_{CC}	Supply	V_{CC}: The V_{CC} pin is the power supply pin.
V_{SS}	Supply	V_{SS}: The V_{SS} pin is the ground connection.
NC	–	No connect: NC pins are not internally connected. These pins can be driven or left unconnected.
DNU	–	Do not use: These pins must be left disconnected.

Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins. This provides a memory device with a low pin count.

The internal memory array is accessed on a page basis. For reads, a page of data is copied from the memory array into the data register. After being copied to the data register, data is output sequentially, byte by byte on x8 devices.

The memory array is programmed on a page basis. After the starting address is loaded into the internal address register, data is sequentially written to the internal data register up to the end of a page. After all of the page data has been loaded into the data register, array programming is started.

In order to increase programming bandwidth, this device incorporates a cache register. In the cache programming mode, data is first copied into the cache register and then into the data register. After the data is copied into the data register, programming begins.

After the data register has been loaded and programming started, the cache register becomes available for loading additional data. Loading of the next page of data into the cache register takes place while page programming is in process.

The INTERNAL DATA MOVE command also uses the internal cache register. Normally, moving data from one area of external memory to another requires a large number of external memory cycles. When the internal cache register and data register are used, array data can be copied from one page and then programmed into another without requiring external memory cycles.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence, as shown in Figures 6 and 7 on pages 13 and 14. Table 3 on page 13 presents address functions internal to the x8 device. See Figure 5 on page 12 for additional memory mapping and addressing details.

Figure 5: Memory Map x8

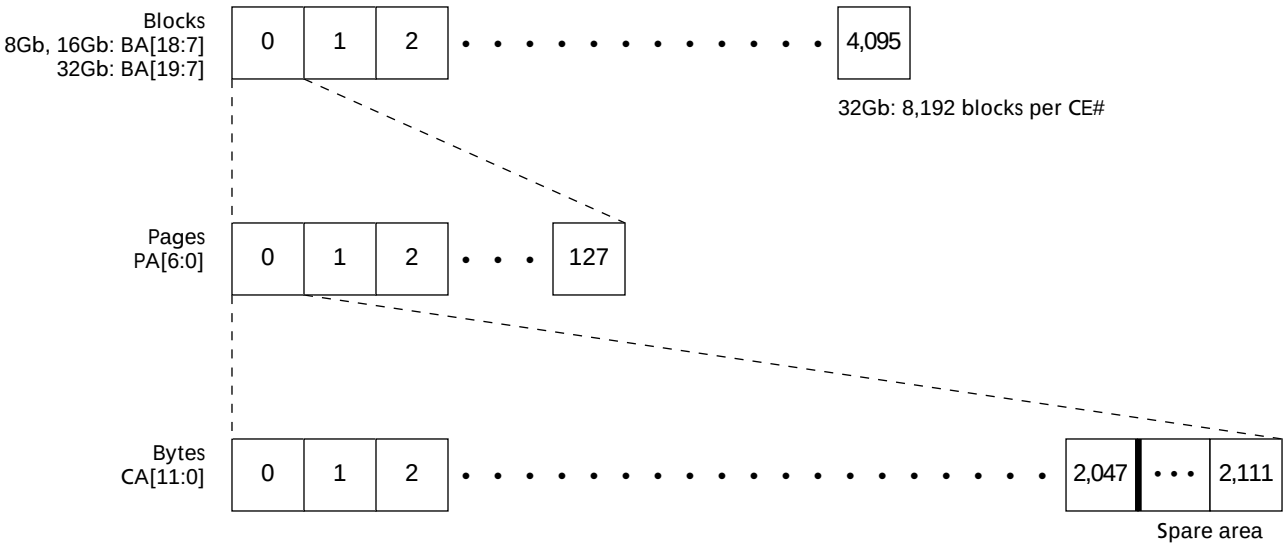
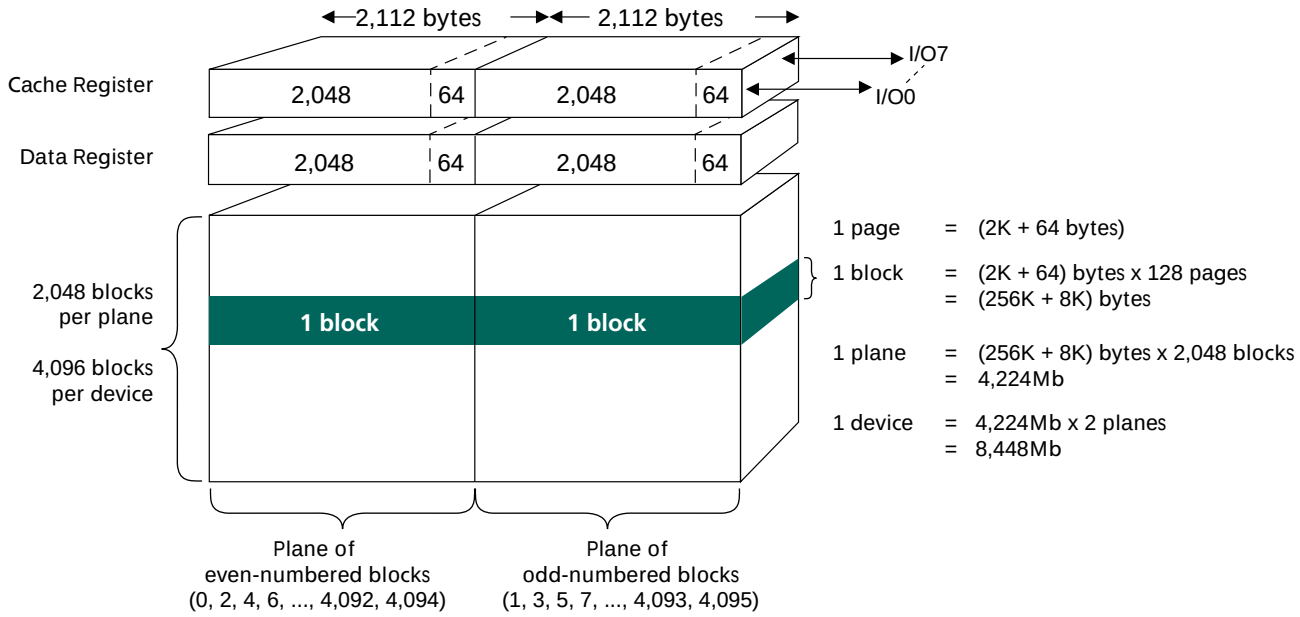


Table 2: Operational Example (8Gb x8)

Block	Page	Min Address in Page	Max Address in Page	Out-of-Bounds Addresses in Page
0	0	0x00000000	0x0000083F	0x00000840-0x00000FFF
0	1	0x00010000	0x0001083F	0x00010840-0x00010FFF
0	2	0x00020000	0x0002083F	0x00020840-0x00020FFF
...	...	...	...	...
4,095	126	0x7FFFE0000	0x7FFFE083F	0x7FFFE0840-0x7FFFE0FFF
4,095	127	0x7FFFF0000	0x7FFFF083F	0x7FFFF0840-0x7FFFF0FFF

Notes: 1. As shown in Table 3 on page 13, the high nibble of address cycle 2 has no assigned address bits; however, these 4 bits must be held LOW during the address cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in address cycle 2 even though they have no address bits assigned to them.
2. Block address concatenated with page address = row address.

Figure 6: Array Organization for MT29F8G08MAA and MT29F16G08QAA (x8)



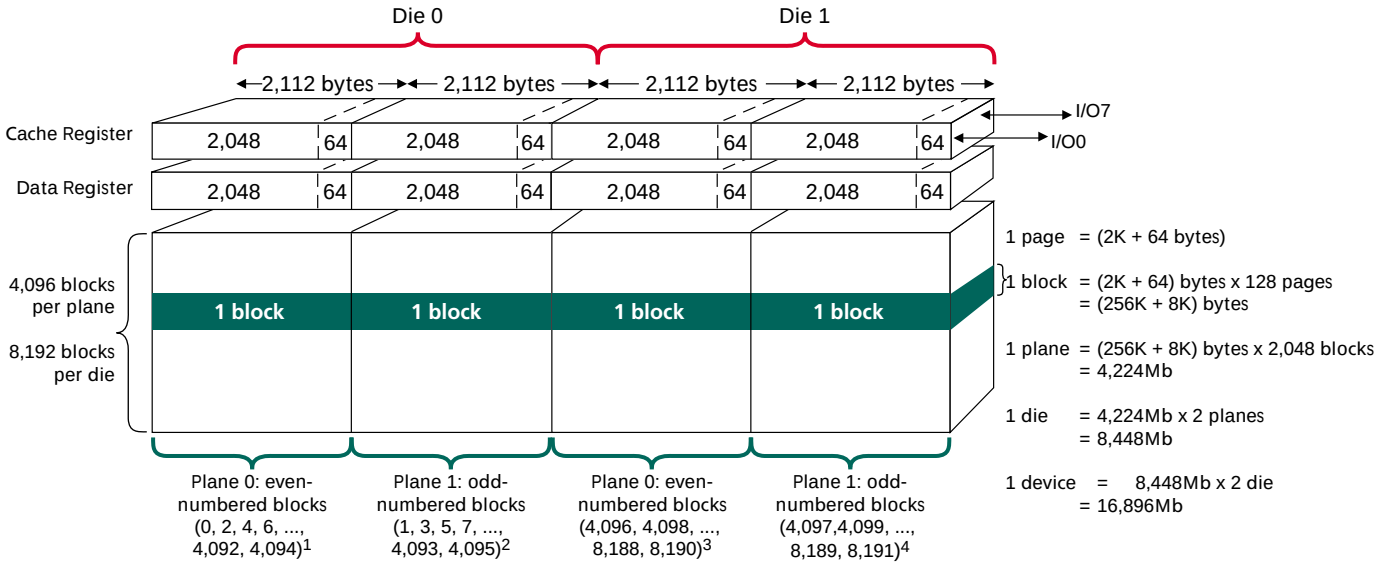
Note: For the 16Gb MT29F16G08QAA, the 8Gb array organization shown applies to each chip enable (CE# and CE2#).

Table 3: Array Addressing: MT29F8G08MAA and MT29F16G08QAA

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7[3]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18	BA17	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is "1," then CA[10:6] must be "0." This keeps a MAX limit of 2,112 bytes addressed per page.
3. Plane select bit.

Figure 7: Array Organization for MT29F32G08TAA (x8)



Notes:
1. Die 0, Plane 0: BA19 = 0; BA7 = 0
2. Die 0, Plane 1: BA19 = 0; BA7 = 1
3. Die 1, Plane 0: BA19 = 1; BA7 = 0
4. Die 1, Plane 1: BA19 = 1; BA7 = 1
5. For the 32Gb MT29F32G08TAA, the 16Gb array organization shown applies to each chip enable (CE# and CE2#).

Table 4: Array Addressing: MT29F32G08TAA

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7[4]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	BA19[3]	BA18	BA17	BA16

Notes:
1. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 is "1," then CA[10:6] must be "0." This keeps a MAX limit of 2,112 bytes addressed per page.
3. Die address boundary: 0 = 0–8Gb; 1 = 8Gb–16Gb.
4. Plane select bit.

Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins.

The command sequence normally consists of a COMMAND LATCH cycle, an address LATCH cycle, and a DATA cycle—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE, and WP# control Flash device READ and WRITE operations. On the 16Gb MT29F16G devices, CE# and CE2# each control an independent 8Gb array. On the 32Gb MT29F32G devices, CE# and CE2# each control independent 16Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable a device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, data, and address information.

When the device is not performing an operation, CE# is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 68 on page 74 and Figure 75 on page 80 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation allows the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an address input cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

As exceptions, the device accepts the READ STATUS, TWO-PLANE/MULTIPLE-DIE READ STATUS and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 62 on page 71).

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH.

See Figure 63 on page 71 for additional address input details.

The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. See Tables 6 and 7 on pages 20 and 21.

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

See Figure 64 on page 72 for additional data input details.

READ

After a READ command is issued, data is transferred from the memory array to the data register from the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. When data is available in the data register, it is clocked out of the device by RE# going LOW. See Figure 67 on page 74 for detailed timing information.

The READ STATUS (70h) or TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command or the R/B# signal can be used to determine when the device is ready.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and it transitions to LOW after the appropriate command is written to the device. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically, R/B# would be connected to an interrupt pin on the system controller (see Figure 8 on page 17).

On 16Gb MT29F16G devices, R/B# indicates the 8Gb section enabled by CE#, and R/B2# does the same for the 8Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 8Gb section.

On 32Gb MT29F32G devices, R/B# indicates the 16Gb section enabled by CE#, and R/B2# does the same for the 16Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 16Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = *Rp* (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance.

Figure 9 on page 17 and Figure 10 on page 18 depict approximate Rp values for a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp = \frac{VCC(MAX) - VOL(MAX)}{IOL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 8: READY/BUSY# Open Drain

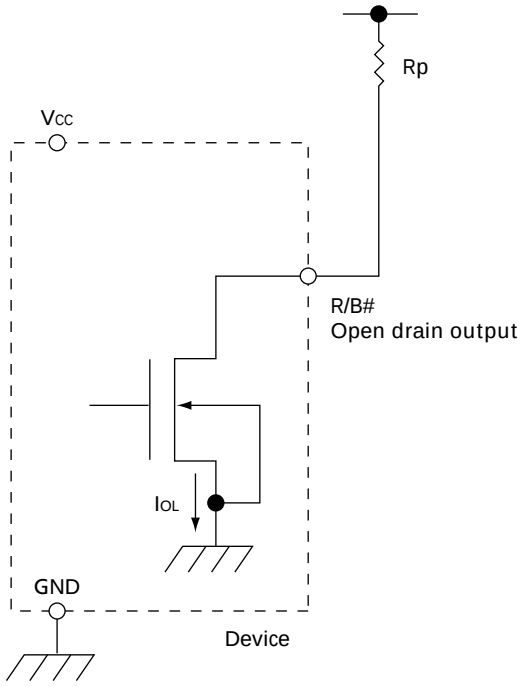
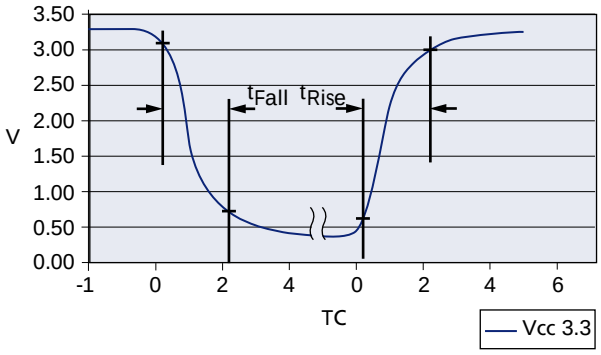
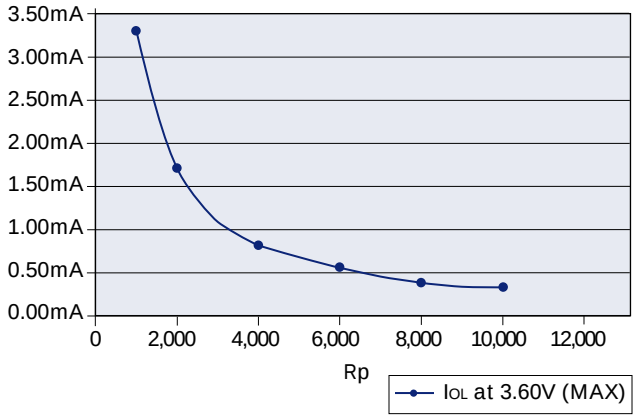


Figure 9: ^{t}Fall and ^{t}Rise



Notes:
1. ^{t}Fall and ^{t}Rise are calculated at 10 percent–90 percent points.
2. ^{t}Rise is dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall ≈ 10ns at 3.3V.
5. See TC values in Figure 11 on page 18 for approximate Rp value and TC.

Figure 10: I_{OL} vs. Rp



Note: To calculate Rp value, see page 16.

Figure 11: TC vs. Rp

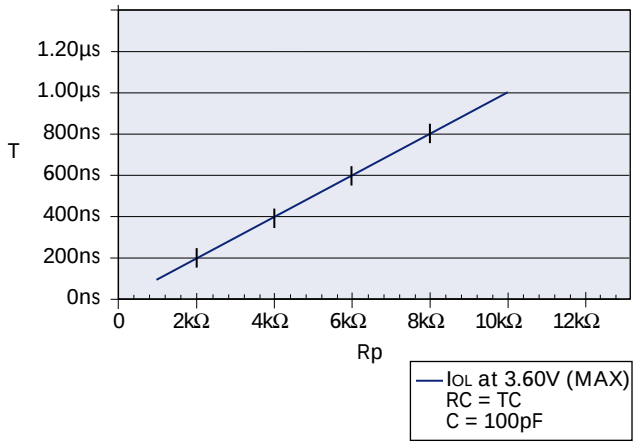


Table 5: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#[1]	Mode	
H	L	L	↑	H	X	Read mode	Command input
L	H	L	↑	H	X		Address input
H	L	L	↑	H	H	Write mode	Command input
L	H	L	↑	H	H		Address input
L	L	L	↑	H	H	Data input	
L	L	L	H	↓	X	Sequential read and data output	
X	X	X	X	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/V_{CC}	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Command Definitions

Table 6: Command Set

Operation	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	
PAGE READ CACHE MODE	31h	–	No	–	No	2
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	2
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	3
RANDOM DATA READ	05h	2	No	E0h	No	4
READ ID	90h	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	3
RANDOM DATA INPUT	85h	2	Yes	–	No	5
BLOCK ERASE	60h	3	No	D0h	No	
RESET	FFh	–	No	–	Yes	

Notes: 1. Indicates required DATA cycles between COMMAND cycle 1 and COMMAND cycle 2.
2. Do not cross block address boundaries when using PAGE READ CACHE MODE operations. See Table 4 on page 14 for die address boundary definitions.
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE. See Table 4 on page 14 for die address boundary definitions.
4. RANDOM DATA READ command is limited to use within a single page.
5. RANDOM DATA INPUT command is limited to use within a single page.

Table 7: Two-Plane Command Set

Operation	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	2
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h	5	10h	No	
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h	5	15h	No	3
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-80h	5	10h	No	1
TWO-PLANE BLOCK ERASE	60h	3	60h	3	D0h	No	

Notes: 1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE and TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Table 4 on page 14 for die address boundary definitions.
2. TWO-PLANE RANDOM DATA READ command is limited to use within a single page.
3. Do not cross block address boundaries when using cache operations. See Table 4 on page 14 for die address boundary definitions.

READ Operations

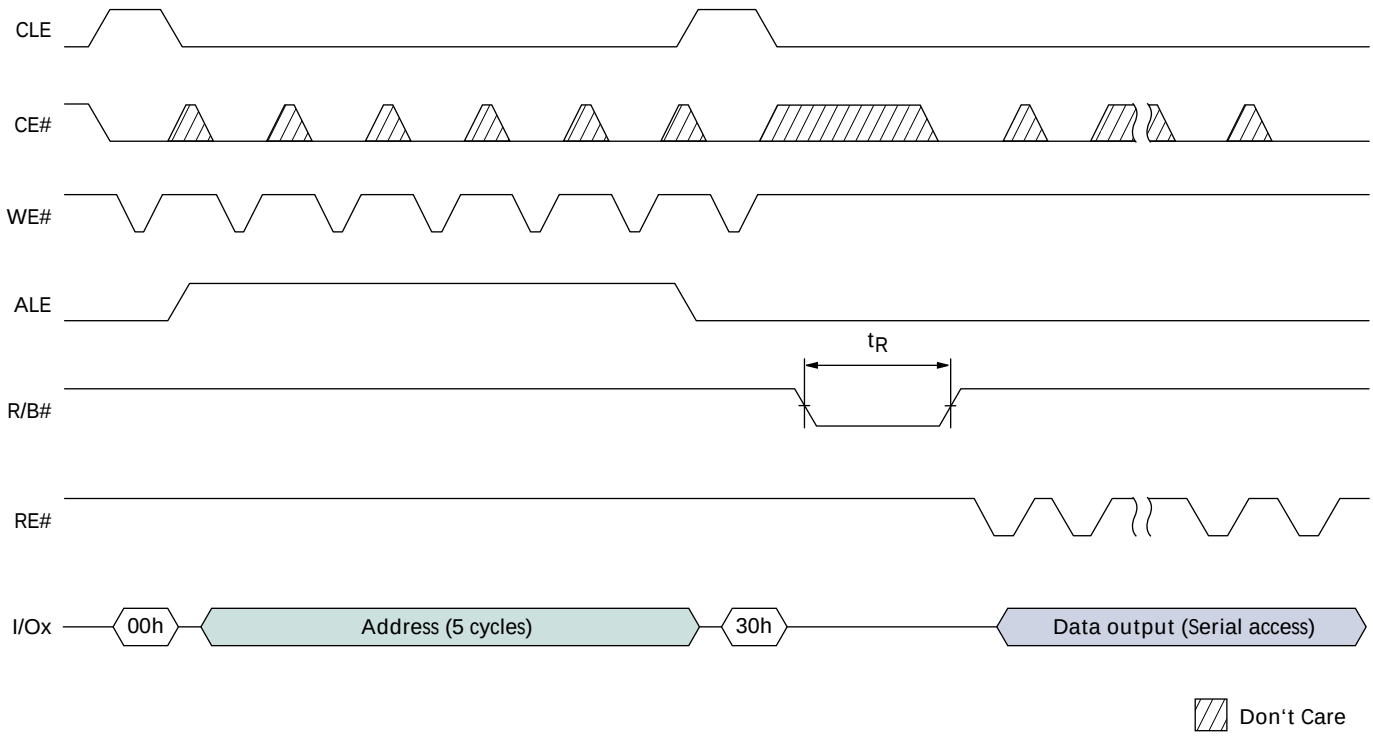
PAGE READ 00h-30h

To enter READ mode while the device is in operation, write the 00h command to the command register, then write 5 address cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the Flash array to the data register (^{t}R), monitor the R/B# signal, or, alternatively, issue a READ STATUS command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register (see Figure 72 on page 78 and Figure 73 on page 79 for examples). After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address and going to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 12).

Figure 12: PAGE READ Operation



RANDOM DATA READ 05h-E0h

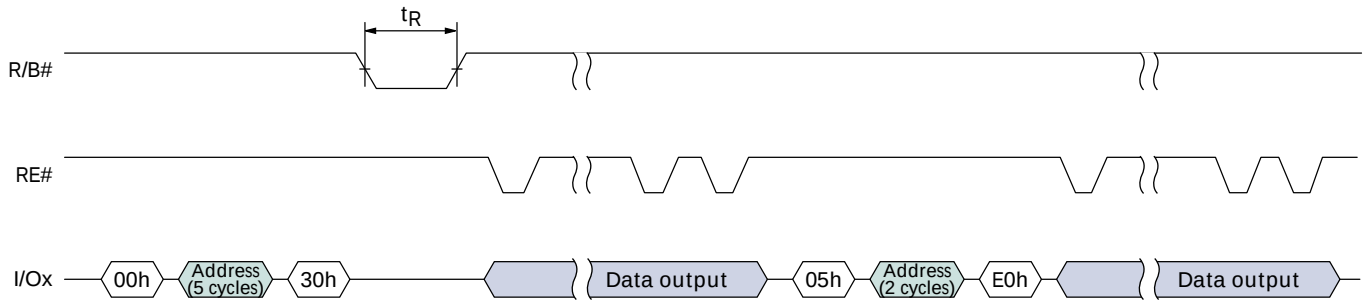
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h sequence).

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing RE# outputs data sequentially (see Figure 13).

Figure 13: RANDOM DATA READ Operation



PAGE READ CACHE MODE Start 31h; PAGE READ CACHE MODE Start Last 3Fh

Micron NAND Flash devices have a cache register that can be used to increase the READ operation speed when accessing sequential pages in a block.

First, a normal PAGE READ (00h-30h) command sequence is issued (see Figure 14 on page 25 for operation details). The R/B# signal goes LOW for ^{t}R during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into the command register. R/B# goes LOW for ^{t}DCBSYR1 while data is being transferred from the data register to the cache register. After the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing of RE#) from the cache register. If the total time to output data exceeds ^{t}R, then the PAGE READ is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to ^{t}DCBSYR2. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuance of the next 31h command (see Table 18 on page 69 for timing parameters). If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

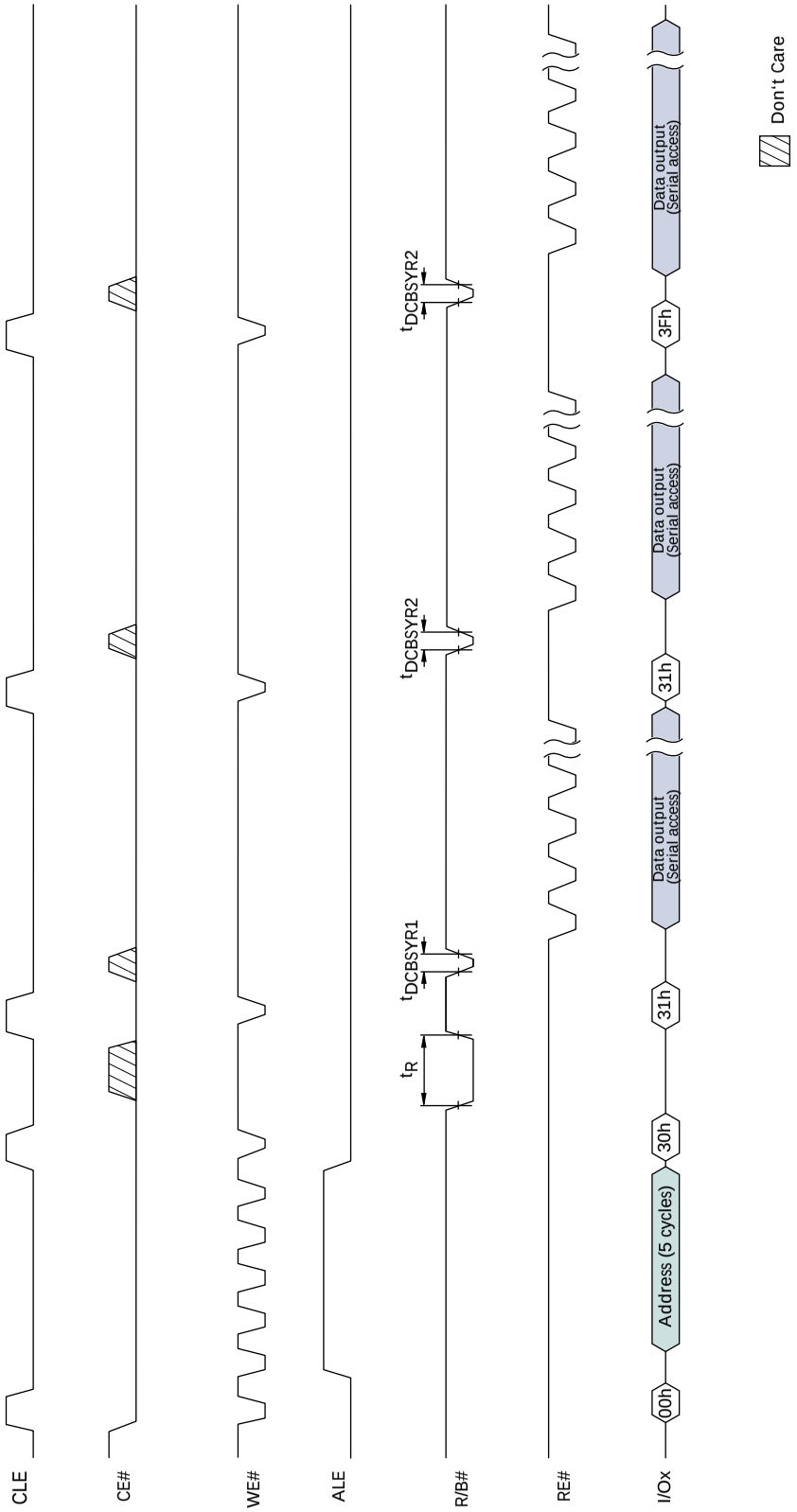
To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ (see Figure 14 on page 25).

Random DATA READ commands are permitted during a PAGE READ CACHE MODE operation.

PAGE READ CACHE MODE cannot be used to cross block boundaries.

If monitoring the progress of PAGE READ CACHE MODE via the read status register, use only READ STATUS (70h) commands. TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) commands are not supported during a PAGE READ CACHE MODE operation.

Figure 14: PAGE READ CACHE MODE

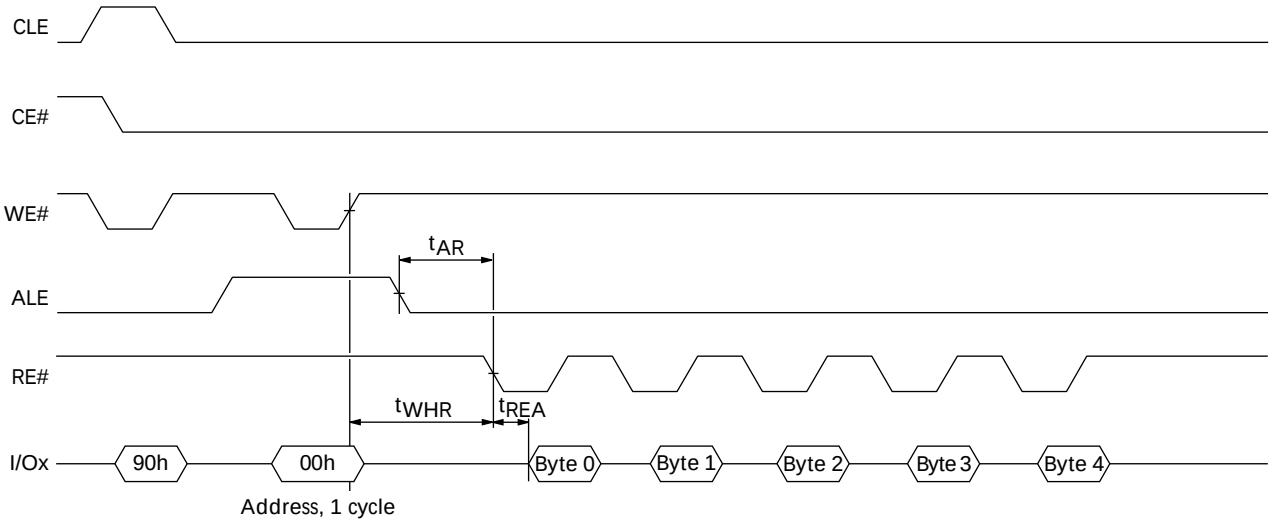


READ ID 90h

The READ ID command is used to read the 5 bytes of identifier codes programmed into the devices. The READ ID command reads a 5-byte table that includes manufacturer's ID, device configuration, and part-specific information. See Table 8 on page 27, which shows complete listings of all configuration details.

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see Figure 15**).**

Figure 15: READ ID Operation



Note: See Table 8 on page 27 for byte definitions.

Table 8: Device ID and Configuration Codes

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
MT29F8G08MAA	8Gb, x8, 3.3V	1	1	0	1	0	0	1	1	D3h	
MT29F16G08QAA	16Gb, x8, 3.3V	1	1	0	1	0	0	1	1	D3h	2
MT29F32G08TAA	32Gb, x8, 3.3V	1	1	0	1	0	1	0	1	D5h	
Byte 2											
Number of die per CE	1							0	0	00b	
	2							0	1	01b	
Cell type	MLC					0	1			00b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	MT29F8Gxx	1	0	0	1	0	1	0	0	94h	
	MT29F16Gxx	1	0	0	1	0	1	0	0	94h	
	MT29F32Gxx	1	1	0	1	0	1	0	1	D5h	
Byte 3											
Page size	2KB							0	1	01b	
Spare area size (bytes)	64B						1			1b	
Block size (w/o spare)	256KB			1	0					10b	
Organization	x8		0							0b	
Serial access (MIN)	50ns/30ns	0				0				0xxx0b	
	25ns	1				0				1xxx0b	
Byte value	MT29FxG08	1	0	1	0	0	1	0	1	A5h	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane size	4Gb		1	1	0					110b	
Reserved		0								0b	
Byte value	MT29F8Gxx	0	1	1	0	0	1	0	0	64h	
	MT29F16Gxx	0	1	1	0	0	1	0	0	64h	2
	MT29F32Gxx	0	1	1	0	1	0	0	0	68h	

Notes: 1. b = binary; h = hex.
2. The MT29F16Gxx device ID code reflects the configuration of each 8Gb section.

READ STATUS 70h

These NAND Flash devices have an 8-bit status register that the software can read during device operation. Table 9 describes the status register.

After a READ STATUS (70h) command, all READ cycles are from the status register until a new command is given. Changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ cycle to see these changes.

In devices that have more than one die sharing a common CE# connection, the READ STATUS (70h) command reports the status of the die that was last addressed. If concurrent operations are started on both die, then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will respond until the next operation is issued.

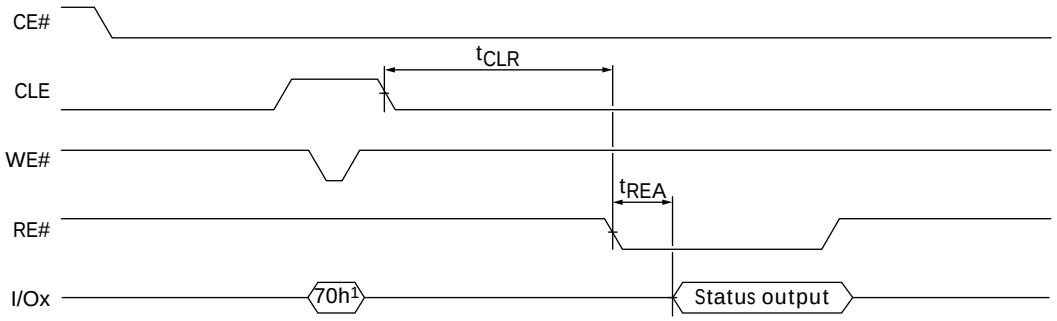
While monitoring the read status to determine when the transfer from the Flash array to the data register (^{t}R) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 9: Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0[1]	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N -1)	–	–	–	0 = Successful PROGRAM 1 = Error in PROGRAM
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy[2]	Ready/busy	Ready/busy[2]	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	0 = Busy 1 = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected

Notes:
1. Status register bit 0 reports a “1” if a TWO-PLANE PROGRAM operation fails on one or both planes. Status register bit 1 reports a “1” if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) to determine the plane on which the operation failed.
2. Status register bit 5 is “0” during the actual programming operation. If cache mode is used, this bit will be “1” when all internal operations are complete.
3. Status register bit 6 is “1” when the cache is ready to accept new data. R/B# follows bit 6 (see Figure 14 on page 25 and Figure 19 on page 31).

Figure 16: Status Register Operation



Notes: 1. Command can be 70h or 78h.

PROGRAM Operations

PROGRAM PAGE 80h-10h

Micron NAND Flash devices are inherently page-programmed devices. Within a block, the pages must be programmed consecutively from the least significant page address to the most significant page address. Random page address programming is prohibited.

These MLC NAND Flash devices do not support partial-page programming operations—a page can only be programmed one time before requiring an ERASE operation.

If a RESET (FFh) command is issued during a PROGRAM PAGE operation while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting a programming operation on one page could corrupt the data in another page within the block being programmed.

SERIAL DATA INPUT 80h

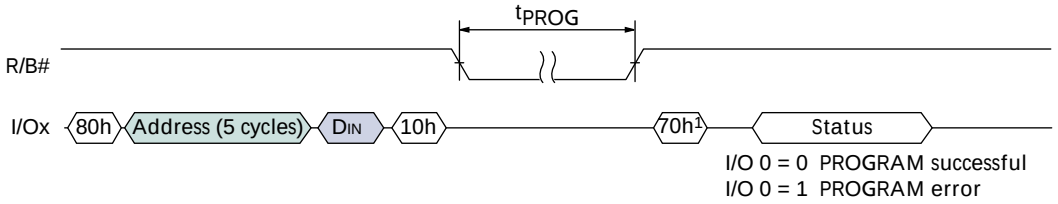
PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by 5 address cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h, 78h) and the RESET (FFh) commands are the only commands valid during the programming operation. Bit 5 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the programming operation passed or failed (see Figure 17). The command register stays in read status register mode until another valid command is written to it.

RANDOM DATA INPUT 85h

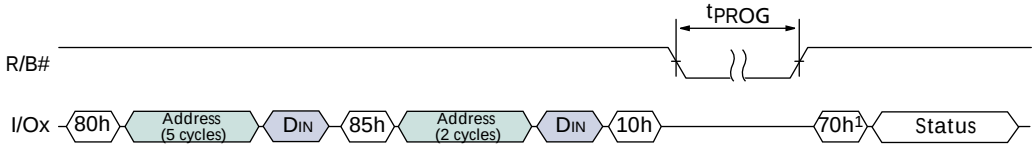
After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuance of the PAGE WRITE (10h) command. See Figure 18 for the proper command sequence.

Figure 17: PROGRAM and READ STATUS Operation



Notes: 1. Command can be 70h or 78h.

Figure 18: RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h.

PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by 5 cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE WRITE (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

The PROGRAM PAGE CACHE MODE command can cross block boundaries; it cannot cross die boundaries. RANDOM DATA INPUT commands are allowed during PROGRAM PAGE CACHE MODE operations.

Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h, 78h) commands to determine when the cache register is ready to accept new data. R/B# always follows bit 6.

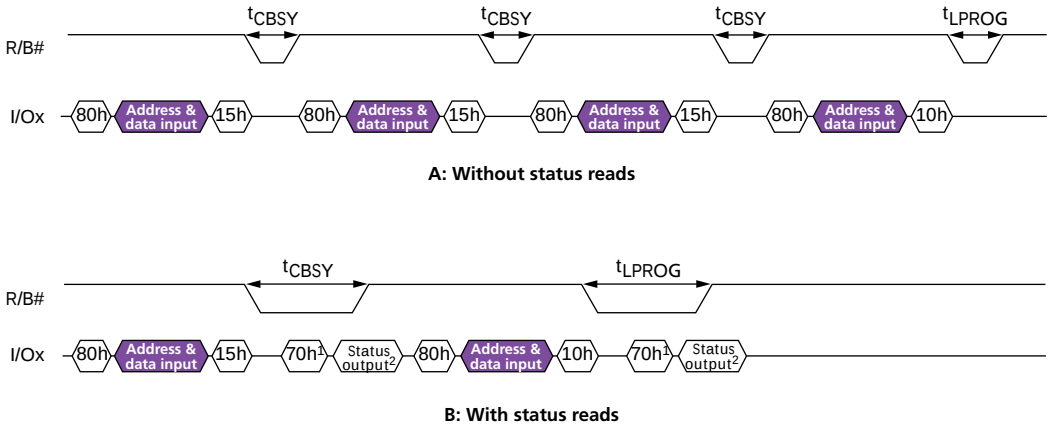
Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just R/B# is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 19 on page 31).

Bit 0 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a "1" (ready state) (see Figure 19).

If a RESET (FFh) command is issued during a PROGRAM PAGE CACHE MODE operation while R/B# or bit 5 or bit 6 of the status register is LOW, the data in the shared memory cells being programmed could become invalid. Interruption of a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 19: PROGRAM PAGE CACHE MODE Example



Notes: 1. Command can be 70h or 78h.
2. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass/fail. RE# can stay LOW or pulse multiple times after a 70h or 78h command.

Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. Data moves are only supported within the plane from which data is read.

READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (5 cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

The written column addresses are ignored even though all 5 address cycles are required.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Please refer to the description of this command in the following section.

PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register, and programming of the new destination page begins. The sequence: 85h, destination address (5 cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS commands and bit 6 of the status register can be used instead of the R/B# line to determine when the write is complete. Bit 0 of the status register indicates if the operation was successful.

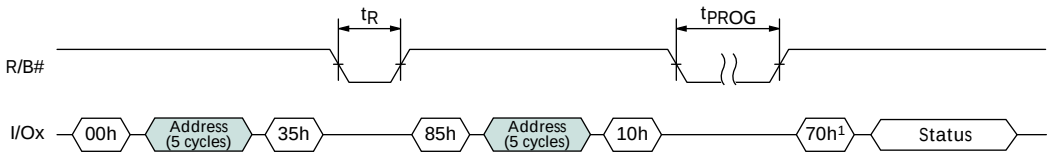
The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figures 20 and 21 on page 33).

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. If multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that can correct more than the minimum 4 bits per sector required.

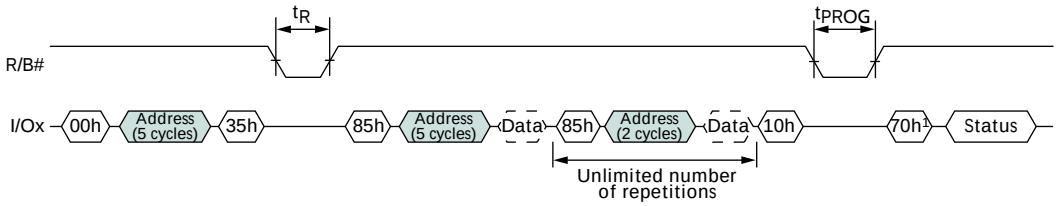
If a RESET (FFh) command is issued during a PROGRAM for INTERNAL DATA MOVE operation while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting a programming operation on one page could corrupt the data in another page within the block being programmed.

Figure 20: INTERNAL DATA MOVE



Notes: 1. Command can be 70h or 78h.

Figure 21: INTERNAL DATA MOVE with RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h.

BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

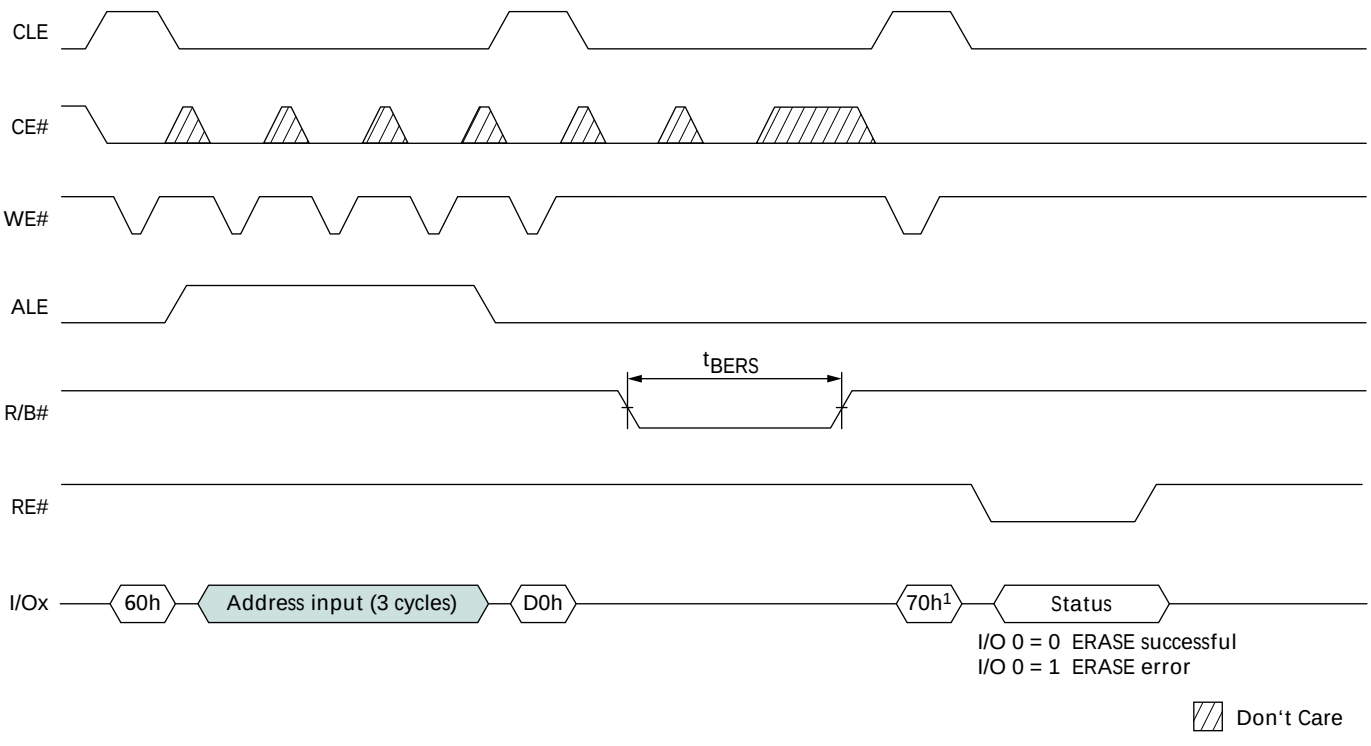
Erasing occurs at the block level. The MT29F8G, MT29F16G, and MT29F32G devices have 4,096, 8,192, and 16,384 blocks, respectively. These blocks are organized into 128 pages per block, 2,112 bytes per page (2,048 + 64 bytes). Each block is 264K bytes (256K + 8K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 22).

Three cycles of addresses [PA0–BA18] are required for 8Gb and 16Gb devices, and 3 cycles of addresses [PA0–BA19] are required for 32Gb devices. Although [PA0–PA6] are loaded, they are a "Don't Care" and are ignored for BLOCK ERASE operations, since these bits normally specify the page address within a block. See Figure 5 on page 12 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then 3 cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h, 78h) commands can be used to check the status of the error. When bit 6 = 1, the ERASE operation is complete. Bit 0 indicates a pass/fail condition where 0 = pass (see Figure 22, and Table 9 on page 28).

Figure 22: BLOCK ERASE Operation



Notes: 1. Command can be 70h or 78h.

Two-Plane Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 2,112-byte data register, a 2,112-byte cache register, and a 2,048-block Flash array. Two-plane commands make better use of the Flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, significantly improving system performance.

Two-Plane Addressing

Two-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit (BA7), must be different for each address.
- The most significant block address bit for 32Gb devices (BA19), must be identical for both addresses.
- The page address bits, PA[6:0], must be identical for both addresses.

TWO-PLANE PAGE READ 00h-00h-30h

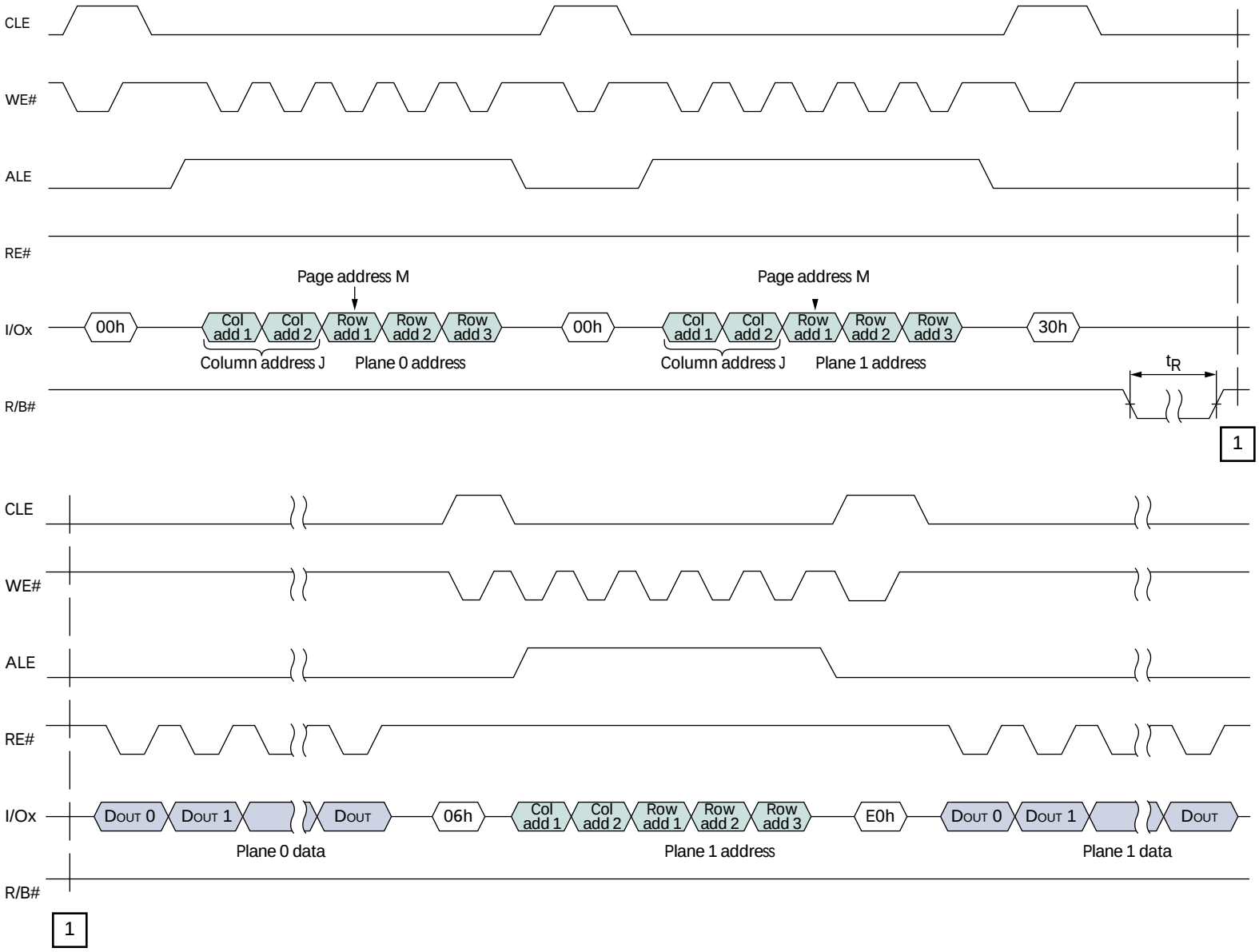
The TWO-PLANE PAGE READ (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfer two pages of data from the Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the TWO-PLANE PAGE READ mode, write the 00h command to the command register, then write 5 address cycles for plane 0 (BA7 = 0). Next, write the 00h command to the command register, then write 5 address cycles for plane 1 (BA7 = 1). Finally, issue the 30h command. The first plane and second plane addresses must meet the two-plane addressing requirements, and, in addition, they must have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# returns HIGH. To read out the data from the first plane data register, pulse RE#. After the DATA cycle from the plane address completes, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the second-plane address, then pulse RE# to read out the data from the second-plane data register. Alternatively, the READ STATUS (70h) command can monitor the data transfers. When the transfers are complete, status register bit 6 is set to “1.”

To read data from one of the two planes, the user must first issue the TWO-PLANE RANDOM DATA READ (06h-E0h) command, followed by 5 address cycles (see Figure 23 on page 36). To read out data from the plane and column address specified by the TWO-PLANE RANDOM DATA READ command, pulse RE#. When the DATA cycle is complete, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE#.

Figure 23: TWO-PLANE PAGE READ



Notes: 1. Column and page addresses must be the same.
2. The least significant block address bit must not be the same for the first- and second-plane addresses.

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TWO-PLANE RANDOM DATA READ 06h-E0h

The TWO-PLANE RANDOM DATA READ (06-E0h) command selects a plane and column address from which to read data after a TWO-PLANE PAGE READ (00h-00h-30h) command.

To issue a TWO-PLANE RANDOM DATA READ command, issue the 06h command, then 5 address cycles, and follow with the E0h command. Pulse RE# to read data from the new plane beginning at the specified column address.

The primary purpose of the TWO-PLANE RANDOM DATA READ command is to select a new plane and column address within that plane. If a new plane does not need to be selected, then the RANDOM DATA READ (05h-E0h) command can be used instead. See Figure 24 on page 38.

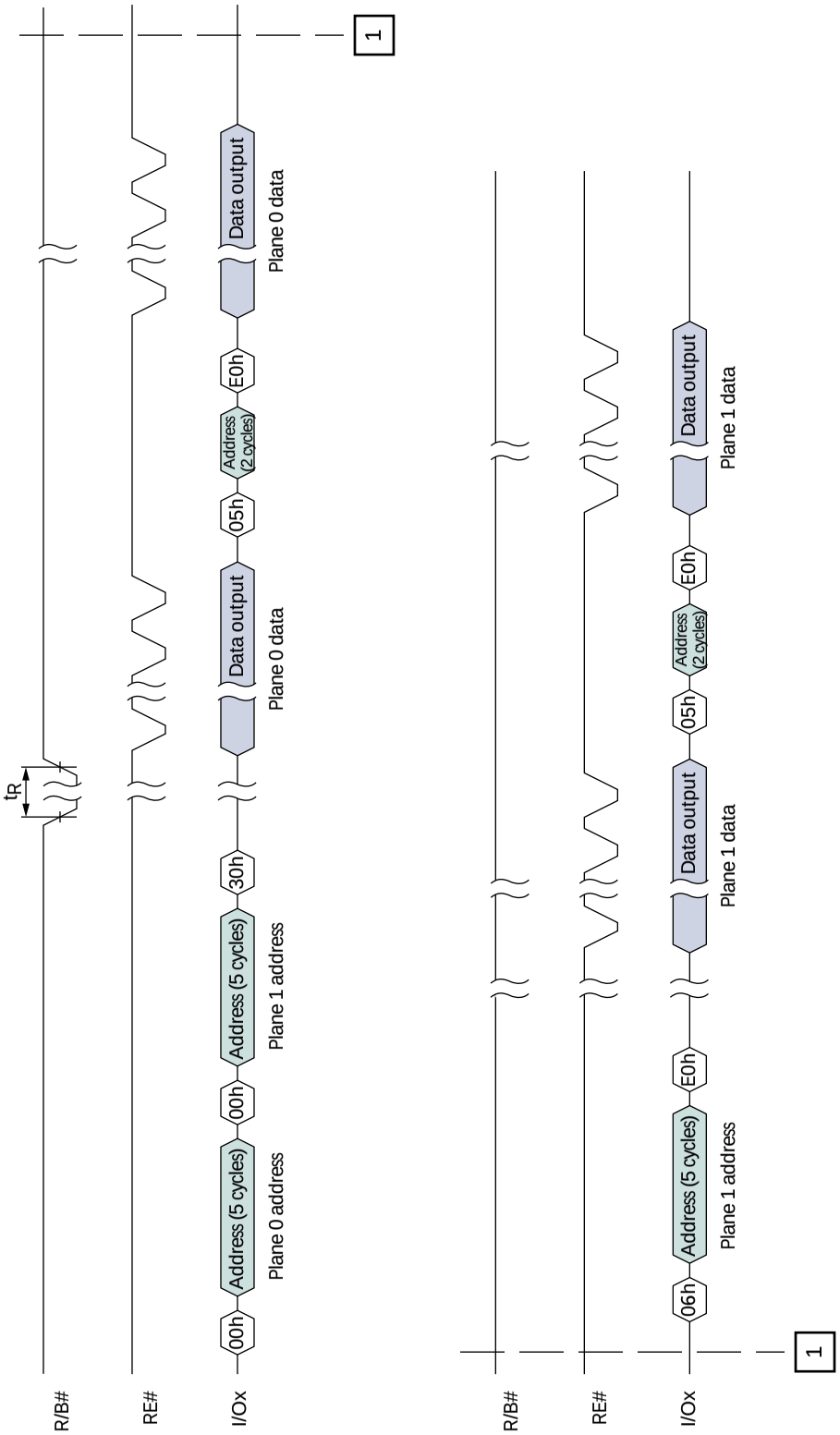


Figure 24: TWO-PLANE PAGE READ with RANDOM DATA READ

TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h

The TWO-PLANE PROGRAM PAGE operation is similar to the PROGRAM PAGE (80h-10h) operation. It programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first plane address and the second plane address must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 35).

To begin the TWO-PLANE PROGRAM PAGE operation, write the 80h command, followed by 5 address cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles, starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h, 78h) commands also indicate that the device is ready when the status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command, followed by 5 address cycles for the second plane; then write the data. The PROGRAM (10h) command is written after the second plane data input is complete.

After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. PROGRAM verification only detects "1s" that are not successfully written to "0s."

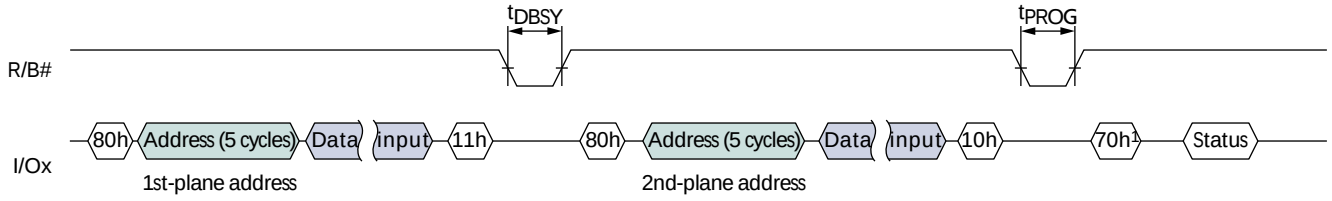
R/B# goes LOW for the duration of the array programming time (^{t}PROG). When programming and verification are complete, R/B# returns HIGH. The READ STATUS commands also indicate that the device is ready when the status register bit 6 is set to "1." The only valid commands during ^{t}PROG are the READ STATUS (70h, 78h) commands and RESET (FFh).

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) operation while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting a programming operation on one page could corrupt the data in another page within the blocks being programmed.

If a READ STATUS command indicates an error in the operation (status register bit 0 = 1), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operations failed.

During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane's page. See Figure 25 for more details on TWO-PLANE PROGRAM PAGE operation.

Figure 25: TWO-PLANE PROGRAM PAGE

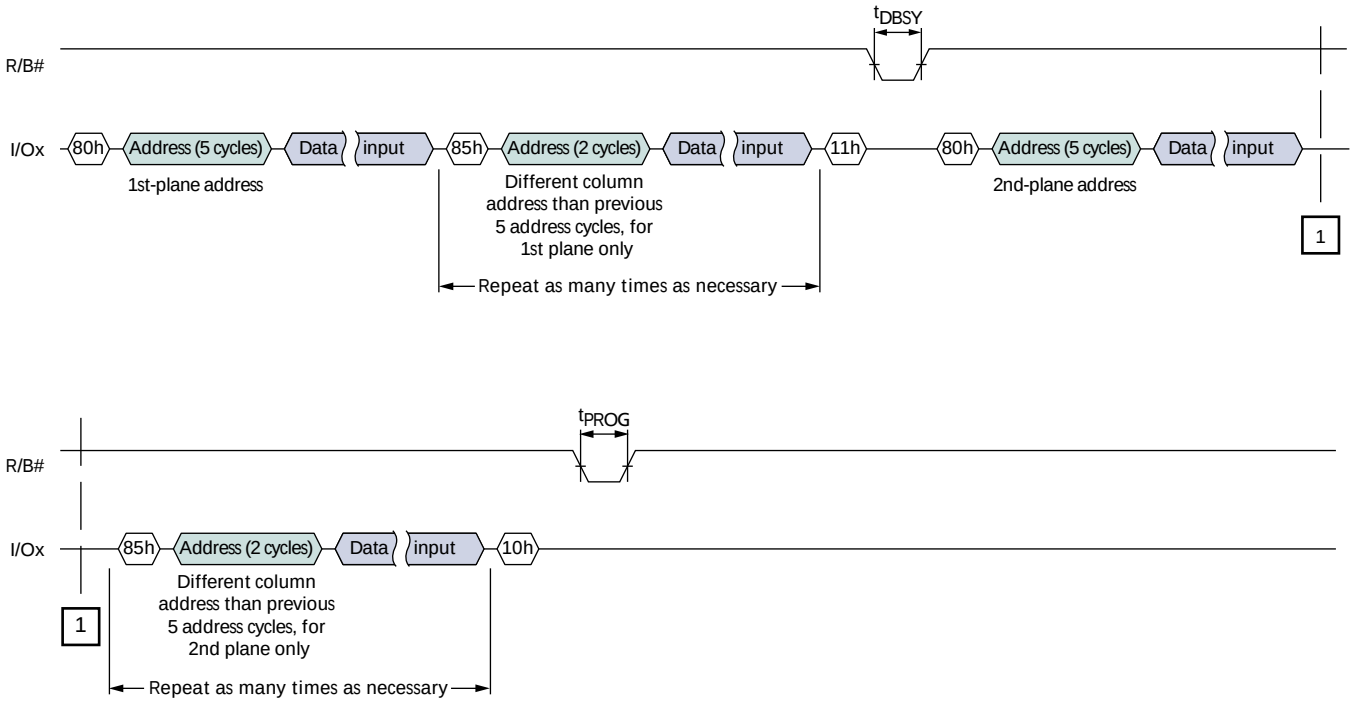


Notes: 1. Command can be 70h or 78h.

TWO-PLANE RANDOM DATA INPUT 80h-85h-11h (or 80h-85h-10h)

After the initial data set is input, additional data can be written to a new column address in the data register with the TWO-PLANE RANDOM DATA INPUT (85h) command. The TWO-PLANE RANDOM DATA INPUT command can be used any number of times. It can be used while inputting data to either plane. See Figure 26 for the proper command sequence.

Figure 26: TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT



TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h

The TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) operation is similar to the PROGRAM PAGE CACHE MODE (80h-15h) operation. It cache programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first plane and second plane address must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 35).

To enter the TWO-PLANE PROGRAM PAGE CACHE MODE, write the 80h command to the command register, write 5 address cycles for the first plane, then write the data. Serial data is loaded on consecutive WE# cycles, starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1."

The PROGRAM PAGE CACHE MODE command can cross block boundaries; it cannot cross die boundaries.

The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh). After ^{t}DBSY, write the 80h command to the command register, write 5 address cycles for the second plane, then write the data. The CACHE WRITE (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers and R/B# returns HIGH, memory array programming to both planes begins.

When R/B# returns HIGH, new data can be written to the cache registers by issuing another TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) sequence. The time that R/B# stays LOW (^{t}CBSY) is determined by the actual programming time of the previous operation. For the first cache operation, ^{t}CBSY duration is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent TWO-PLANE PROGRAM PAGE CACHE MODE operations, transfer from the cache registers to the data registers is delayed until the contents of the current data registers have been programmed into the arrays.

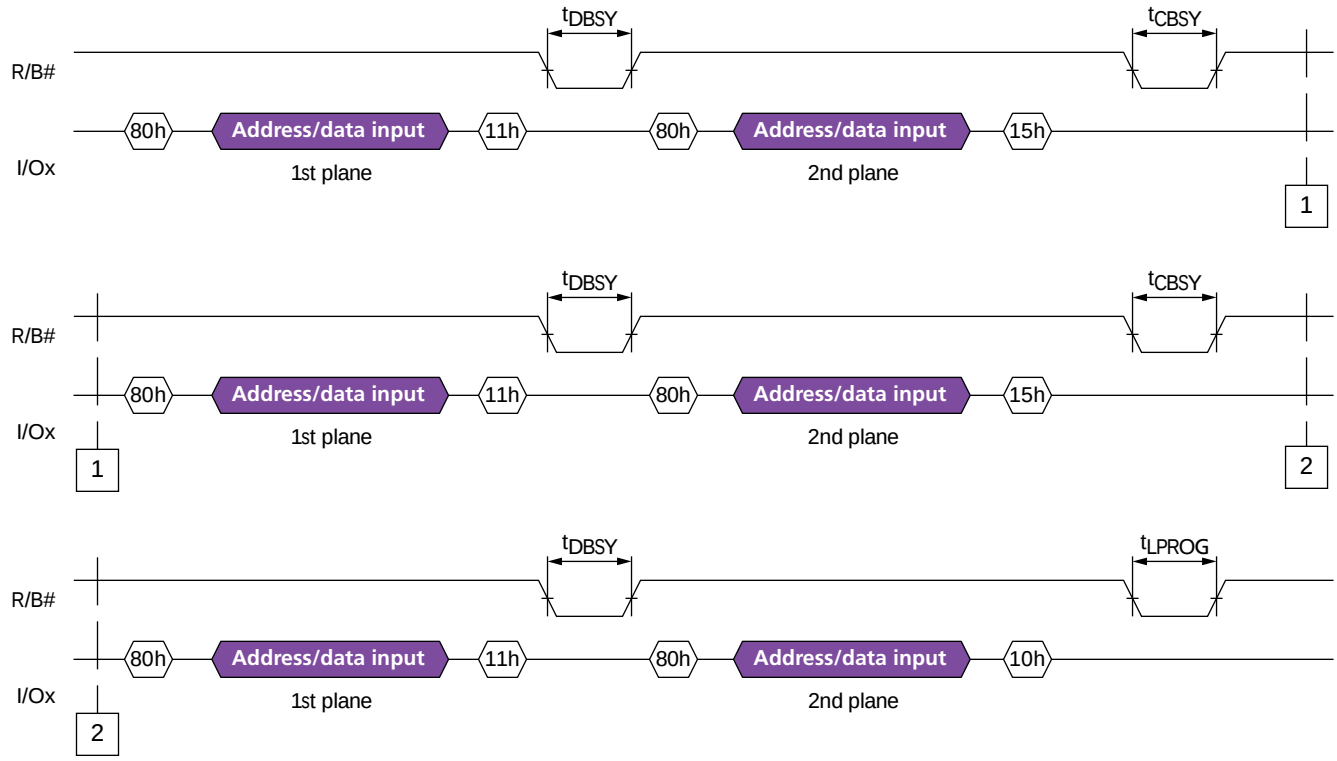
If R/B# is used to determine programming completion, the last operation of the program sequence must use the TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command instead of the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command. If the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command is used for the last operation, then use READ STATUS (70h, 78h) to monitor the operation's progress; status register bit 5 indicates when programming is complete.

To determine when the current TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-10h) operation has completed, issue the READ STATUS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 or bit 1 = 1, indicating a failed operation, then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which current or previous plane operation failed. For more information on status register bit definitions, see Table 9 on page 28.

During the serial data input for either plane, the TWO-PLANE RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane.

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE CACHE MODE operation while R/B# or bit 5 or bit 6 of the status register is LOW, the data in the shared memory cells being programmed could become invalid. Interruption of a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 27: TWO-PLANE PROGRAM PAGE CACHE MODE



TWO-PLANE INTERNAL DATA MOVE 00h-00h-35h/85h-11h-80h-10h

A TWO-PLANE INTERNAL DATA MOVE operation is similar to an INTERNAL DATA MOVE operation and requires two sequences. First, issue a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command, then issue the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command. Data moves are only supported within the planes from which data is read. The first plane and second plane addresses must meet the two-plane addressing requirements for both the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) and TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) commands (see “Two-Plane Addressing” on page 35).

TWO-PLANE READ for INTERNAL DATA MOVE 00h-00h-35h

The TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is used in conjunction with the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command. First, write 00h to the command register, then write the first plane internal source address (5 cycles). Again, write 00h to the command register, followed by

the second-plane internal source address (5 cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for ^{t}R while two pages are read into their respective cache registers.

The memory device is now ready to accept the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command.

TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-80h-10h

After the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command has been issued and R/B# goes HIGH (or the status register bit 6 = 1), the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first-plane destination address (5 cycles), then write 11h to the command register. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. A READ STATUS command also indicates that the device is ready when status register bit 6 is set to 1. The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register, then write the second-plane destination address (5 cycles), then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

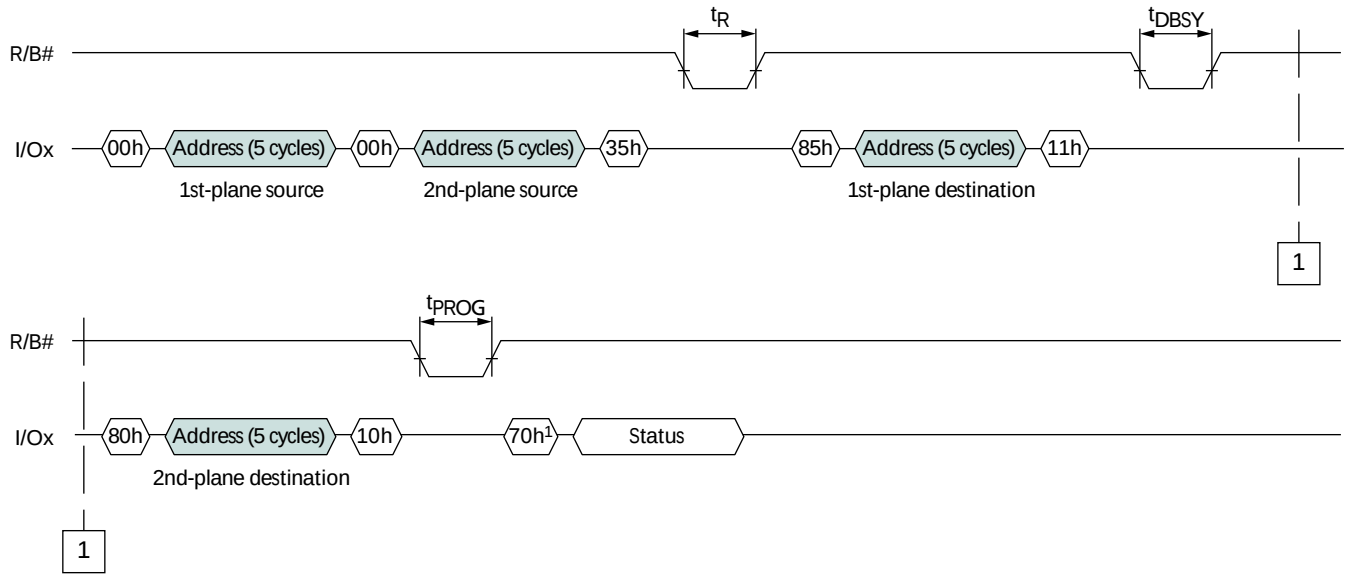
R/B# goes LOW for the duration of array programming time, ^{t}PROG. When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is "1." The only valid commands during ^{t}PROG are READ STATUS (70h, 78h) commands and RESET (FFh).

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) operation while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting a programming operation on one page could corrupt the data in another page within the blocks being programmed.

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = 1), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operation failed.

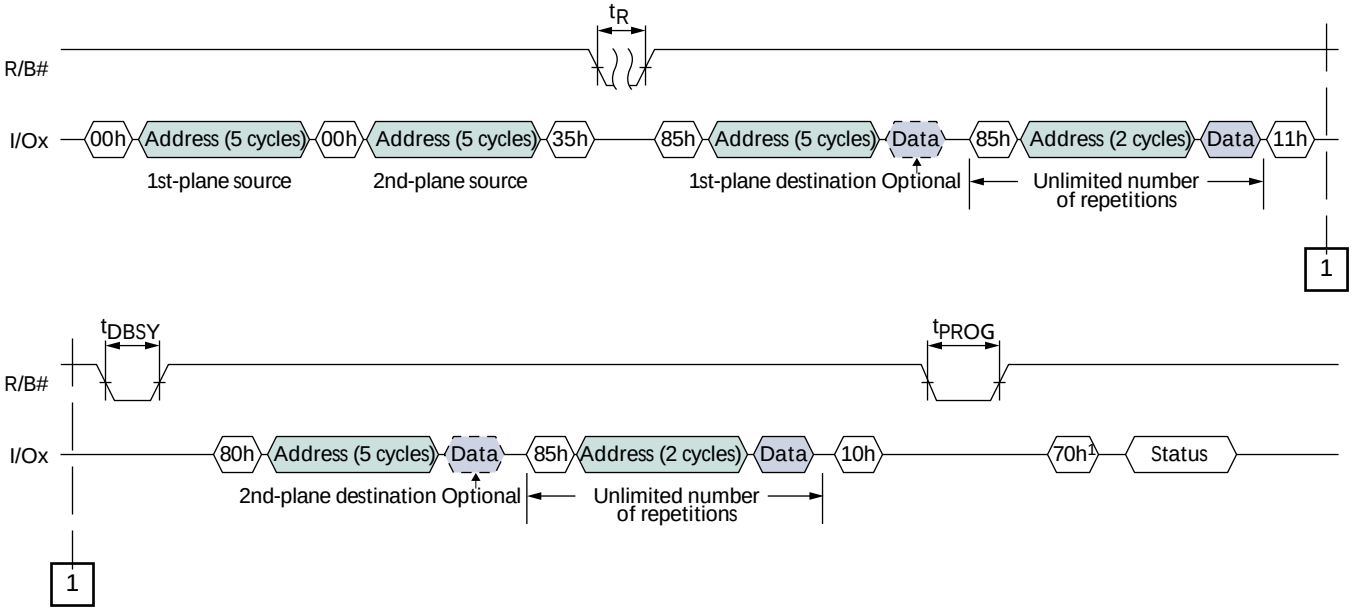
During the serial data input for either plane, the TWO-PLANE RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane. See Figure 29 on page 44 for an example.

Figure 28: TWO-PLANE INTERNAL DATA MOVE



Notes: 1. Command can be 70h or 78h.

Figure 29: TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h.

TWO-PLANE BLOCK ERASE 60h-60h-D0h

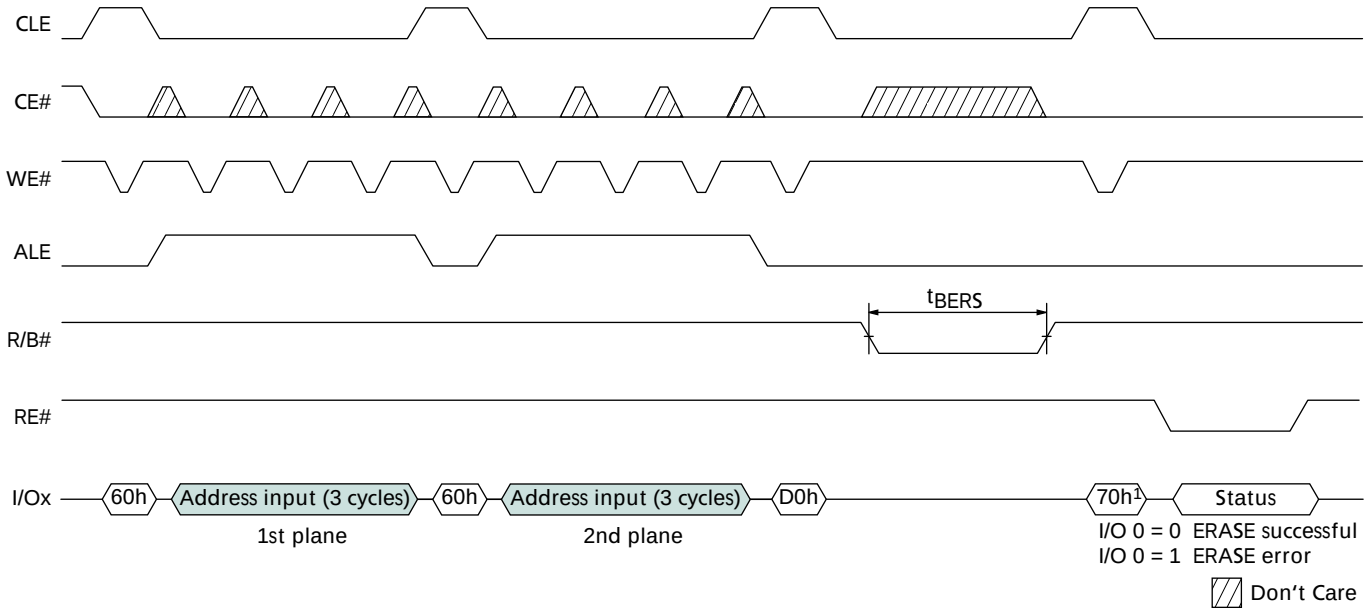
The TWO-PLANE BLOCK ERASE (60h-60h-D0h) operation is similar to the BLOCK ERASE (60h-D0h) operation. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first plane and second plane addresses must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 54). Additionally, the page addresses, PA[6:0], for both planes must be LOW.

Begin a TWO-PLANE BLOCK ERASE operation by writing 60h to the command register, followed by 3 address cycles of the first plane block address. Then write 60h again to the command register, followed by 3 address cycles of the second-plane block address. Finally, issue the D0h command.

R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erasure is complete, R/B# returns HIGH. A READ STATUS command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}BERS are READ STATUS (70h, 78h) and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = 1), then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—one time for each plane—to determine which plane operation failed.

Figure 30: TWO-PLANE BLOCK ERASE Operation



Notes: 1. Command can be 70h or 78h.

TWO PLANE/MULTIPLE-DIE READ STATUS 78h

In Micron NAND Flash devices that have two planes and possibly more than one die in a package that share the same CE# connection, it is possible to independently poll the status register of a particular plane and die using the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. This feature operates regardless of device size, organization, or status. This command can be used to check the status during and after two-plane operations.

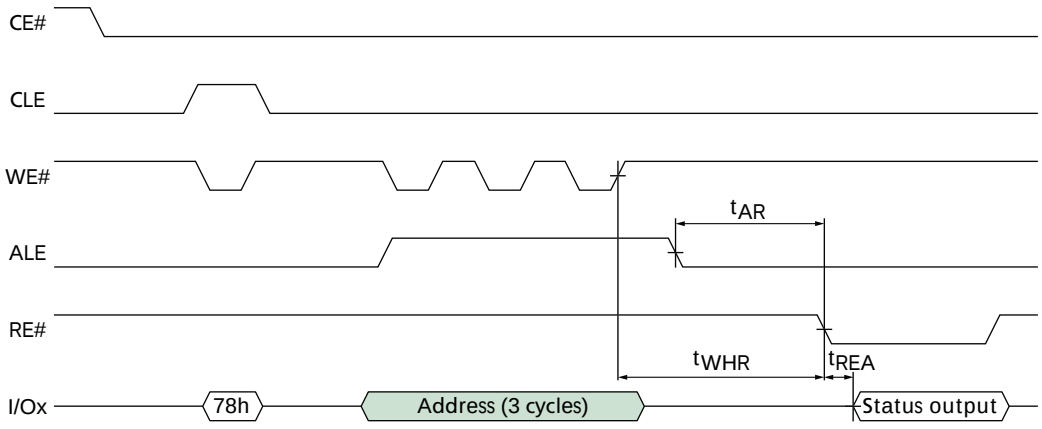
After the 78h command is issued, the device requires 3 address cycles containing the block and page addresses. The most significant block address bit in the third address cycle selects the proper die, and the least significant block address bit in the first address cycle selects the proper plane within that die.

After the 78h command and the 3 address cycles, the status register is output on I/O[7:0] when RE# is LOW. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to issue a new READ STATUS command to see these changes. The status register bit definitions are identical to those reported by the READ STATUS command (see Table 9 on page 28).

While monitoring the read status to determine when the transfer from the Flash array to the data register (^{t}R) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line could result in outputting data, starting from the initial column address.

The TWO-PLANE/MULTIPLE-DIE READ STATUS command may be used with all TWO-PLANE operations on one die.

Figure 31: TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



Interleaved Die Operations

In devices that have more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is "1"), issue a command to the first die. Then, while the first die is busy (R/B# is LOW), issue a command to the other die.

There are two methods to determine operation completion. The R/B# signal indicates when both die have finished their operations. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command can report the status of each die individually. If a die is performing a cache operation, like PROGRAM PAGE CACHE MODE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h), then the die is able to accept the data for another cache operation when status register bit 6 is "1." All operations, including cache operations, are complete on a die when status register bit 5 is "1."

During and following interleaved die operations, the READ STATUS (70h) command is prohibited. Instead, use the 78h command to monitor status. These commands select which die will report status. Interleaved two-plane commands must also meet the requirements in "Two-Plane Addressing" on page 35.

PAGE READ, TWO-PLANE PAGE READ, PROGRAM PAGE, PROGRAM PAGE CACHE MODE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, BLOCK ERASE, and TWO-PLANE BLOCK ERASE can be used in any combination as interleaved operations on separate die that share a common CE#.

Interleaved PAGE READ Operations

Figures 32 and 33 show how to perform two types of interleaved PAGE READ operations. In Figure 32, the R/B# signal is monitored for operation completion. In Figure 33 on page 48, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

In an interleaved PAGE READ operation, the TWO-PLANE/MULTIPLE-DIE RANDOM DATA READ (06h-E0h) command must be used before data is read from each die. The 06h-E0h command selects the die that will output data at the specified column address.

Figure 32: Interleaved PAGE READ with R/B# Monitoring

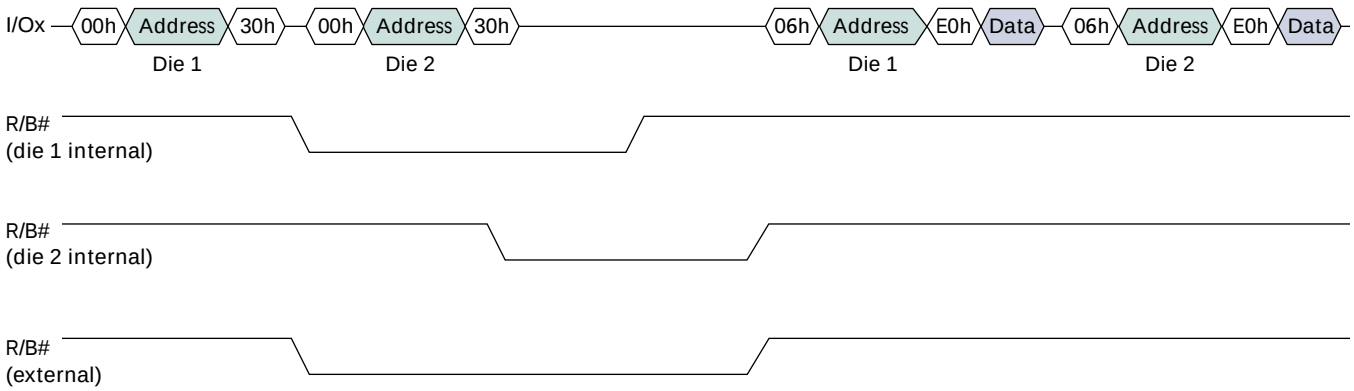
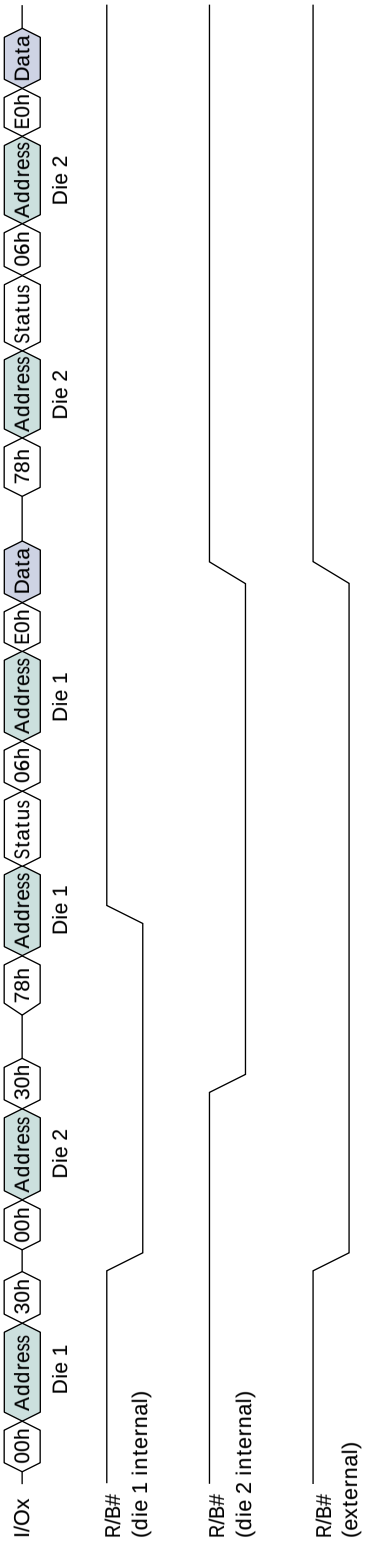


Figure 33: Interleaved PAGE READ with Status Register Monitoring



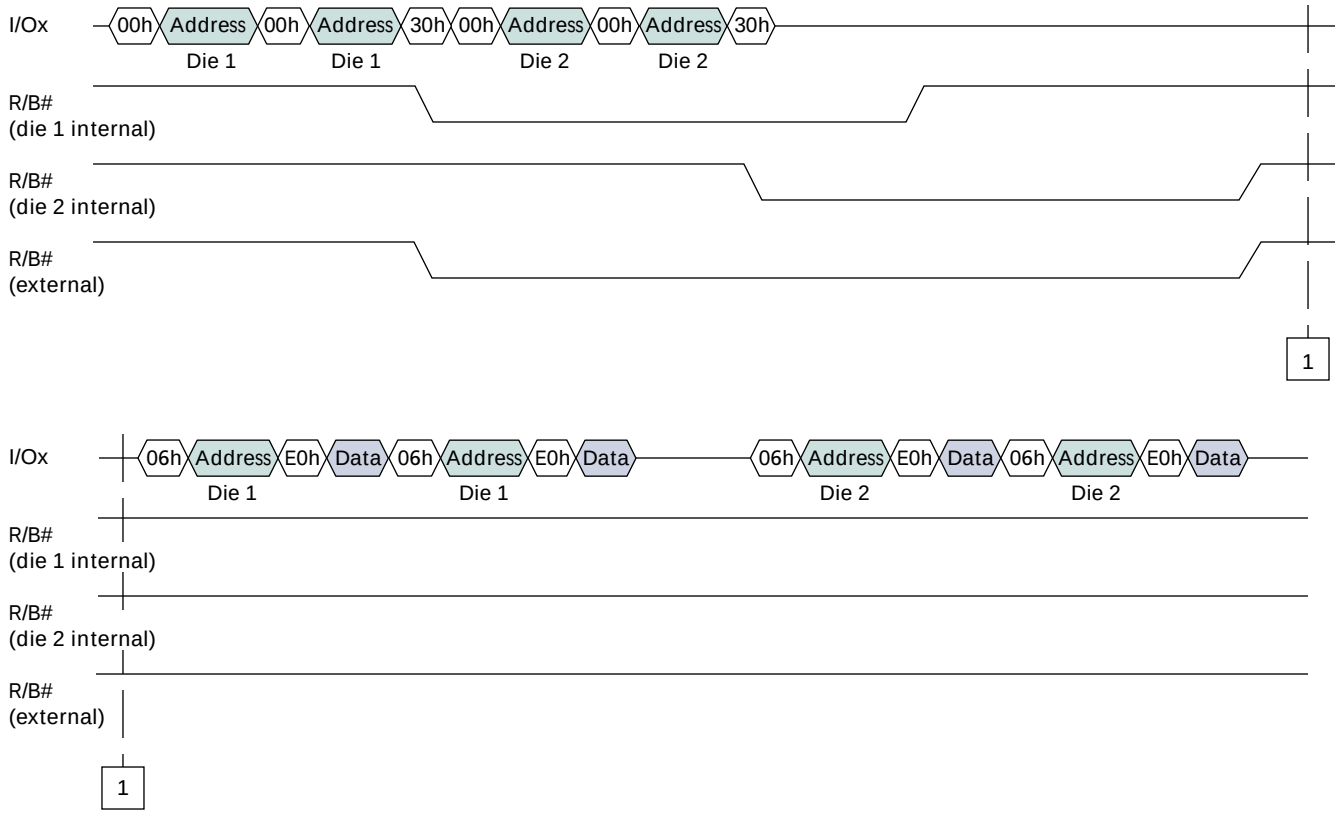
Interleaved TWO-PLANE PAGE READ Operations

Figures 34 and 35 show how to perform two types of interleaved TWO-PLANE PAGE READ operations. In Figure 34, the R/B# signal is monitored for operation completion. In Figure 35 on page 50, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

In an interleaved TWO-PLANE PAGE READ operation, the TWO-PLANE/MULTIPLE-DIE RANDOM DATA READ (06h-E0h) command must be used before data is read from each die and each plane. This command selects the die that will output data at the specified column address.

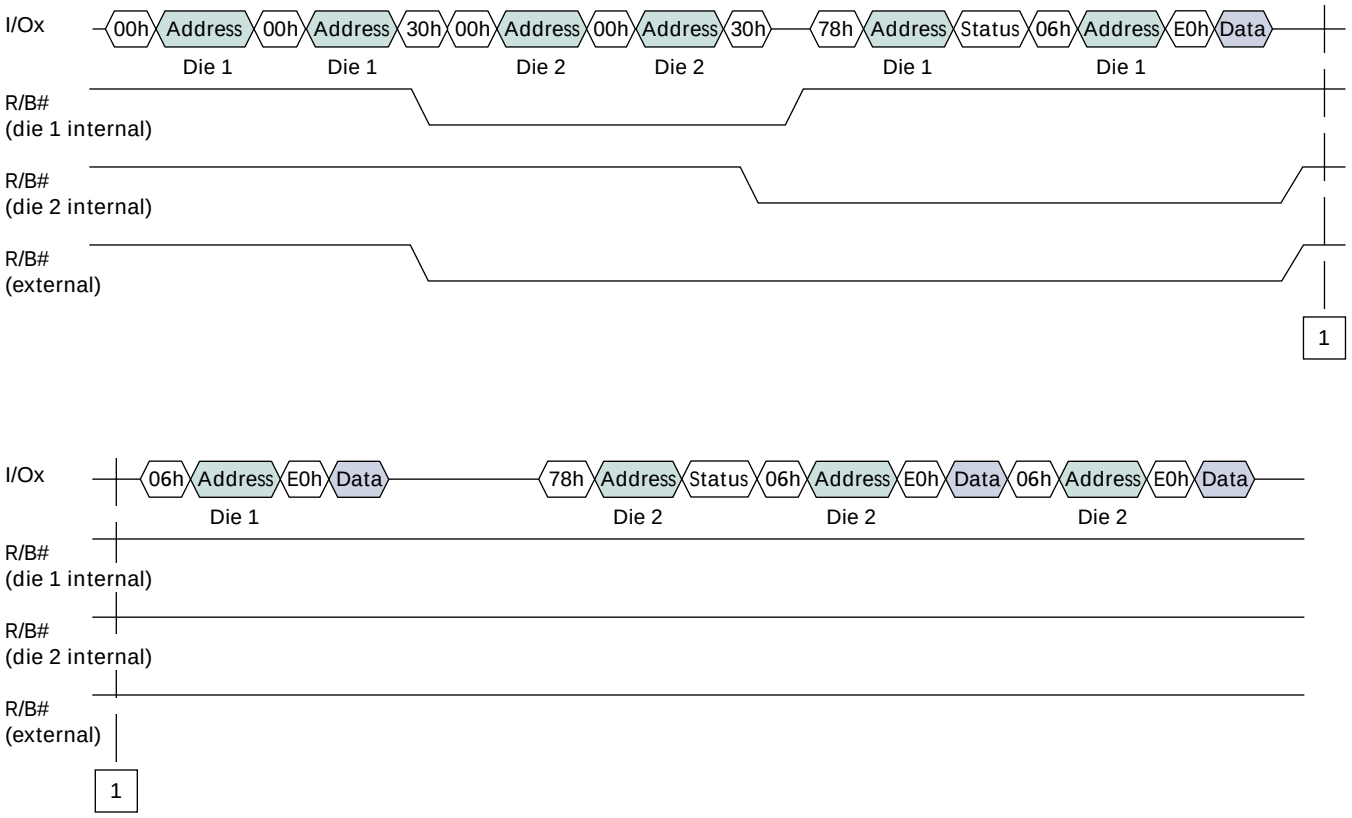
The interleaved TWO-PLANE PAGE READ operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 35 for details.

Figure 34: Interleaved TWO-PLANE PAGE READ with R/B# Monitoring



Notes: 1. Two-plane addressing requirements apply.

Figure 35: Interleaved TWO-PLANE PAGE READ with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

Interleaved PROGRAM PAGE Operations

Figures 36 and 37 show how to perform two types of interleaved PROGRAM PAGE operations. In Figure 36, the R/B# signal is monitored for operation completion. In Figure 37, the status register is monitored for operation completion with the TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE operations.

Figure 36: Interleaved PROGRAM PAGE with R/B# Monitoring

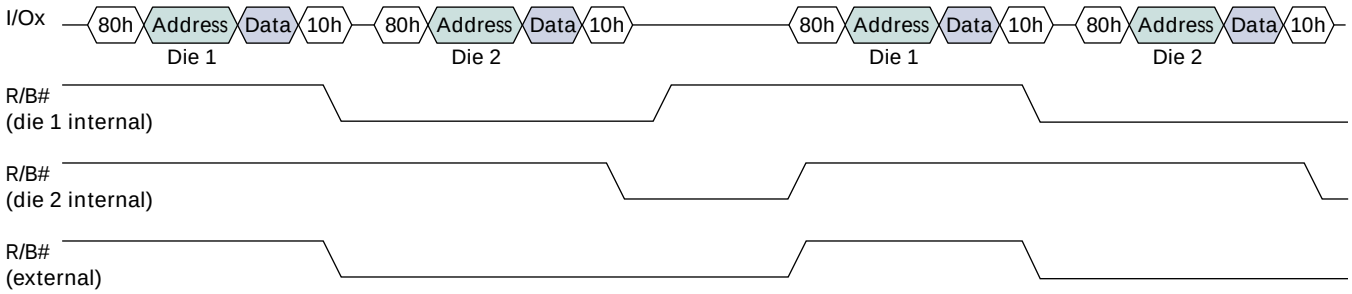
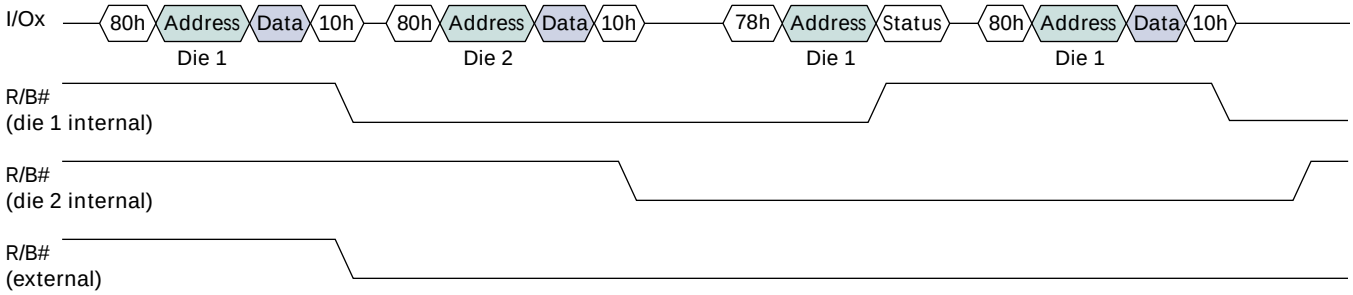


Figure 37: Interleaved PROGRAM PAGE with Status Register Monitoring



Interleaved PROGRAM PAGE CACHE MODE Operations

Figures 38 and 39 show how to perform two types of interleaved PROGRAM PAGE CACHE MODE operations. In Figure 38, the R/B# signal is monitored. In Figure 39, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE CACHE MODE operations.

Figure 38: Interleaved PROGRAM PAGE CACHE MODE with R/B# Monitoring

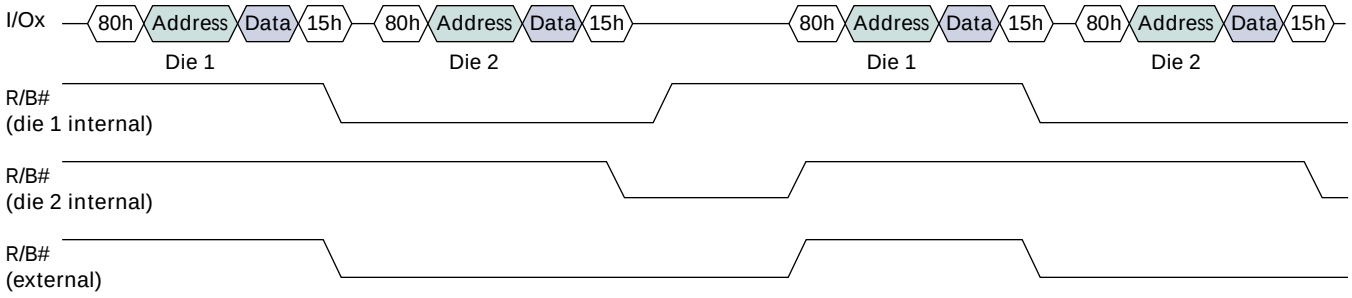
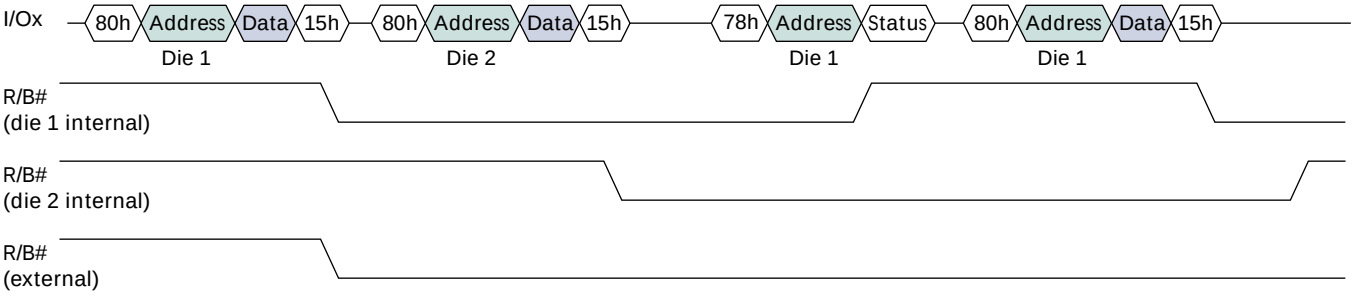


Figure 39: Interleaved PROGRAM PAGE CACHE MODE with Status Register Monitoring



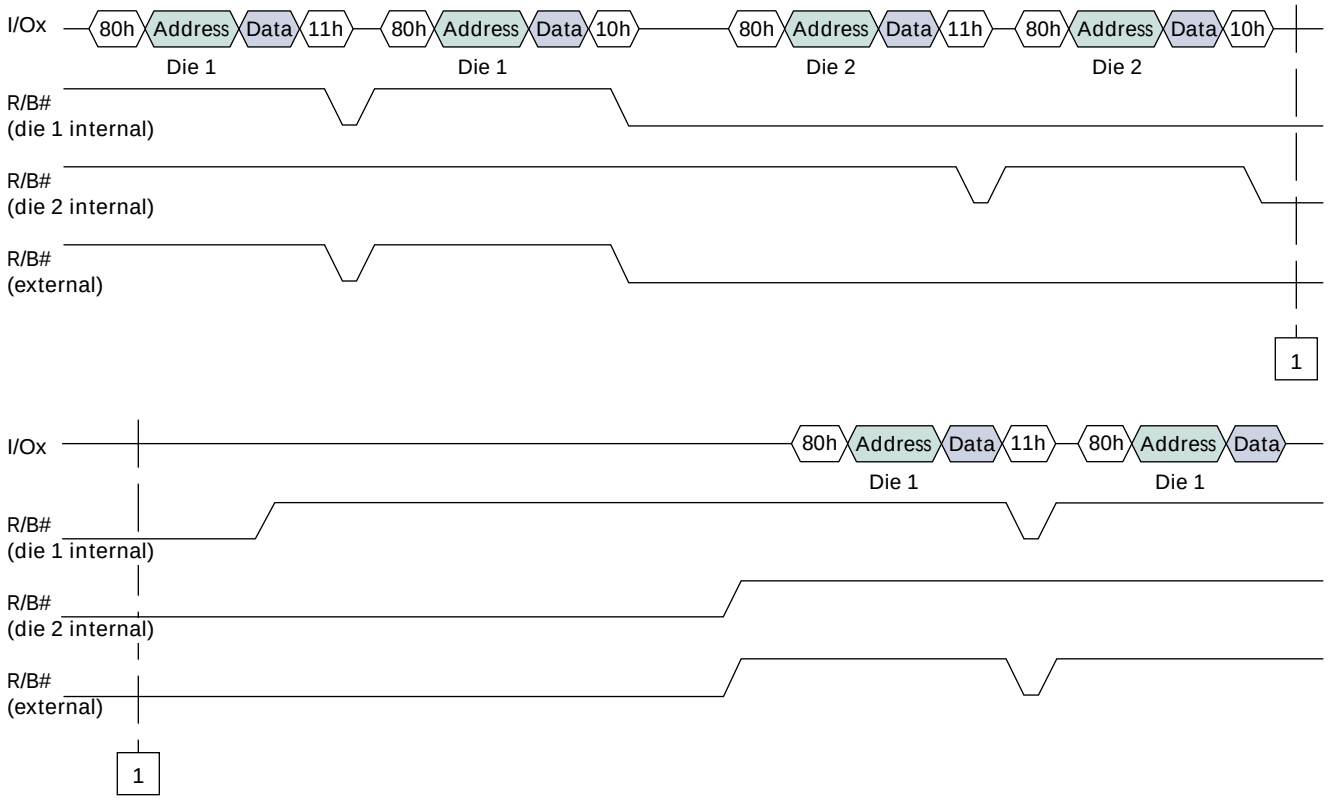
Interleaved TWO-PLANE PROGRAM PAGE Operation

Figures 40 and 41 show how to perform two types of interleaved TWO-PLANE PROGRAM PAGE operations. In Figure 40, the R/B# signal is monitored for operation completion. In Figure 41 on page 54, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM PAGE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 35 for details.

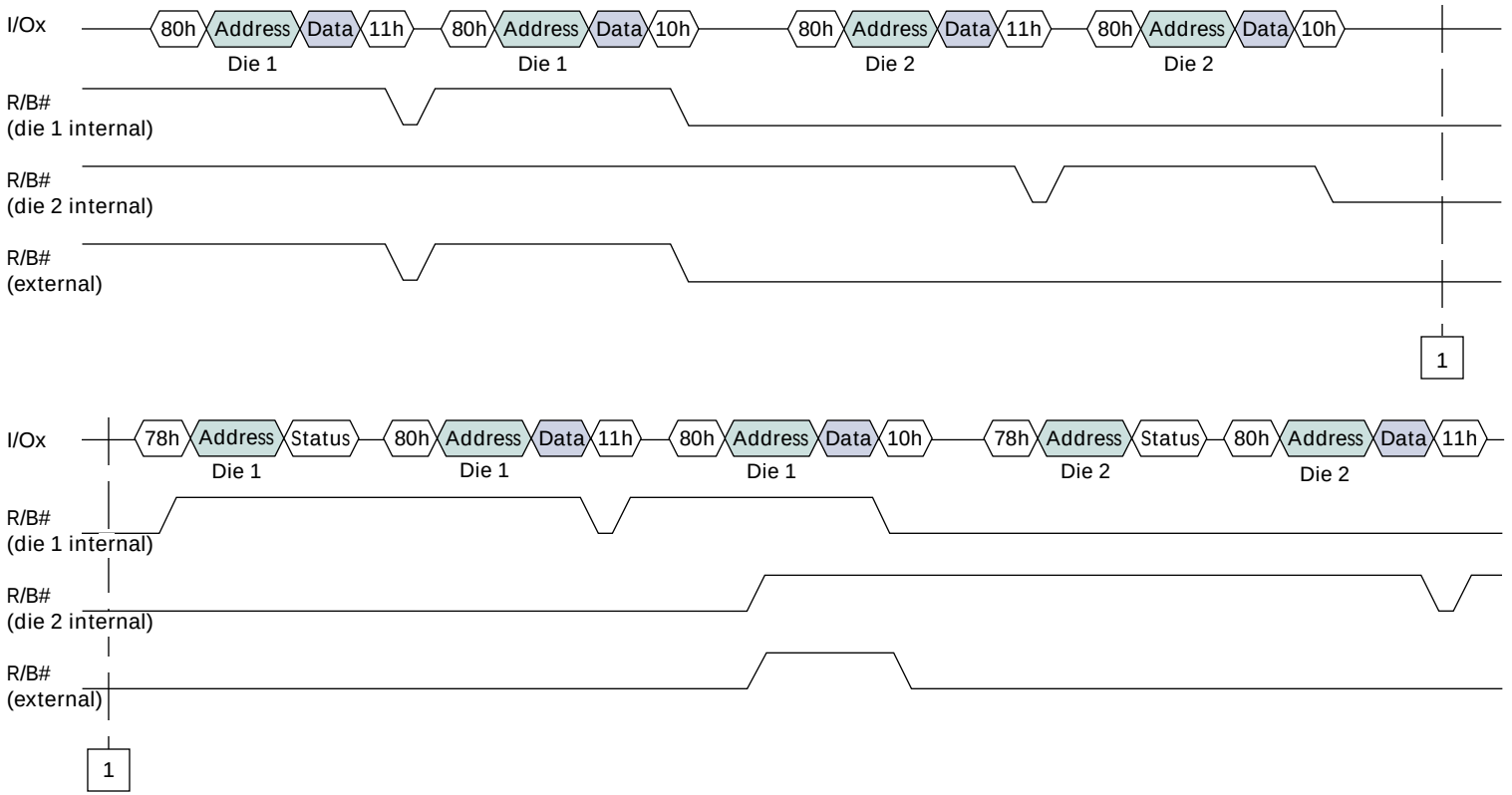
RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE operations.

Figure 40: Interleaved TWO-PLANE PROGRAM PAGE with R/B# Monitoring



Notes: 1. Two-plane addressing requirements apply.

Figure 41: Interleaved TWO-PLANE PROGRAM PAGE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

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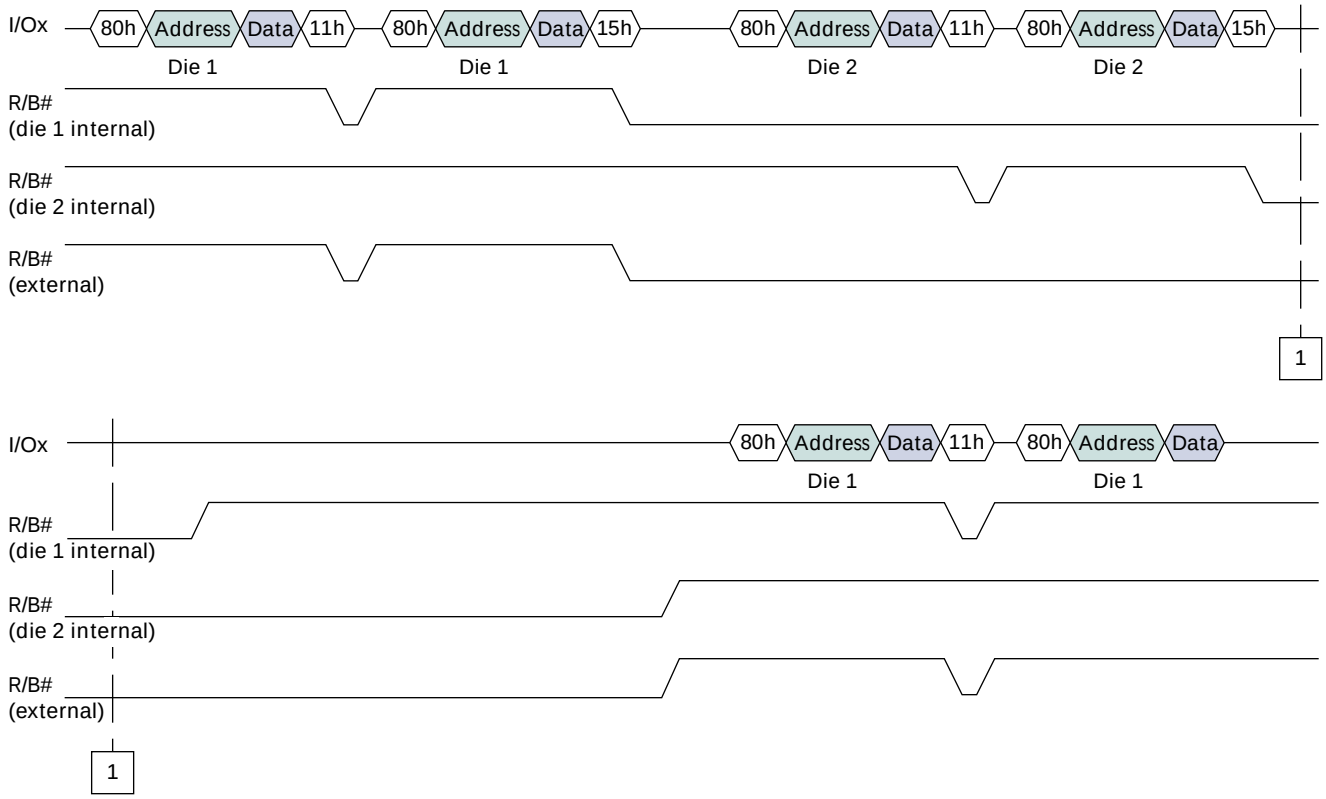
Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Operations

Figures 42 and 43 show how to perform two types of interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations. In Figure 42, the R/B# signal is monitored. In Figure 43 on page 56, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

The interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 35 for details.

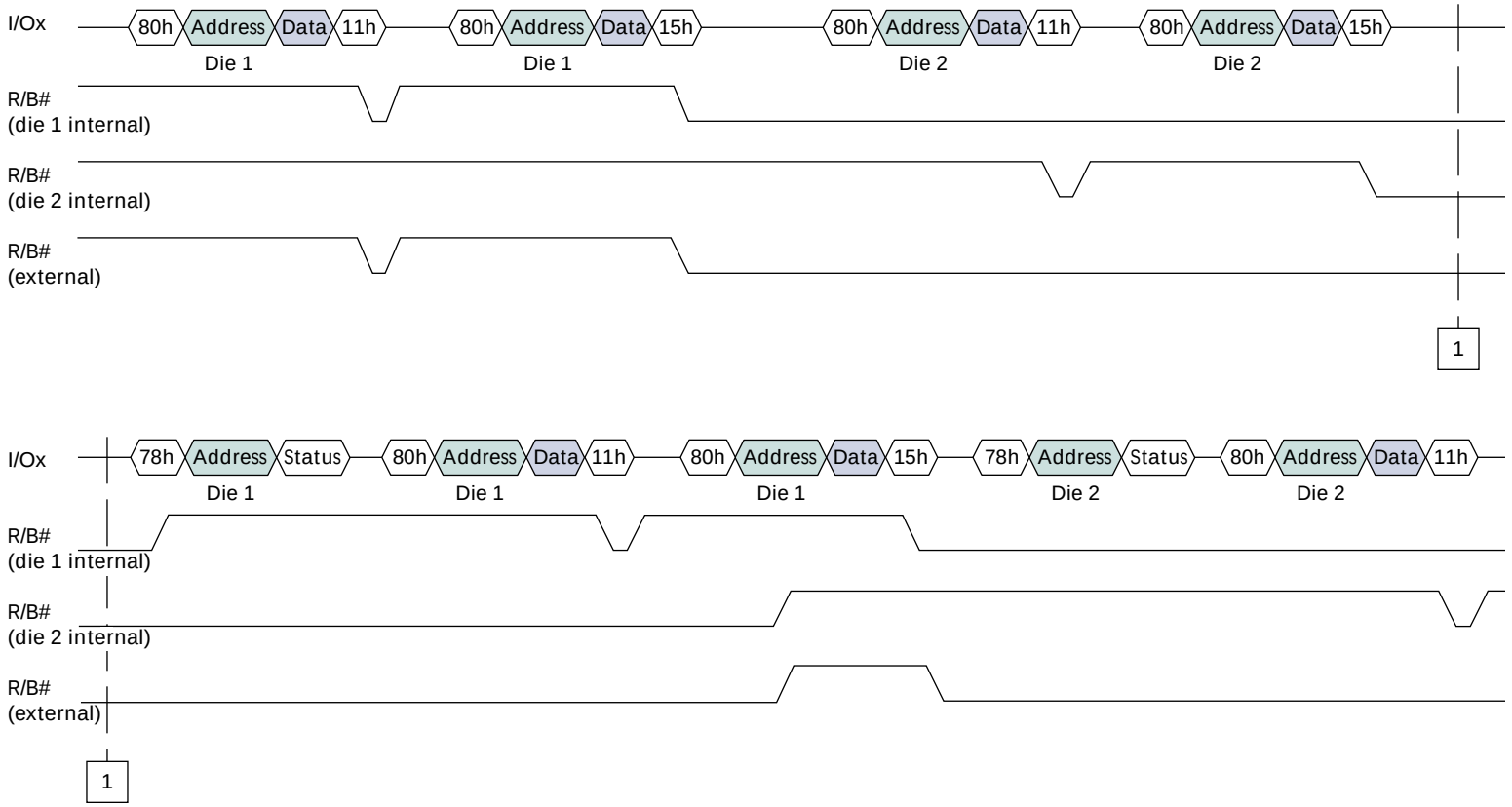
RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations.

Figure 42: Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with R/B# Monitoring



Notes: 1. Two-plane addressing requirements apply.

Figure 43: Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

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8gb_nand_j41b_mlc_3.fm - Rev. B 11/07 EN

Interleaved BLOCK ERASE Operations

Figures 44 and 45 show how to perform two types of interleaved BLOCK ERASE operations. In Figure 44, the R/B# signal is monitored for operation completion. In Figure 45, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

Figure 44: Interleaved BLOCK ERASE with R/B# Monitoring

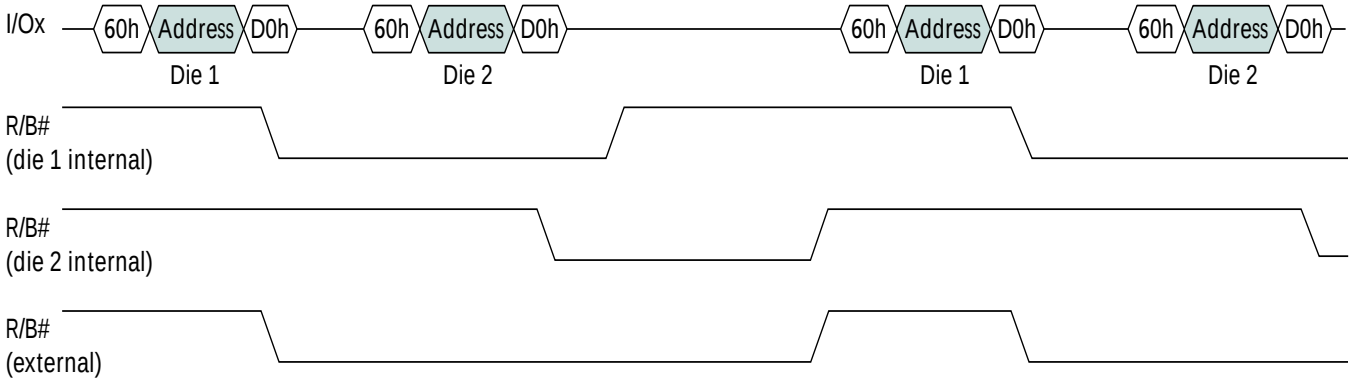
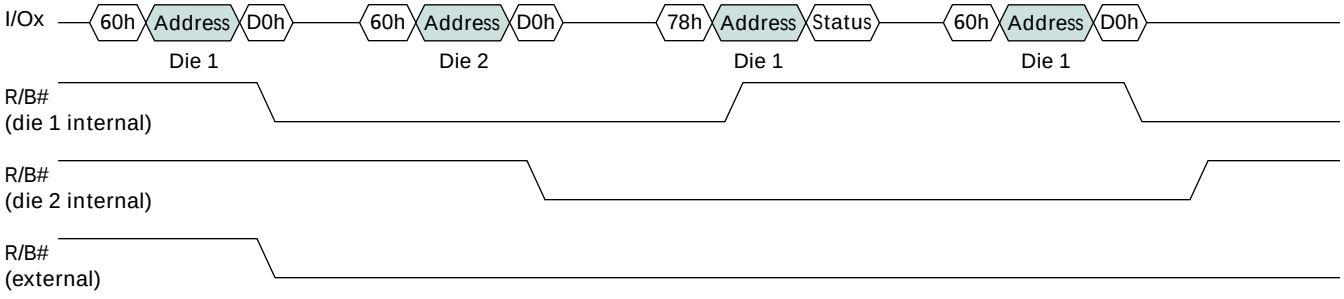


Figure 45: Interleaved BLOCK ERASE with Status Register Monitoring

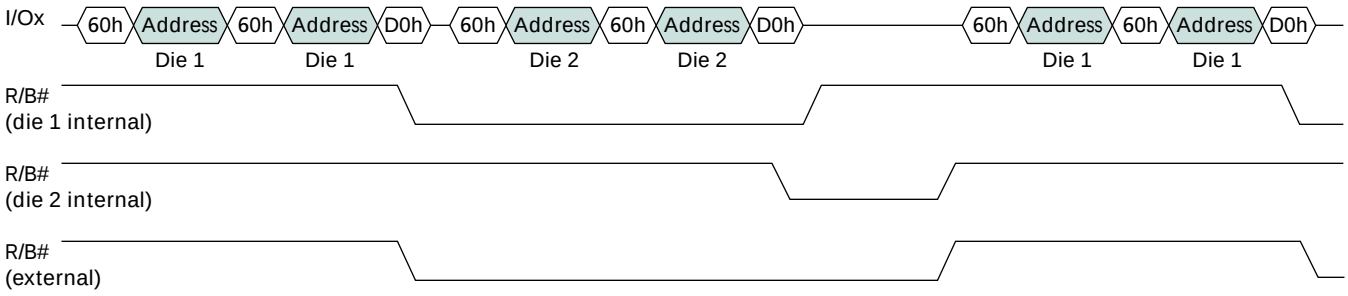


Interleaved TWO-PLANE BLOCK ERASE Operations

Figures 46 and 47 show how to perform two types of interleaved TWO-PLANE BLOCK ERASE operations. In Figure 46, the R/B# signal is monitored for operation completion. In Figure 47 on page 59, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

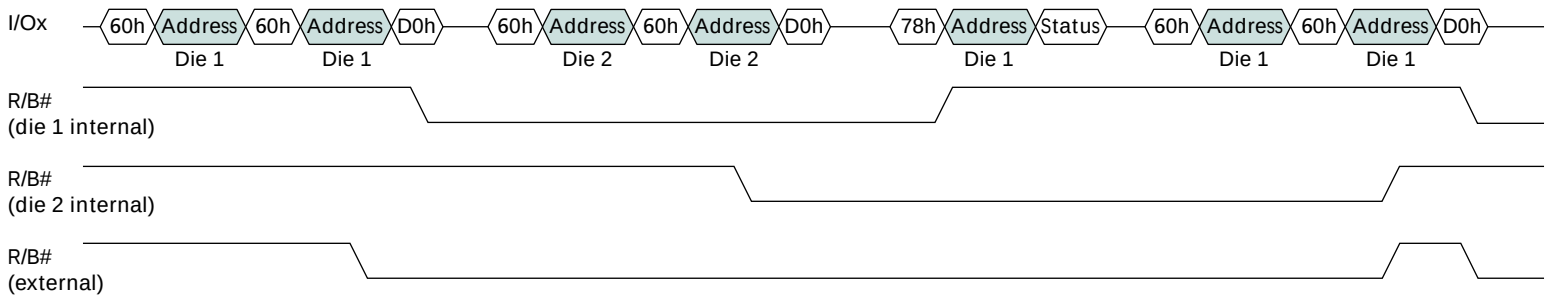
The interleaved TWO-PLANE BLOCK ERASE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 35 for details.

Figure 46: Interleaved TWO-PLANE BLOCK ERASE with R/B# Monitoring



Notes: 1. Two-plane addressing requirements apply.

Figure 47: Interleaved TWO-PLANE BLOCK ERASE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

RESET Operation

RESET FFh

The RESET command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

If a RESET command is issued during any type of programming operation (PROGRAM PAGE, PROGRAM PAGE CACHE MODE, PROGRAM for INTERNAL DATA MOVE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, or TWO-PLANE PROGRAM for INTERNAL DATA MOVE) while R/B# is LOW, the data in the shared memory cells being programmed could become invalid. Interrupting any programming operation on one page could corrupt the data in another page within the block being programmed.

The status register contains the value E0h when WP# is HIGH; otherwise, it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register (see Figure 48 and Table 10).

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms. During and following the initial RESET (FFh) command, and prior to issuing the next command, use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited.

Figure 48: RESET Operation

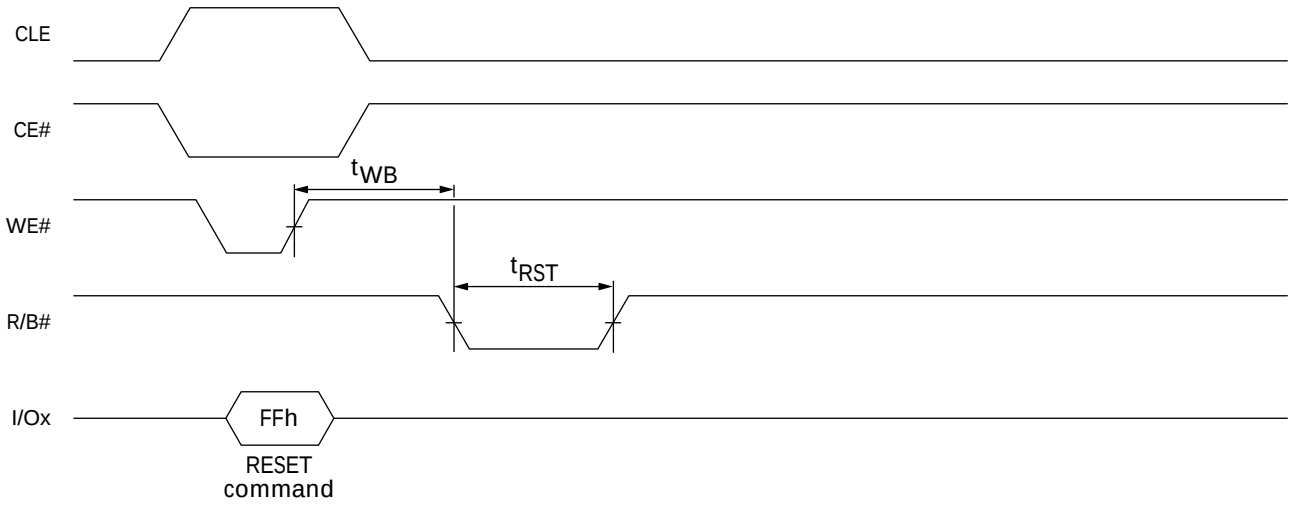


Table 10: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using WP#. Figures 49 through 60 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, WP# must not be toggled until the command is complete and the device is ready (status register bit 5 is "1").

Figure 49: ERASE Enable

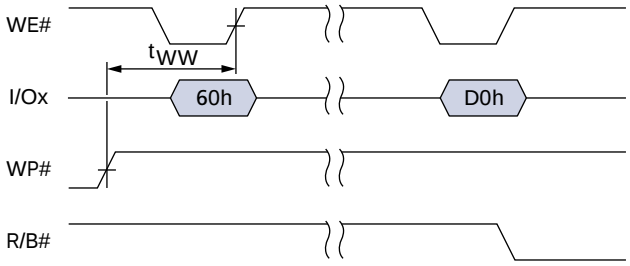


Figure 50: ERASE Disable

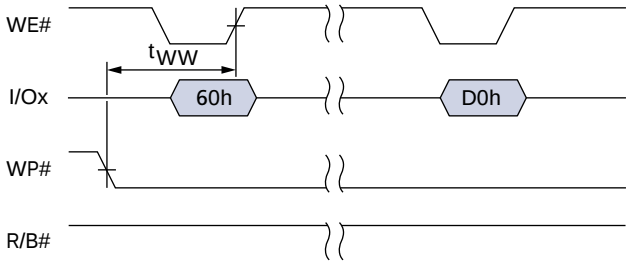


Figure 51: PROGRAM Enable

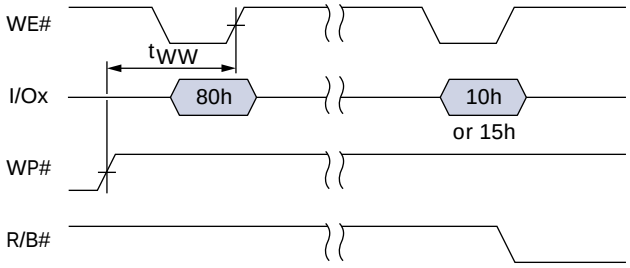


Figure 52: PROGRAM Disable

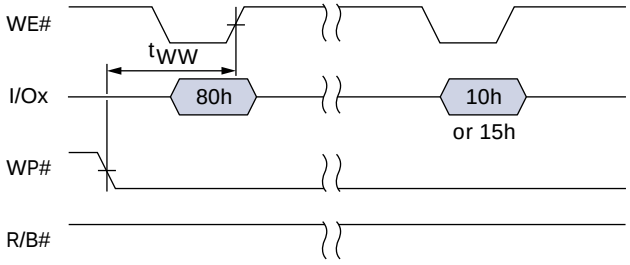


Figure 53: PROGRAM for INTERNAL DATA MOVE Enable

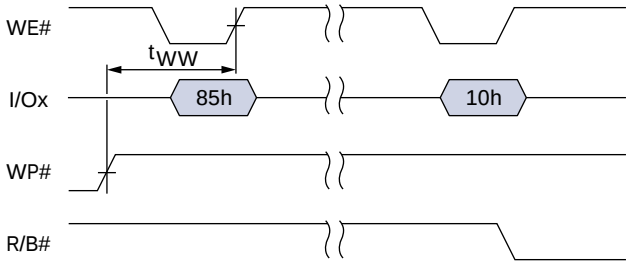


Figure 54: PROGRAM for INTERNAL DATA MOVE Disable

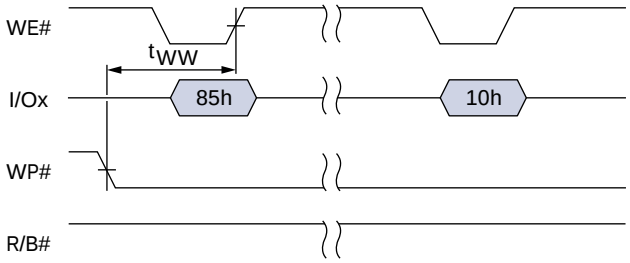


Figure 55: TWO-PLANE ERASE Enable

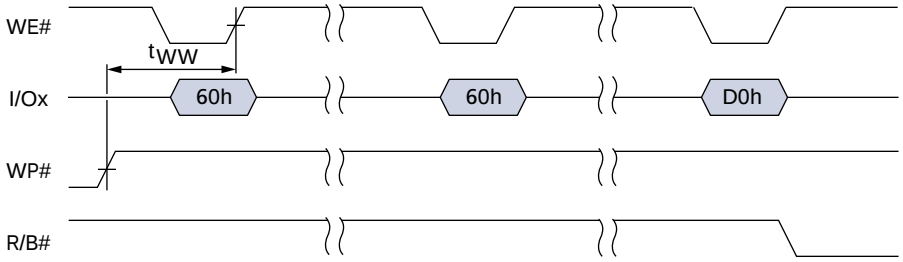


Figure 56: TWO-PLANE ERASE Disable

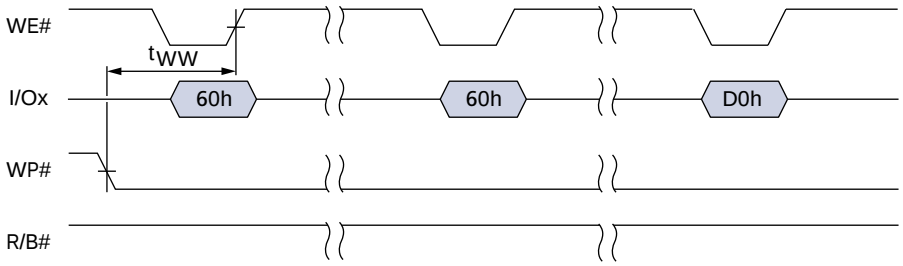


Figure 57: TWO-PLANE PROGRAM Enable

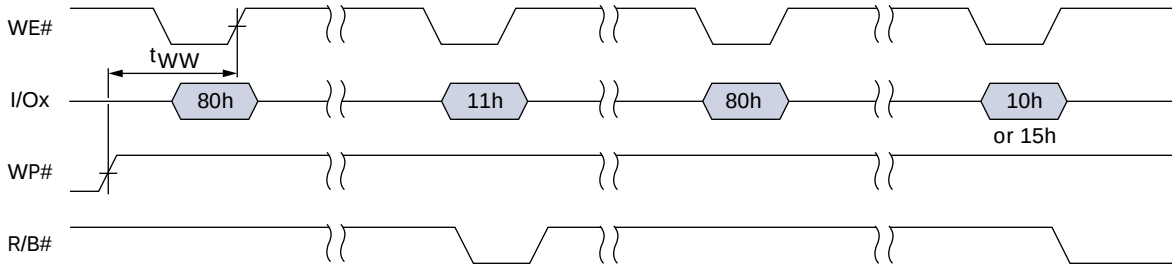


Figure 58: TWO-PLANE PROGRAM Disable

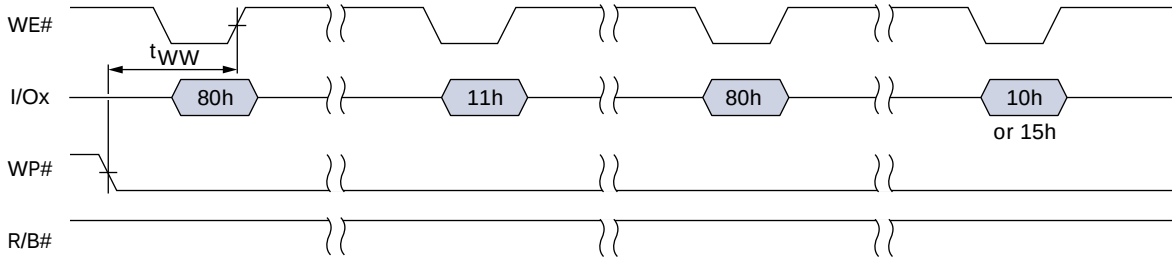


Figure 59: TWO-PLANE PROGRAM for INTERNAL DATA MOVE Enable

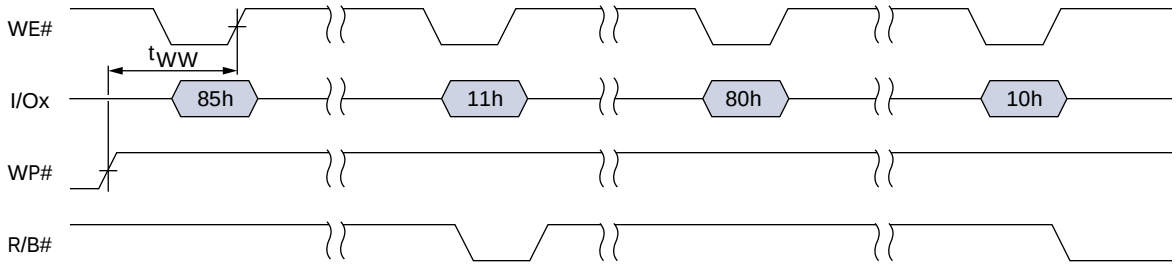
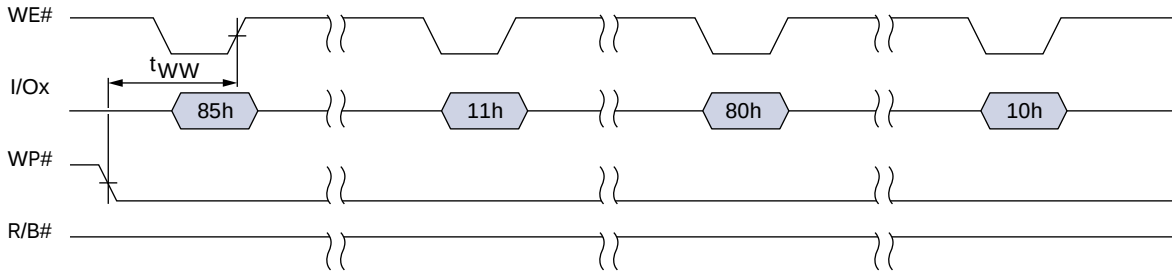


Figure 60: TWO-PLANE PROGRAM for INTERNAL DATA MOVE Disable



Error Management

Micron NAND Flash devices are specified to have a minimum of 3,996 valid blocks (NVB) out of every 4,096 total available blocks for every 8Gb. This means the devices may have blocks that are invalid when they are shipped. Invalid blocks are blocks that contain more bad bits than can be corrected by required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block mapping, replacement, and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the Flash device.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Before NAND Flash devices are shipped from Micron, they are erased. The factory identifies invalid blocks before shipping by programming data other than FFh into the first spare location (column address 2,048) of the first page (page 0) or the second page (page 1) of each bad block.

System software should check the first spare address on the first 2 pages of each block prior to performing any erase or programming operations on the Flash device. A bad block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked “bad” may be marginal, it may not be possible to recover these bad block markings if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the Flash device, certain precautions must be taken:

- Always check status after a PROGRAM, ERASE, or DATA MOVE operation.
- Under typical use conditions, utilize a minimum of 4-bit ECC per 528 bytes of data.
- Use a bad-block replacement algorithm.

Electrical Characteristics

Table 11: Absolute Maximum Ratings by Device
Voltage on any pin relative to V_{SS}

Parameter/Condition		Symbol	Min	Max	Unit
Voltage input	MT29FxGxx	V_{IN}	–0.6	+4.6	V
V_{CC} supply voltage	MT29FxGxx	V_{CC}	–0.6	+4.6	V
Storage temperature		T_{STG}	–65	+150	°C
Short circuit output current, I/Os			–	5	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Extended		–40	–	+85	°C
V_{CC} supply voltage	MT29FxGxx	V_{CC}	2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

VCC Power Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. (The WP# signal permits additional hardware protection during power transitions.) When VCC reaches 2.3V for a 3V device, a minimum of 100µs should be allowed for the Flash device to initialize before any commands are executed (see Figure 61 for the states of signals during VCC power cycling).

The RESET command must be issued to all CE#s as the first command after the NAND Flash device is powered on. Each CE# will be busy for a maximum of 1ms after a RESET command is issued.

Figure 61: AC Waveforms During Power Transitions

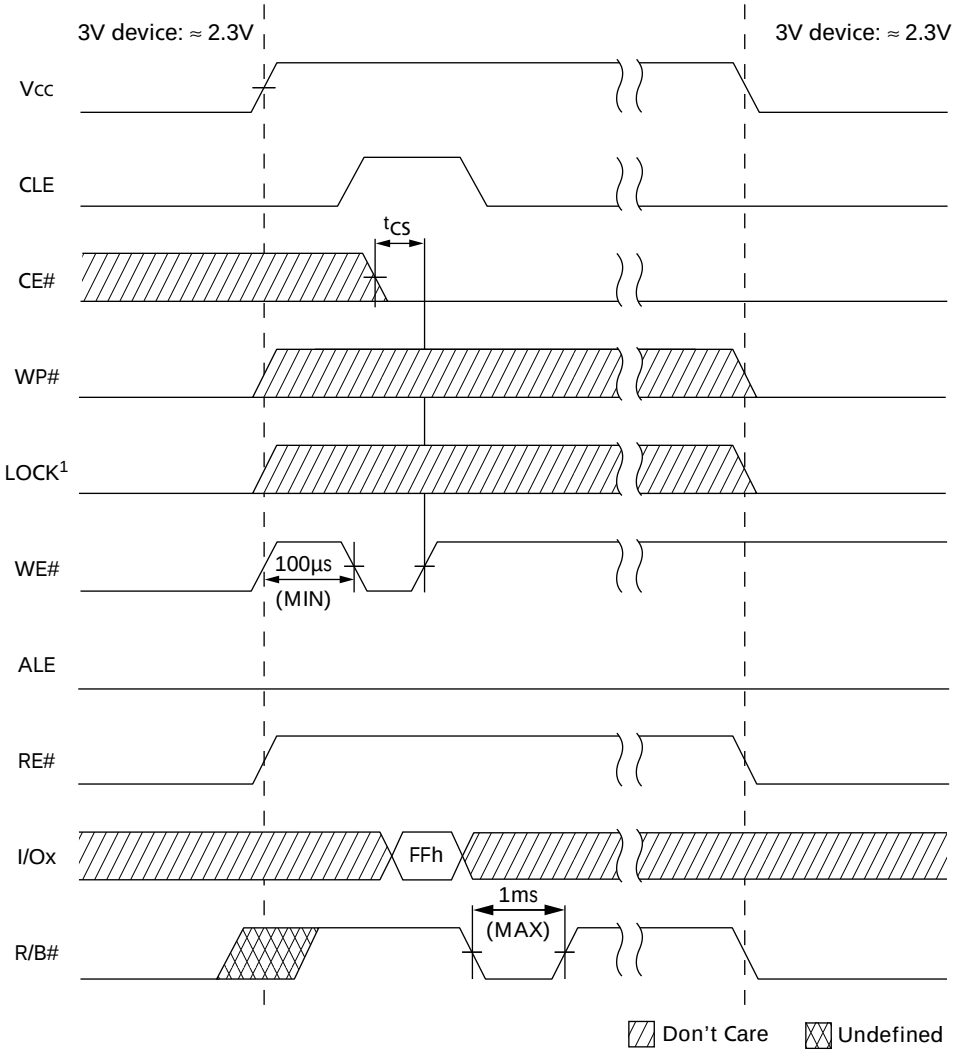


Table 13: M29FxGxx Device DC and Operating Characteristics

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current		$^tRC = ^tRC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	$I_{CC}1$	–	15	20	mA
Program current		–	$I_{CC}2$	–	15	20	mA
Erase current		–	$I_{CC}3$	–	15	20	mA
Standby current (TTL)		CE# = V_{IH}; WP# = 0V/V_{CC}	$I_{SB}1$	–	–	1	mA
Standby current (CMOS)							
	MT29F8G08MAA	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA
	MT29F16G08QAA			–	20	100	µA
	MT29F32G08TAA			–	40	200	µA
Input leakage current							
	MT29F8G08MAA	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA
	MT29F16G08QAA			–	–	±20	µA
	MT29F32G08TAA			–	–	±40	µA
Output leakage current							
	MT29F8G08MAA	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA
	MT29F16G08QAA			–	–	±20	µA
	MT29F32G08TAA			–	–	±40	µA
Input high voltage		I/O [7:0], I/O [15:0], CE#, CLE, ALE, WE#, RE#, R/B#, WP#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V
Input low voltage (all inputs)		–	V_{IL}	–0.3	–	0.2 x V_{CC}	V
Output high voltage		I_{OH} = –400µA	V_{OH}	2.4	–	–	V
Output low voltage		I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V
Output low current (R/B#)		V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA

Table 14: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	N_{VB}	MT29F8Gxx	3,996	4,096	blocks	1, 2, 3
		MT29F16Gxx	7,992	8,192		1, 2, 3
		MT29F32Gxx	15,984	16,384		1, 2, 4

Notes:
1. Invalid blocks are blocks that contain more bad bits than can be corrected by required ECC. See "Error Management" on page 64 for device ECC requirements. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below N_{VB} during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid with ECC when shipped from factory.
3. Each CE# has a maximum of 100 invalid blocks.
4. Each CE# has a maximum of 200 invalid blocks, not to exceed 100 invalid blocks for each NAND Flash die.

Table 15: Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	CIN	MT29F8Gxx	10	pF	1, 2
		MT29F16Gxx	20		
		MT29F32Gxx	40		
Input/output capacitance (I/O)	COUT	MT29F8Gxx	10	pF	1, 2
		MT29F16Gxx	20		
		MT29F32Gxx	40		

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_c = 25°C; f = 1 MHz; V_{IN} = 0V.

Table 16: Test Conditions

Parameter		Value	Notes
Input pulse levels	MT29FxGxx	0.0V to 3.3V	
Input rise and fall times		5ns	
Input and output timing levels		VCC/2	
Output load	MT29FxGxx (VCC = 3.0V ± 10%)	1 TTL GATE and CL = 50pF	1
	MT29FxGxx (VCC = 3.3V ± 10%)	1 TTL GATE and CL = 100pF	1

Notes: 1. Verified in device characterization; not 100 percent tested.

Table 17: AC Characteristics – Command, Data, and Address Input

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	70	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	15	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	10	–	ns	
WRITE cycle time	^{t}WC	25	–	ns	
WE# pulse width HIGH	^{t}WH	10	–	ns	
WE# pulse width	^{t}WP	12	–	ns	
WP# setup time	^{t}WW	30	–	ns	

Notes: 1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 18: AC Characteristics – Normal Operation

Parameter	Symbol	Cache Mode		Standard Mode		Unit	Notes
		Min	Max	Min	Max		
ALE to RE# delay	^{t}AR	10	–	10	–	ns	
CE# access time	^{t}CEA	–	25	–	25	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	30	–	30	ns	2
CLE to RE# delay	^{t}CLR	10	–	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	15	–	ns	
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	7	30	7	30	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	50	^{t}DCBSYR1	50	µs	
Output High-Z to RE# LOW	^{t}IR	0	–	0	–	ns	1
Data transfer from Flash array to data register	^{t}R	–	50	–	50	µs	
READ cycle time	^{t}RC	35	–	25	–	ns	1
RE# access time	^{t}REA	–	22	–	15	ns	1
RE# HIGH hold time	^{t}REH	15	–	10	–	ns	1
RE# HIGH to output hold	^{t}RHOH	15	–	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	100	–	100	ns	2
RE# LOW to output hold	^{t}RLOH	5	–	5	–	ns	
RE# pulse width	^{t}RP	17	–	12	–	ns	1
Ready to RE# LOW	^{t}RR	20	–	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	–	100	ns	3, 4
WE# HIGH to RE# LOW	^{t}WHR	60	–	60	–	ns	

Notes:
1. For PAGE READ CACHE MODE and PROGRAM PAGE CACHE MODE operations, the cache mode timing applies.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device goes busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 19: PROGRAM/ERASE Characteristics

Parameter	Description	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	1	cycles	1
^{t}BERS	BLOCK ERASE operation time	2	10	ms	
^{t}CBSY	Busy time for PROGRAM CACHE operation	30	2,200	µs	2
^{t}DBSY	Busy time for TWO-PLANE PROGRAM PAGE operation	0.5	1	µs	
^{t}LPROG	LAST PROGRAM PAGE operation time	–	–	–	3
^{t}PROG	PROGRAM PAGE operation time	650	2,200	µs	

Notes: 1. One total to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

Timing Diagrams

Figure 62: COMMAND LATCH Cycle

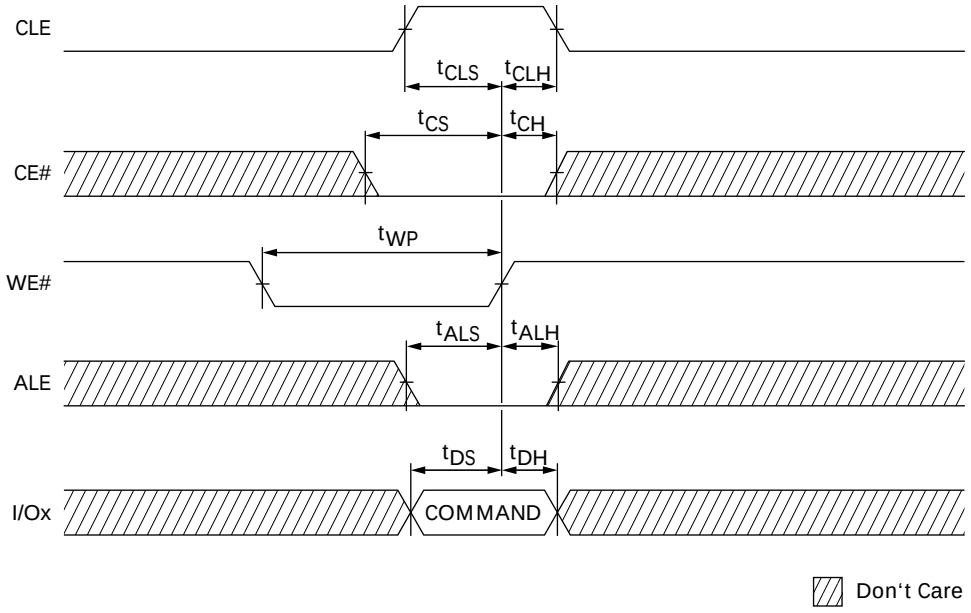


Figure 63: ADDRESS LATCH Cycle

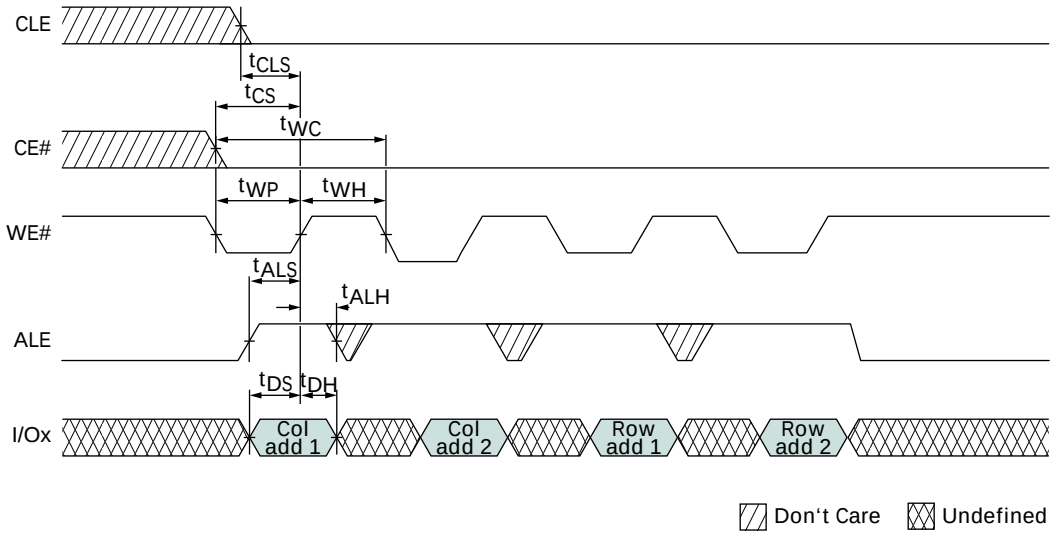
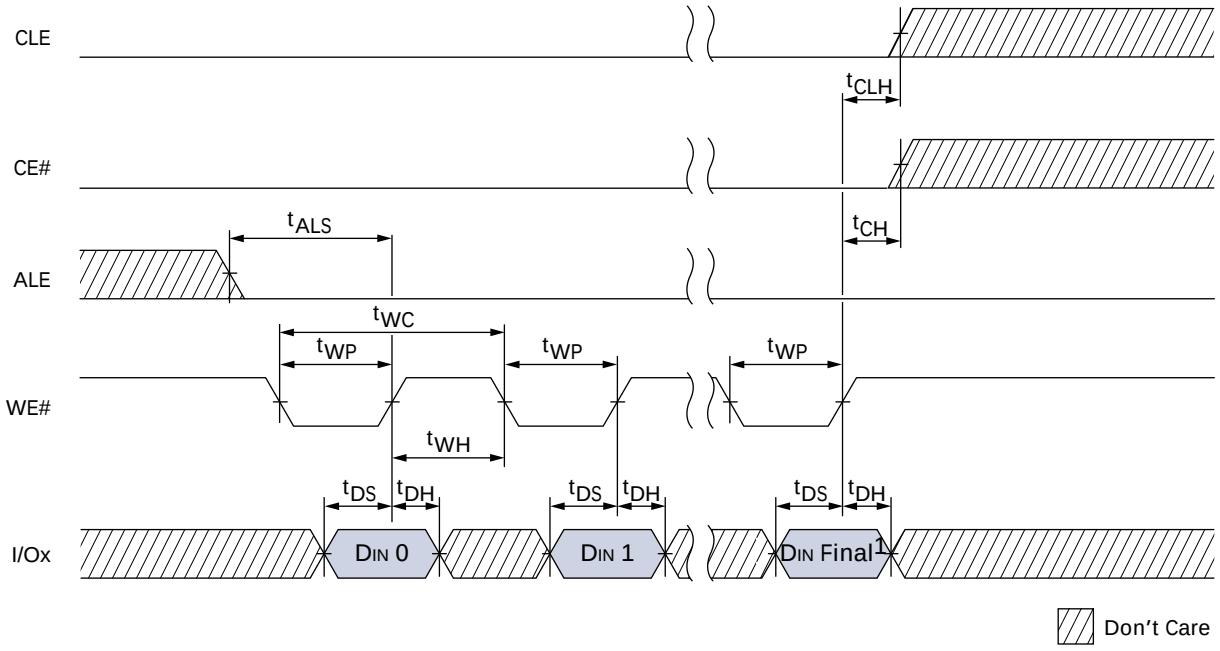


Figure 64: INPUT DATA LATCH Cycle



Notes: 1. DIN Final = 2,111.

Figure 65: SERIAL ACCESS Cycle After READ

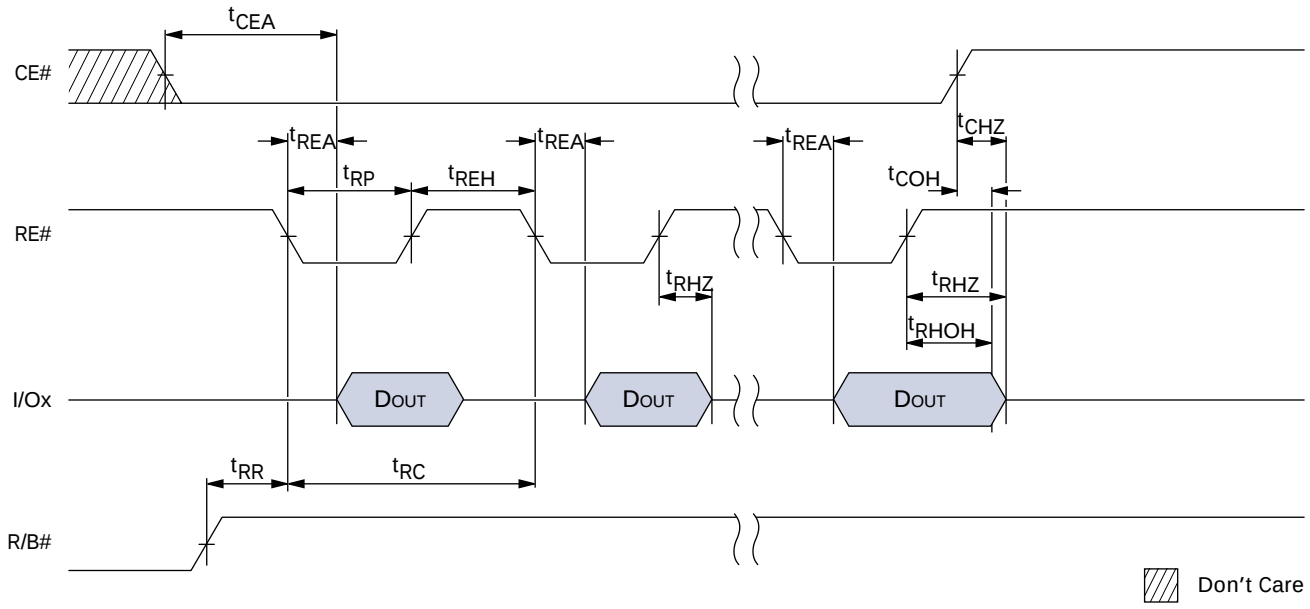
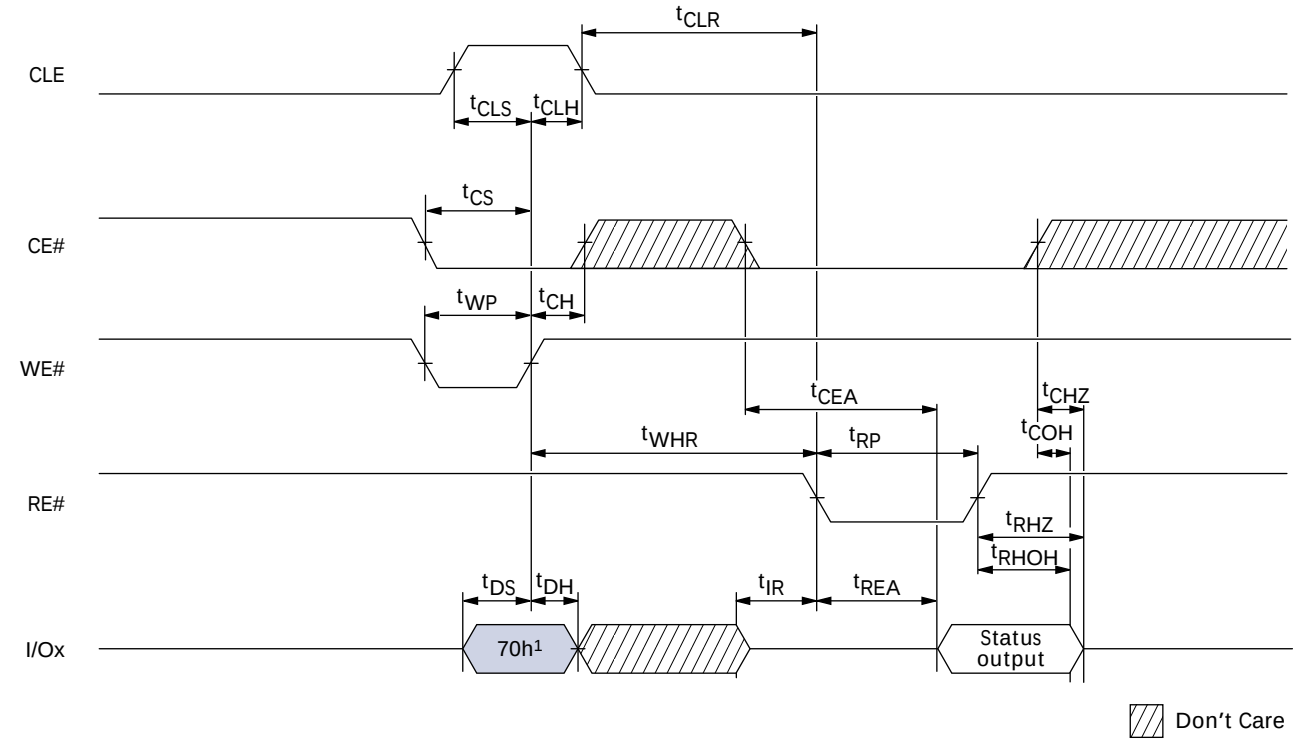


Figure 66: READ STATUS Cycle



Notes: 1. Command can be 70h or 78h.

Figure 67: PAGE READ Operation

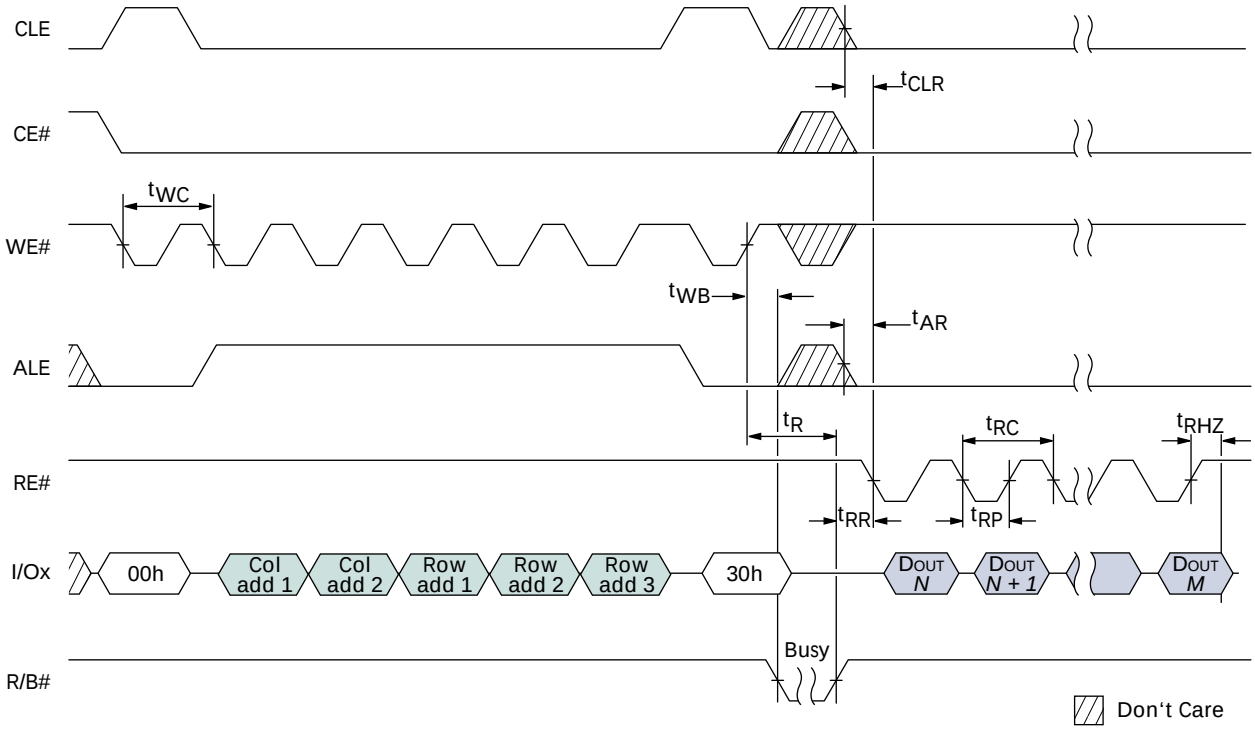


Figure 68: READ Operation with CE# "Don't Care"

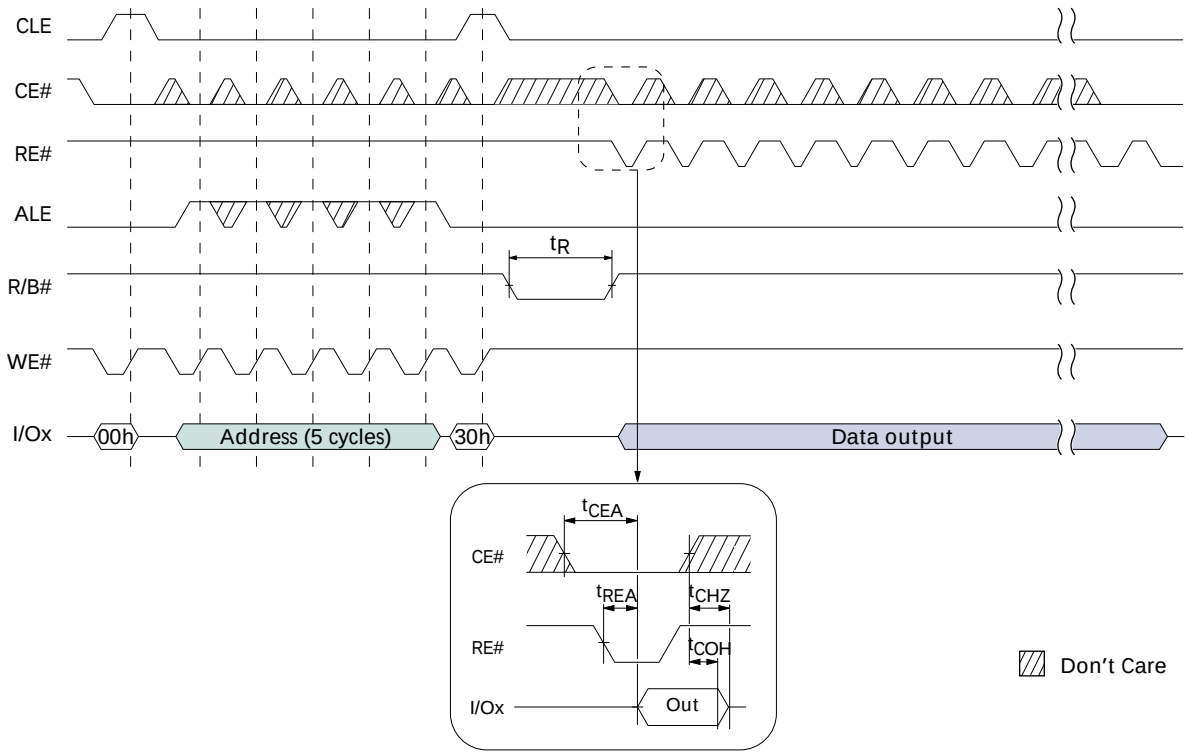
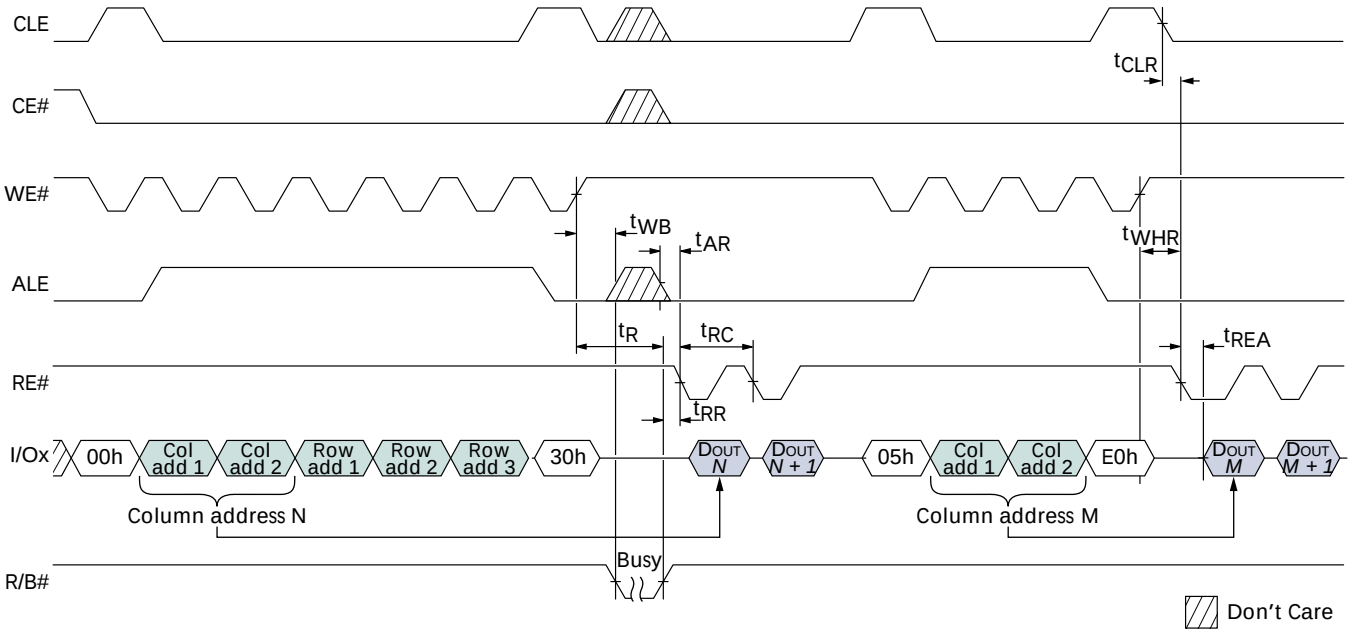


Figure 69: RANDOM DATA READ Operation



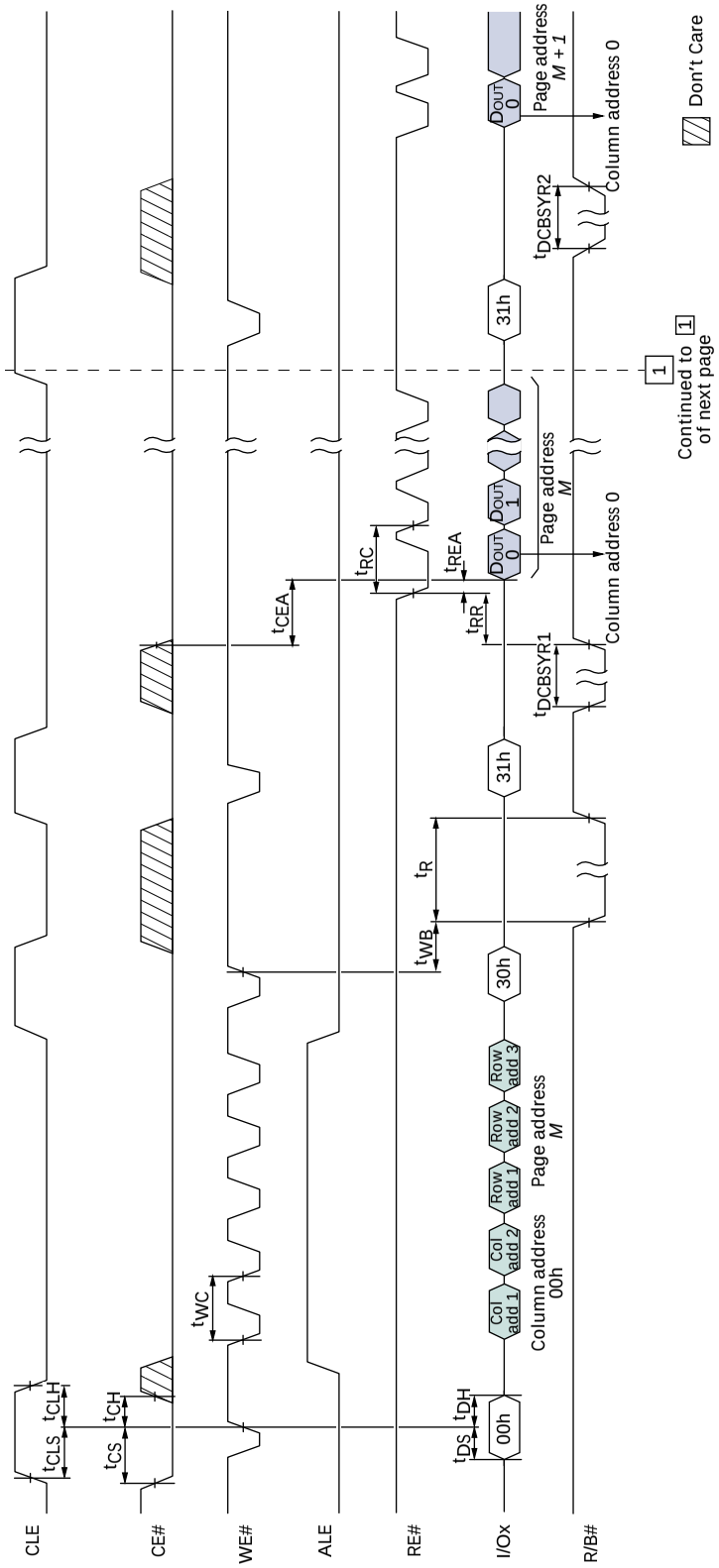


Figure 70: PAGE READ CACHE MODE Operation, Part 1 of 2

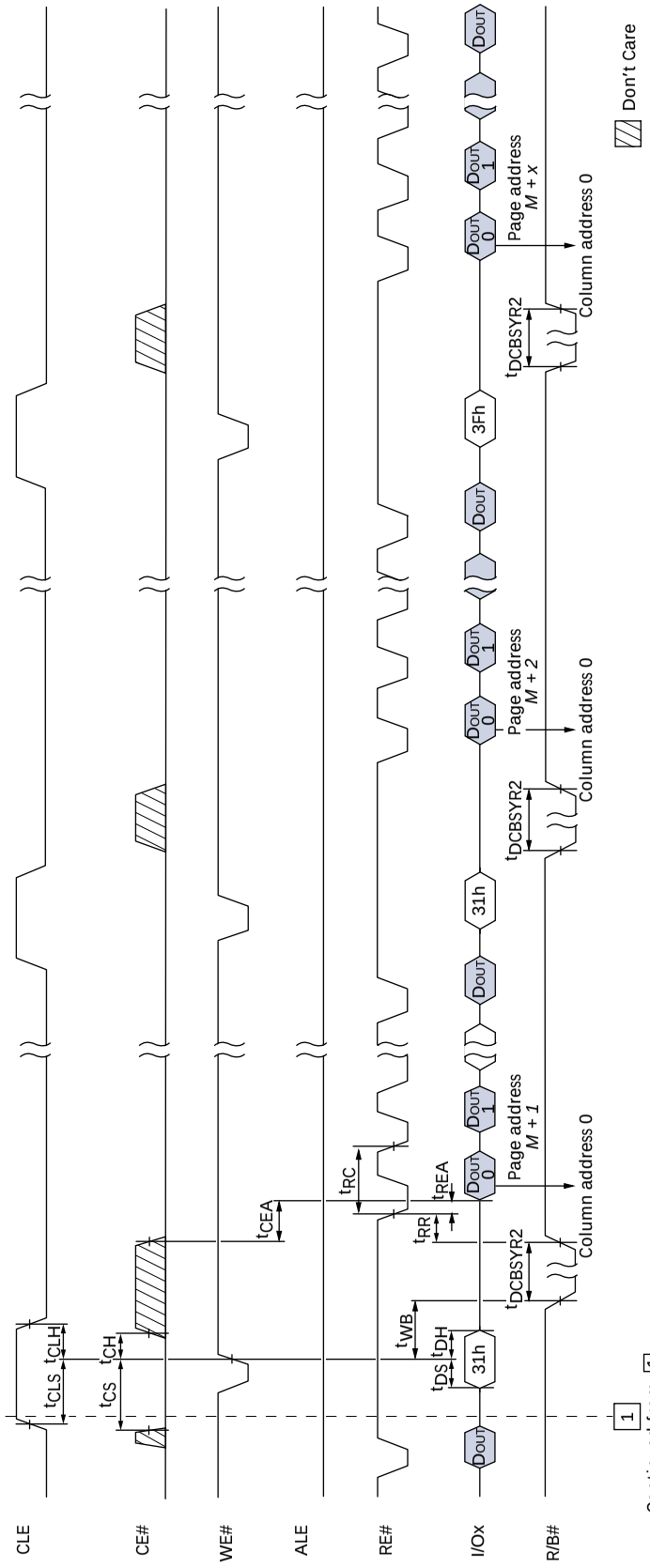


Figure 71: PAGE READ CACHE MODE Operation, Part 2 of 2

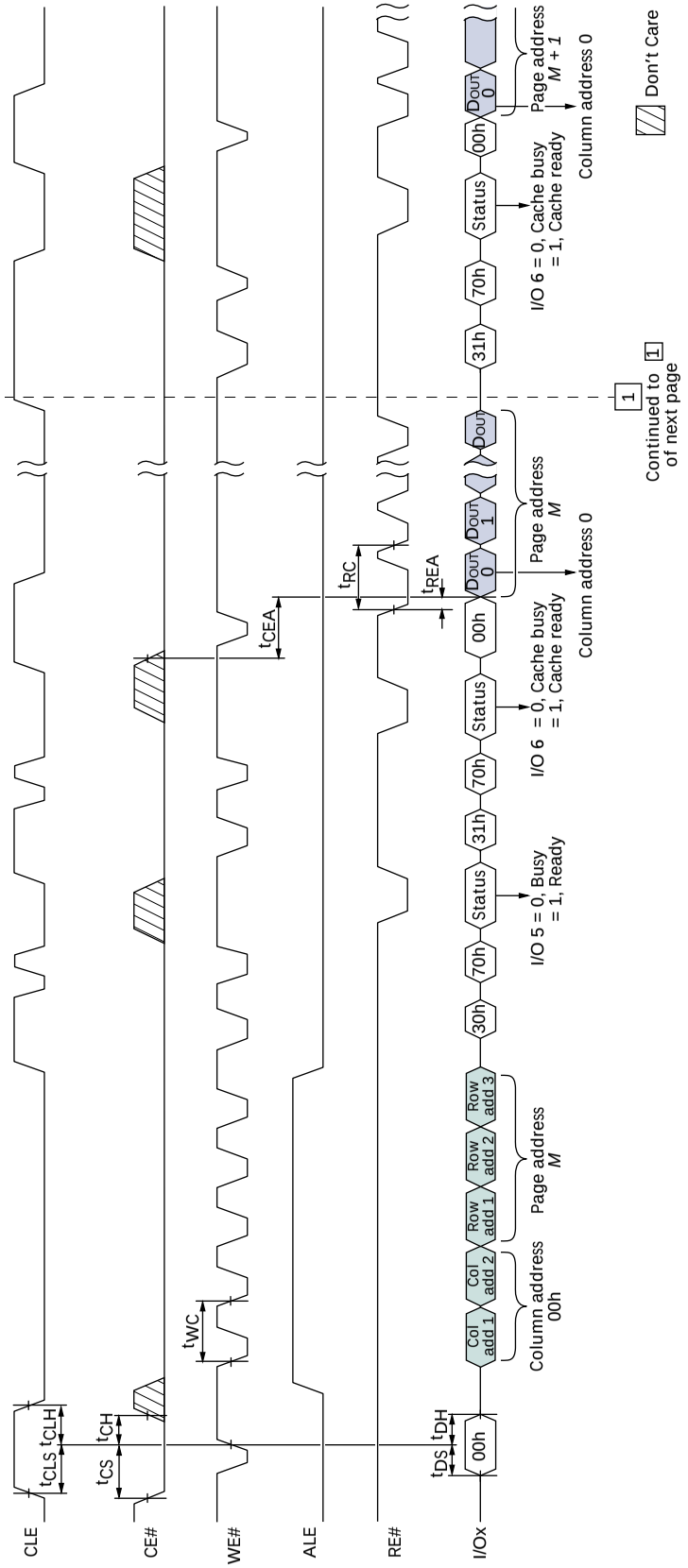


Figure 72: PAGE READ CACHE MODE Operation without R/B#, Part 1 of 2

Figure 73: PAGE READ CACHE MODE Operation without R/B#, Part 2 of 2

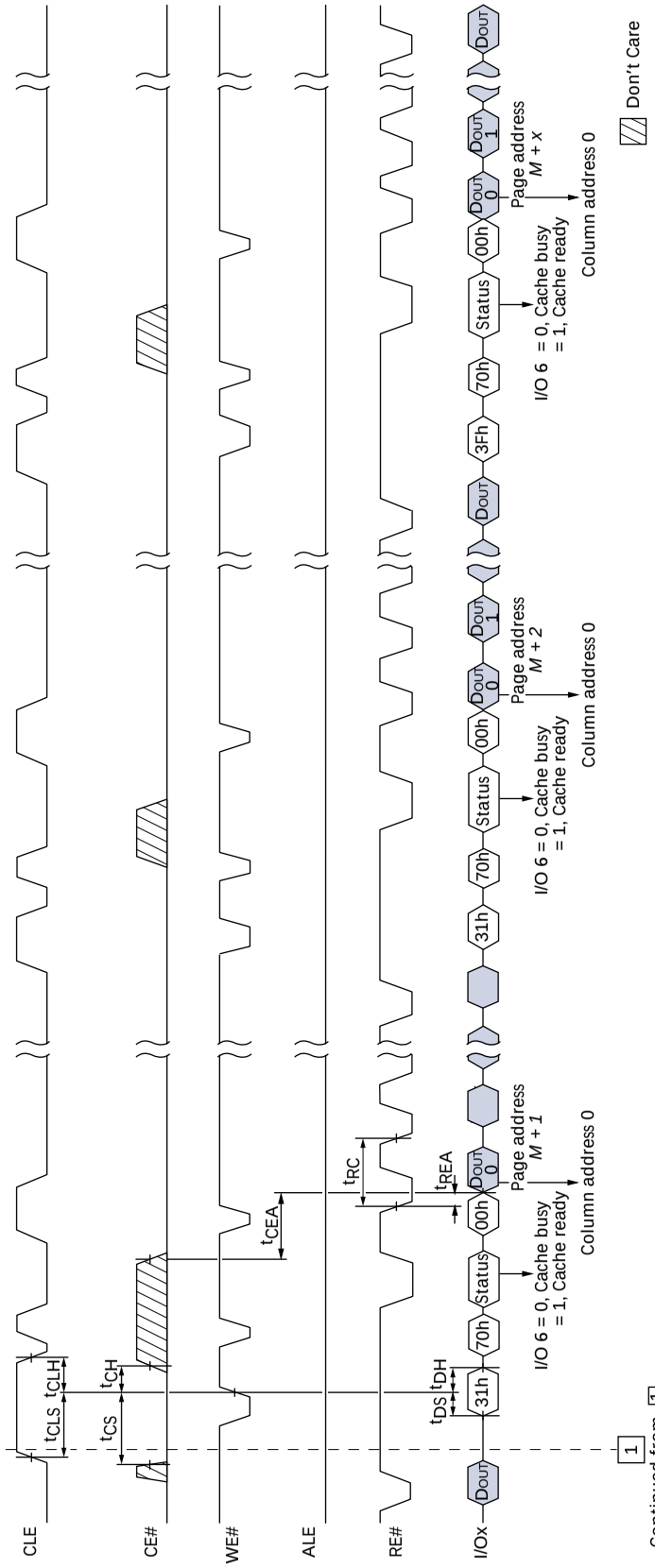
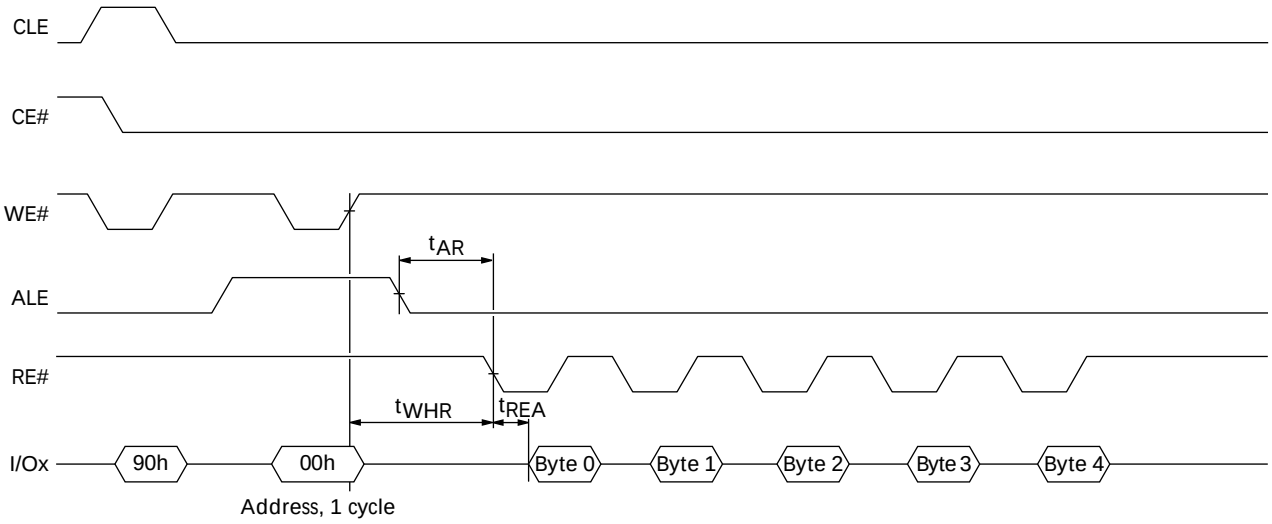


Figure 74: READ ID Operation



Note: See Table 8 on page 27 for actual values.

Figure 75: PROGRAM Operation with CE# "Don't Care"

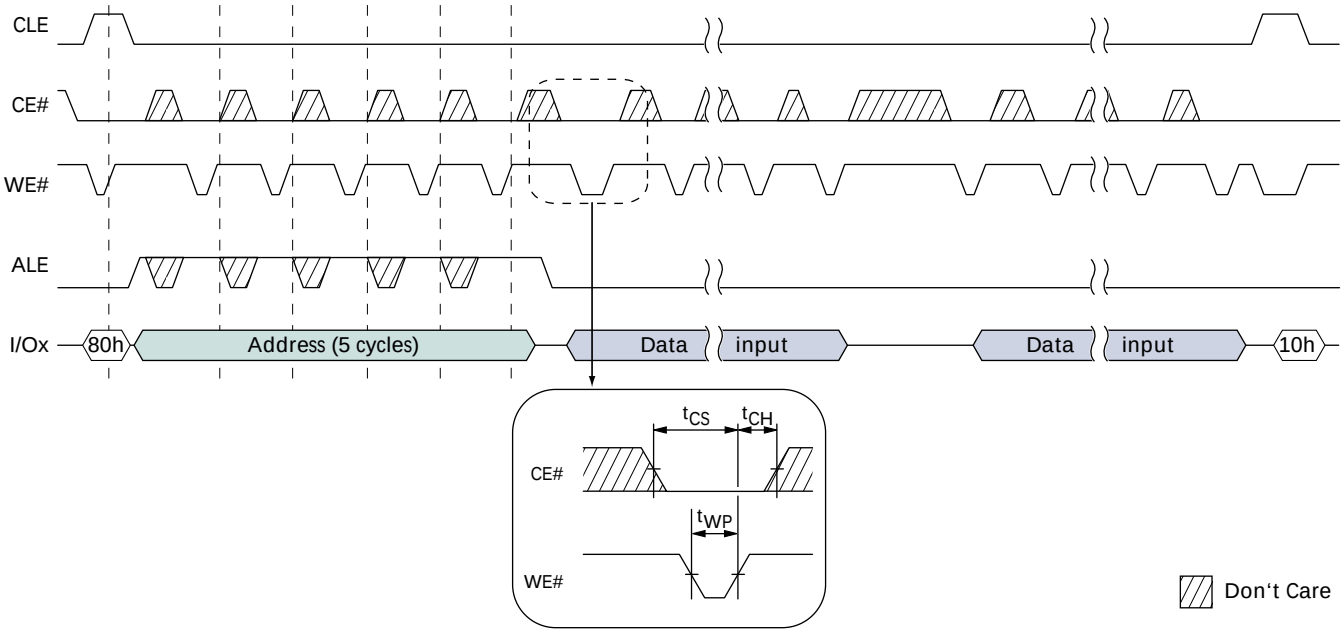
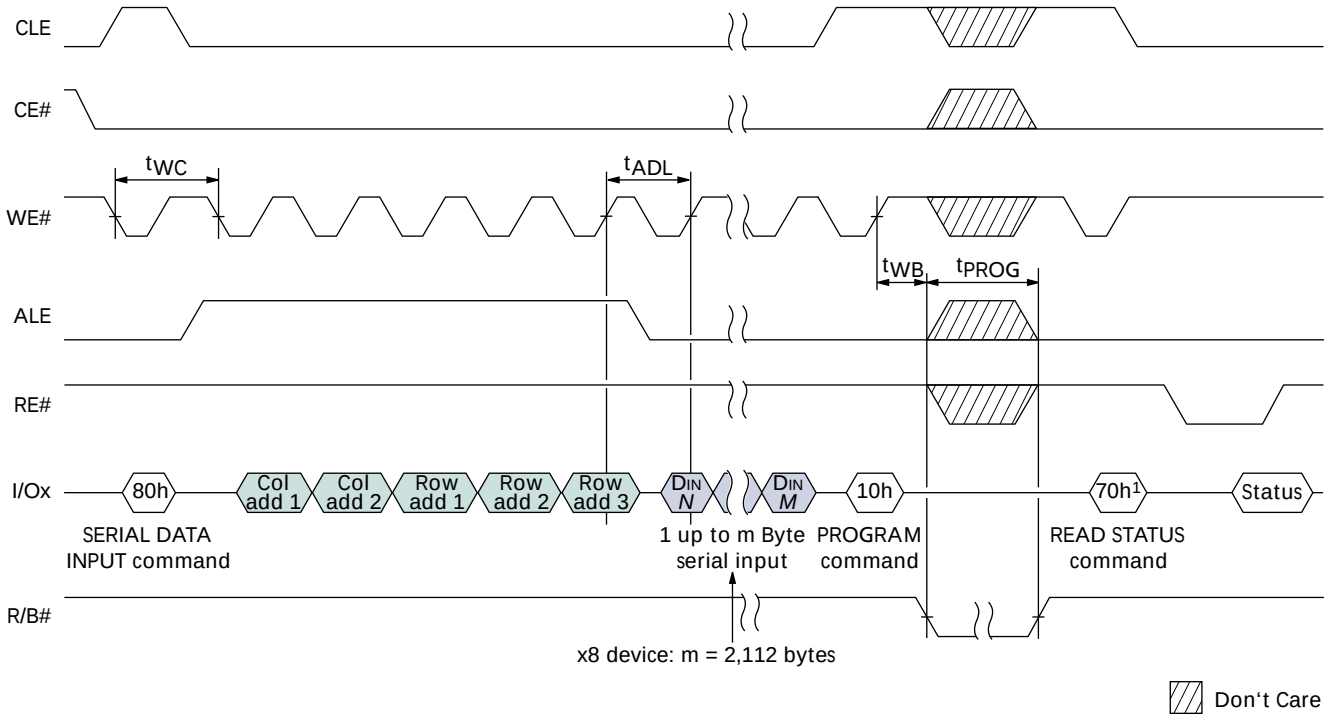
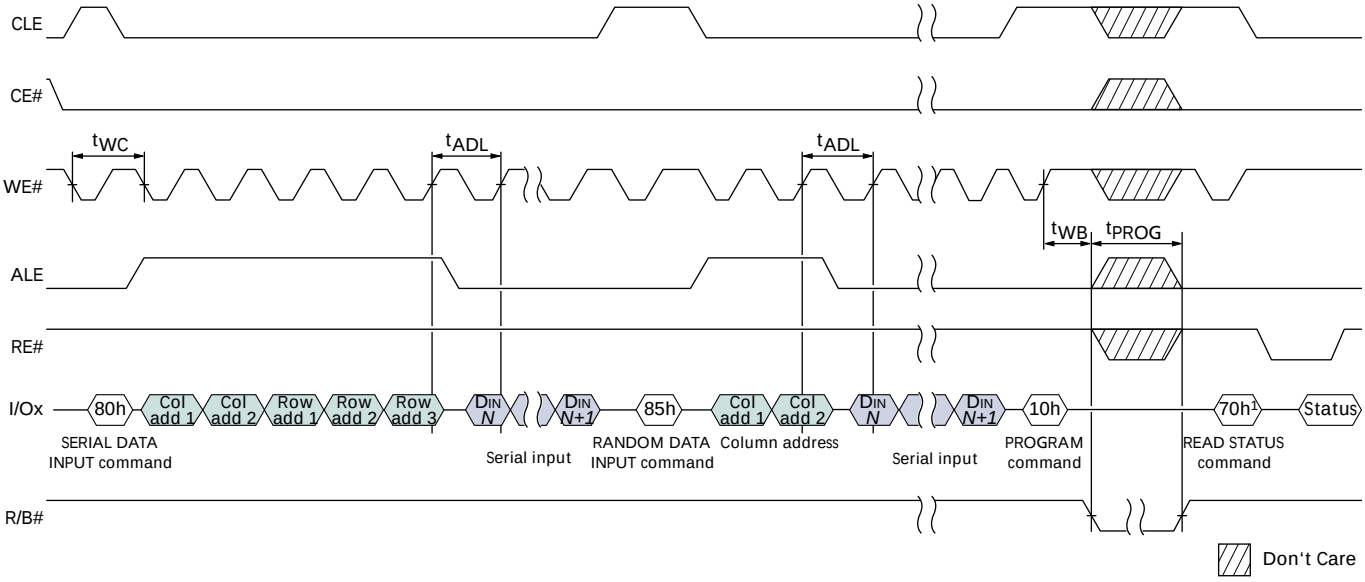


Figure 76: PROGRAM PAGE Operation



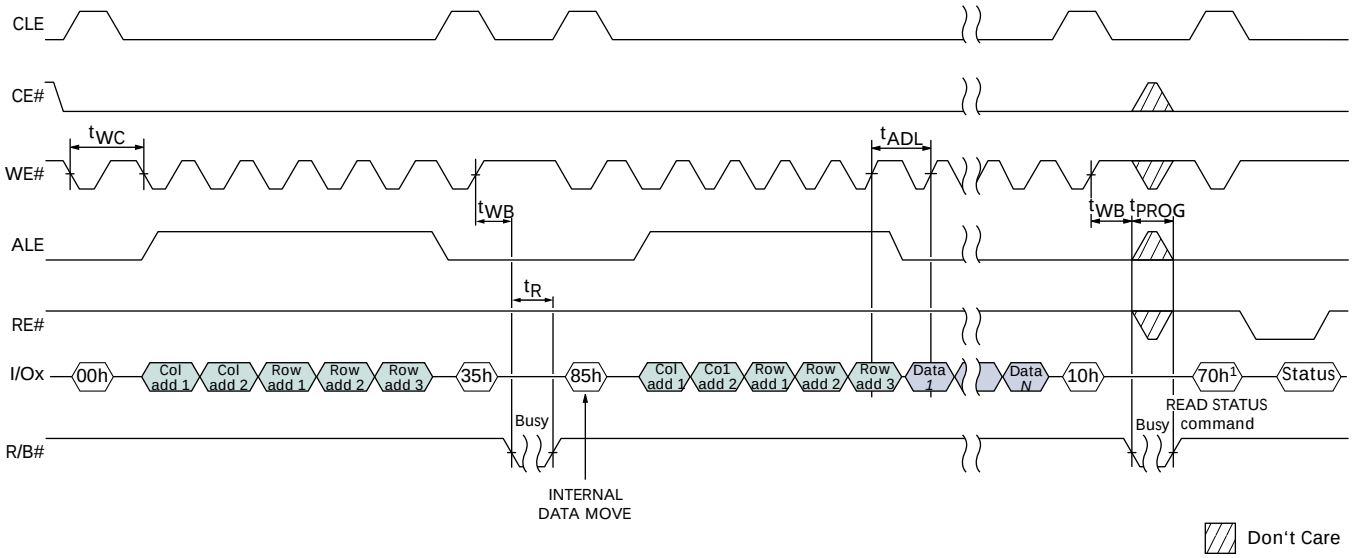
Notes: 1. Command can be 70h or 78h.

Figure 77: PROGRAM PAGE Operation with RANDOM DATA INPUT



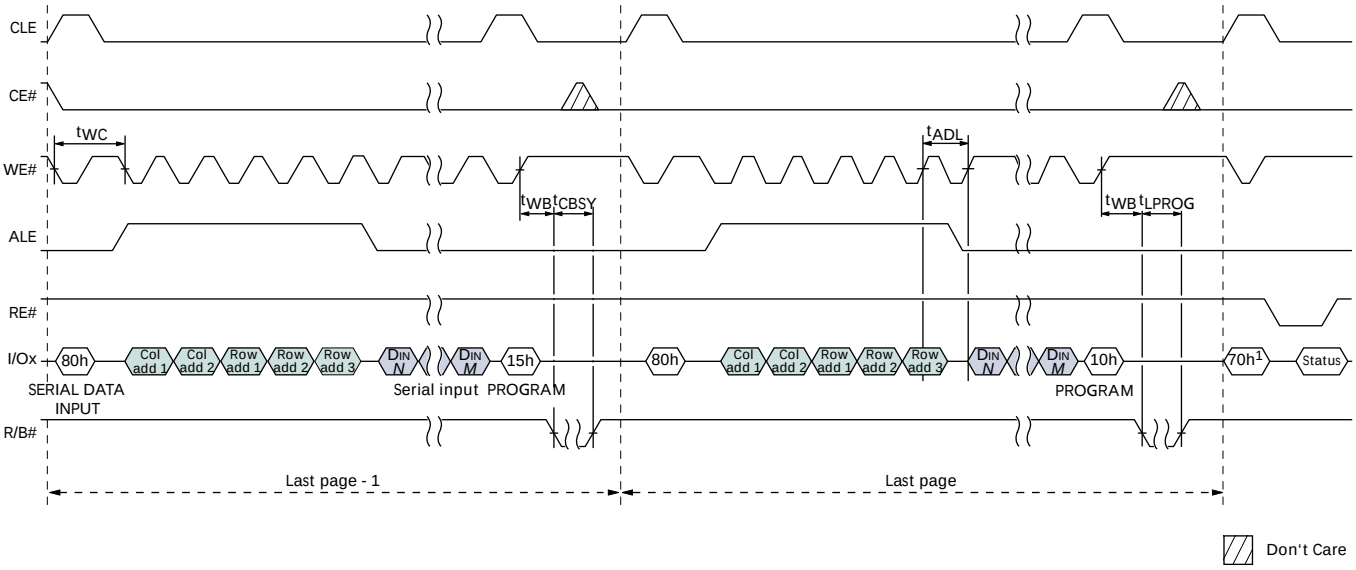
Notes: 1. Command can be 70h or 78h.

Figure 78: INTERNAL DATA MOVE Operation



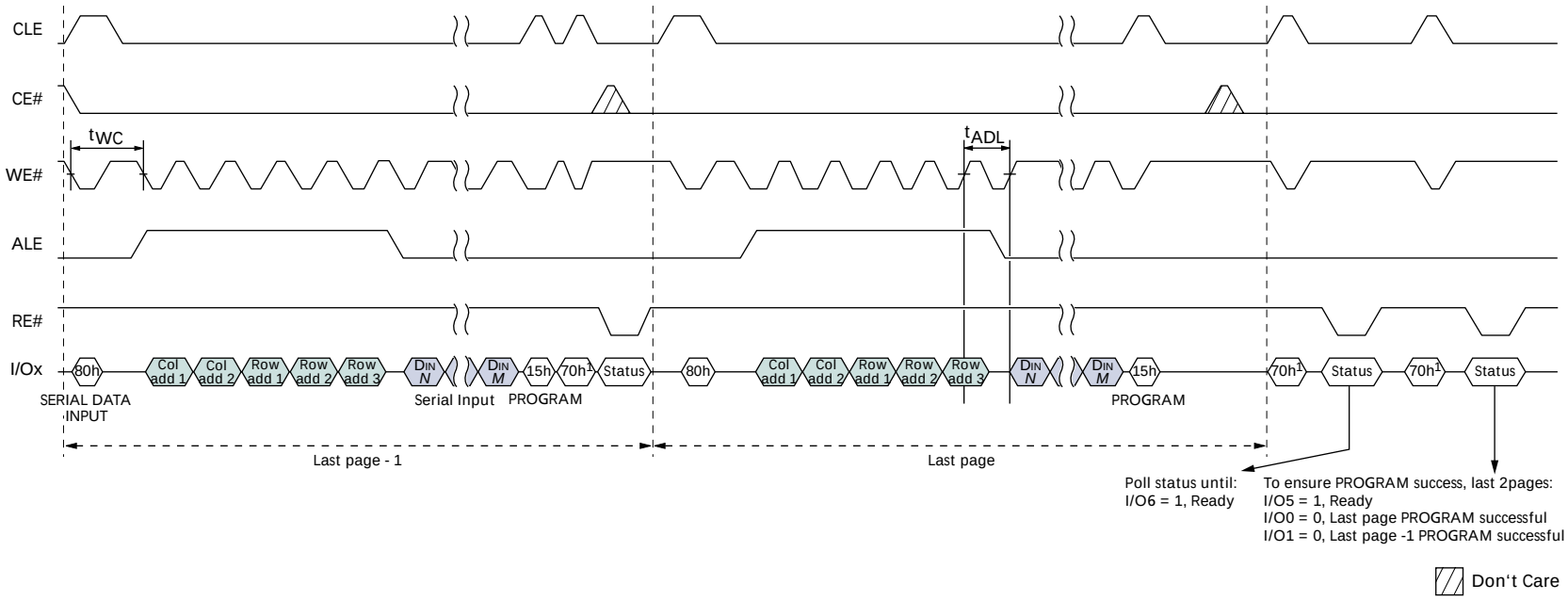
Notes: 1. Command can be 70h or 78h.

Figure 79: PROGRAM PAGE CACHE MODE Operation



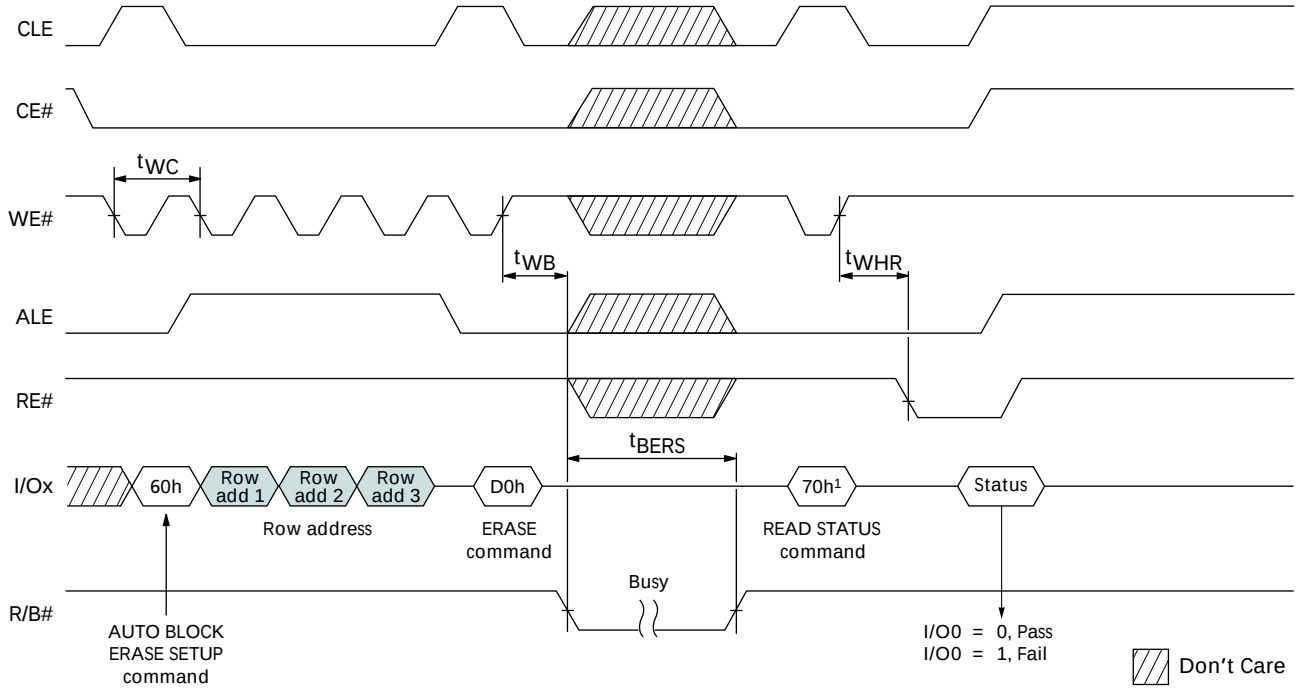
Notes: 1. Command can be 70h or 78h.
2. PROGRAM PAGE CACHE MODE operations must not cross die address boundaries.

Figure 80: PROGRAM PAGE CACHE MODE Operation Ending on 15h



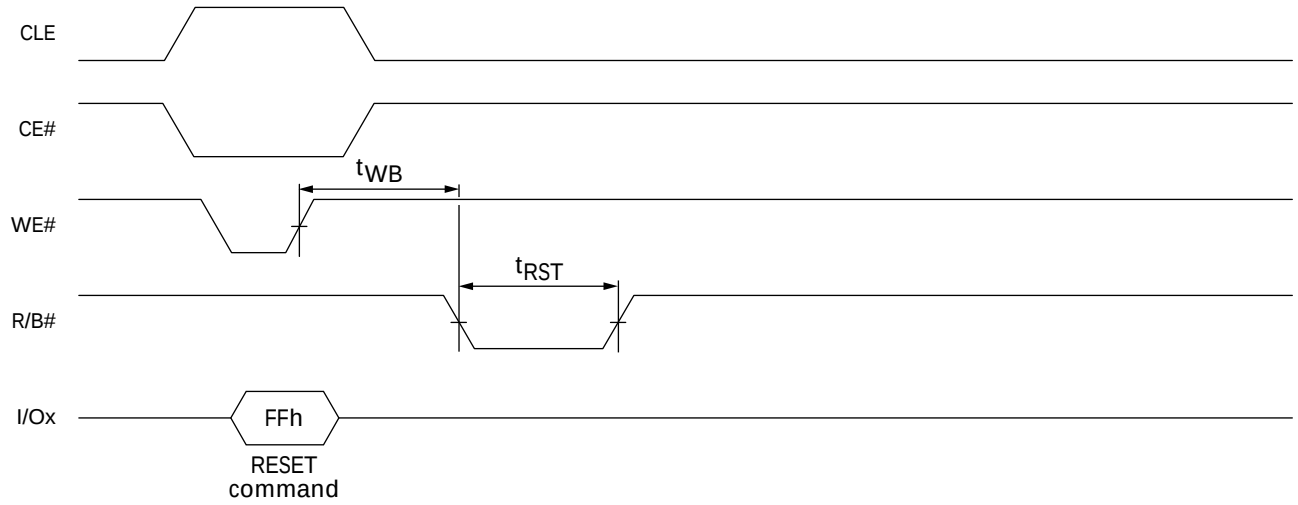
Notes: 1. Command can be 70h or 78h.

Figure 81: BLOCK ERASE Operation



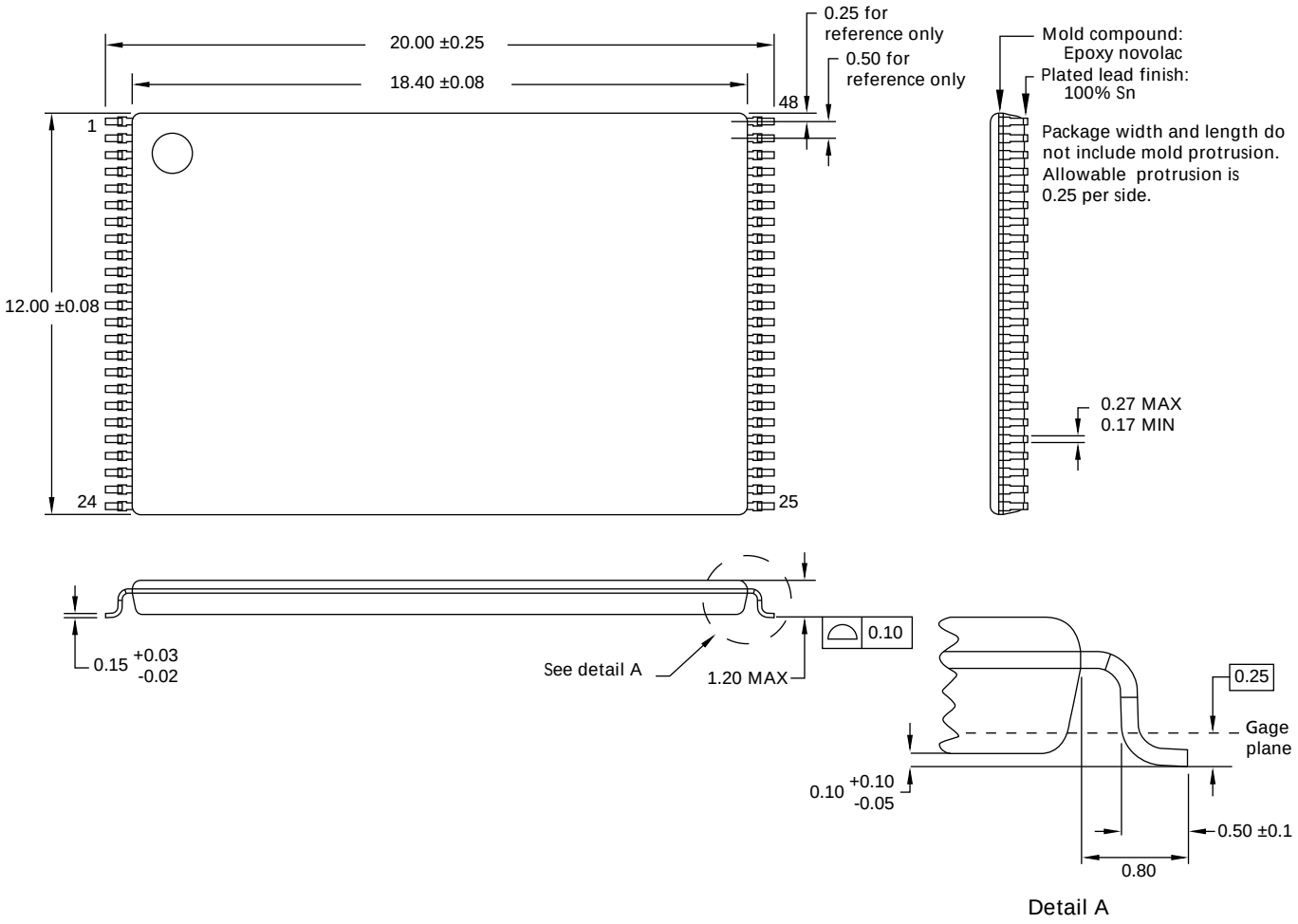
Notes: 1. Command can be 70h or 78h.

Figure 82: RESET Operation



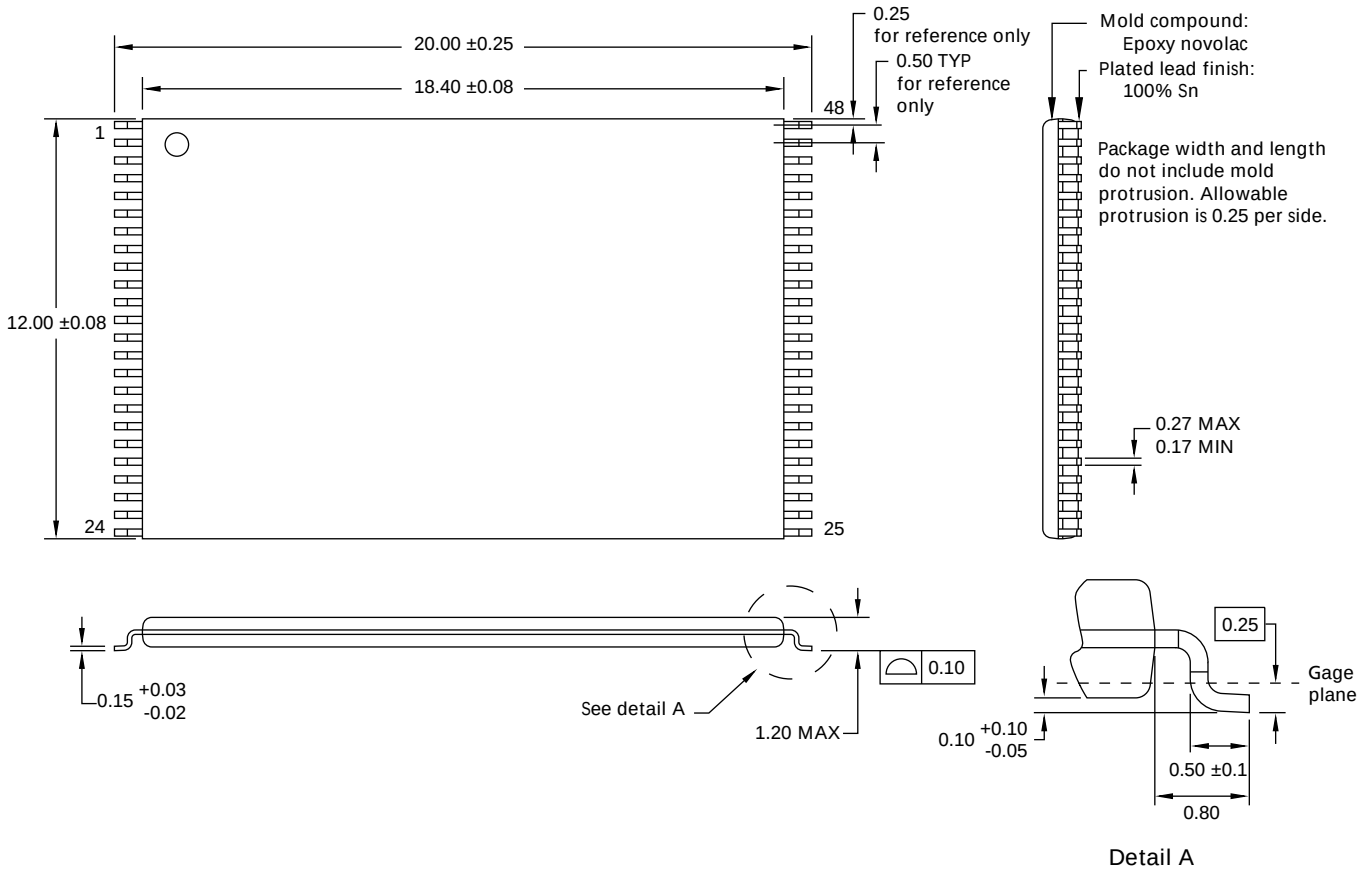
Package Dimensions

Figure 83: 48-Pin TSOP Type 1 OCPL (WC Package Code)



Note: All dimensions are in millimeters.

Figure 84: 48-Pin TSOP Type 1 CPL (WP Package Code)



Note: All dimensions are in millimeters.

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Revision History

Rev. B,. 10/07

- "Error Management" on page 64: Updated NVB to 3,996.
- Table 13, "M29FxGxx Device DC and Operating Characteristics," on page 67: Updated values for Icc1, Icc2, and Icc3.
- Table 14, "Valid Blocks," on page 67: Updated MIN valid blocks to 3,996 for the MT29F8Gxx; to 7,992 for the MT29F16Gxx, and to 15,984 for the MT29F32Gxx. Updated Note 3 from 160 to 100 (MAX) invalid blocks per CE#. Updated Note 4 from 320 to 200 (MAX) invalid blocks per CE#, and the not-to-exceed count from 200 to 160 per NAND Flash die.

Rev A. 9/07

- Initial restricted release.