NAND Flash with Mobile LPDDR2 162-Ball MCP

MT29RZ4B2DZZHHTB-18W.80F, MT29RZ4B2DZZHHTB-18I.80F

Features

- Micron NAND Flash and LPDDR2 components
- RoHS-compliant, "green" package
- Separate NAND Flash and LPDDR2 interfaces
- Space-saving multichip package (MCP)
- Low-voltage operation (1.70–1.95V)
- Wireless temperature range: –30°C to +85°C
- Industrial temperature range: –40°C to +85°C

NAND Flash-Specific Features

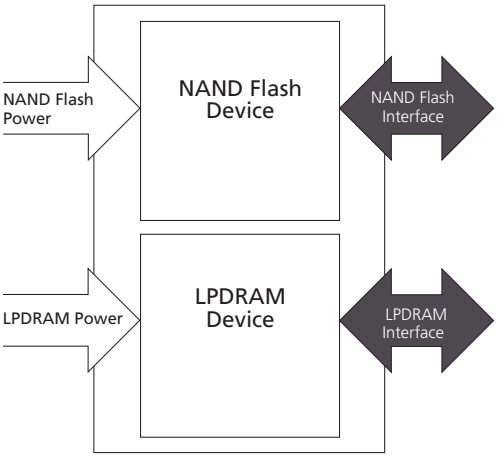
Organization

- Page size
  - x8: 4320 bytes (4096 + 224 bytes)
- 1.8V (V_{CC}: 1.70–1.95V)
- Block size: 64 pages (128K + 4K bytes)
- Plane size: 2 planes x 1024 blocks per plane

LPDDR2-Specific Features

- Ultra-low-voltage 1.2V core power supply
- 1.2V HSUL-compatible inputs
- Programmable READ and WRITE latencies
- Programmable burst lengths: 4, 8, or 16
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- Adjustable clock frequency and clock stop capabilities

Figure 1: MCP Block Diagram



Note: 1. For physical part markings, see Part Numbering Information (page 2).

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	READ Latency	WRITE Latency
-18	533	1066	8	4

Table 2: S4 Configuration Addressing

Architecture	64 Meg x 32
Die configuration	2 x 8 Meg x 16 x 8 banks
Row addressing	8K (A[12:0])
Column addressing	1K (A[9:0])
Number of die	2
Die per rank	2
Ranks per channel[1]	1

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Table 3: Part Number References

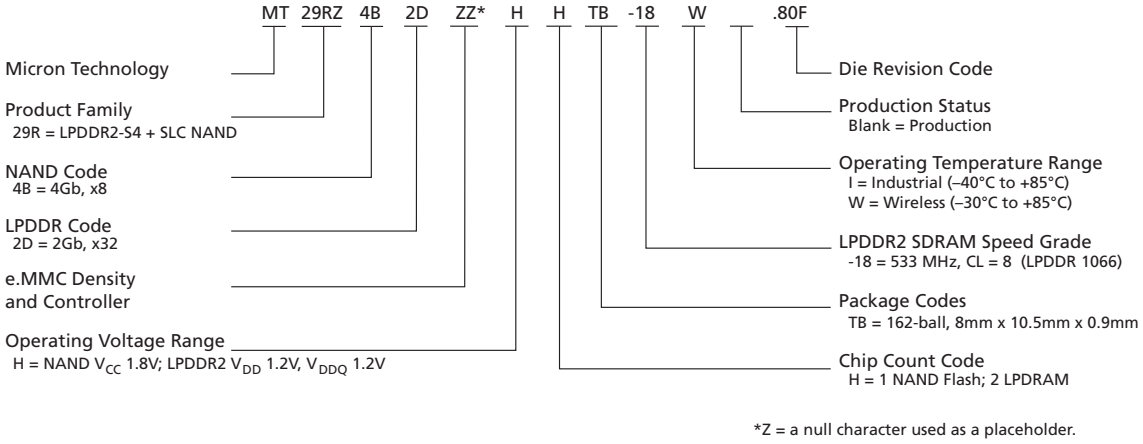
MCP	NAND Discrete	NAND READ ID Parameter
MT29RZ4B2DZZHHTB-18W.80F MT29RZ4B2DZZHHTB-18I.80F	MT29F4G08	MT29F4G08ABBEA 4Gb, x8, 1.8V

Note: 1. While this is the NAND 1.8V device, the lock pin is not supported, and the LOCK feature does not apply.

Part Numbering Information

Micron NAND Flash and LPDRAM devices are available in different configurations and densities. The MCP/PoP part numbering guide is available at www.micron.com/numbering.

Figure 2: Part Number Chart



*Z = a null character used as a placeholder.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

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MCP General Description

Micron MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile LPDRAM devices are also members of the Micron memory products portfolio.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

Ball Assignments and Descriptions

Figure 3: 162-Ball FBGA (x8, x16 NAND; x32 LPDDR2) Ball Assignments

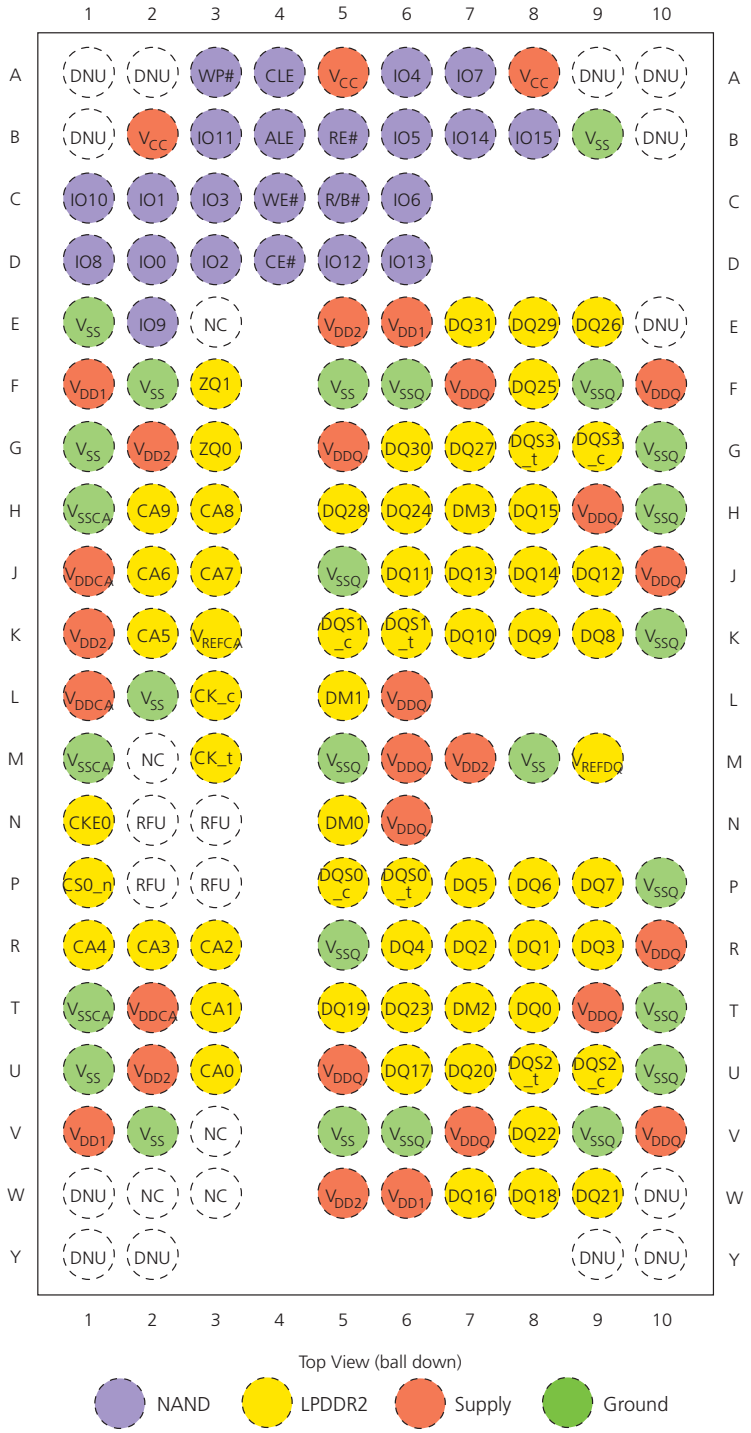


Table 4: NAND Ball Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.
CE#	Input	Chip enable: Gates transfers between the host system and the NAND device.
CLE	Input	Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.
RE#	Input	Read enable: Gates information from the NAND device to the host system.
WE#	Input	Write enable: Gates information from the host system to the NAND device.
WP#	Input	Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.
I/O[7:0] (x8) I/O[15:0] (x16)	Input/ output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.I/O[15:8] are RFU[1] for NAND x8 devices.
R/B#	Output	Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress.
V_{CC}	Supply	V_{CC}: NAND power supply.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 5: LPDDR2 Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE0	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS_n	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.

Table 5: LPDDR2 Ball/Pad Descriptions (Continued)

Symbol	Type	Description
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ0, ZQ1	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.

Table 6: Non-Device-Specific Descriptions

Symbol	Type	Description
V_{SS}	Supply	V_{SS}: Shared ground.
Symbol	**Type**	**Description**
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.
RFU[1]	–	Reserved for future use.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Electrical Specifications

Table 7: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
V_{CC} supply voltage relative to V_{SS}	V_{CC}	–0.6	2.4	V
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.3	V
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.6	V
V_{DDCA} and V_{DDQ} supply voltage relative to V_{SS}	V_{DDCA}, V_{DDQ}	–0.4	1.6	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.4	1.6 or (V_{DDQ} + 0.3), whichever is less	V
Storage temperature range	–	–55	+125	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

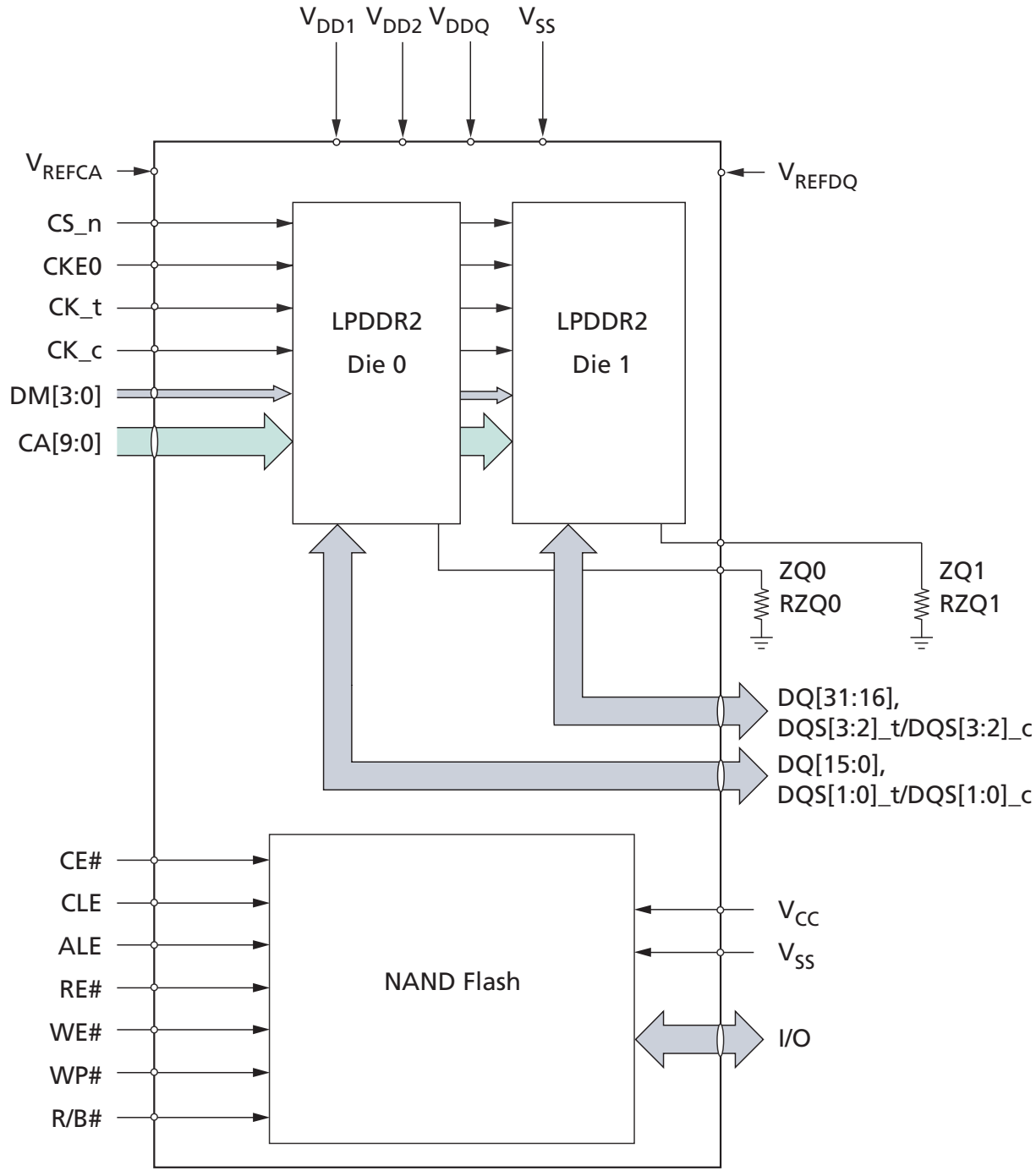
Table 8: Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	1.70	1.80	1.95	V
Supply voltage		V_{DD1}	1.70	1.80	1.95	V
Supply voltage		V_{DD2}	1.14	1.20	1.30	V
I/O supply voltage		V_{DDCA}/ V_{DDQ}	1.14	1.20	1.30	V
Operating temperature range	Wireless Temperature	–	–30	–	+85	°C
	Industrial Temperature	–	–40	–	+85	°C

Note: 1. This operating temperature range pertains to this MCP device. Other temperature ranges mentioned in data sheet apply to discrete components, respectively.

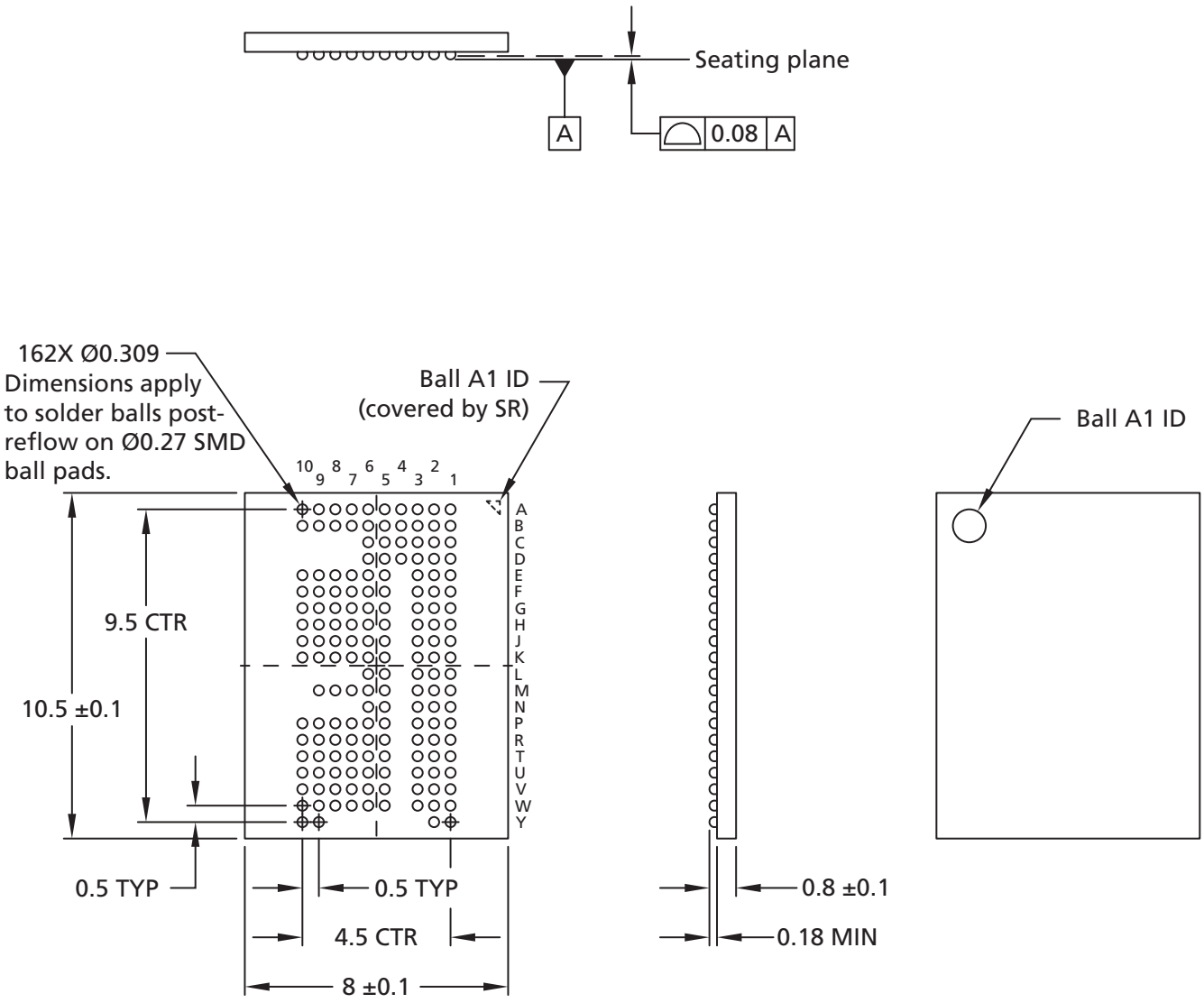
Device Diagrams

Figure 4: Functional Block Diagram



Package Dimensions

Figure 5: 162-Ball VFBGA (Package Code: TB)



Notes:
1. Solder ball material: LF35 with Cu OSP ball pads (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).
2. All dimensions are in millimeters.

4Gb: x8, x16 NAND Flash Memory

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4320 bytes (4096 + 224 bytes)
  - Page size x16: 2160 words (2048 + 112 words)
  - Block size: 64 pages (256K + 14K bytes)
  - Plane size: 2 planes x 1024 blocks per plane
  - Device size: 4Gb: 2048 blocks
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 20ns (3.3V), 30ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP)
  - Erase block: 2ms (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program page cache mode
  - Read page cache mode
  - One-time programmable (OTP) mode
  - Block lock (1.8V only)
  - Programmable drive strength
  - Two-plane commands
  - Multi-die (LUN) operations
  - Read unique ID
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) provides a hardware method of detecting operation completion
- WP#: Write protect entire device

- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization after power-up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: JESD47G-compliant; see qualification report
  - Endurance: 60,000 PROGRAM/ERASE cycles
- Operating voltage range
  - V_{CC}: 2.7–3.6V
  - V_{CC}: 1.7–1.95V
- Operating temperature
  - Commercial: 0°C to +70°C
  - Industrial (IT): –40°C to +85°C

Note: 1. The ONFI 1.0 specification is available at www.onfi.org.

General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.

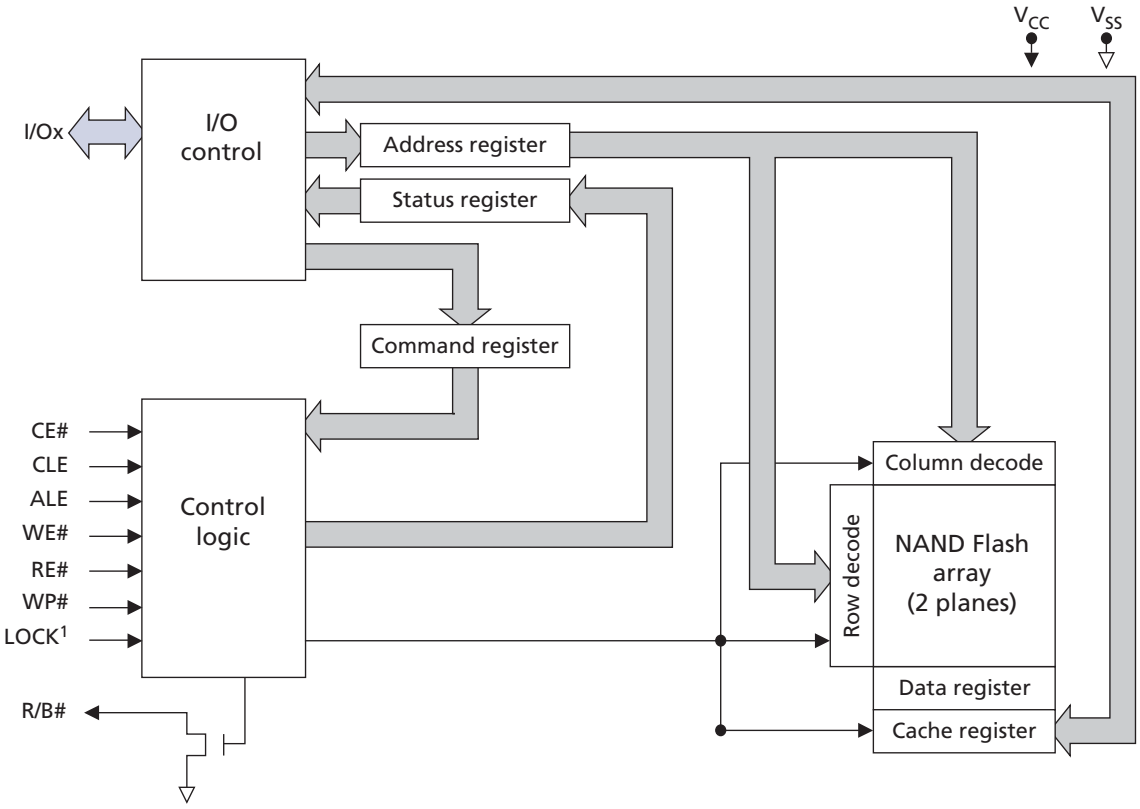
Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput. The status register reports the status of die operations.

Figure 6: NAND Flash Die (LUN) Functional Block Diagram



Note: 1. The LOCK pin is used on the 1.8V device.

Device and Array Organization

Figure 7: Array Organization – MT29F4G (x8)

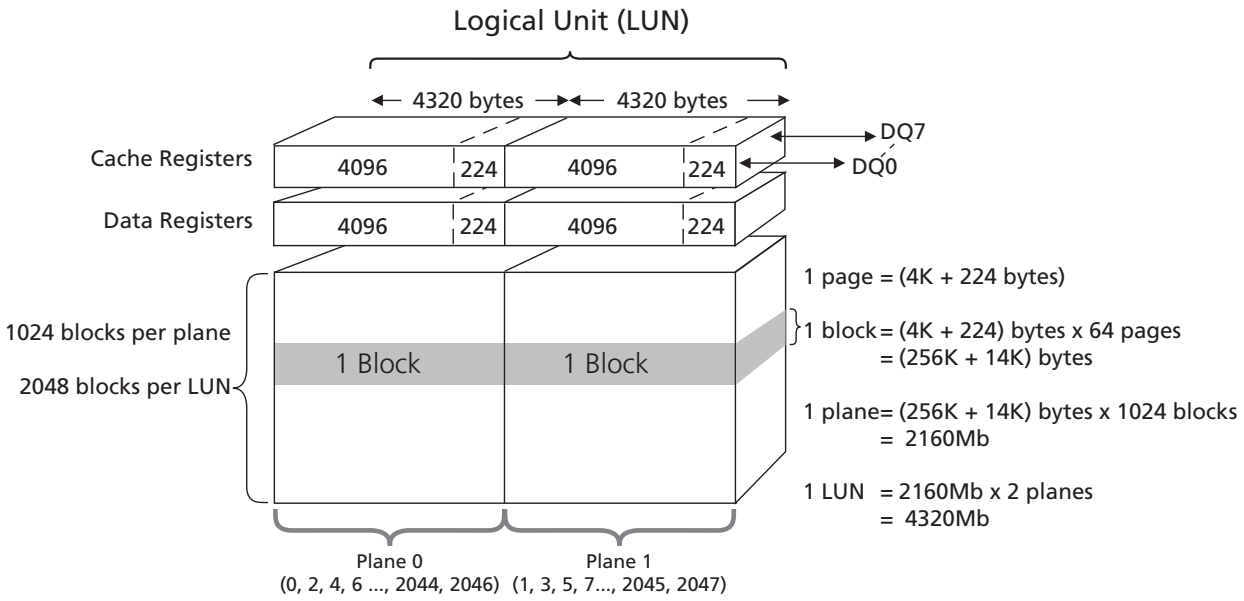


Table 9: Array Addressing (MT29F4G08)

Cycle	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA12 is 1, then CA[11:8] must be 0.
3. BA6 controls plane selection.

Figure 8: Array Organization – MT29F4G (x16)

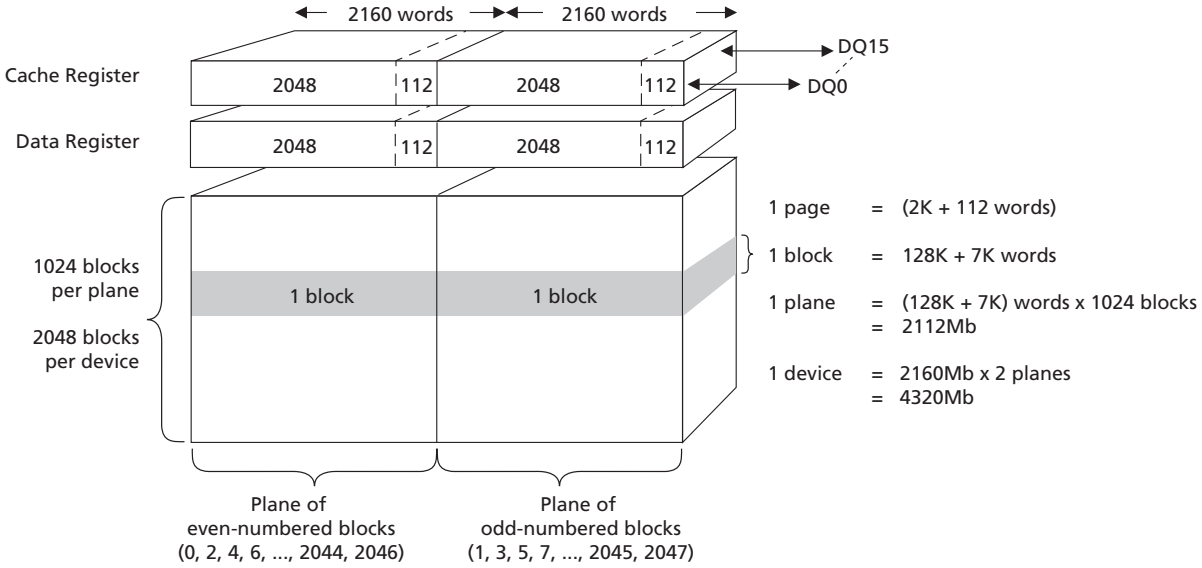


Table 10: Array Addressing (MT29F4G16xxx – x16)

Cycle	I/O[15:8]	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA11 = 1, then CA[10:7] must be 0.
3. BA6 controls plane selection.

Asynchronous Interface Bus Operation

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

Table 11: Asynchronous Interface Mode Selection

Mode[1]	CE#	CLE	ALE	WE#	RE#	I/Ox	WP#
Standby[2]	H	X	X	X	X	X	0V/V_{CC}
Command input	L	H	L	↑	H	X	H
Address input	L	L	H	↑	H	X	H
Data input	L	L	L	↑	H	X	H
Data output	L	L	L	H	↓	X	X
Write protect	X	X	X	X	X	X	L

Notes:
1. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.
2. WP# should be biased to CMOS LOW or HIGH for standby.

Asynchronous Enable/Standby

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

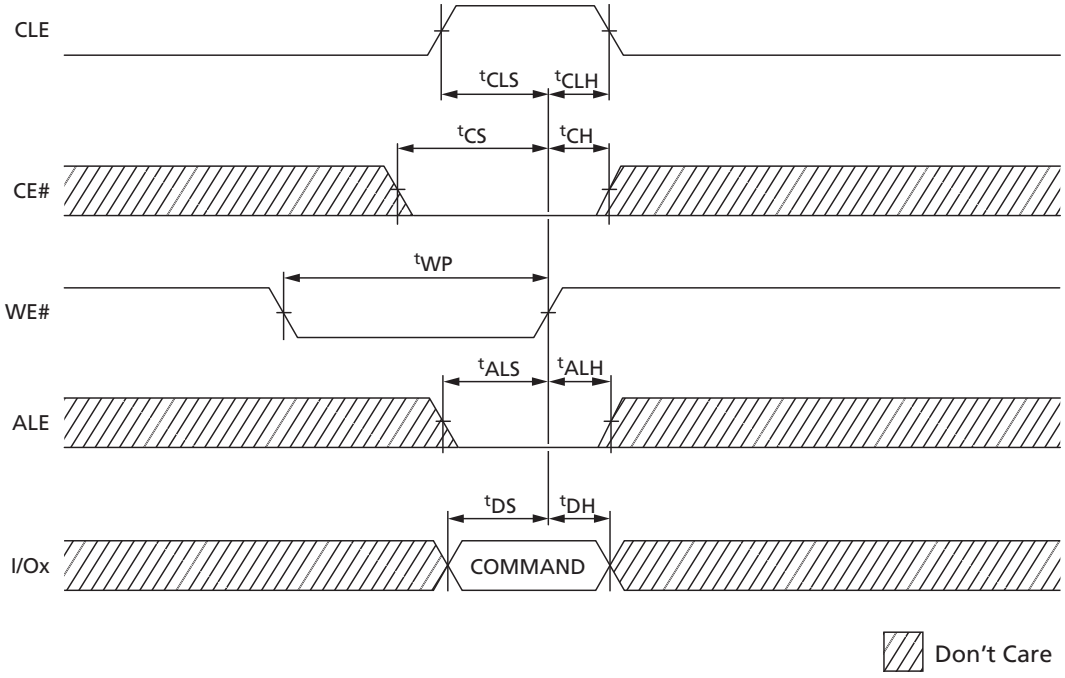
Asynchronous Commands

An asynchronous command is written from I/O[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

For devices with a x16 interface, I/O[15:8] must be written with zeros when a command is issued.

Figure 9: Asynchronous Command Latch Cycle



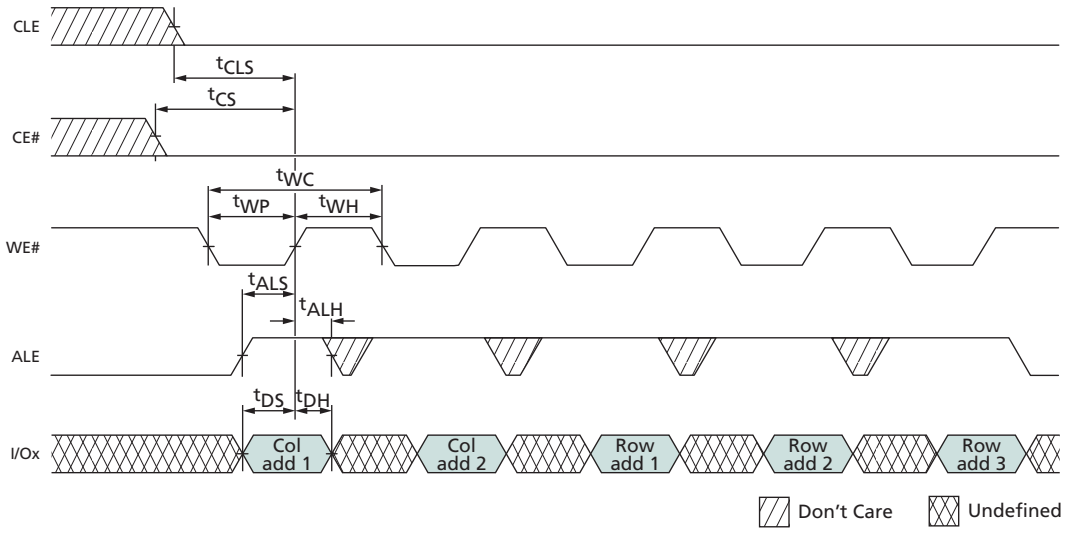
Asynchronous Addresses

An asynchronous address is written from I/O[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, like address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 10: Asynchronous Address Latch Cycle



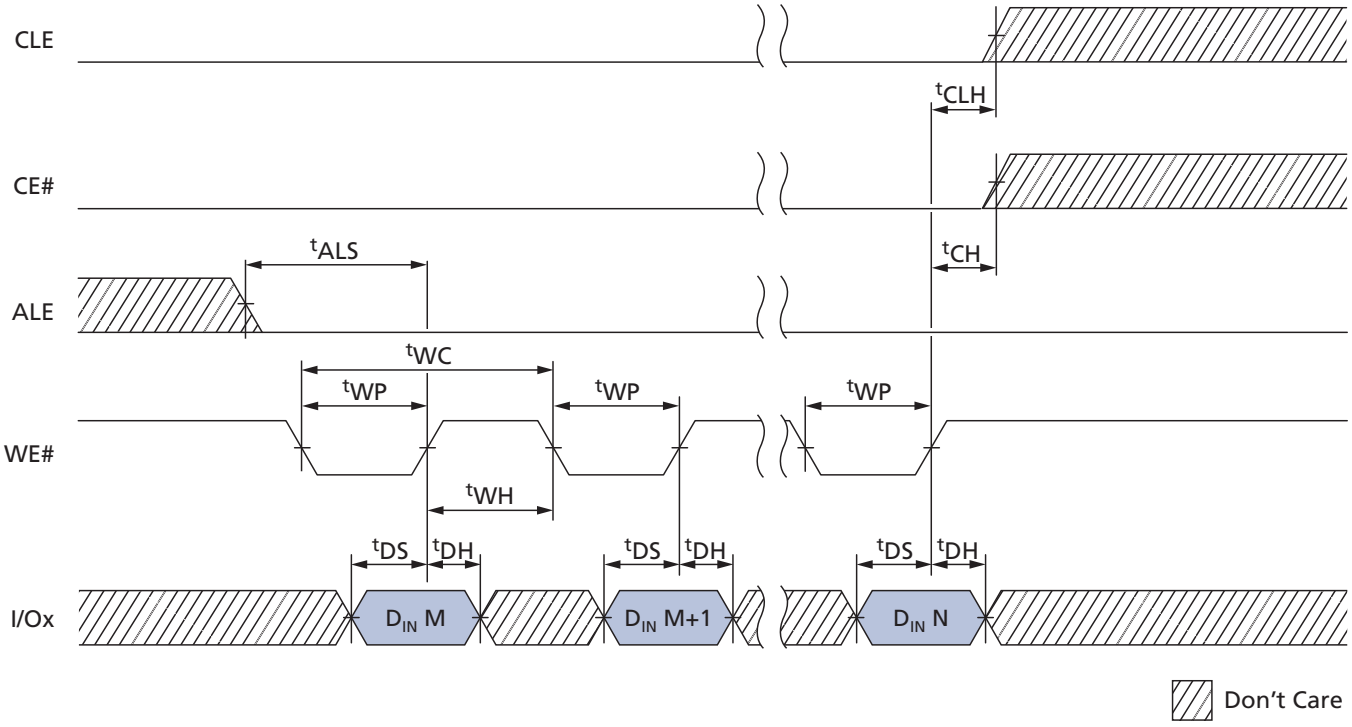
Asynchronous Data Input

Data is written from I/O[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0). Data is written to the data register on the rising edge of WE# when CE#, CLE, and ALE are LOW, and the device is not busy.

Data is input on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices.

Figure 11: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to I/O[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see the figure below for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE#.

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS or READ STATUS ENHANCED (78h) command.

Figure 12: Asynchronous Data Output Cycles

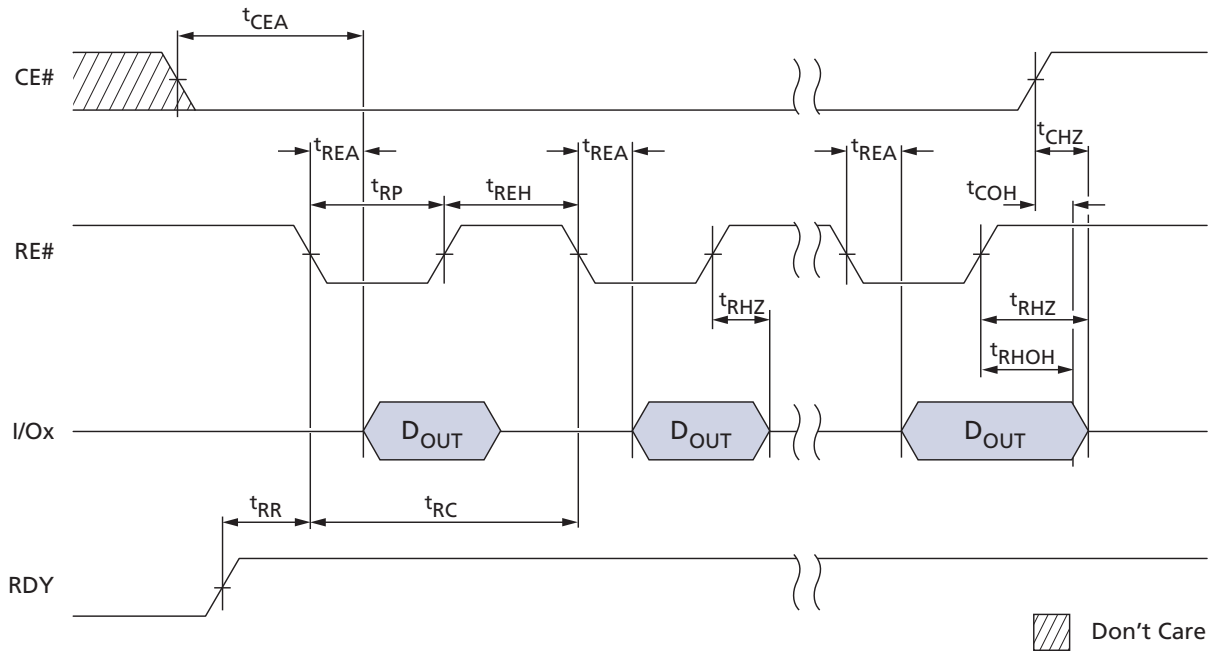
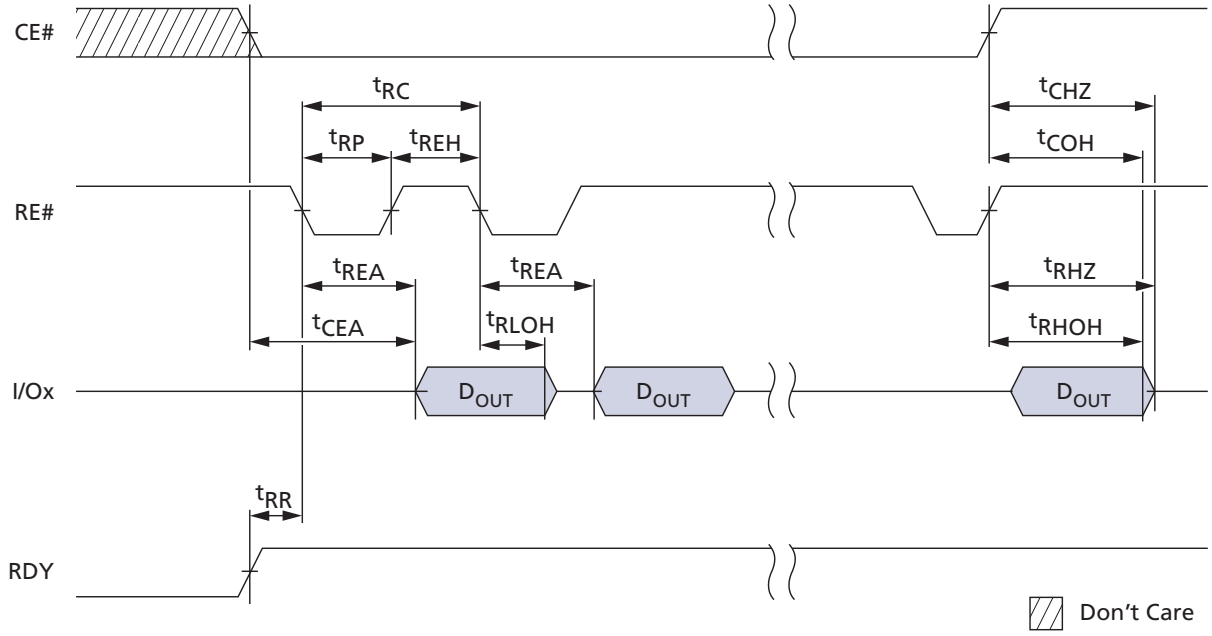


Figure 13: Asynchronous Data Output Cycles (EDO Mode)



Write Protect#

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled. When WP# is LOW or toggled LOW during a READ operation, read will be performed as normal. It is recommended that the host drive WP# LOW during power-on until V_{CC} is stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization for additional details).

If WP# is toggled during PROGRAM or ERASE (while RB# is LOW), then the following will occur

- The PROGRAM or ERASE operation is aborted
- In asynchronous mode, toggling WP# LOW during a NAND PROGRAM or ERASE operation will act like a RESET (FFh) command. In synchronous mode, it will act like a SYNCHRONOUS RESET (FCh) command
- The data that was being programmed or erased (targeted page or block) is not valid anymore
- The status register will be set to 60h until a RESET, new operation, or new power up command is given

After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10% and 90% points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$T_C = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 19 (page 35).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp = \frac{V_{CC}(MAX) - V_{OL}(MAX)}{I_{OL} + \Sigma_{IL}}$$

Where Σ_{IL} is the sum of the input currents of all devices tied to the R/B# pin.

Figure 14: READ/BUSY# Open Drain

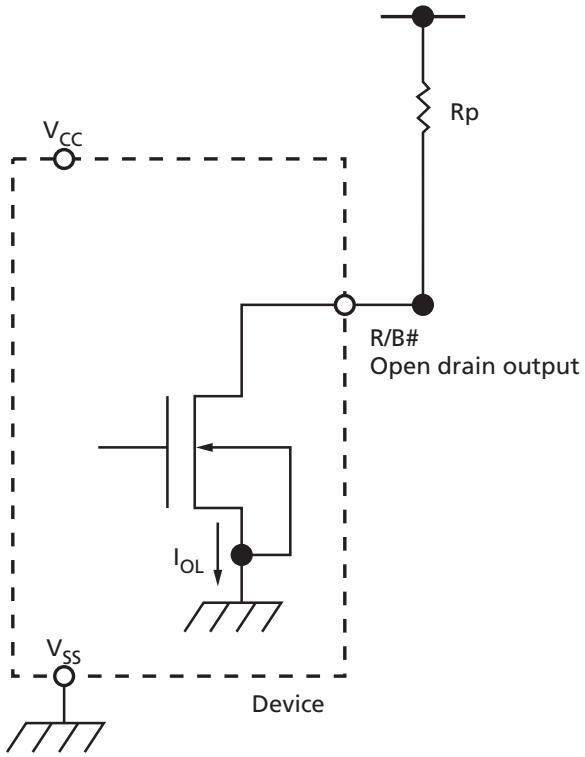
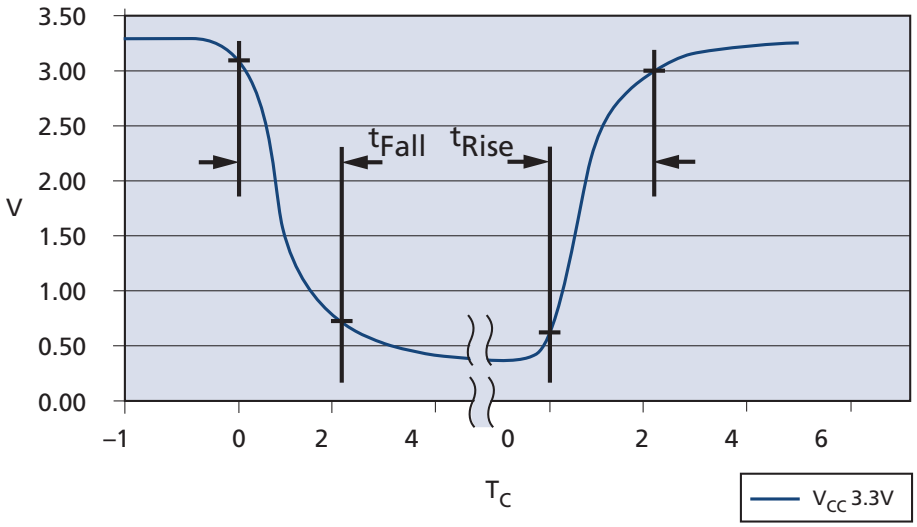
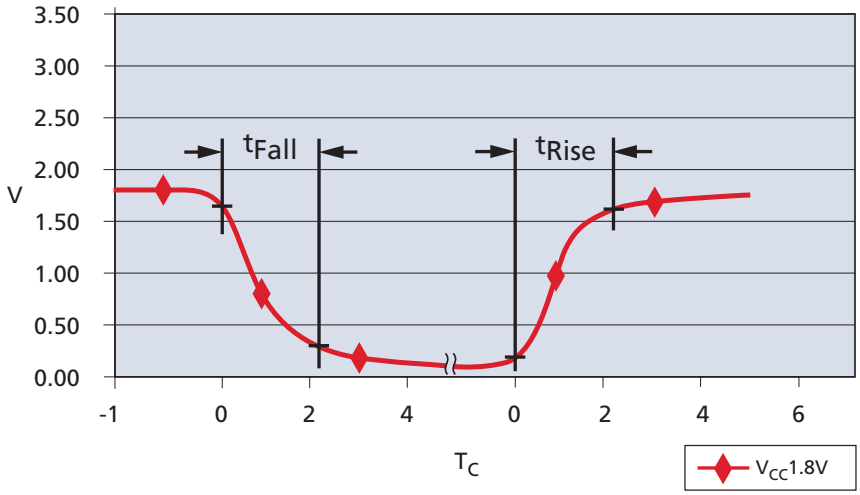


Figure 15: ^{t}Fall and ^{t}Rise (3.3V V_{CC})



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10% and 90% points.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall = 10ns at 3.3V.
5. See TC values in Figure 19 (page 35) for approximate Rp value and TC.

Figure 16: ^{t}Fall and ^{t}Rise (1.8V V_{CC})



Notes:
1. ^{t}Fall and ^{t}Rise are calculated at 10% and 90% points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 19 (page 35) for TC and approximate Rp value.

Figure 17: I_{OL} vs. Rp (V_{CC} = 3.3V V_{CC})

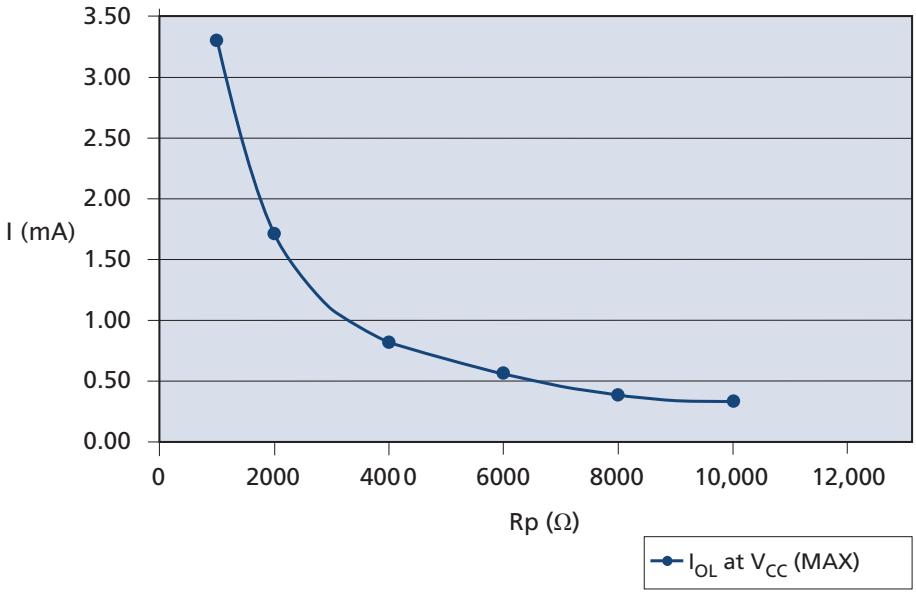


Figure 18: I_{OL} vs. Rp (1.8V V_{CC})

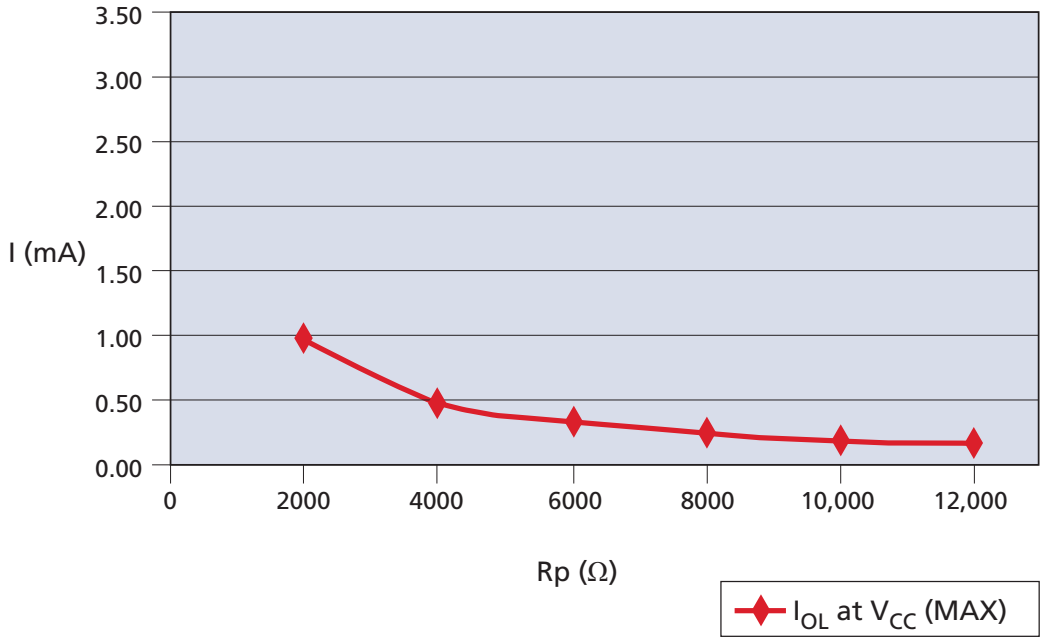
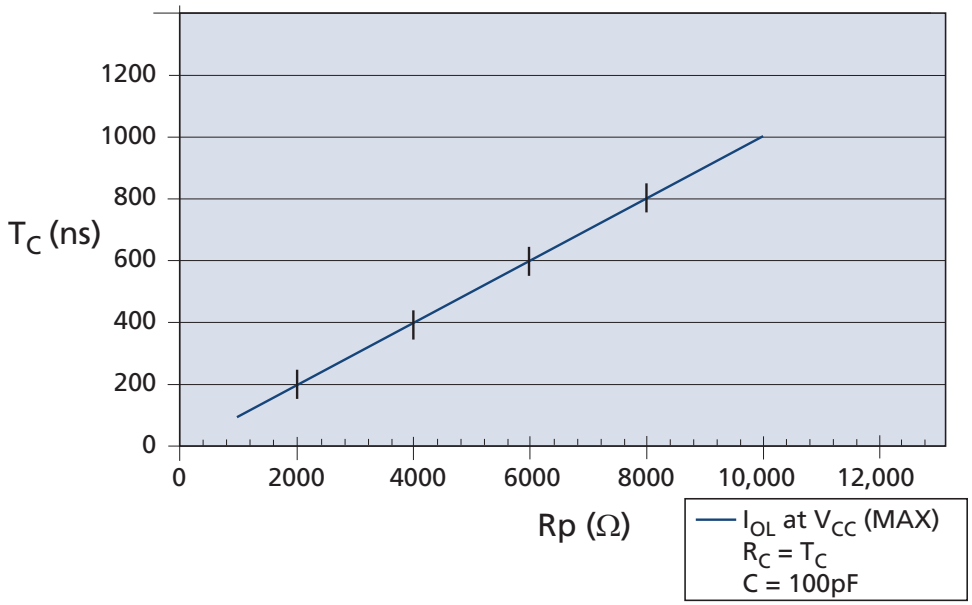


Figure 19: TC vs. Rp

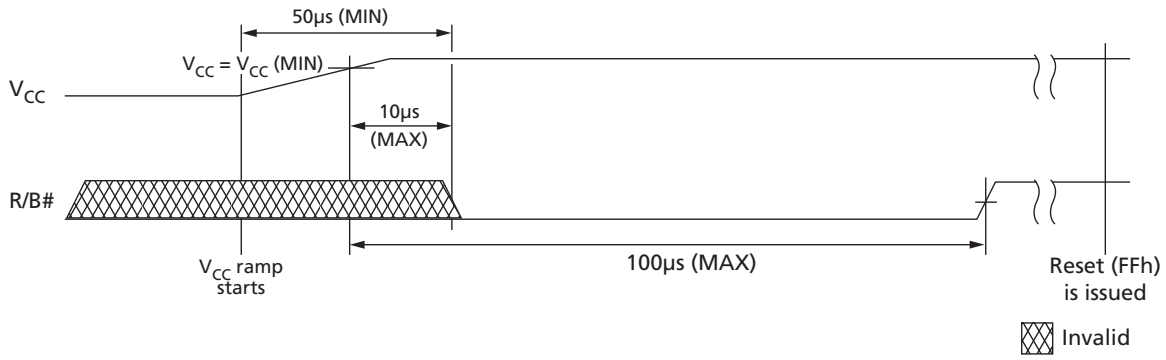


Device Initialization

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CC} reaches V_{CC} (MIN).
3. If not monitoring R/B#, the host must wait at least 100µs after V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
4. The asynchronous interface is active by default for each target. Each LUN draws less than an average of 10mA (I_{ST}) measured over intervals of 1ms until the RESET (FFh) command is issued.
5. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for 1ms after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
6. The device is now initialized and ready for normal operation.

Figure 20: R/B# Power-On Behavior



Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 12: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

Command Definitions

Table 13: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Operations							
RESET	FFh	0	–	–	Yes	Yes	
Identification Operation							
READ ID	90h	1	–	–	No	No	
READ PARAMETER PAGE	ECh	1	–	–	No	No	
READ UNIQUE ID	EDh	1	–	–	No	No	
Feature Operations							
GET FEATURES	EEh	1	–	–	No	No	
SET FEATURES	EFh	1	4	–	No	No	
Status Operations							
READ STATUS	70h	0	–	–	Yes		
READ STATUS ENHANCED	78h	3	–	–	Yes	Yes	
Column Address Operations							
RANDOM DATA READ	05h	2	–	E0h	No	Yes	
RANDOM DATA INPUT	85h	2	Optional	–	No	Yes	
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	–	No	Yes	3
READ OPERATIONS							
READ MODE	00h	0	–	–	No	Yes	
READ PAGE	00h	5	–	30h	No	Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	No	Yes	4
READ PAGE CACHE RANDOM	00h	5	–	31h	No	Yes	4
READ PAGE CACHE LAST	3Fh	0	–	–	No	Yes	4
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h	No	Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h	No	Yes	5
Erase Operations							
ERASE BLOCK	60h	3	–	D0h	No	Yes	
Internal Data Move Operations							
READ FOR INTERNAL DATA MOVE	00h	5	–	35h	No	Yes	3

Table 13: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	10h	No	Yes	
Block Lock Operations							
BLOCK UNLOCK LOW	23h	3	–	–	No	Yes	
BLOCK UNLOCK HIGH	24h	3	–	–	No	Yes	
BLOCK LOCK	2Ah	–	–	–	No	Yes	
BLOCK LOCK-TIGHT	2Ch	–	–	–	No	Yes	
BLOCK LOCK READ STATUS	7Ah	3	–	–	No	Yes	
One-Time Programmable (OTP) Operations							
OTP DATA LOCK BY BLOCK (ONFI)	80h	5	No	10h	No	No	6
OTP DATA PROGRAM (ONFI)	80h	5	Yes	10h	No	No	6
OTP DATA READ (ONFI)	00h	5	No	30h	No	No	6

Notes:
1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations (see Interleaved Die Multi-LUN Operations).
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE.
4. Issuing a READ PAGE CACHE series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE series command; otherwise, it is prohibited.
5. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
6. OTP commands can be entered only after issuing the SET FEATURES command with the feature address.

Table 14: Two-Plane Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Command Cycle #2	Number of Valid Address Cycles	Command Cycle #3	Valid While Selected LUN is Busy	Valid While Other LUNs are Busy	Notes
READ PAGE TWO-PLANE	00h	5	00h	5	30h	No	Yes	
READ FOR TWO-PLANE INTERNAL DATA MOVE	00h	5	00h	5	35h	No	Yes	1

Table 14: Two-Plane Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Command Cycle #2	Number of Valid Address Cycles	Command Cycle #3	Valid While Selected LUN is Busy	Valid While Other LUNs are Busy	Notes
RANDOM DATA READ TWO-PLANE	06h	5	E0h	–	–	No	Yes	2
PROGRAM PAGE TWO-PLANE	80h	5	11h-80h	5	10h	No	Yes	
PROGRAM PAGE CACHE MODE TWO-PLANE	80h	5	11h-80h	5	15h	No	Yes	
PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE	85h	5	11h-85h	5	10h	No	Yes	1
BLOCK ERASE TWO-PLANE	60h	3	D1h-60h	3	D0h	No	Yes	3

Notes:
1. Do not cross plane boundaries when using READ FOR INTERNAL DATA MOVE TWO-PLANE or PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE.
2. The RANDOM DATA READ TWO-PLANE command is limited to use with the PAGE READ TWO-PLANE command.
3. D1h command can be omitted.

Reset Operations

RESET (FFh)

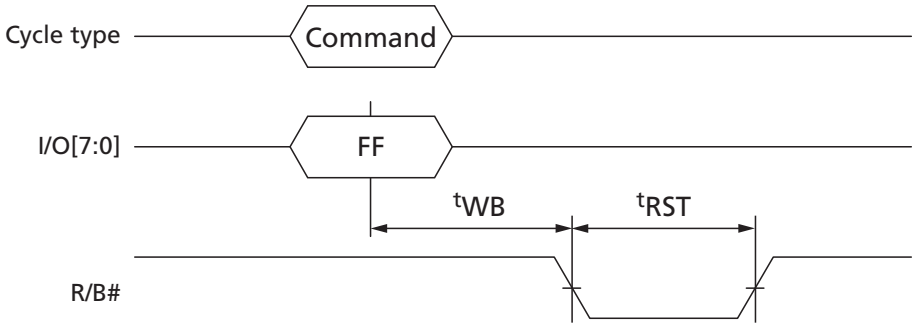
The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register.

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms.

Figure 21: RESET (FFh) Operation



Identification Operations

READ ID (90h)

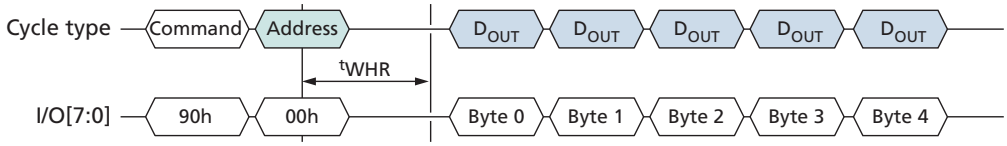
The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

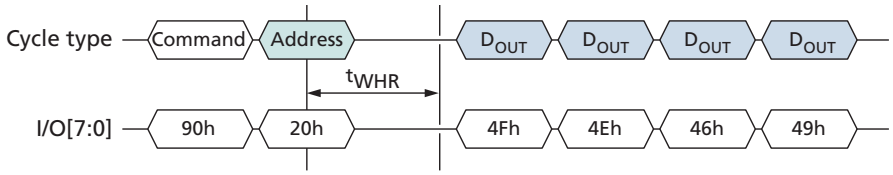
When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

Figure 22: READ ID (90h) with 00h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 23: READ ID (90h) with 20h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 15: READ ID Parameters for Address 00h

		Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]
Byte 0 – Manufacturer ID											
Manufacturer		Micron	0	0	1	0	1	1	0	0	2Ch
Byte 1 – Device ID											
MT29F4G08ABBEA		4Gb, x8, 1.8V	1	0	1	0	1	1	0	0	ACh
MT29F4G16ABBEA		4Gb, x16, 1.8V	1	0	1	1	1	1	0	0	BCh
MT29F4G08ABAEA		4Gb, x8, 3.3V	1	1	0	1	1	1	0	0	DCh
MT29F4G16ABAEA		4Gb, x16, 3.3V	1	1	0	0	1	1	0	0	CCh
Byte 2											
Number of die per CE		1							0	0	00b
Cell type		SLC					0	0			00b
Number of simultaneously programmed pages		2			0	1					01b
Interleaved operations between multiple die		Not supported		0							0b
Cache programming		Supported	1								1b
Byte value		MT29F4G	1	0	0	1	0	0	0	0	90h
Byte 3											
Page size		4KB							1	0	10b
Spare area size (bytes)		224B						1			1b
Block size (w/o spare)		256KB			1	0					10b
Organization		x8		0							0b
		x16		1							
Serial access (MIN)	1.8V	30ns	0				0				0xxx0b
	3.3V	20ns	1				0				1xxx0b
Byte value		MT29F4G08ABBEA	0	0	1	0	0	1	1	0	26h
		MT29F4G16ABBEA	0	1	1	0	0	1	1	0	66h
		MT29F4G08ABAEA	1	0	1	0	0	1	1	0	A6h
		MT29F4G16ABAEA	1	1	1	0	0	1	1	0	E6h
Byte 4											
Reserved									0	0	00b
Planes per CE#		2					0	1			01b
Plane size		2Gb		1	0	1					101b
Reserved			0								0b
Byte value		MT29F4G	0	0	0	1	0	1	0	0	54h

Note: 1. b = binary; h = hexadecimal.

Table 16: READ ID Parameters for Address 20h

Byte	Options	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00	Value	Notes
0	"O"	0	1	0	0	1	1	1	1	4Fh	1
1	"N"	0	1	0	0	1	1	1	0	4Eh	
2	"F"	0	1	0	0	0	1	1	0	46h	
3	"I"	0	1	0	0	1	0	0	1	49h	
4	Undefined	X	X	X	X	X	X	X	X	XXh	

Note: 1. h = hexadecimal.

READ PARAMETER PAGE (ECh)

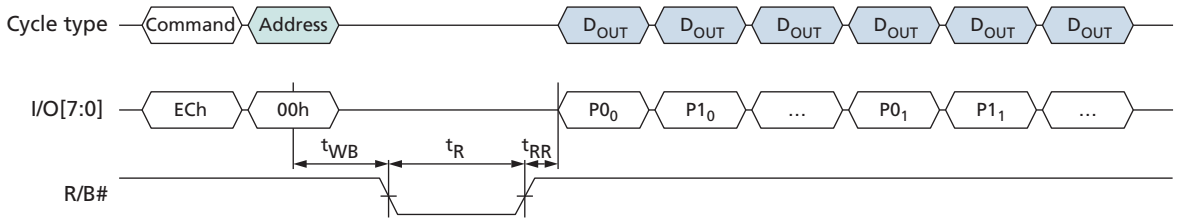
The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the location of data output.

Figure 24: READ PARAMETER (ECh) Operation



Parameter Page Data Structure Tables

Table 17: Parameter Page Data Structure

Byte	Description		Value
0–3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4–5	Revision number		02h, 00h
6–7	Features supported	MT29F4G08ABBEA3W	18h, 00h
		MT29F4G16ABBEA3W	19h, 00h
		MT29F4G08ABAEA3W	18h, 00h
		MT29F4G16ABAEA3W	19h, 00h
		MT29F4G08ABBEAH4	18h, 00h
		MT29F4G16ABBEAH4	19h, 00h
		MT29F4G08ABAEAWP	18h, 00h
		MT29F4G16ABAEAWP	19h, 00h
		MT29F4G08ABAEAH4	18h, 00h
		MT29F4G16ABAEAH4	19h, 00h
8–9	Optional commands supported		3Fh, 00h
10–31	Reserved		00h
32–43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model	MT29F4G08ABBEA3W	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 42h, 45h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F4G16ABBEA3W	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 42h, 45h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F4G08ABAEA3W	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 41h, 45h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F4G16ABAEA3W	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 41h, 45h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
		MT29F4G08ABBEAH4	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 42h, 45h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F4G16ABBEAH4	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 42h, 45h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F4G08ABAEAWP	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 41h, 45h, 41h, 57h, 50h, 20h, 20h, 20h, 20h
		MT29F4G16ABAEAWP	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 41h, 45h, 41h, 57h, 50h, 20h, 20h, 20h, 20 h
		MT29F4G08ABAEAH4	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 41h, 45h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
		MT29F4G16ABAEAH4	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 41h, 45h, 41h, 48h, 34h, 20h, 20h, 20h, 20h
64	Manufacturer ID		2Ch
65–66	Date code		00h, 00h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
67–79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80–83	Number of data bytes per page		00h, 10h, 00h, 00h
84–85	Number of spare bytes per page		E0h, 00h
86–89	Number of data bytes per partial page		00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page		38h, 00h
92–95	Number of pages per block		40h, 00h, 00h, 00h
96–99	Number of blocks per unit		00h, 08h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		23h
102	Number of bits per cell		01h
103–104	Bad blocks maximum per unit		28h, 00h
105–106	Block Endurance		06h, 04h
107	Guaranteed valid blocks at beginning of target		01h
108–109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of bits ECC bits		08h
113	Number of interleaved address bits		01h
114	Interleaved operation attributes		0Eh
115–127	Reserved		00h
128	I/O pin capacitance		0Ah
129–130	Timing mode support	MT29F4G08ABBEA3W	0Fh, 00h
		MT29F4G16ABBEA3W	0Fh, 00h
		MT29F4G08ABAEA3W	3Fh, 00h
		MT29F4G16ABAEA3W	3Fh, 00h
		MT29F4G08ABBEAH4	0Fh, 00h
		MT29F4G16ABBEAH4	0Fh, 00h
		MT29F4G08ABAEAWP	3Fh, 00h
		MT29F4G16ABAEAWP	3Fh, 00h
		MT29F4G08ABAEAH4	3Fh, 00h
		MT29F4G16ABAEAH4	3Fh, 00h

Table 17: Parameter Page Data Structure (Continued)

Byte	Description		Value
131–132	Program cache timing mode support	MT29F4G08ABBEA3W	0Fh, 00h
		MT29F4G16ABBEA3W	0Fh, 00h
		MT29F4G08ABAEA3W	3Fh, 00h
		MT29F4G16ABAEA3W	3Fh, 00h
		MT29F4G08ABBEAH4	0Fh, 00h
		MT29F4G16ABBEAH4	0Fh, 00h
		MT29F4G08ABAEAWP	3Fh, 00h
		MT29F4G16ABAEAWP	3Fh, 00h
		MT29F4G08ABAEAH4	3Fh, 00h
		MT29F4G16ABAEAH4	3Fh, 00h
133–134	^{t}PROG Maximum page program time		58h, 02h
135–136	^{t}BERS Maximum block erase time		10h, 27h
137–138	^{t}R Maximum page read time		19h, 00h
139–140	^{t}CCS Minimum		64h, 00h
141–163	Reserved		00h
164–165	Vendor-specific revision number		01h, 00h
166–253	Vendor-specific		01h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 01h, 02h, 01h, 0Ah, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254–255	Integrity CRC		Set at test
256–511	Value of bytes 0–255		
512–767	Value of bytes 0–255		
768+	Additional redundant parameter pages		

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

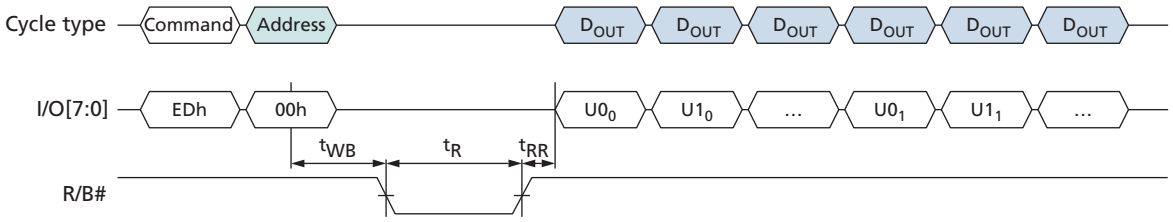
When the EDh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the data output location.

The upper eight I/Os on a x16 device are not used and are a "Don't Care" for x16 devices.

Figure 25: READ UNIQUE ID (EDh) Operation



Feature Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in below. The SET FEATURES (EFh) command writes subfeature parameters (P1–P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1–P4) at the specified feature address.

Table 18: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–FFh	Reserved
90h	Array operation mode

Table 19: Feature Address 90h – Array Operation Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Operation mode option	Normal	Reserved (0)							0	00h	1
	OTP operation	Reserved (0)							1	01h	
	OTP protection	Reserved (0)						1	1	03h	
		Reserved (0)								00h	
		Reserved (0)								00h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Note: 1. These bits are reset to 00h on power cycle.

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1–P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

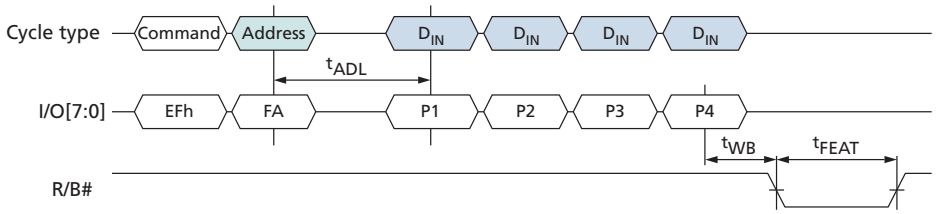
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address. The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC.

Figure 26: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1–P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited prior to and during data output.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters.

Figure 27: GET FEATURES (EEh) Operation

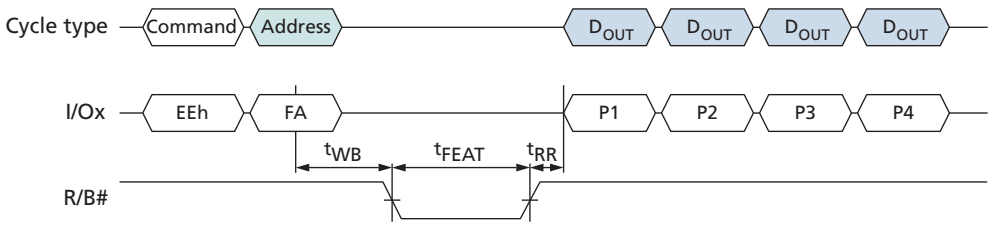


Table 20: Feature Addresses 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1, 2
	Mode 1	Reserved (0)					0	0	1	01h	2
	Mode 2	Reserved (0)					0	1	0	02h	2, 4
	Mode 3	Reserved (0)					0	1	1	03h	2
	Mode 4	Reserved (0)					1	0	0	04h	3
	Mode 5	Reserved (0)					1	0	1	05h	3
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes:
1. The timing mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.
2. Supported for both 1.8V and 3.3V.
3. Supported for 3.3V only.
4. Supported for 1.8V only. ^{t}WHR, ^{t}REA, ^{t}CEA, and ^{t}RHZ per timing mode 2. (See AC Characteristics: Normal Operation (1.8V) table for details.)

Table 21: Feature Addresses 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. The programmable drive strength feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 22: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarters							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on I/O[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see Read Operations).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations).

Table 23: Status Register Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected
6	RDY	RDY cache[1]	RDY	RDY cache[1]	RDY	0 = Busy 1 = Ready
5	ARDY	ARDY[2]	ARDY	ARDY[2]	ARDY	0 = Busy 1 = Ready
4	–	–	–	–	–	Reserved (0)
3	–	–	–	–	–	Reserved (0)
2	–	–	–	–	–	Reserved (0)
1	FAILC (N–1)	FAILC (N–1)	–	–	–	0 = Pass 1 = Fail
0	FAIL	FAIL (N)	–	–	FAIL	0 = Pass 1 = Fail

Notes:
1. Status register bit 6 is 1 when the cache is ready to accept new data. R/B# follows bit 6.
2. Status register bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.
3. A status register bit 0 reports a 1 if a TWO-PLANE PROGRAM PAGE or TWO-PLANE BLOCK ERASE operation fails on one or both planes. A status register bit 1 reports a 1 if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use READ STATUS ENHANCED (78h) to determine the plane to which the operation failed.

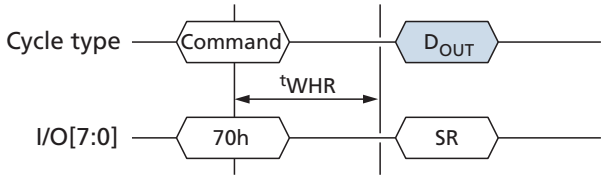
READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

Figure 28: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

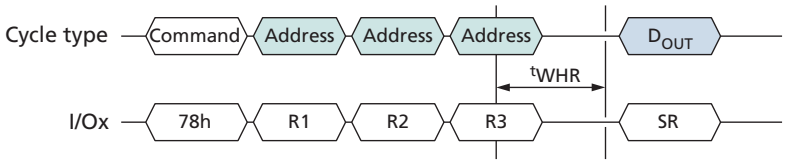
Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all planes on the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the RANDOM DATA READ TWO-PLANE (06h-E0h) command after the die (LUN) is ready.

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 29: READ STATUS ENHANCED (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

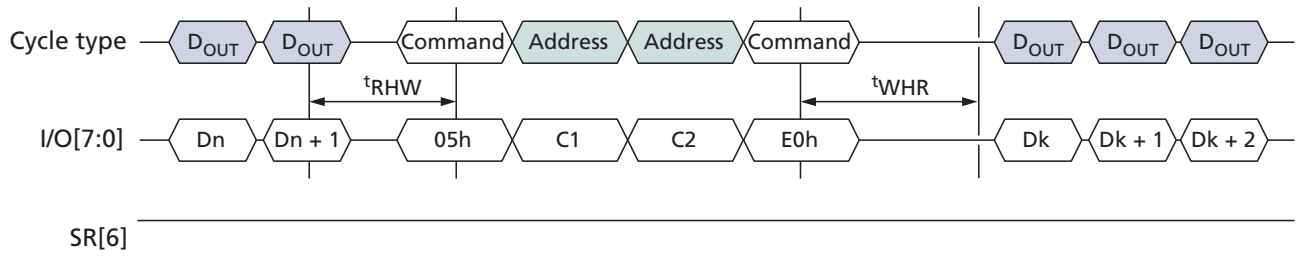
RANDOM DATA READ (05h-E0h)

The RANDOM DATA READ (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the RANDOM DATA READ (05h-E0h). In this situation, using the RANDOM DATA READ (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention because two or more die (LUNs) could output data.

Figure 30: RANDOM DATA READ (05h-E0h) Operation



RANDOM DATA READ TWO-PLANE (06h-E0h)

The RANDOM DATA READ TWO-PLANE (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

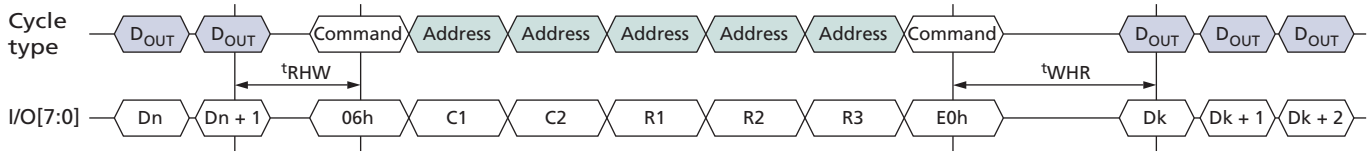
Following a two-plane read page operation, the RANDOM DATA READ TWO-PLANE (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the RANDOM DATA READ TWO-PLANE (06h-E0h). In this situation, using the RANDOM DATA READ TWO-PLANE (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the RANDOM DATA READ (05h-E0h) command can be used instead.

Figure 31: RANDOM DATA READ TWO-PLANE (06h-E0h) Operation



RANDOM DATA INPUT (85h)

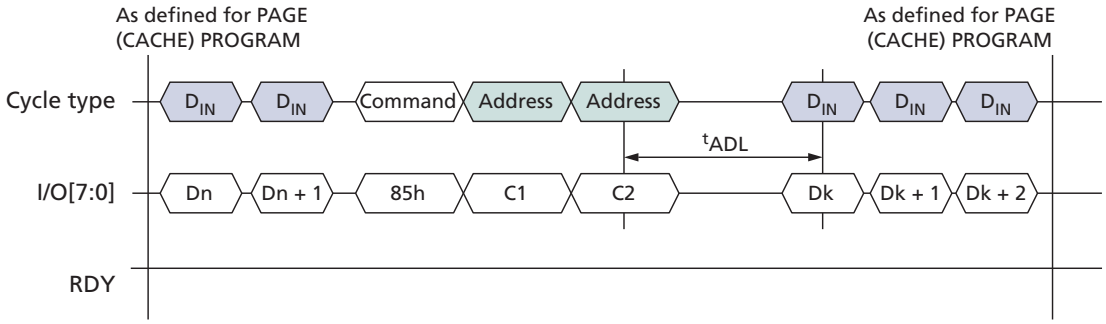
The RANDOM DATA INPUT (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}ADL before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The RANDOM DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h), PROGRAM FOR INTERNAL DATA MOVE (85h-10h), and PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE (85h-11h).

In devices that have more than one die (LUN) per target, the RANDOM DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 32: RANDOM DATA INPUT (85h) Operation



PROGRAM FOR INTERNAL DATA INPUT (85h)

The PROGRAM FOR INTERNAL DATA INPUT (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected device for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}ADL before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE TWO-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), PROGRAM FOR INTERNAL DATA MOVE (85h-10h), and PROGRAM FOR TWO-PLANE INTERNAL DATA MOVE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

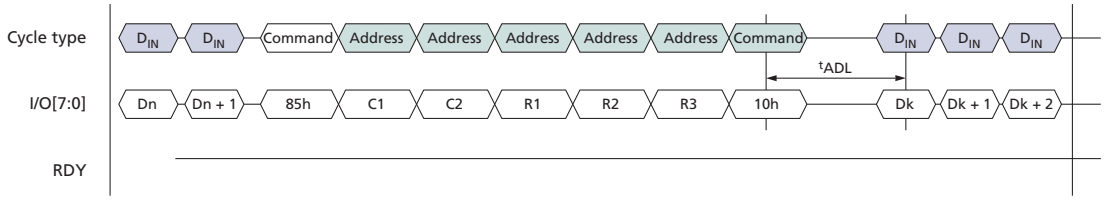
The PROGRAM FOR INTERNAL DATA INPUT (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with the RANDOM DATA READ (05h-E0h) or RANDOM DATA READ TWO-PLANE (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM FOR INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

Figure 33: PROGRAM FOR INTERNAL DATA INPUT (85h) Operation



Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h) – copies the page specified in this command from the NAND Flash array to its corresponding data register

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE series (31h, 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

Two-Plane Read Operations

Two-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by pre-pending one or more READ PAGE TWO-PLANE (00h-00h-30h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the RANDOM DATA READ TWO-PLANE (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Two-Plane Read Cache Operations

Two-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE TWO-PLANE (00h-00h-30h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a two-plane read page cache sequence, begin by issuing a READ PAGE TWO-PLANE operation using the READ PAGE TWO-PLANE (00h-00h-30h) and READ PAGE (00h-30h) commands. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential pages from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE TWO-PLANE (00h-00h-30h) [in some cases, followed by READ PAGE CACHE RANDOM (00h-31h)] – copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next pages begin copying data from the array to the data registers. After ^{t}RCBSY, R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command to determine which cache register will output data. After data is output, the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional TWO-PLANE READ CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data registers are copied into the cache registers. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command to determine which cache register will output data. After data is output, the RANDOM DATA READ TWO-PLANE (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), two-plane read cache series (31h, 00h-00h-30h, 00h-31h), RANDOM DATA READ (06h-E0h, 05h-E0h), and RESET (FFh).

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-3Ah, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, then write *n* address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

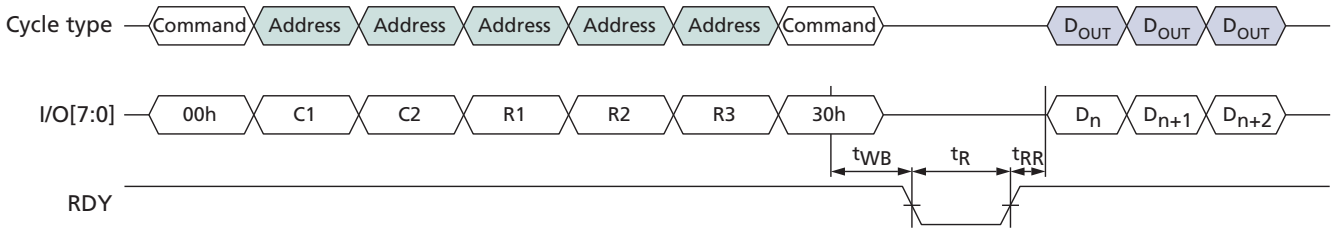
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the RANDOM DATA READ (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a two-plane read operation. It is preceded by one or more READ PAGE TWO-PLANE (00h-00h-30h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The RANDOM DATA READ TWO-PLANE (06h-E0h) command is used to enable data output in the other cache registers.

Figure 34: READ PAGE (00h-30h) Operation



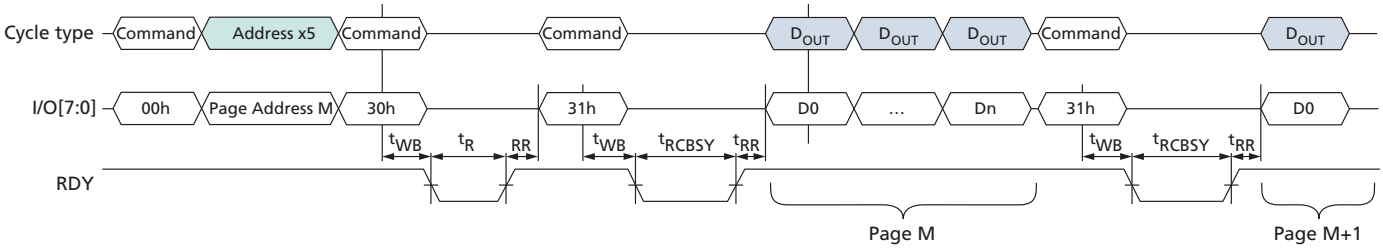
READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

Figure 35: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h-31h)

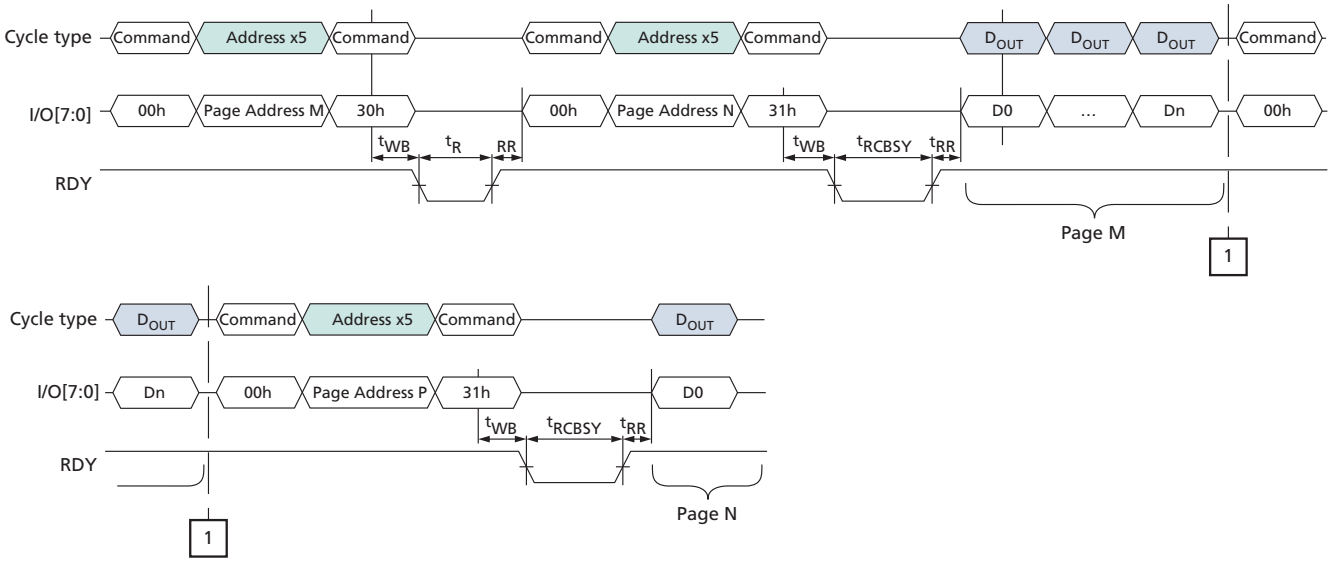
The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write *n* address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 36: READ PAGE CACHE RANDOM (00h-31h) Operation



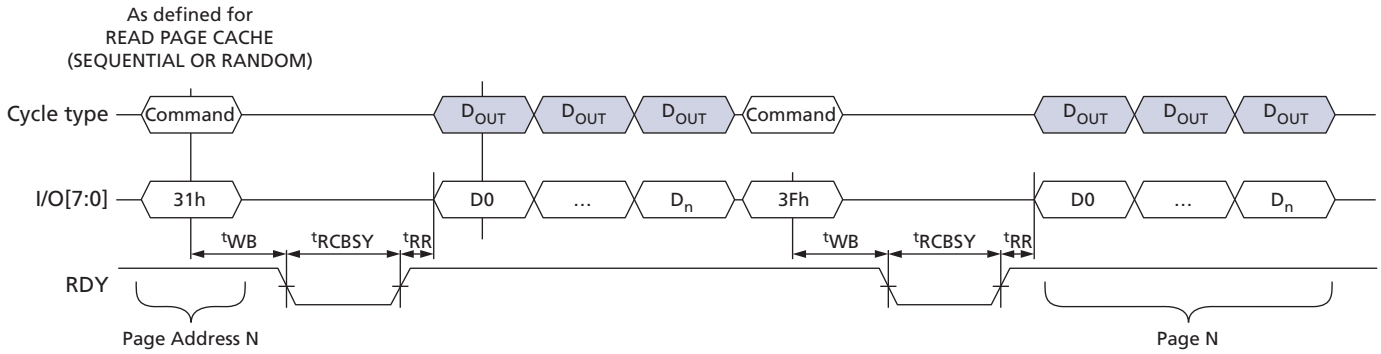
READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 37: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE TWO-PLANE 00h-00h-30h

The READ PAGE TWO-PLANE (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfers two pages of data from the NAND Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the READ PAGE TWO-PLANE mode, write the 00h command to the command register, and then write five address cycles for plane 0 (BA6 = 0). Next, write the 00h command to the command register, and five address cycles for plane 1 (BA6 = 1). Finally, issue the 30h command. The first-plane and second-plane addresses must meet the two-plane addressing requirements, and, in addition, they must have identical column addresses.

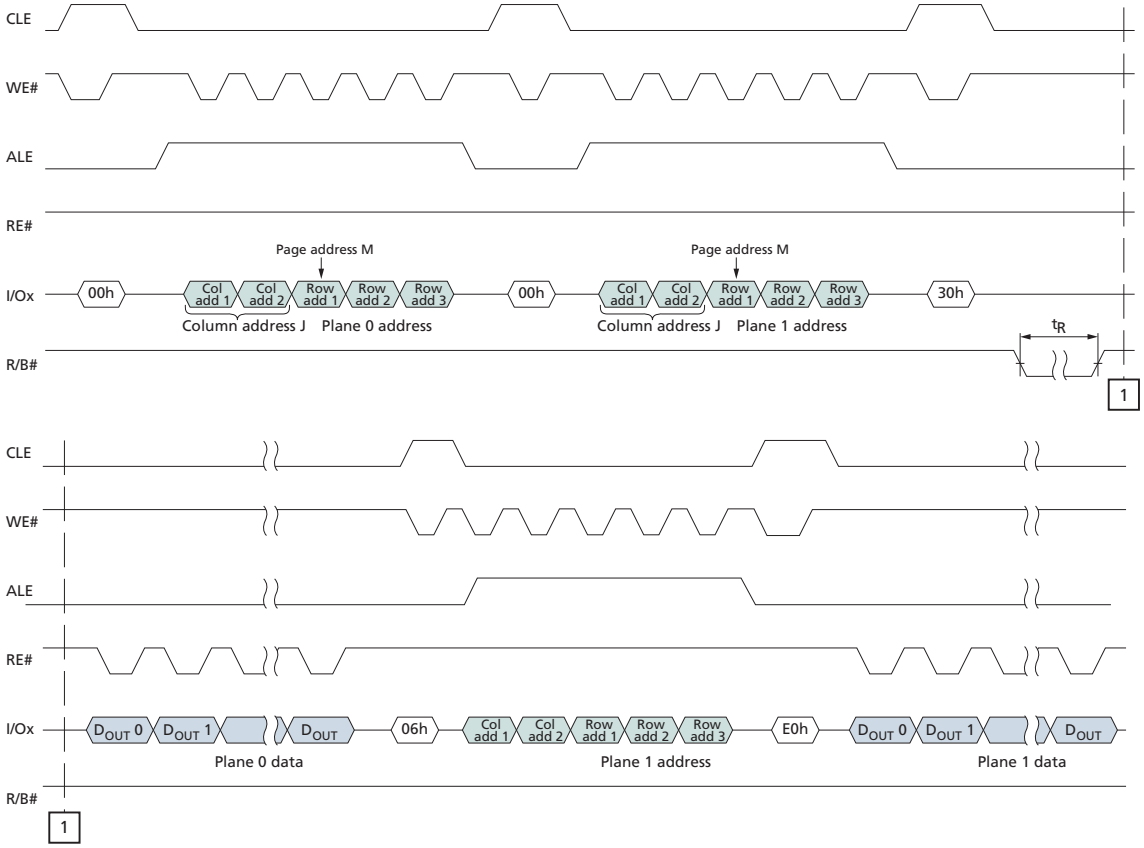
After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# goes HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a RANDOM DATA READ TWO-PLANE (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternatively, the READ STATUS (70h) command can monitor data transfers. When the transfers are complete, status register bit 6 is set to 1. To read data from the first of the two planes, the user must first issue the RANDOM DATA READ TWO-PLANE (06h-E0h) command and pulse RE# repeatedly.

When the data cycle is complete, issue a RANDOM DATA READ TWO-PLANE (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.

Use of the READ STATUS ENHANCED (78h) command is prohibited during and following a PAGE READ TWO-PLANE operation.

Figure 38: READ PAGE TWO-PLANE (00h-00h-30h) Operation



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (0, 1, 2, ….., 63). During a program operation, the contents of the cache and/or data registers are modified by the internal control logic.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE TWO-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), RANDOM DATA INPUT (85h), PROGRAM FOR INTERNAL DATA INPUT (85h), and RESET (FFh).

Two-Plane Program Operations

The PROGRAM PAGE TWO-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command.

Two-Plane Program Cache Operations

The PROGRAM PAGE TWO-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

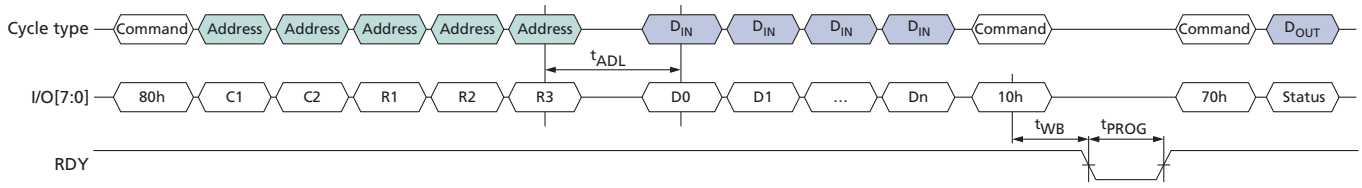
To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a two-plane program operation. It is preceded by one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h).

Figure 39: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a two-plane program cache operation. It is preceded by one or more PROGRAM PAGE TWO-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h).

Figure 40: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

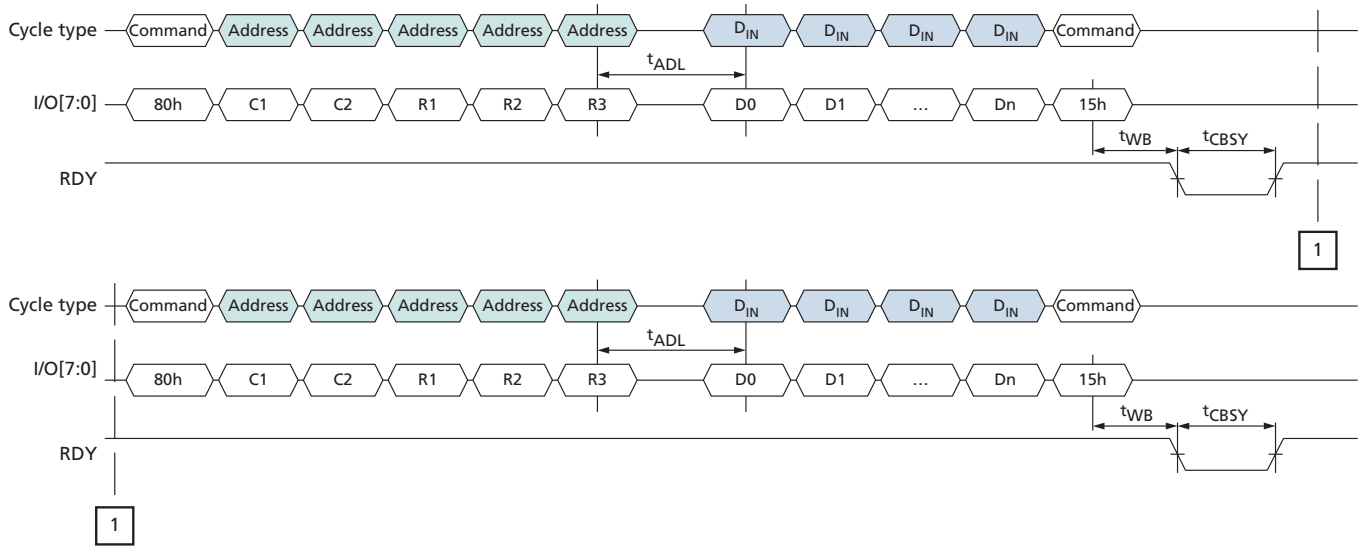
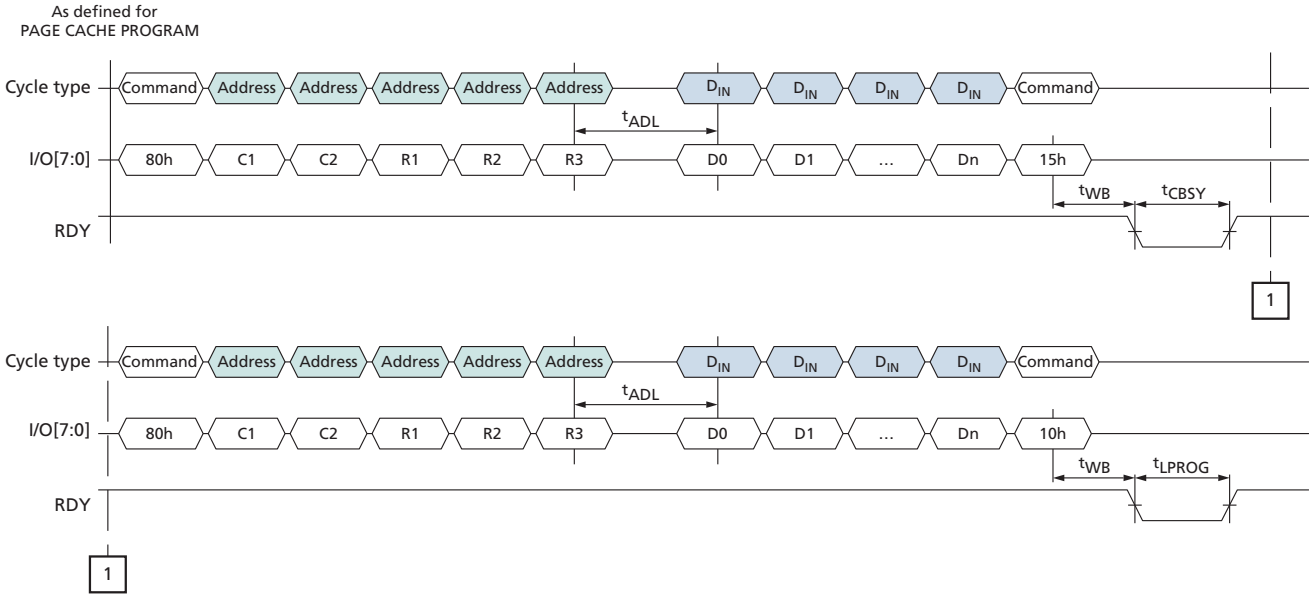


Figure 41: PROGRAM PAGE CACHE (80h–15h) Operation (End)



PROGRAM PAGE TWO-PLANE (80h-11h)

The PROGRAM PAGE TWO-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE TWO-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle, the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

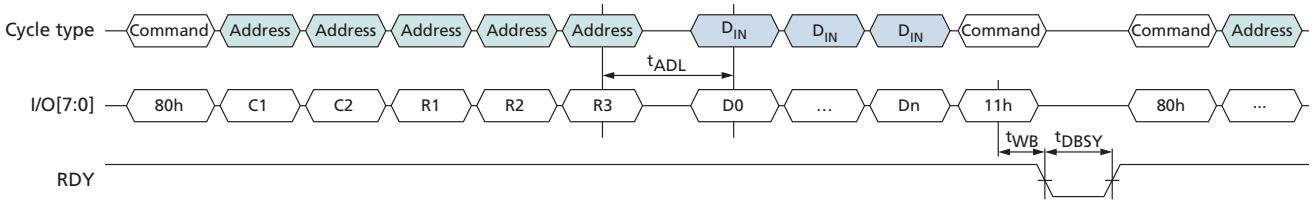
To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE TWO-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a two-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a program cache two-plane operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE TWO-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Two-Plane Operations for two-plane addressing requirements.

Figure 42: PROGRAM PAGE TWO-PLANE (80h–11h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK TWO-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

TWO-PLANE ERASE Operations

The ERASE BLOCK TWO-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK TWO-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Two-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

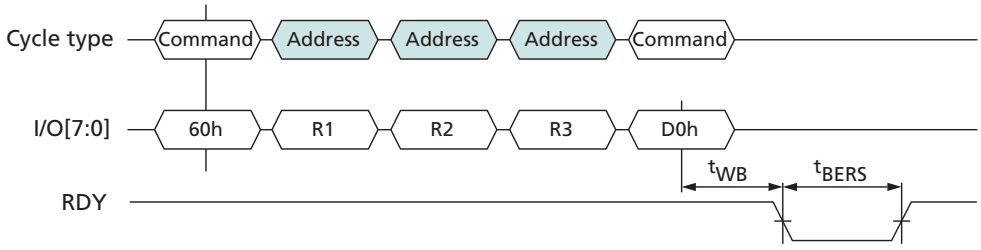
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of an erase two-plane operation. It is preceded by one or more ERASE BLOCK TWO-PLANE (60h-D1h) commands. All blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Two-Plane Operations for two-plane addressing requirements.

Figure 43: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK TWO-PLANE (60h-D1h)

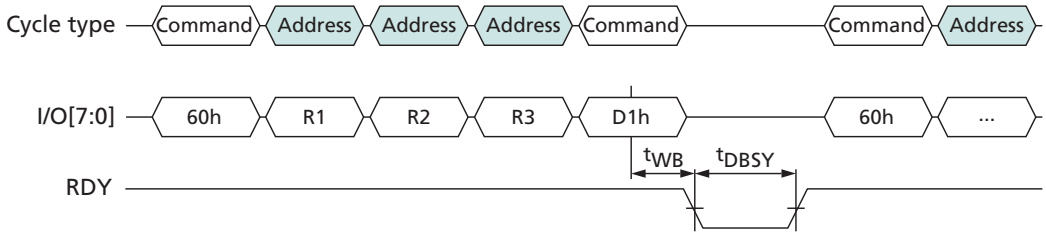
The ERASE BLOCK TWO-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK TWO-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For two-plane addressing requirements for the ERASE BLOCK TWO-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Two-Plane Operations.

Figure 44: ERASE BLOCK TWO-PLANE (60h–D1h) Operation



Internal Data Move Operations

Internal data move operations make it possible to transfer data within a device from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The INTERNAL DATA MOVE operation is a two-step process consisting of a READ FOR INTERNAL DATA MOVE (00h-35h) and a PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. To move data from one page to another on the same plane, first issue the READ FOR INTERNAL DATA MOVE (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple INTERNAL DATA MOVE operations, it is recommended that the host read the data out of the cache register after the READ FOR INTERNAL DATA MOVE (00h-35h) completes and prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. The RANDOM DATA READ (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued, any corrected data can be input. The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used to change the column address.

It is not possible to use the READ FOR INTERNAL DATA MOVE operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or READ FOR INTERNAL DATA MOVE (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the READ FOR INTERNAL DATA MOVE (00h-35h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h) commands, the following commands are supported: status operations (70h, 78h) and column address operations (05h-E0h, 06h-E0h, 85h). The RESET operation (FFh) can be issued after READ FOR INTERNAL DATA MOVE (00h-35h), but the contents of the cache registers on the target are not valid.

In devices that have more than one die (LUN) per target, once the READ FOR INTERNAL DATA MOVE (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued.

Two-Plane Read for Internal Data Move Operations

Two-plane internal data move read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by issuing the READ PAGE TWO-PLANE (00h-00h-30h) command or the READ FOR INTERNAL DATA MOVE (00h-00h-35h) command.

The INTERNAL DATA MOVE PROGRAM TWO-PLANE (85h-11h) command can be used to further system performance of PROGRAM FOR INTERNAL DATA MOVE operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM FOR INTERNAL DATA MOVE (85h-11h) commands in front of the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. See Two-Plane Operations for details.

READ FOR INTERNAL DATA MOVE (00h-35h)

The READ FOR INTERNAL DATA MOVE (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command to prevent the propagation of data errors.

Figure 45: READ FOR INTERNAL DATA MOVE (00h-35h) Operation

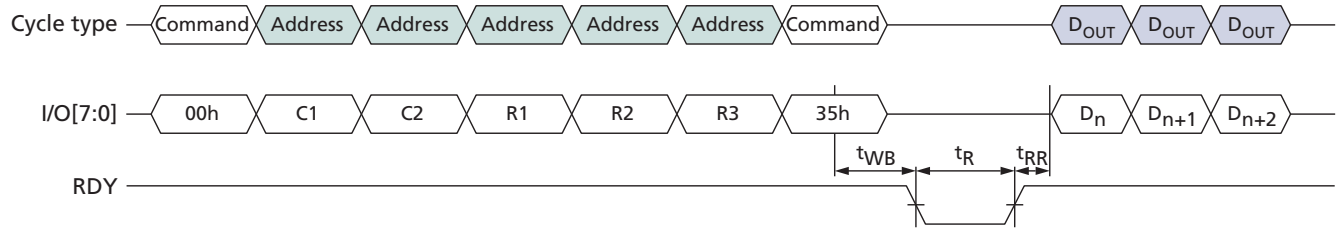
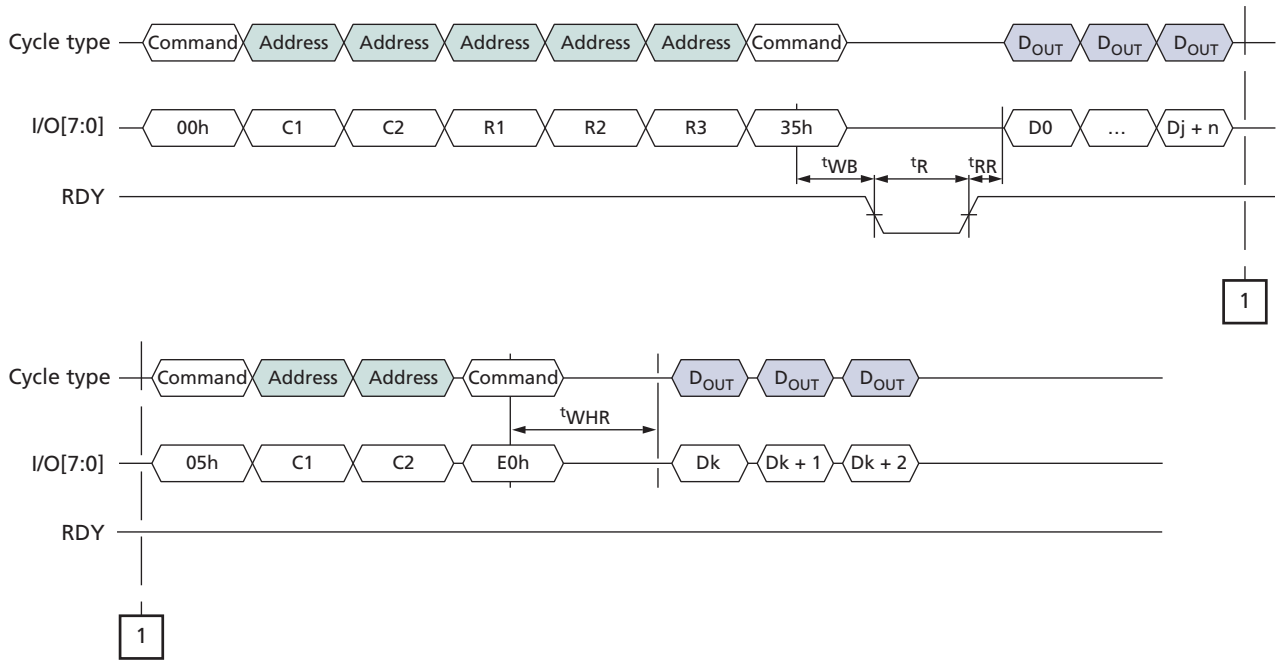


Figure 46: READ FOR INTERNAL DATA MOVE (00h–35h) with RANDOM DATA READ (05h–E0h)



PROGRAM FOR INTERNAL DATA MOVE (85h–10h)

The PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared.

Figure 47: PROGRAM FOR INTERNAL DATA MOVE (85h–10h) Operation

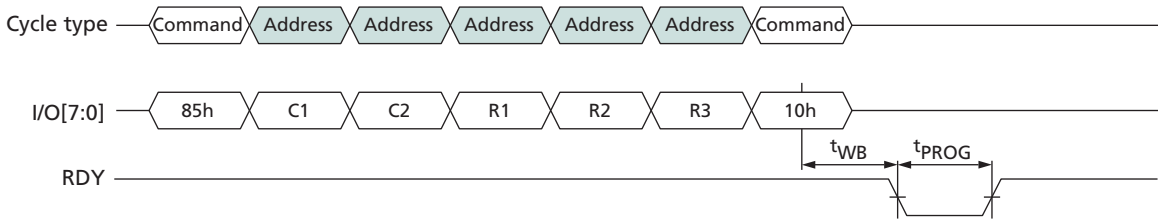
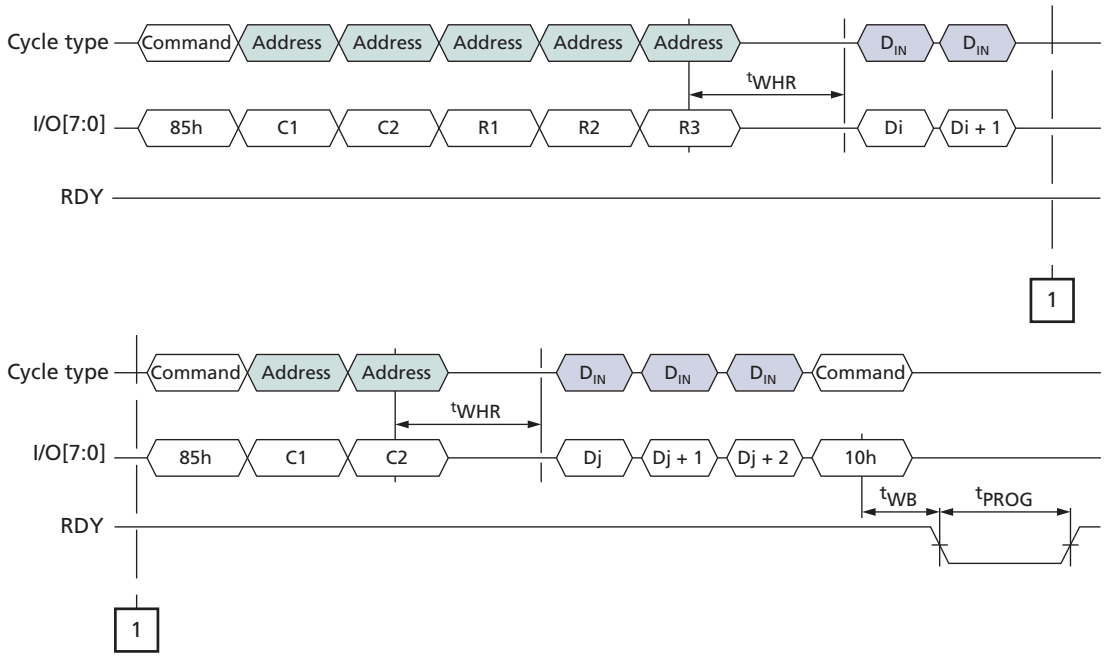


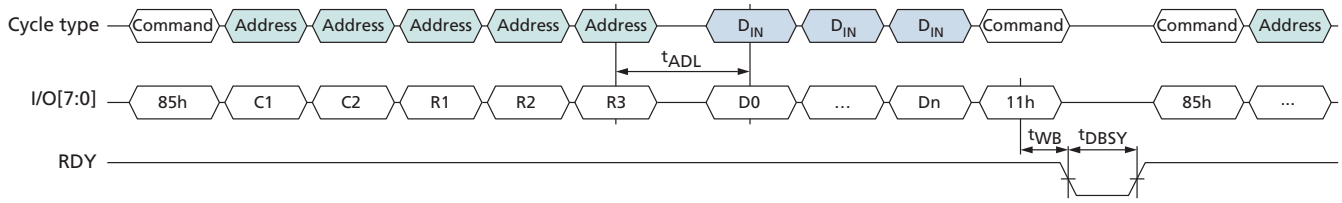
Figure 48: PROGRAM FOR INTERNAL DATA MOVE (85h-10h) with RANDOM DATA INPUT (85h)



PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h)

The PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE TWO-PLANE (85h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See Program Operations for further details.

Figure 49: PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE (85h-11h) Operation



Block Lock Feature

The block lock feature protects either the entire device or ranges of blocks from being programmed and erased. Using the block lock feature is preferable to using WP# to prevent PROGRAM and ERASE operations.

Block lock is enabled and disabled at power-on through the LOCK pin. At power-on, if LOCK is LOW, all BLOCK LOCK commands are disabled. However if LOCK is HIGH at power-on, the BLOCK LOCK commands are enabled and, by default, all the blocks on the device are protected, or locked, from PROGRAM and ERASE operations, even if WP# is HIGH.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and ERASE operations.

Blocks that are locked can be protected further, or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked.

WP# and Block Lock

The following is true when the block lock feature is enabled:

- Holding WP# LOW locks all blocks, provided the blocks are not locked tight.
- If WP# is held LOW to lock blocks, then returned to HIGH, a new UNLOCK command must be issued to unlock blocks.

UNLOCK (23h-24h)

By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. The UNLOCK (23h) command is used to unlock a range of blocks. Unlocked blocks have no protection and can be programmed or erased.

The UNLOCK command uses two registers, a lower boundary block address register and an upper boundary block address register, and the invert area bit to determine what range of blocks are unlocked. When the invert area bit = 0, the range of blocks within the lower and upper boundary address registers are unlocked. When the invert area bit = 1, the range of blocks outside the boundaries of the lower and upper boundary address registers are unlocked. The lower boundary block address must be less than the upper boundary block address. The figures below show examples of how the lower and upper boundary address registers work with the invert area bit.

To unlock a range of blocks, issue the UNLOCK (23h) command followed by the appropriate address cycles that indicate the lower boundary block address. Then issue the 24h command followed by the appropriate address cycles that indicate the upper boundary block address. The least significant page address bit, PA0, should be set to 1 if setting the invert area bit; otherwise, it should be 0. The other page address bits should be 0.

Only one range of blocks can be specified in the lower and upper boundary block address registers. If after unlocking a range of blocks the UNLOCK command is again issued, the new block address range determines which blocks are unlocked. The previous unlocked block address range is not retained.

Figure 50: Flash Array Protected: Invert Area Bit = 0

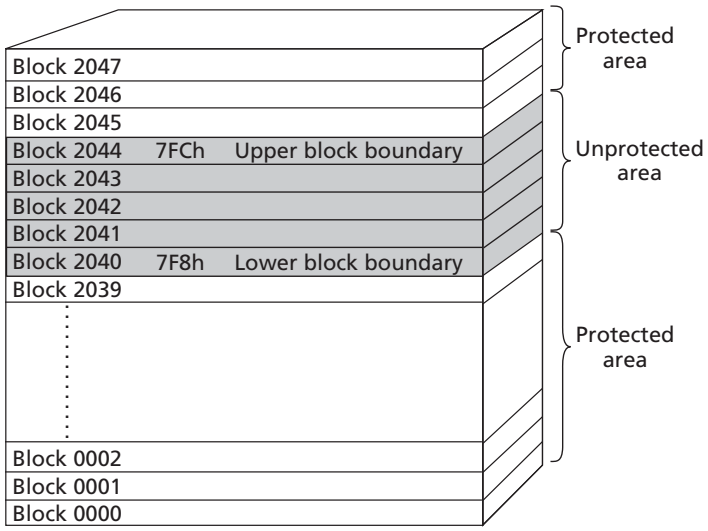


Figure 51: Flash Array Protected: Invert Area Bit = 1

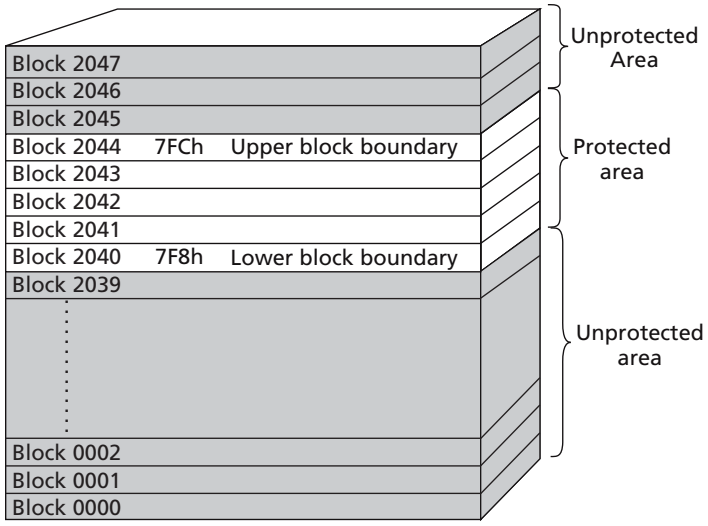
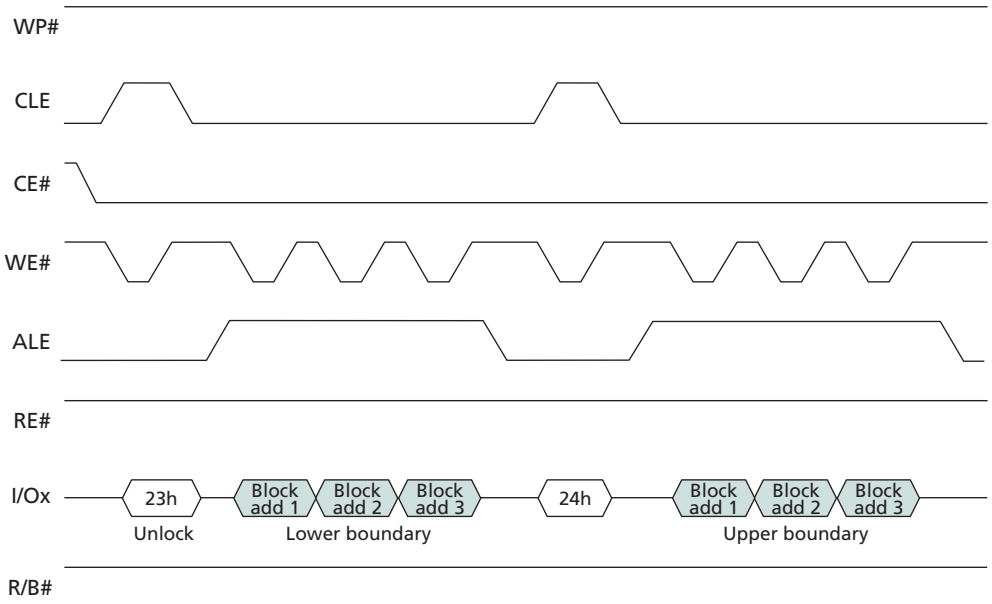


Table 24: Block Lock Address Cycle Assignments

ALE Cycle	I/O[15:8][1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	BA7	BA6	LOW	LOW	LOW	LOW	LOW	Invert area bit[2]
Second	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Third	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes:
1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

Figure 52: UNLOCK Operation



LOCK (2Ah)

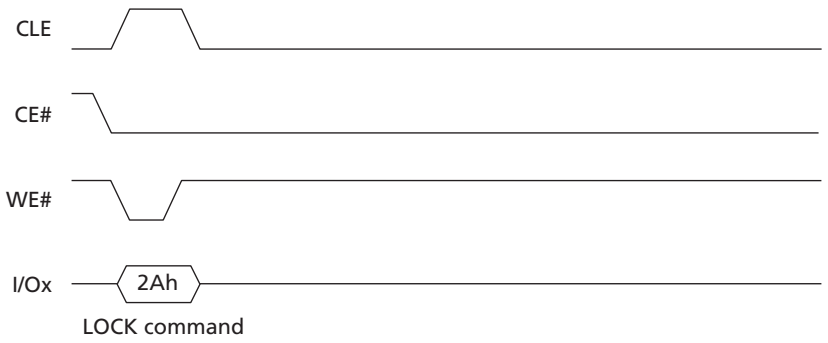
By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. If portions of the device are unlocked using the UNLOCK (23h) command, they can be locked again using the LOCK (2Ah) command. The LOCK command locks all of the blocks in the device. Locked blocks are write-protected from PROGRAM and ERASE operations.

To lock all of the blocks in the device, issue the LOCK (2Ah) command.

When a PROGRAM or ERASE operation is issued to a locked block, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. Any READ STATUS command reports bit 7 as 0, indicating that the block is protected.

The LOCK (2Ah) command is disabled if LOCK is LOW at power-on or if the device is locked tight.

Figure 53: LOCK Operation



LOCK TIGHT (2Ch)

The LOCK TIGHT (2Ch) command prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. When this command is issued, the UNLOCK (23h) and LOCK (2Ah) commands are disabled. This provides an additional level of protection against inadvertent PROGRAM and ERASE operations to locked blocks.

To implement LOCK TIGHT in all of the locked blocks in the device, verify that WP# is HIGH and then issue the LOCK TIGHT (2Ch) command.

When a PROGRAM or ERASE operation is issued to a locked block that has also been locked tight, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. The READ STATUS (70h) command reports bit 7 as 0, indicating that the block is protected. PROGRAM and ERASE operations complete successfully to blocks that were not locked at the time the LOCK TIGHT command was issued.

After the LOCK TIGHT command is issued, the command cannot be disabled via a software command. Lock tight status can be disabled only by power cycling the device or toggling WP#. When the lock tight status is disabled, all of the blocks become locked, the same as if the LOCK (2Ah) command had been issued.

The LOCK TIGHT (2Ch) command is disabled if LOCK is LOW at power-on.

Figure 54: LOCK TIGHT Operation

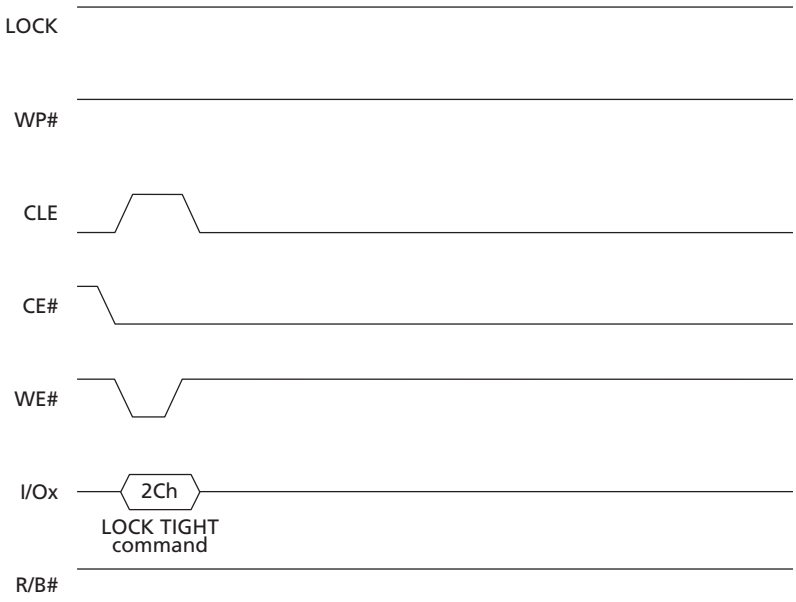
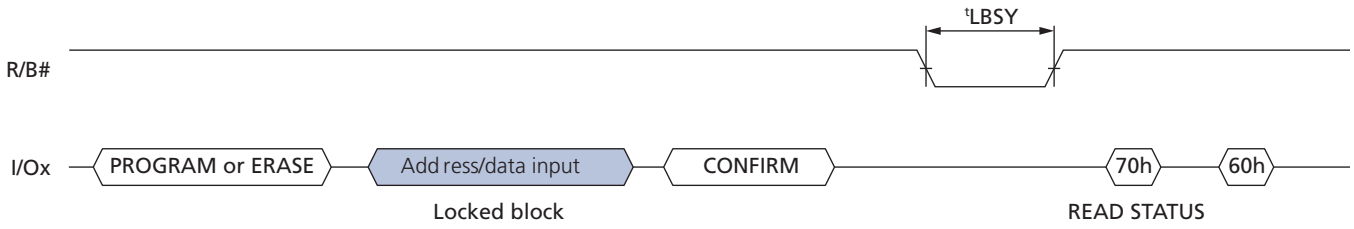


Figure 55: PROGRAM/ERASE Issued to Locked Block



BLOCK LOCK READ STATUS (7Ah)

The BLOCK LOCK READ STATUS (7Ah) command is used to determine the protection status of individual blocks. The address cycles have the same format, as shown below, and the invert area bit should be set LOW. On the falling edge of RE# the I/O pins output the block lock status register, which contains the information on the protection status of the block.

Table 25: Block Lock Status Register Bit Definitions

Block Lock Status Register Definitions	I/O[7:3]	I/O2 (Lock#)	I/O1 (LT#)	I/O0 (LT)
Block is locked tight	X	0	0	1
Block is locked	X	0	1	0
Block is unlocked, and device is locked tight	X	1	0	1
Block is unlocked, and device is not locked tight	X	1	1	0

Figure 56: BLOCK LOCK READ STATUS

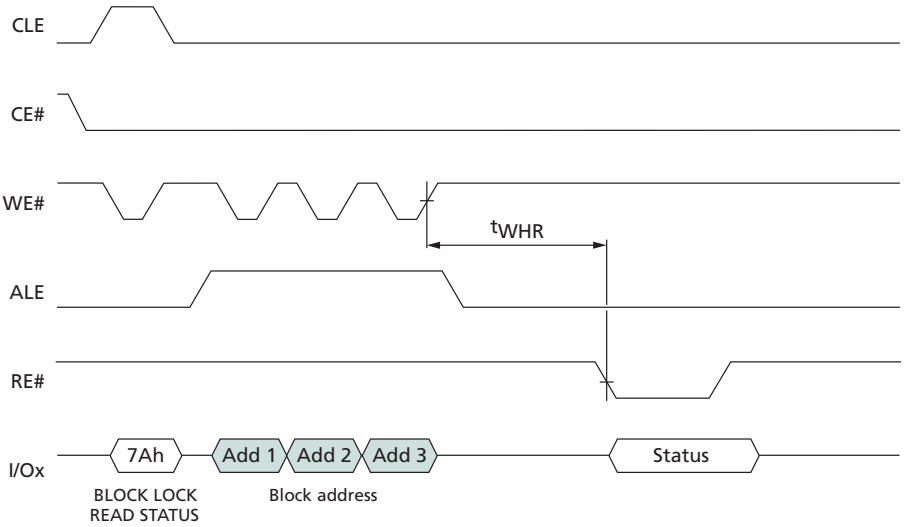
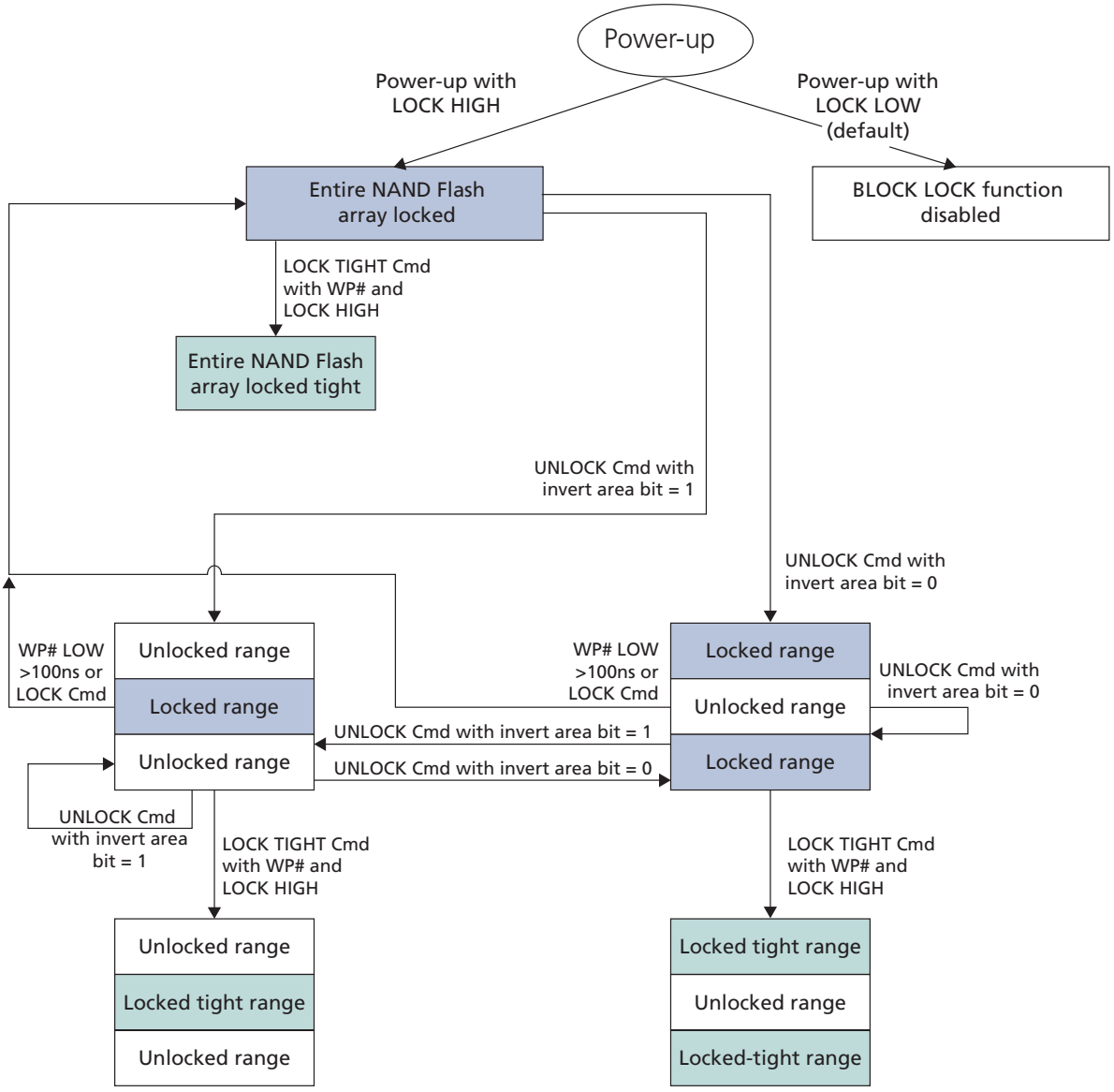


Figure 57: BLOCK LOCK Flowchart



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area any way they choose; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an unwritten state (all bits are 1s). Programming or partial-page programming enables the user to program only 0 bits in the OTP area. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

Micron provides a unique way to program and verify data before permanently protecting it and preventing future changes. The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURE (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2-P4. For parameters to enter OTP mode, see Features Operations.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h-1Fh. To program an OTP page, issue the PROGRAM PAGE (80h-10h) command. The pages must be programmed in the ascending order. Similarly, to read an OTP page, issue the PAGE READ (00h-30h) command.

Protecting the OTP is done by entering OTP protect mode. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to feature address 90h and write 03h to P1, followed by three cycles of 00h to P2-P4.

To determine whether the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command.

To exit OTP operation or protect mode, write 00h to P1 at feature address 90h.

Legacy OTP Commands

For legacy OTP commands, OTP DATA PROGRAM (A0h-10h), OTP DATA PROTECT (A5h-10h), and OTP DATA READ (AFh-30h), refer to the MT29F4GxxAxC data sheet.

OTP DATA PROGRAM (80h-10h)

The OTP DATA PROGRAM (80h-10h) command is used to write data to the pages within the OTP area. An OTP page allows only four partial-page programs. There is no ERASE operation for OTP pages.

PROGRAM PAGE enables programming into an offset of an OTP page using two bytes of the column address (CA[12:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The PROGRAM PAGE command will not execute if the OTP area has been protected.

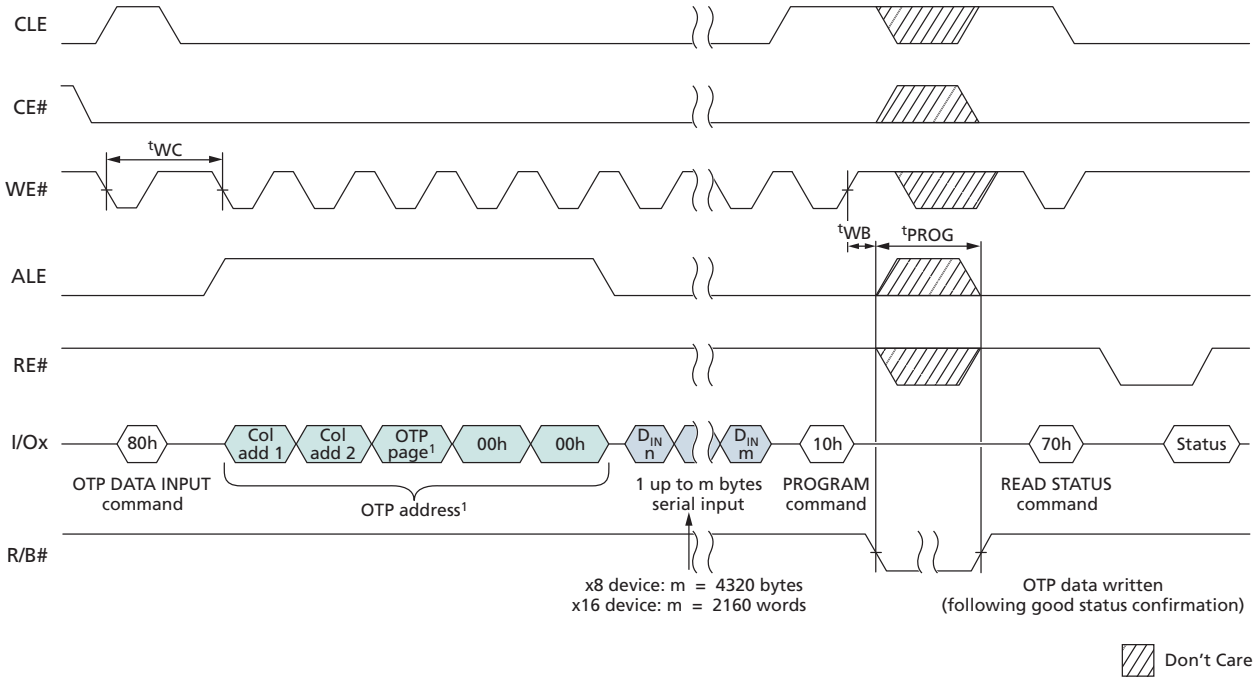
To use the PROGRAM PAGE command, issue the 80h command. Issue *n* address cycles. The first two address cycles are the column address. For the remaining cycles, select a page in the range of 02h-00h through 1Fh-00h. Next, write *n* bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification.

R/B# goes LOW for the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#. When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations). Each OTP page can be programmed to 8 partial-page programming.

RANDOM DATA INPUT (85h)

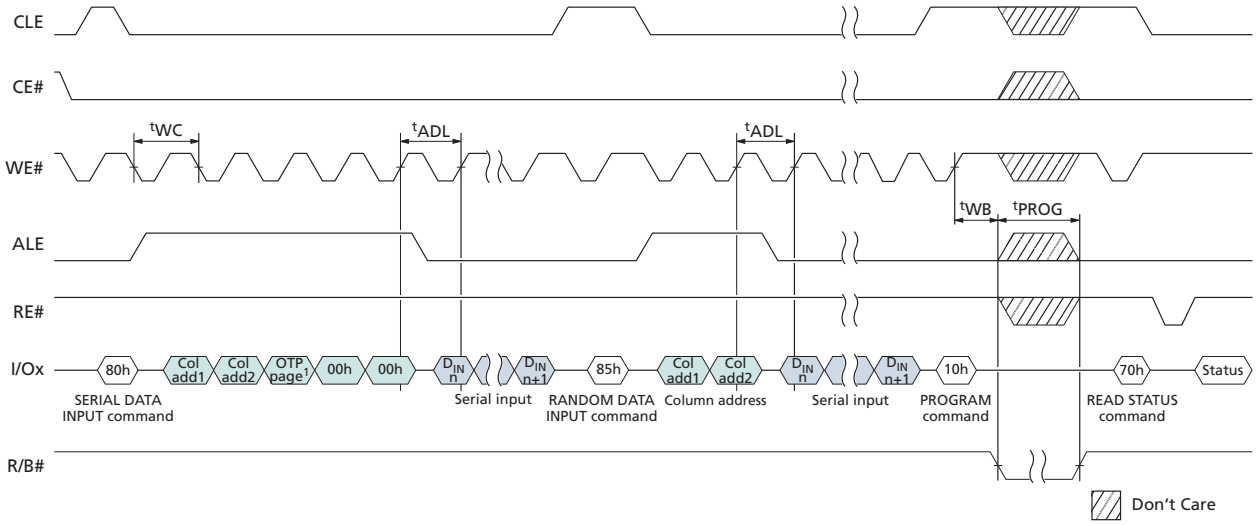
After the initial OTP data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to the OTP PAGE WRITE (10h) command being issued.

Figure 58: OTP DATA PROGRAM (After Entering OTP Operation Mode)



Note: 1. The OTP page must be within the 02h–1Fh range.

Figure 59: OTP DATA PROGRAM Operation with RANDOM DATA INPUT (After Entering OTP Operation Mode)



OTP DATA PROTECT (80h-10)

The OTP area is protected on a block basis. To protect a block, set the device to OTP protect mode, then issue the PROGRAM PAGE (80h-10h) command and write OTP address 00h, 00h, 00h, 00h. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to 90h (feature address) and write 03h to P1, followed by three cycles of 00h to P2-P4.

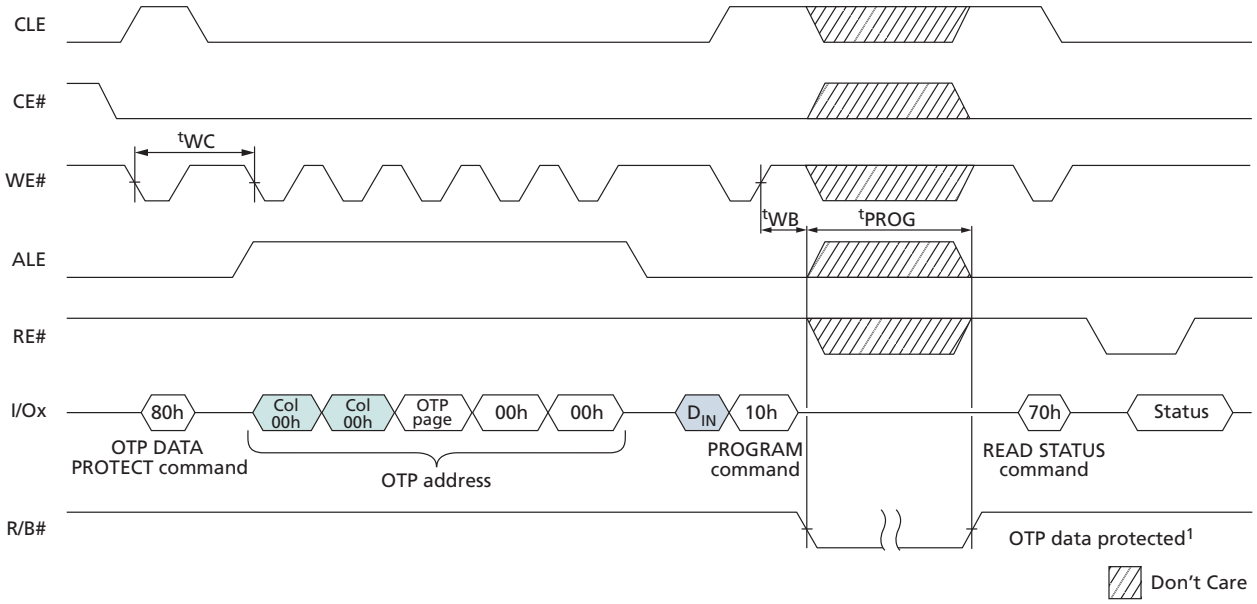
After the data is protected, it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the PROGRAM PAGE command to protect the OTP area, issue the 80h command, followed by *n* address cycles, write 00h data, data cycle of 00h, followed by the 10h command. (An example of the address sequence is shown in the following figure.) If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}OBSY.

The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#.

When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations).

Figure 60: OTP DATA PROTECT Operation (After Entering OTP Protect Mode)



Note: 1. OTP data is protected following a good status confirmation.

OTP DATA READ (00h-30h)

To read data from the OTP area, set the device to OTP operation mode, then issue the PAGE READ (00h-30h) command. Data can be read from OTP pages within the OTP area whether the area is protected or not.

To use the PAGE READ command for reading data from the OTP area, issue the 00h command, and then issue five address cycles: for the first two cycles, the column address; and for the remaining address cycles, select a page in the range of 02h-00h-00h through 1Fh-00h-00h. Lastly, issue the 30h command. The PAGE READ CACHE MODE command is not supported on OTP pages.

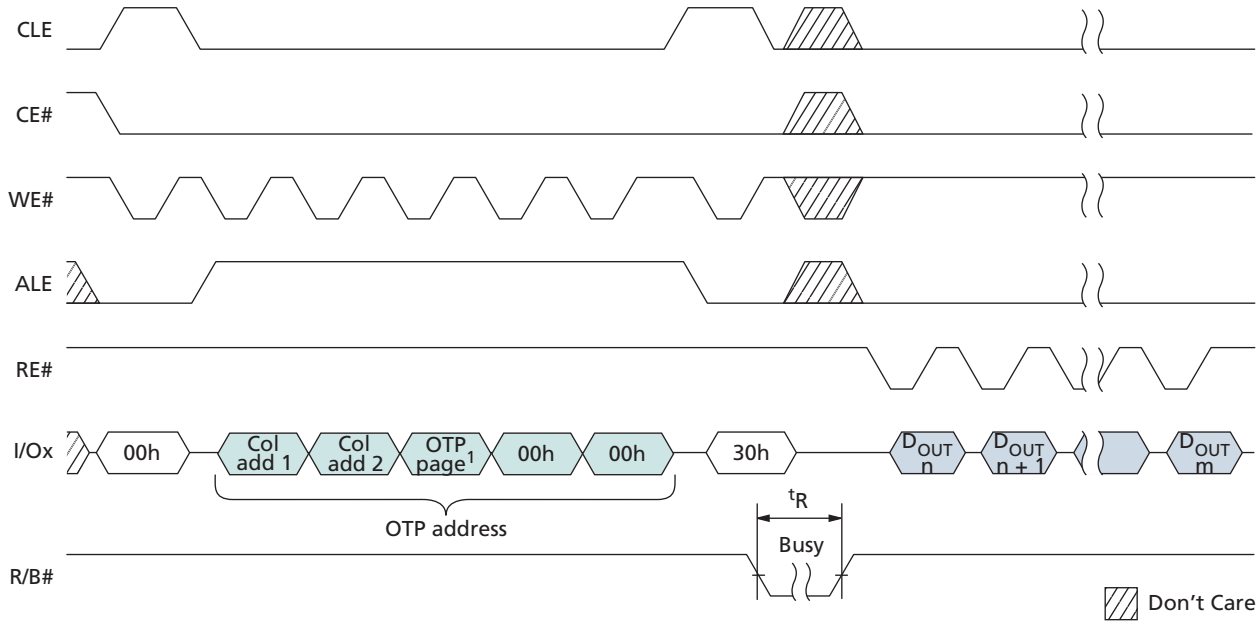
R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B# (see Status Operations).

Normal READ operation timings apply to OTP read accesses. Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

The PAGE READ command is compatible with the RANDOM DATA OUTPUT (05h-E0h) command.

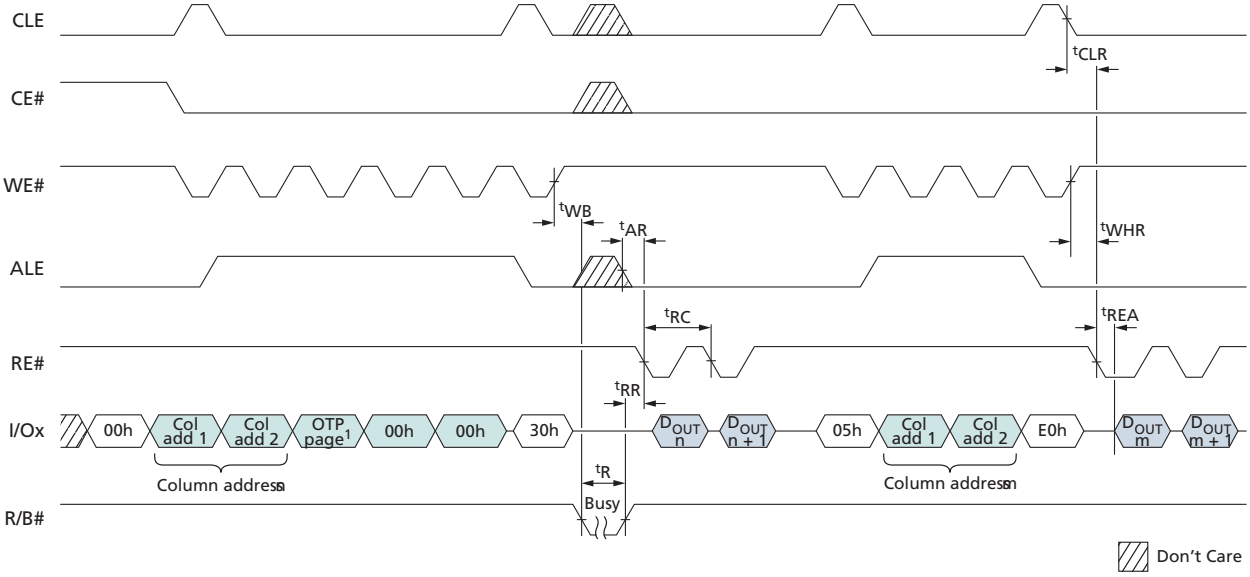
Only data on the current page can be read. Pulsing RE# outputs data sequentially.

Figure 61: OTP DATA READ



Note: 1. The OTP page must be within the 02h–1Fh range.

Figure 62: OTP DATA READ with RANDOM DATA READ Operation



Note: 1. The OTP page must be within the range 02h–1Fh.

Two-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Two-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Two-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing two-plane program or erase operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command to determine which plane operation failed.

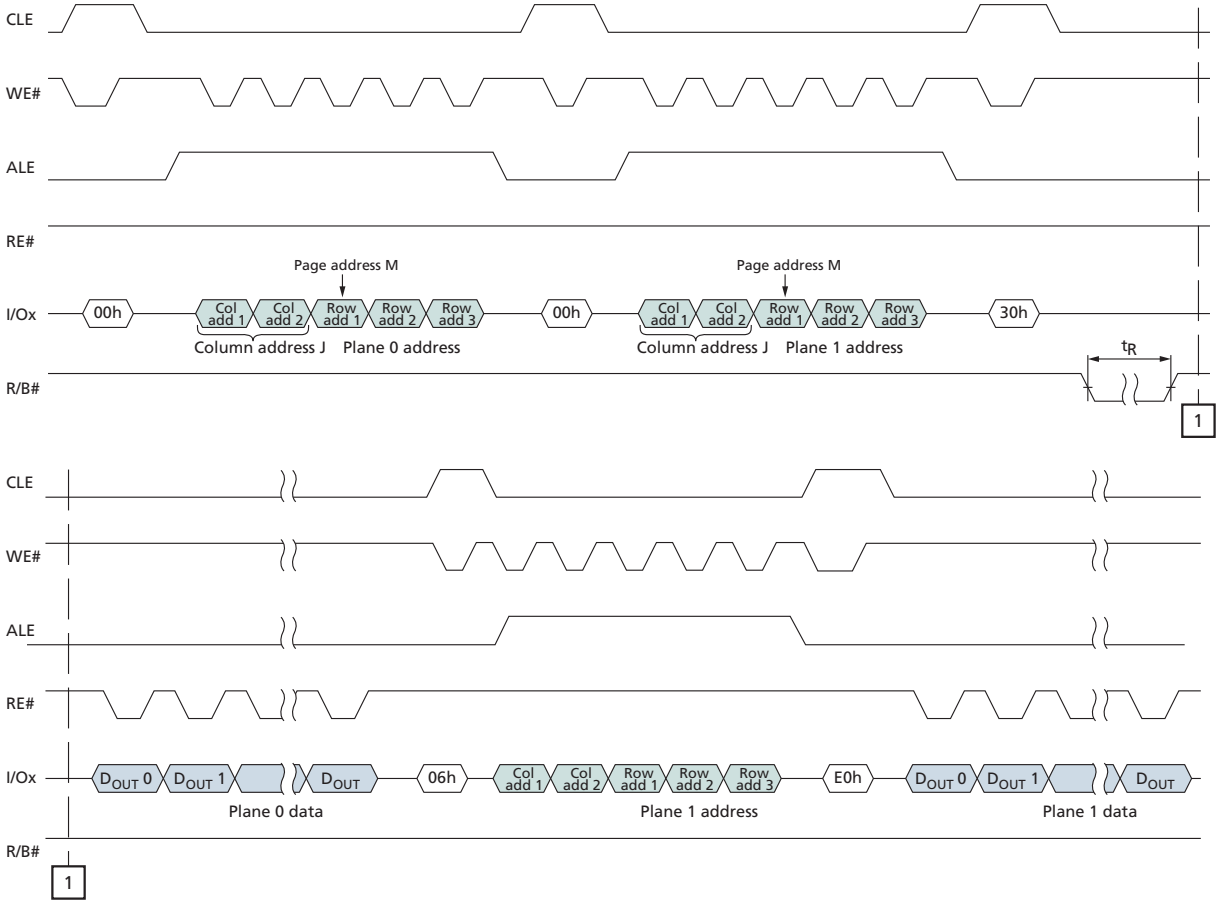
Two-Plane Addressing

Two-plane commands require multiple, five-cycle addresses, one address per operational plane. For a given two-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[6], must be different for each issued address.
- The page address bits, PA[5:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following two-plane program page and erase block operations on a single die (LUN).

Figure 63: TWO-PLANE PAGE READ



Notes: 1. Column and page addresses must be the same.
2. The least significant block address bit, BA6, must be different for the first- and second-plane addresses.

Figure 64: TWO-PLANE PAGE READ with RANDOM DATA READ

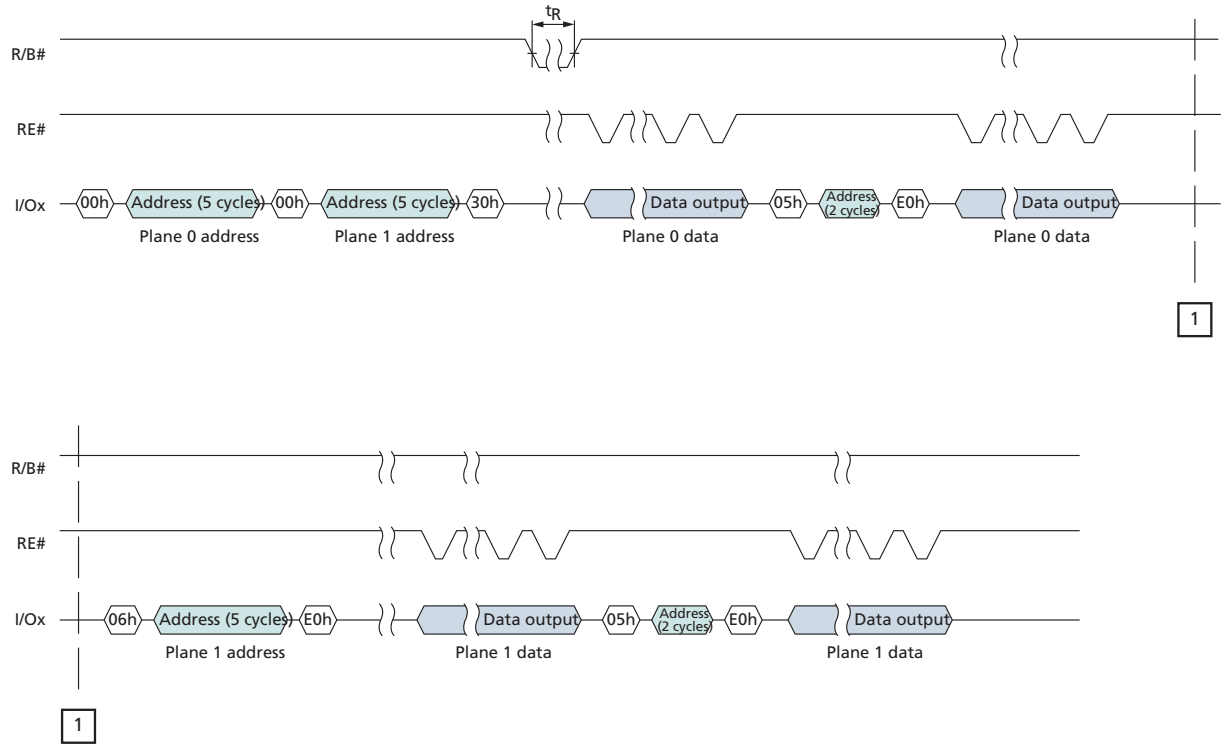


Figure 65: TWO-PLANE PROGRAM PAGE

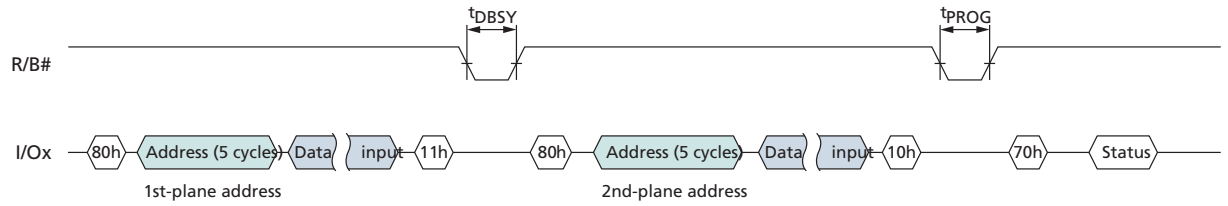


Figure 66: TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT

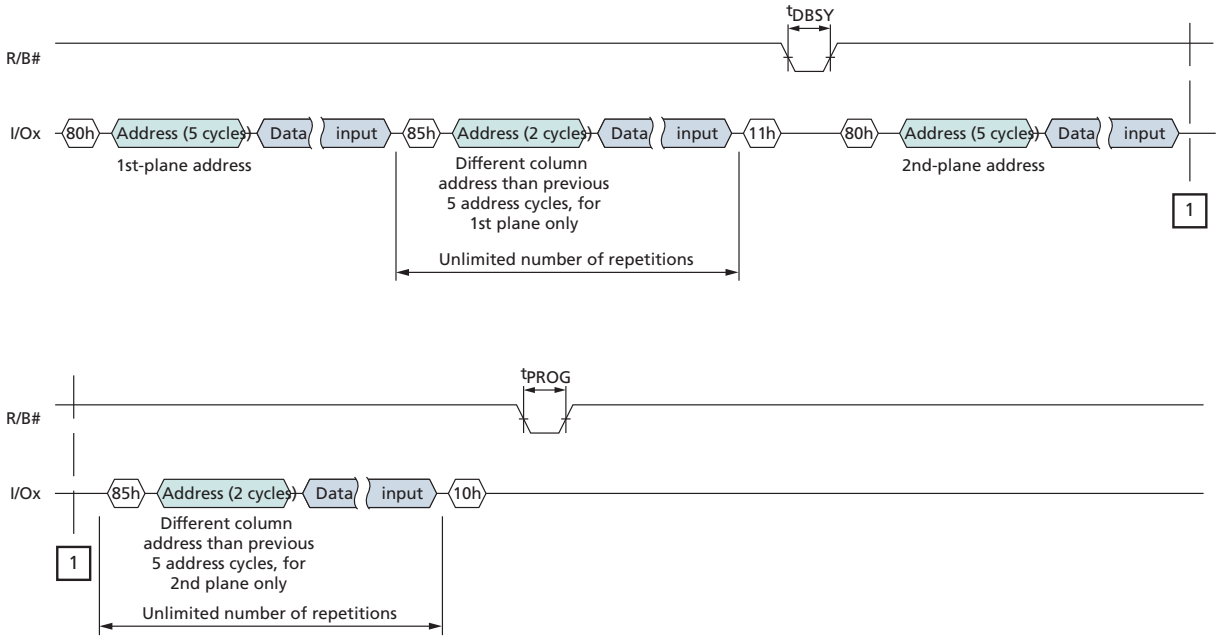


Figure 67: TWO-PLANE PROGRAM PAGE CACHE MODE

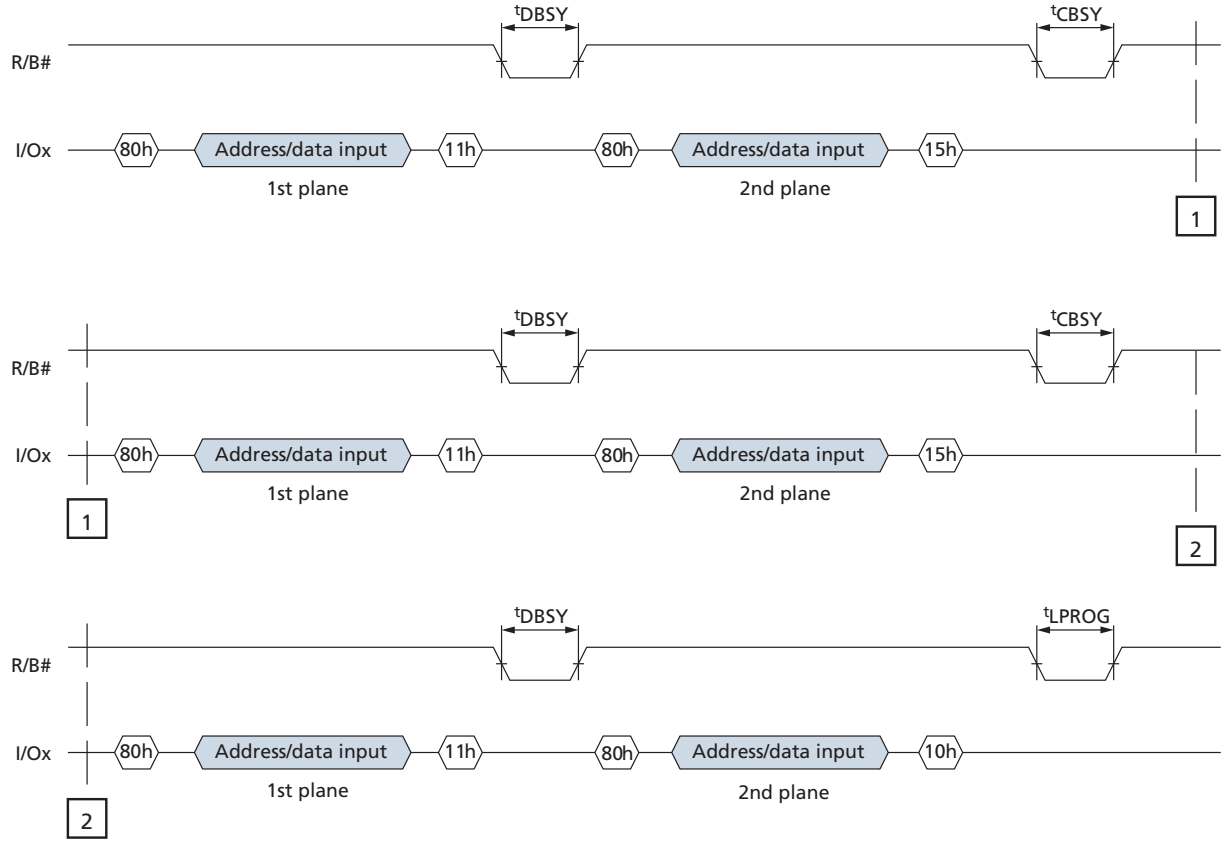


Figure 68: TWO-PLANE INTERNAL DATA MOVE

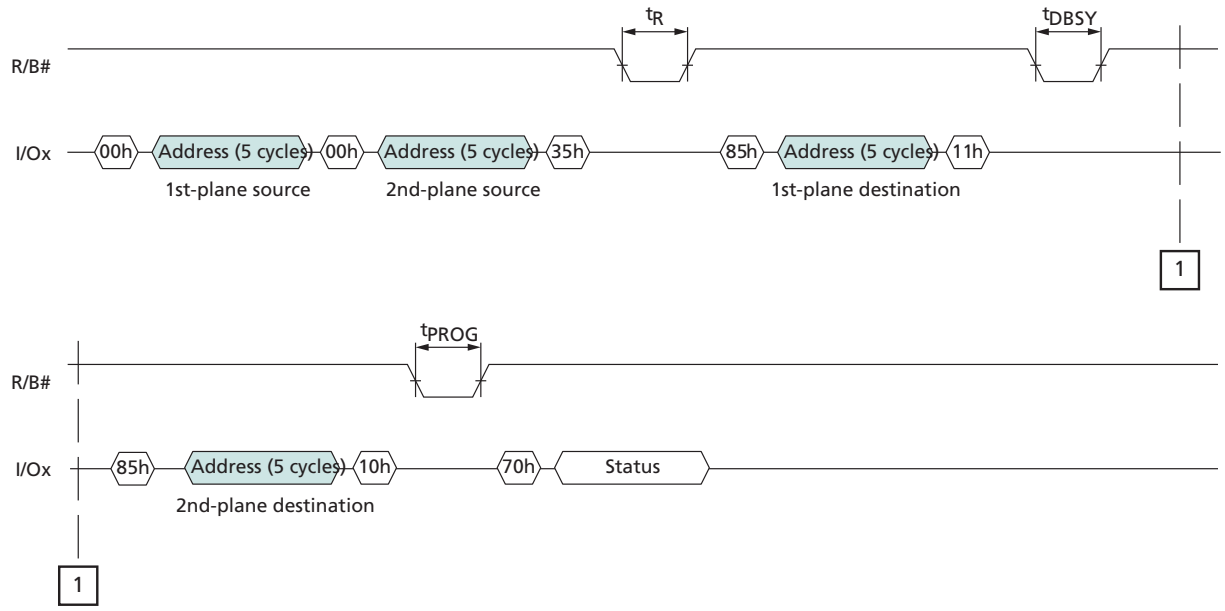


Figure 69: TWO-PLANE INTERNAL DATA MOVE with TWO-PLANE RANDOM DATA READ

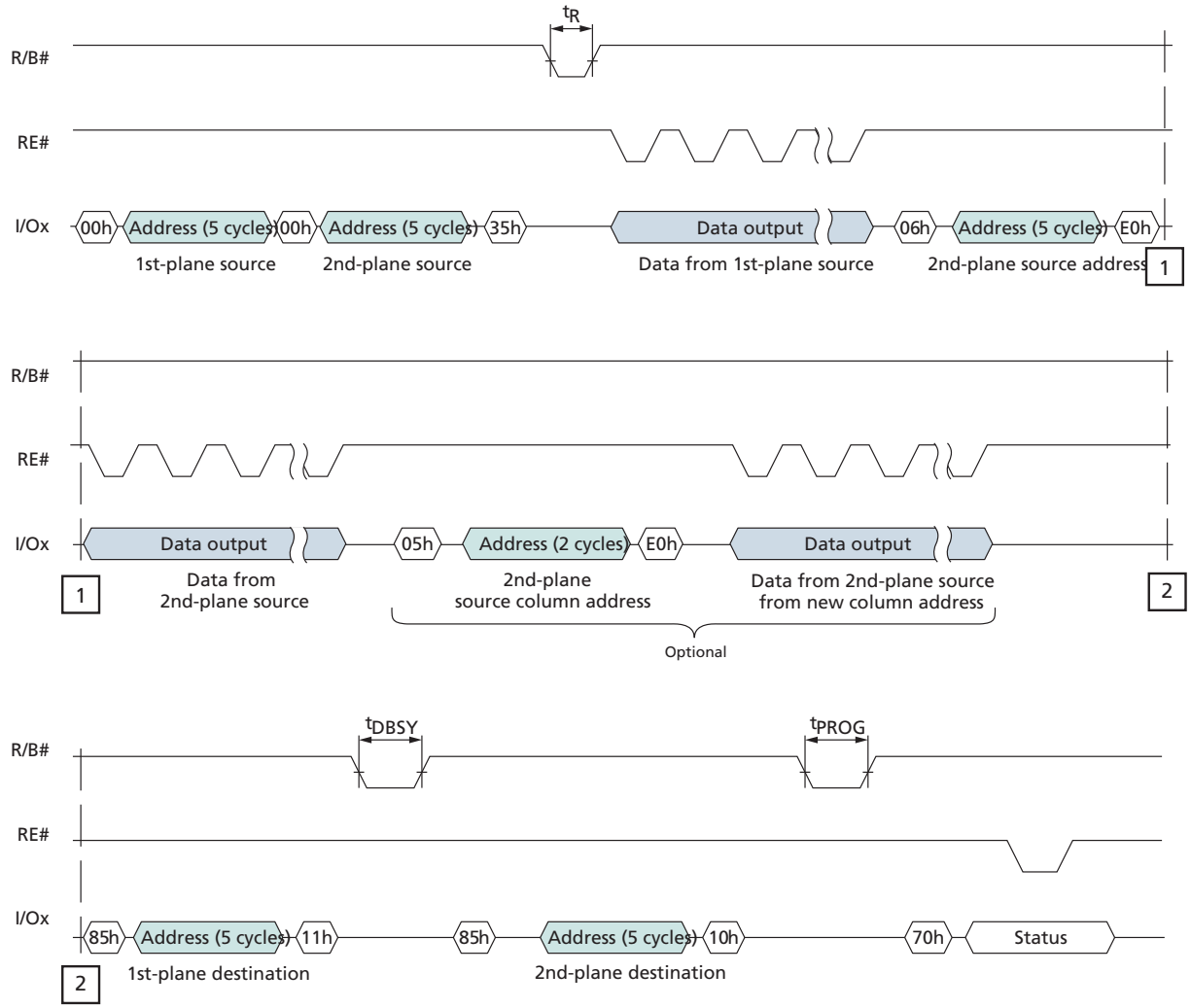


Figure 70: TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT

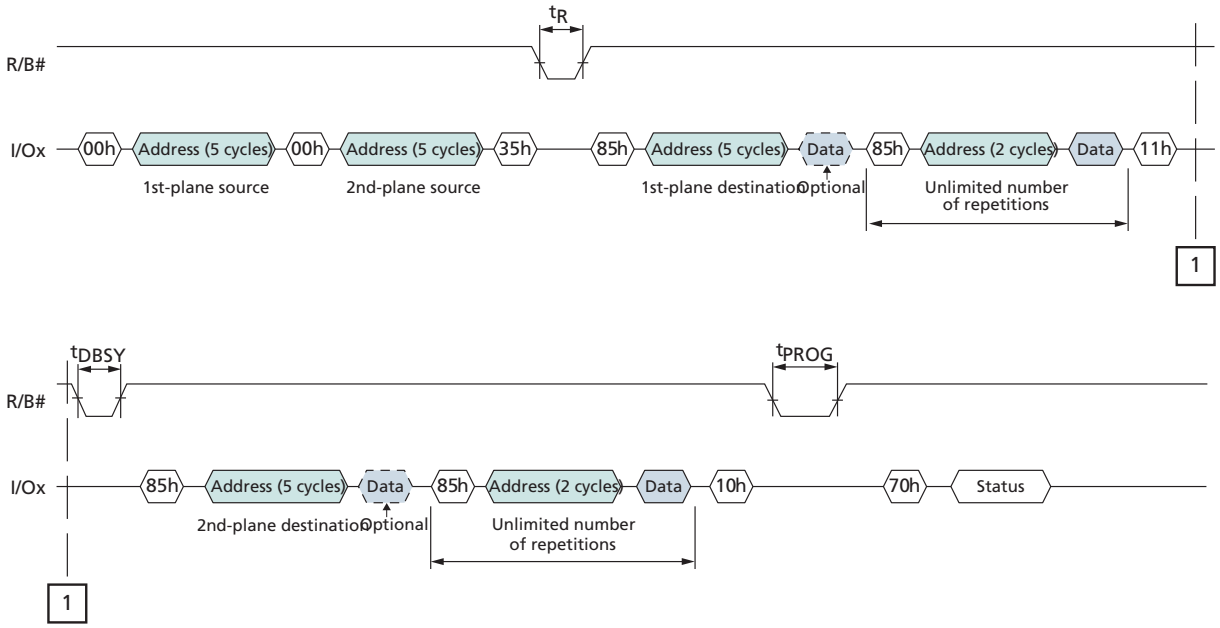


Figure 71: TWO-PLANE BLOCK ERASE

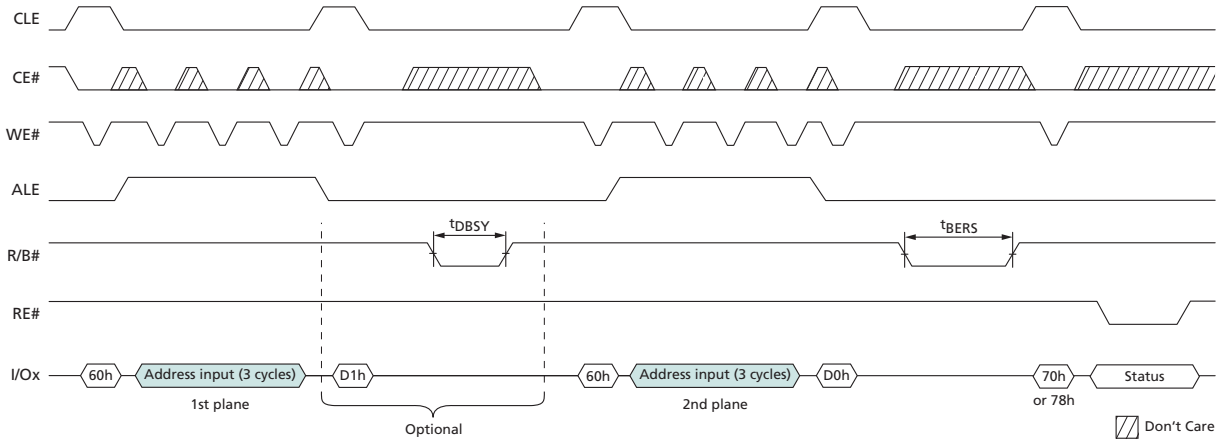
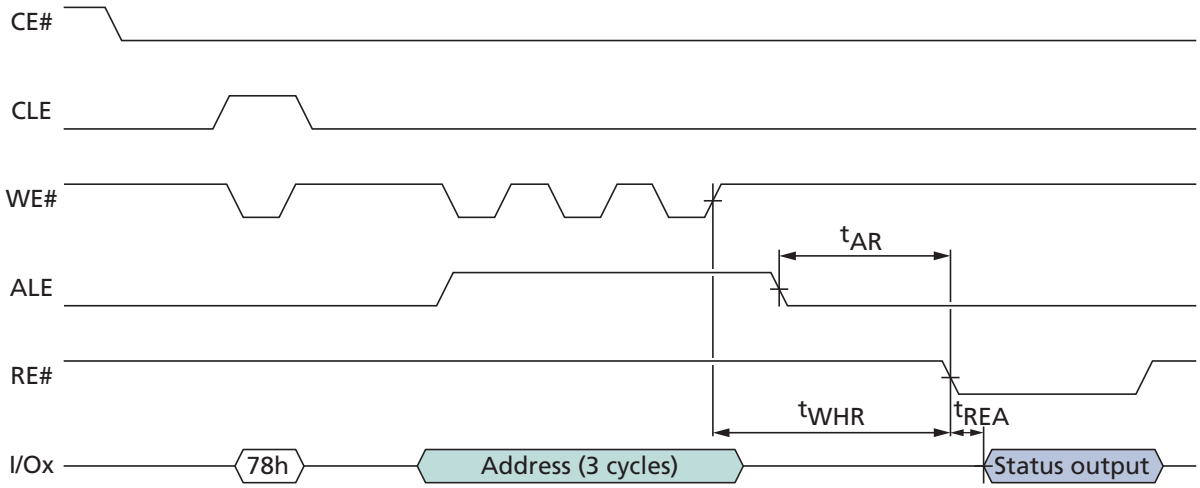


Figure 72: TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that is issued to an idle die (LUN) (RDY = 1) while another die (LUN) is busy (RDY = 0).

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

During and following interleaved die (multi-LUN) operations, the READ STATUS (70h) command is prohibited. Instead, use the READ STATUS ENHANCED (78h) command to monitor status. This command selects which die (LUN) will report status. When two-plane commands are used with interleaved die (multi-LUN) operations, the two-plane commands must also meet the requirements in Two-Plane Operations.

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM series (80h-10h, 80h-15h) operation and a READ operation, the PROGRAM series operation must be issued before the READ series operation. The data from the READ series operation must be output to the host before the next PROGRAM series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad block mark. However, the first spare area location in each bad block is guaranteed to contain the bad block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad block management and wear-leveling algorithms

  The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 26: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2008
Total available blocks per LUN	2048
First spare area location	x8: byte 4096 x16: word 2048
Bad-block mark	x8: 00h x16: 0000h
Minimum required ECC	8-bit ECC per 540 bytes of data

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 27: Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}

Parameter/Condition		Symbol	Min	Max	Unit
Voltage input	1.8V	V_{IN}	–0.6	+2.4	V
	3.3V		–0.6	+4.6	V
Vcc supply voltage	1.8V	V_{CC}	–0.6	+2.4	V
	3.3V		–0.6	+4.6	V
Storage temperature		T_{STG}	–65	+150	°C
Short circuit output current, I/Os		–	–	5	mA

Table 28: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Extended		–40	–	+85	°C
V_{CC} supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table 29: Valid Blocks

Note 1 applies to all

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	MT29F4G	2008	2048	Blocks	2

Notes:
1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid with ECC when shipped from the factory.

Table 30: Capacitance

Capacitance (C_{IN} = C_{IO} = 20pF) for MT29F16G

Description	Symbol	Max	Unit	Notes
Input capacitance	C_{IN}	10	pF	1, 2
Input/output capacitance (I/O)	C_{IO}	10	pF	1, 2

Notes:
1. These parameters are verified in device characterization and are not 100% tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; Vin = 0V.

Table 31: Test Conditions

Parameter	Value	Notes
Input pulse levels	0.0V to V_{CC}	
Input rise and fall times	5ns	
Input and output timing levels	V_{CC}/2	
Output load	1 TTL GATE and CL = 30pF (1.8V)	1
	1 TTL GATE and CL = 50pF (3.3V)	
Output load	1 TTL GATE and CL = 30pF (1.8V)	1
	1 TTL GATE and CL = 50pF (3.3V)	

Note:
1. Verified in device characterization, not 100% tested.

Electrical Specifications – DC Characteristics and Operating Conditions

Table 32: DC Characteristics and Operating Conditions (3.3V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	15	30	mA	4
PROGRAM current	–	I_{CC2}	–	15	30	mA	4
ERASE current	–	I_{CC3}	–	15	30	mA	4
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	I_{SB2}	–	20	100	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	1
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x V_{CC}	–	–	V	2
Output low voltage	I_{OL} = –2.1mA	V_{OL}	–	–	0.4	V	2
Output low current	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	3

Notes:
1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC} (MIN).
2. I_{OL} (R/B#) may need to be relaxed if R/B pull-down strength is not set to full.
3. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.
4. Typical and maximum values are for single-plane operation only. If the device supports dual-plane operation, values are 25mA (TYP) and 35mA (Max).

Table 33: DC Characteristics and Operating Conditions (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	13	20	mA	1, 2
PROGRAM current	–	I_{CC2}	–	10	20	mA	1, 2
ERASE current	–	I_{CC3}	–	10	20	mA	1, 2
Standby current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	I_{SB2}	–	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#, LOCK	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} - 0.1	–	–	V	4
Output low voltage	I_{OL} = –100µA	V_{OL}	–	–	0.1	V	4
Output low current	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	5

Notes:
1. Typical and maximum values are for single-plane operation only. Dual-plane operation values are 20mA (TYP) and 40mA (MAX).
2. Values are for single die operations. Values could be higher for interleaved die operations.
3. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches V_{CC} (MIN).
4. Test conditions for V_{OH} and V_{OL}.
5. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full.

Electrical Specifications – AC Characteristics and Operating Conditions

Table 34: AC Characteristics: Command, Data, and Address Input (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	70	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	15	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	7	–	ns	
WRITE cycle time	^{t}WC	20	–	ns	1
WE# pulse width HIGH	^{t}WH	7	–	ns	1
WE# pulse width	^{t}WP	10	–	ns	1
WP# transition to WE# LOW	^{t}WW	100	–	ns	

Note: 1. Timing for ^{t}ADL begins in the address cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 35: AC Characteristics: Command, Data, and Address Input (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	100	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	25	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	10	–	ns	
WRITE cycle time	^{t}WC	30	–	ns	1
WE# pulse width HIGH	^{t}WH	10	–	ns	1
WE# pulse width	^{t}WP	15	–	ns	1
WP# transition to WE# LOW	^{t}WW	100	–	ns	

Note: 1. Timing for ^{t}ADL begins in the address cycle on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 36: AC Characteristics: Normal Operation (1.8V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	30	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	50	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	30	–	ns	
RE# access time	^{t}REA	–	25	ns	
RE# HIGH hold time	^{t}REH	10	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	65	ns	2
RE# pulse width	^{t}RP	15	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	80	–	ns	

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will be busy for a maximum of 1ms. Thereafter, the device is busy for a maximum of 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 37: AC Characteristics: Normal Operation (3.3V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	25	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	20	–	ns	
RE# access time	^{t}REA	–	16	ns	
RE# HIGH hold time	^{t}REH	7	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	2
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	
RE# LOW to output hold	^{t}RLOH	5	–	ns	
RE# pulse width	^{t}RP	10	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to "full."
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Electrical Specifications – Program/Erase Characteristics

Table 38: Program/Erase Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial-page programs	NOP	–	4	cycles	1
BLOCK ERASE operation time	^{t}BERS	2	10	ms	2
Busy time for PROGRAM CACHE operation	^{t}CBSY	3	600	µs	3
Busy time for TWO-PLANE PROGRAM PAGE or TWO-PLANE BLOCK ERASE operation	^{t}DBSY	0.5	1	µs	
Cache read busy time	^{t}RCBSY	3	25	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	–	4
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	30	µs	
Busy time for PROGRAM/ERASE on locked blocks	^{t}LBSY	–	3	µs	
PROGRAM PAGE operation time	^{t}PROG	200	600	µs	2
Power-on reset time	^{t}POR	–	1	ms	
READ PAGE operation time	^{t}R	–	25	µs	

Notes:
1. Four total partial-page programs to the same page.
2. Typical ^{t}PROG and ^{t}BERS time may increase for two-plane operations.
3. ^{t}CBSY MAX time depends on timing between internal program completion and data-in.
4. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

Asynchronous Interface Timing Diagrams

Figure 73: RESET Operation

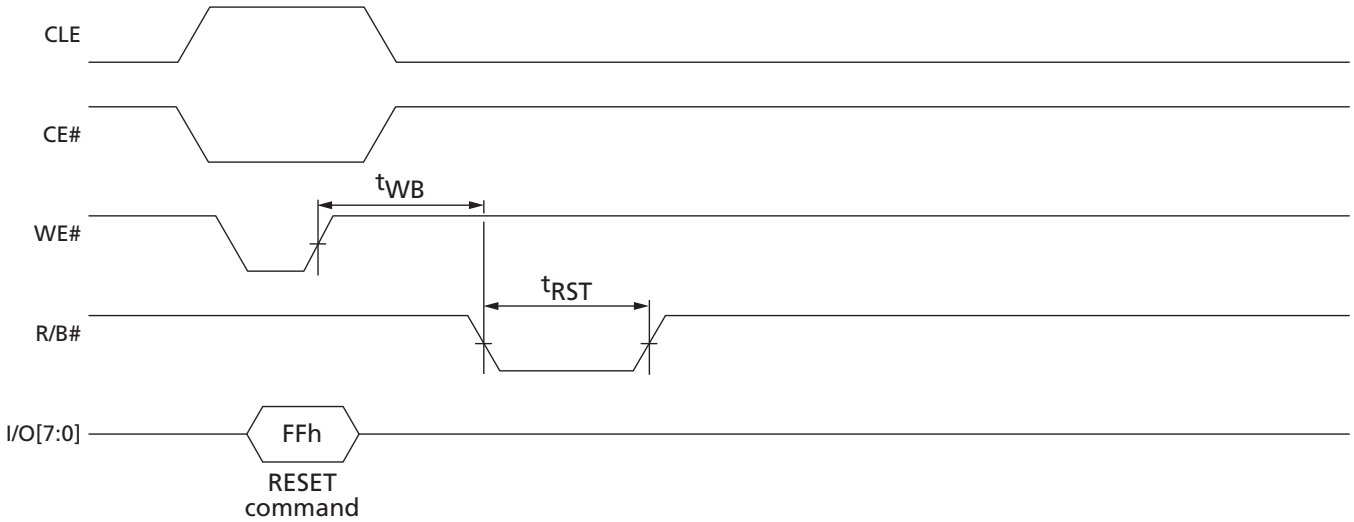


Figure 74: READ STATUS Cycle

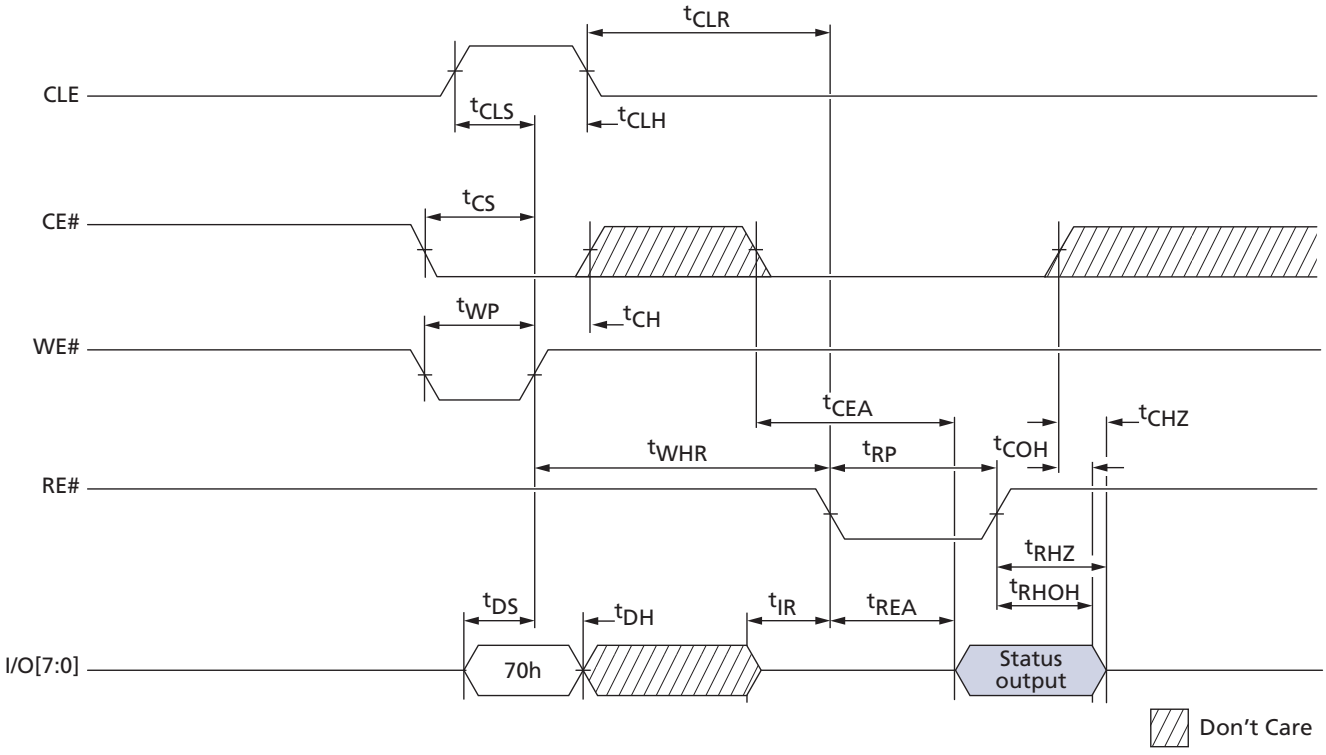


Figure 75: READ STATUS ENHANCED Cycle

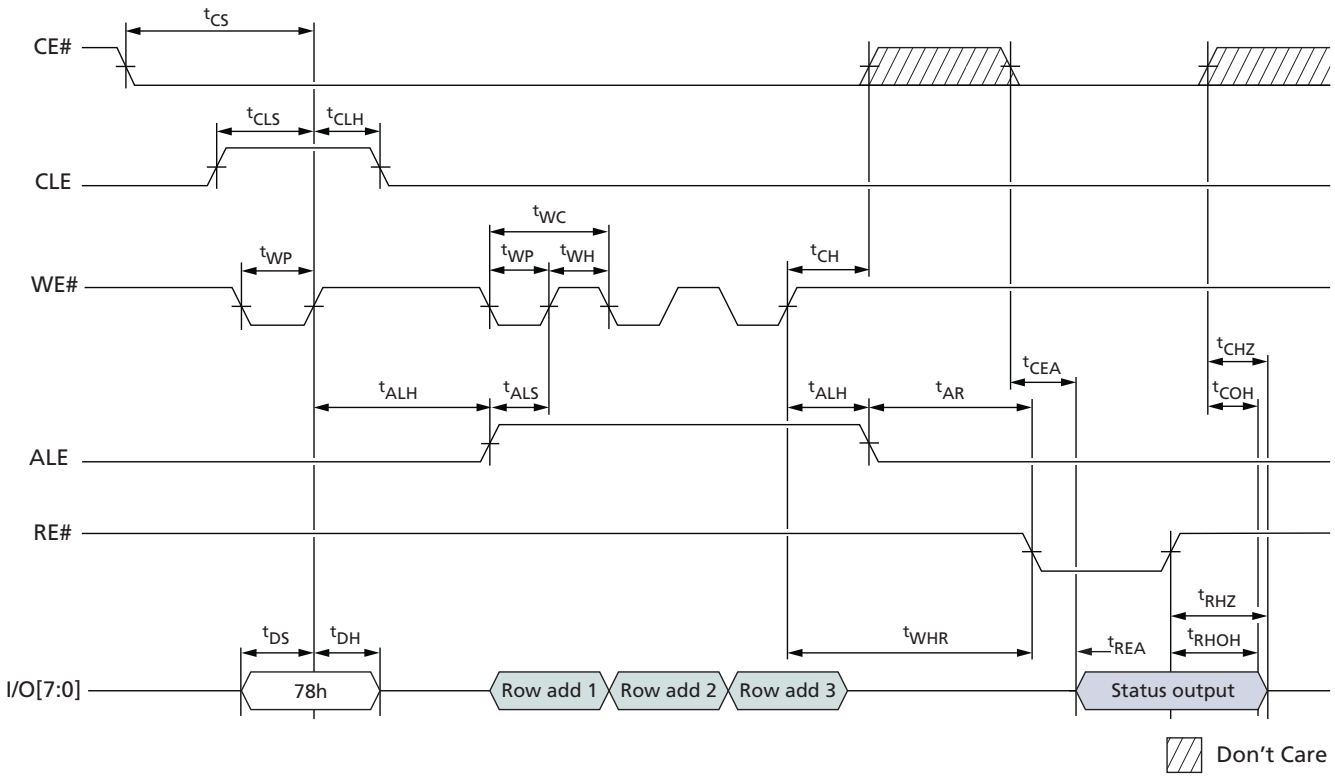


Figure 76: READ PARAMETER PAGE

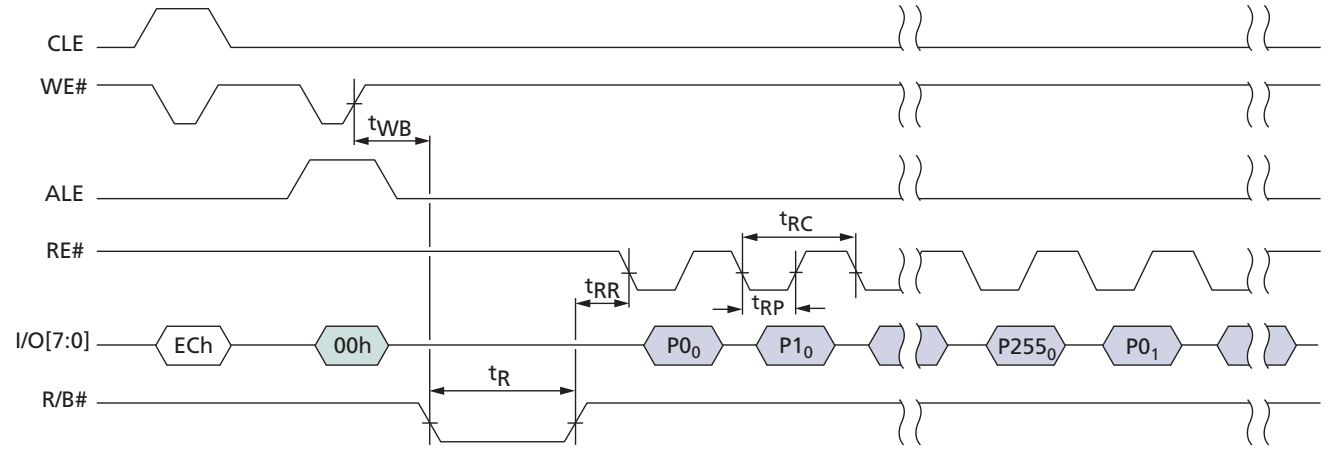


Figure 77: READ PAGE

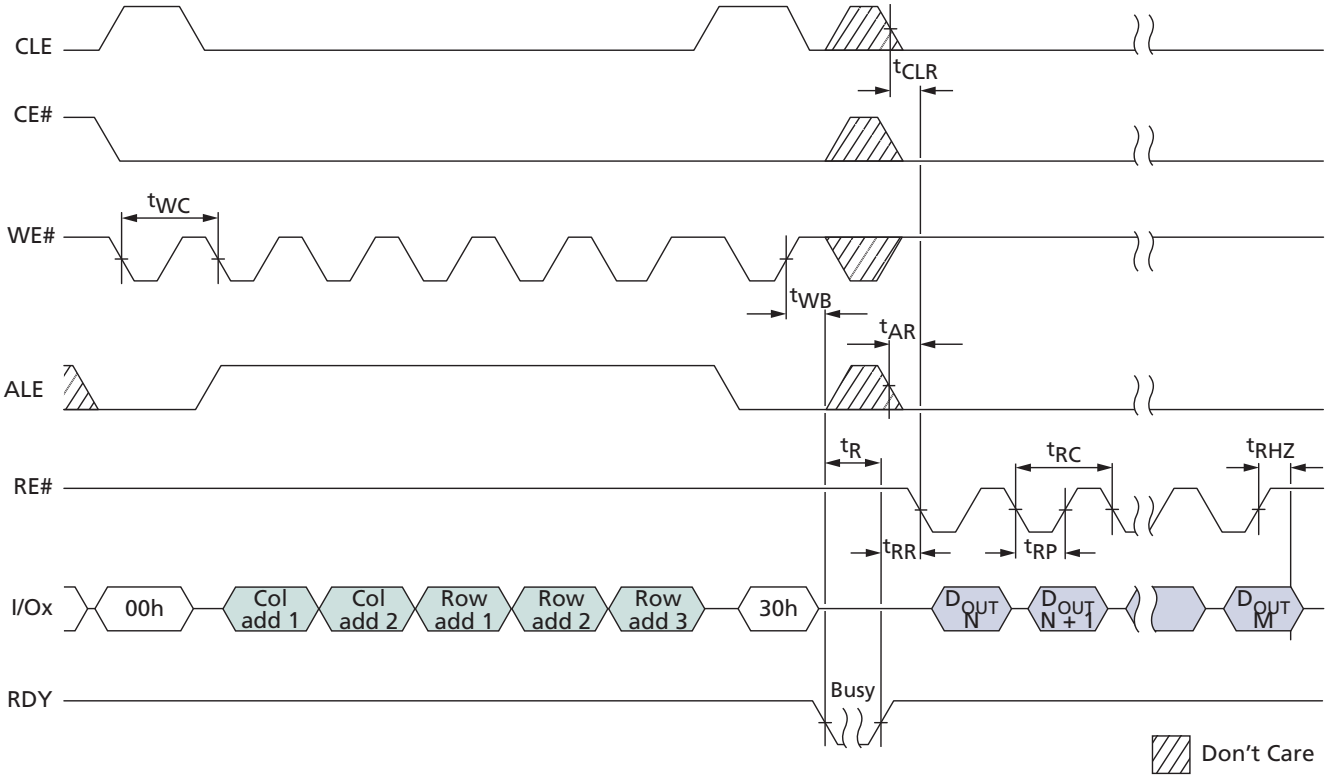


Figure 78: READ PAGE Operation with CE# "Don't Care"

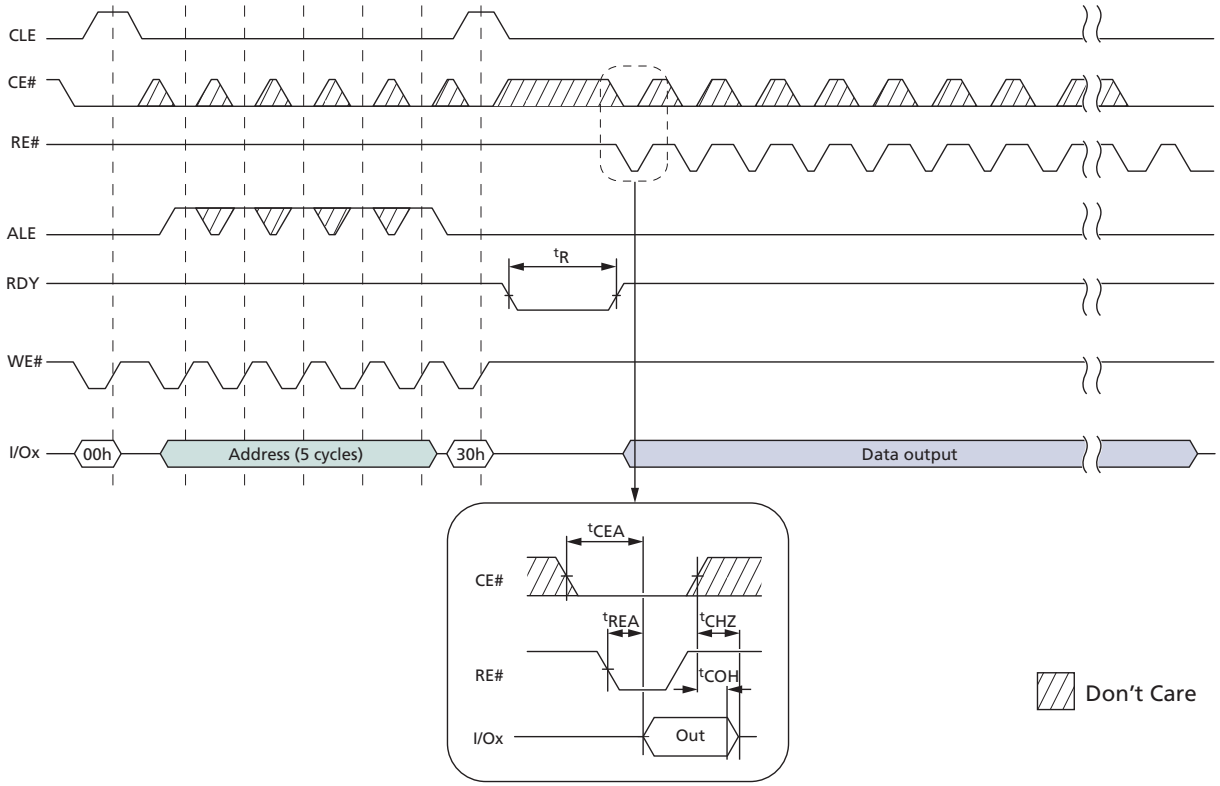


Figure 79: RANDOM DATA READ

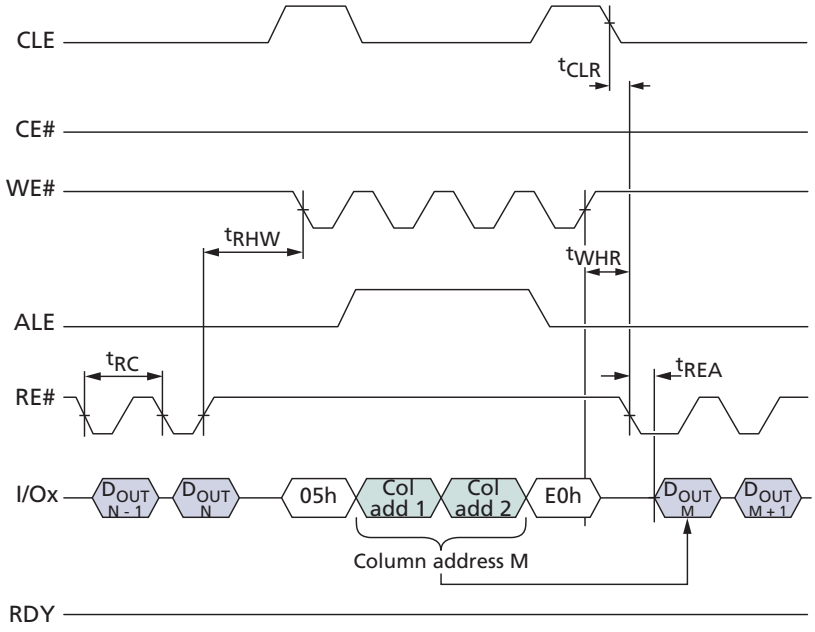


Figure 80: READ PAGE CACHE SEQUENTIAL

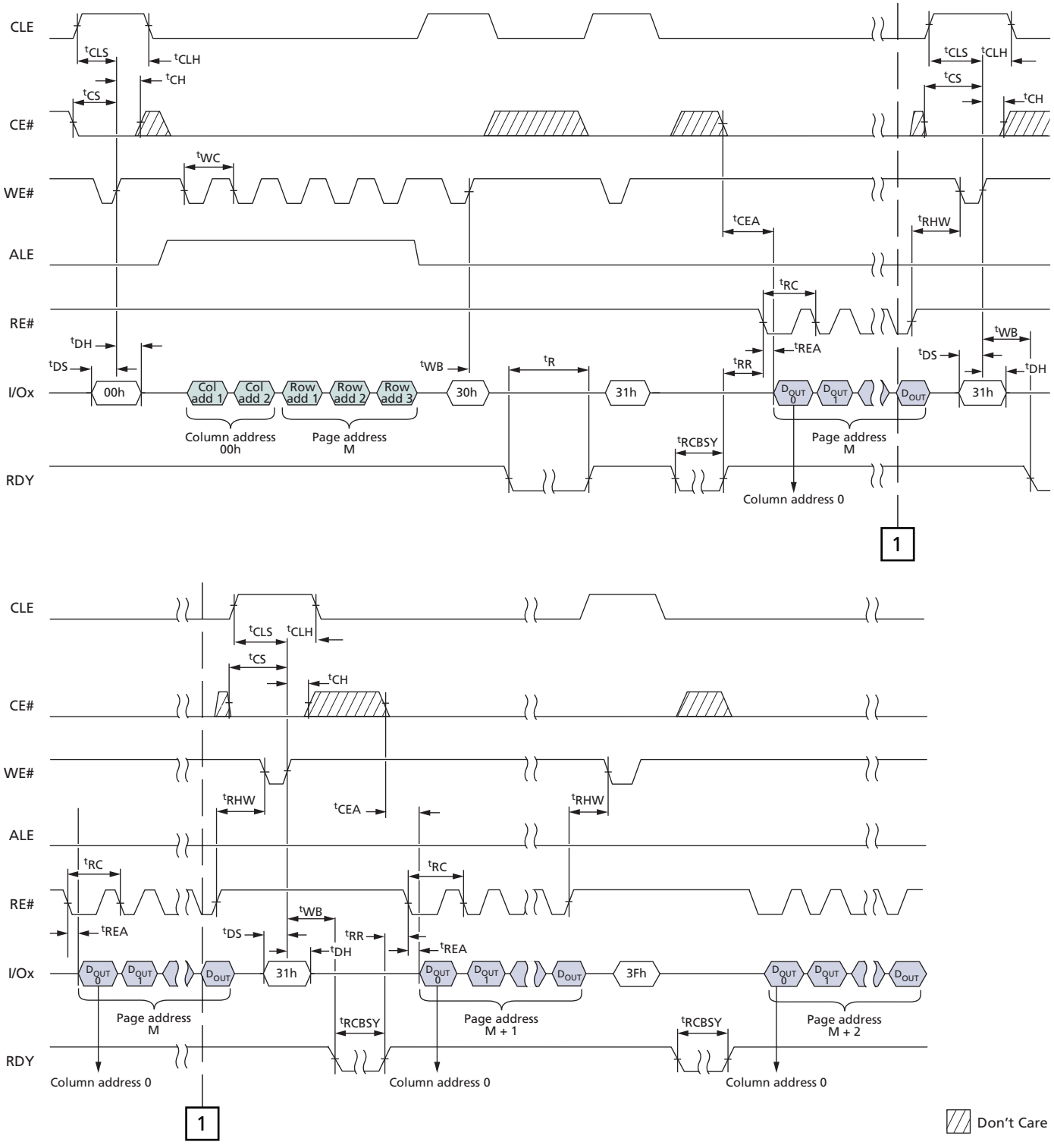


Figure 81: READ PAGE CACHE RANDOM

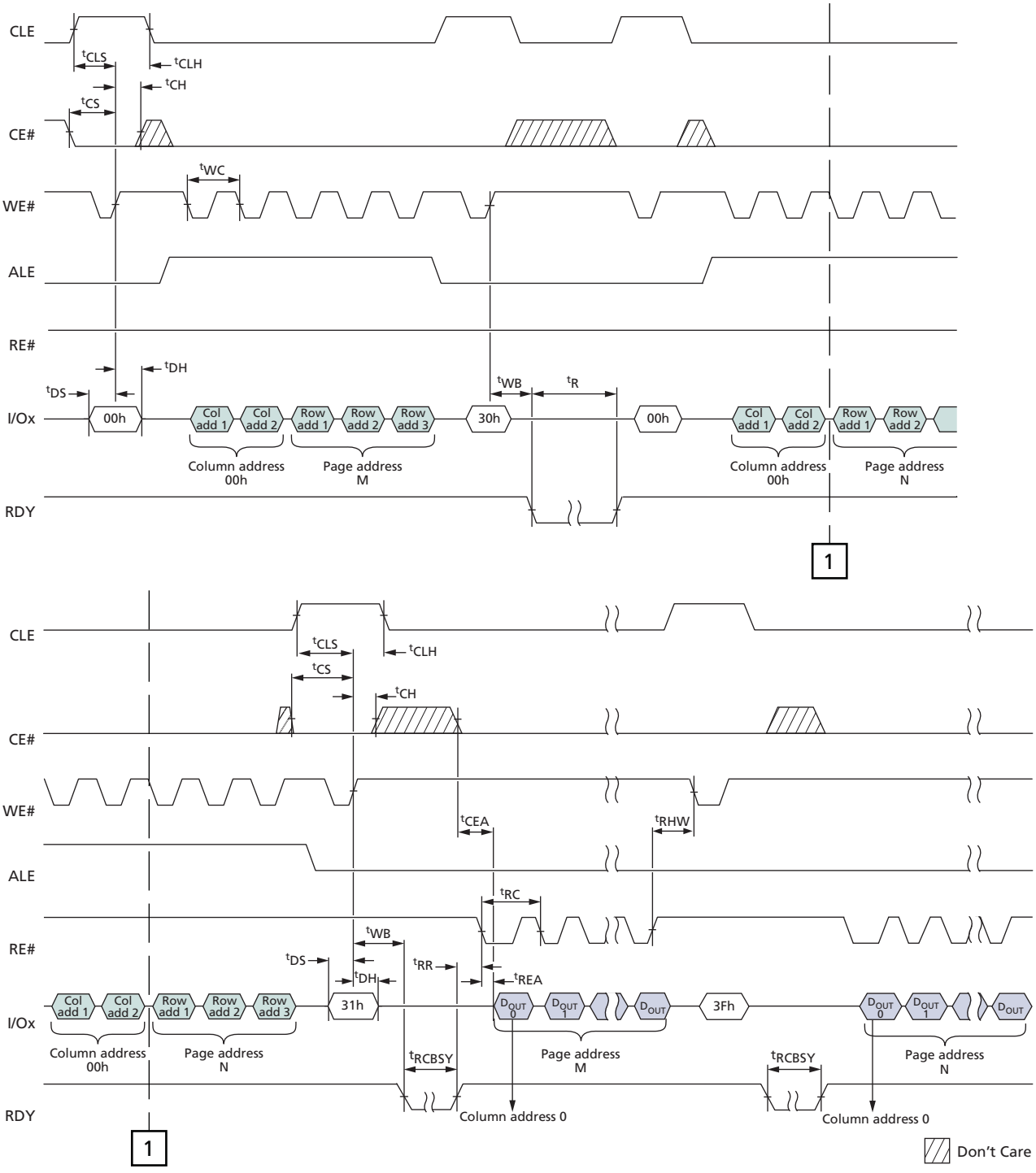


Figure 82: READ ID Operation

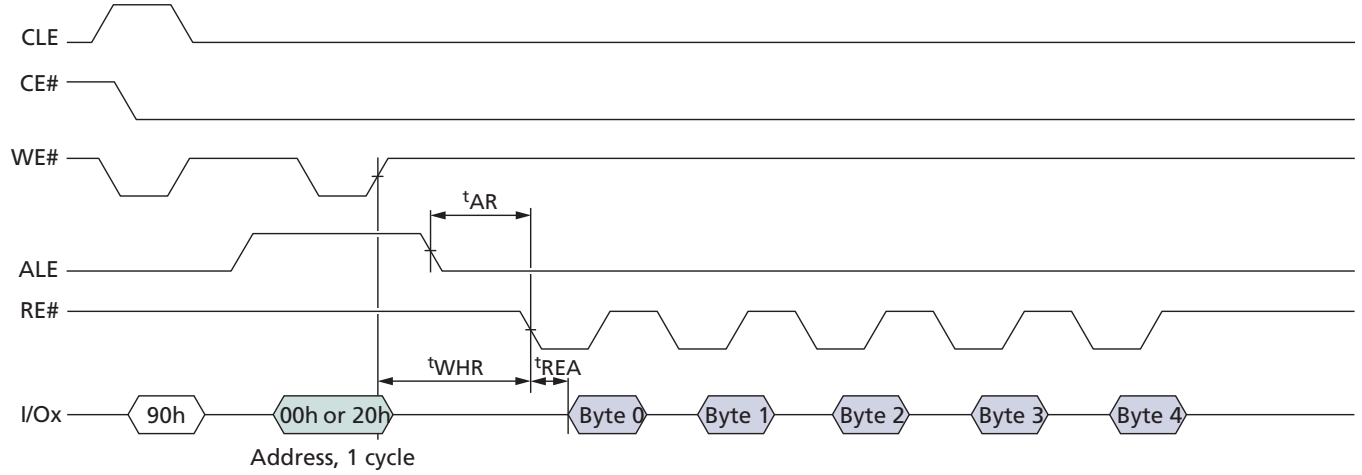


Figure 83: PROGRAM PAGE Operation

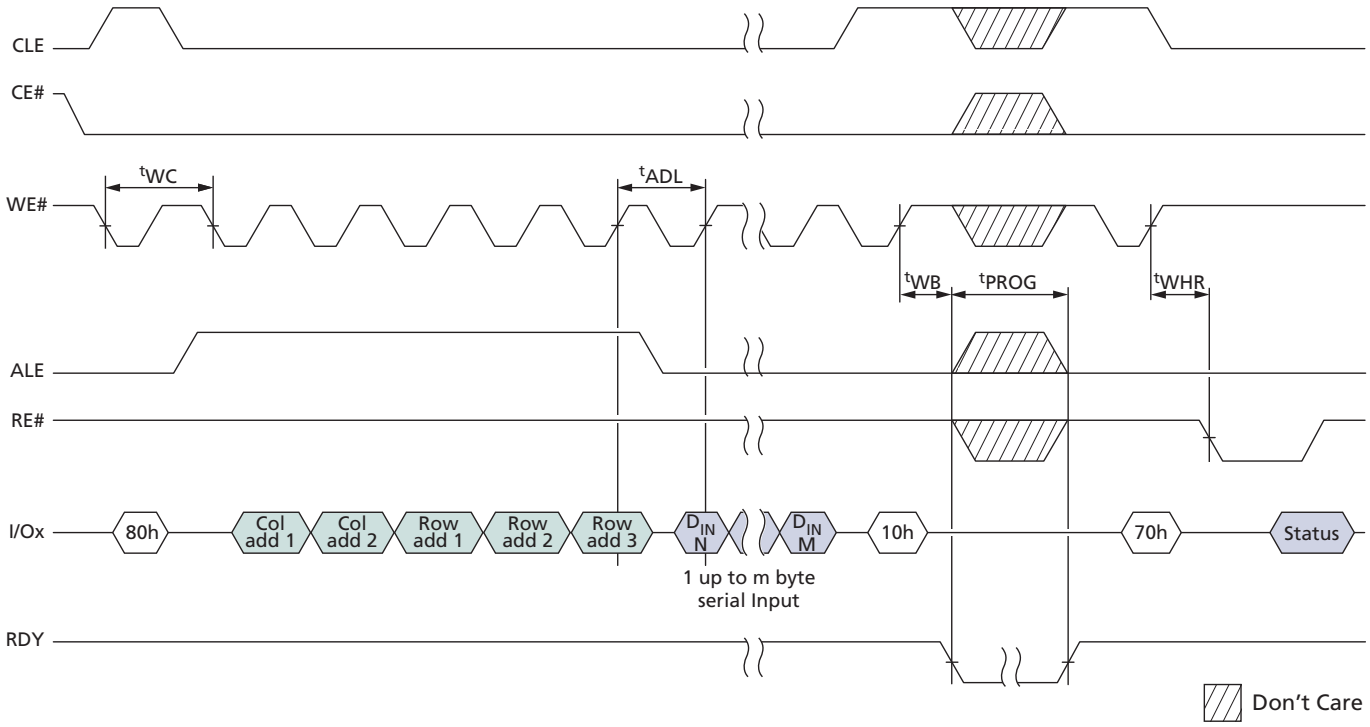


Figure 84: PROGRAM PAGE Operation with CE# "Don't Care"

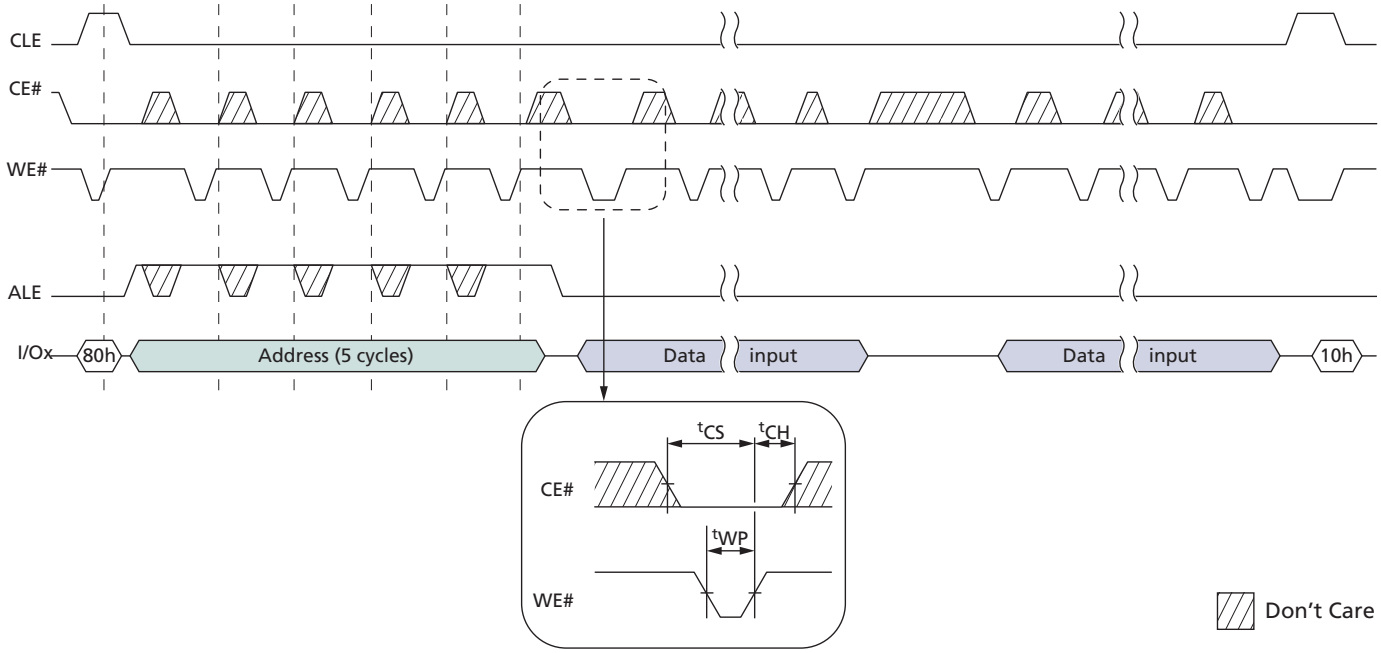


Figure 85: PROGRAM PAGE Operation with RANDOM DATA INPUT

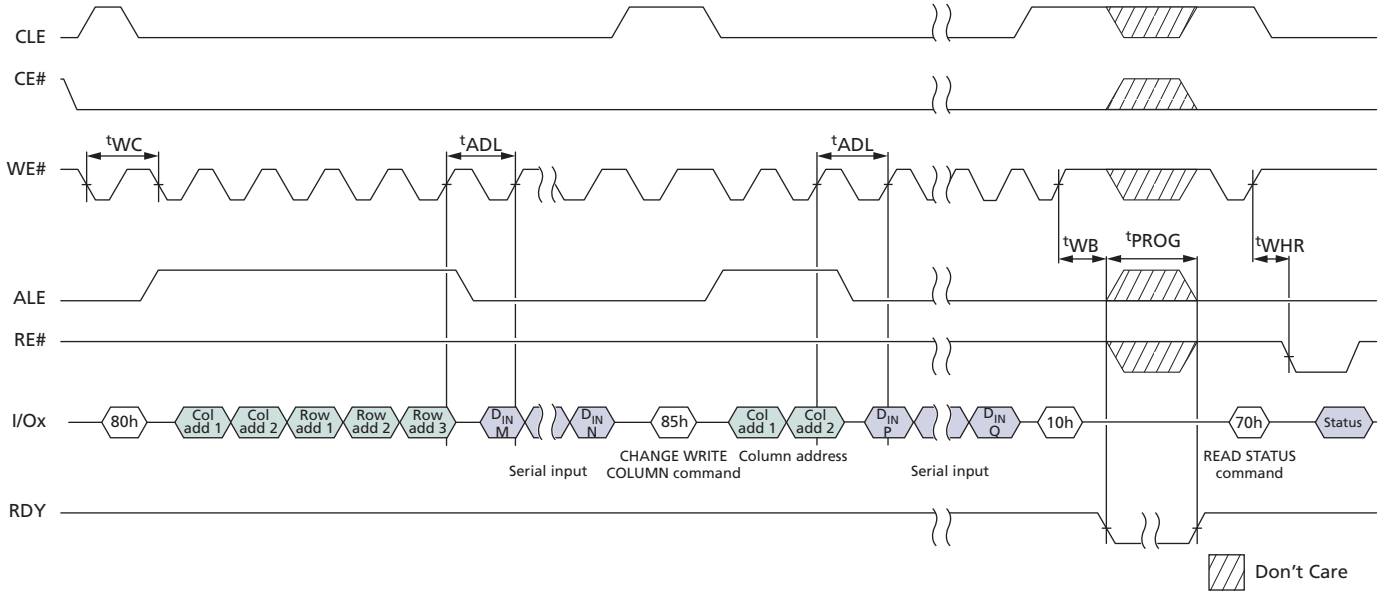


Figure 86: PROGRAM PAGE CACHE

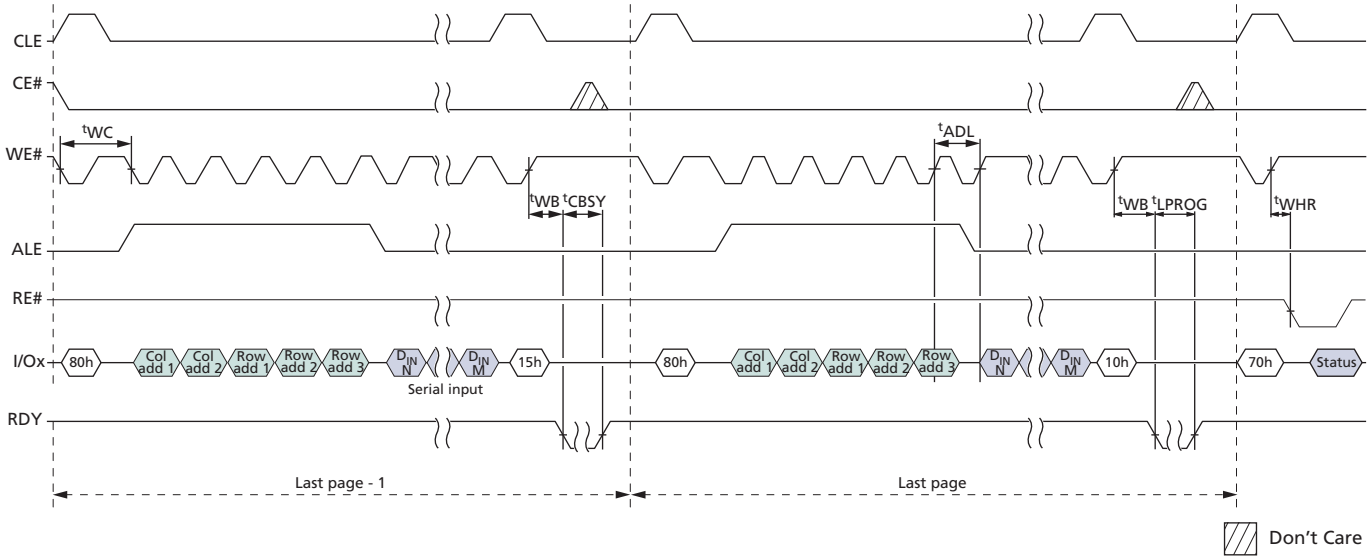


Figure 87: PROGRAM PAGE CACHE Ending on 15h

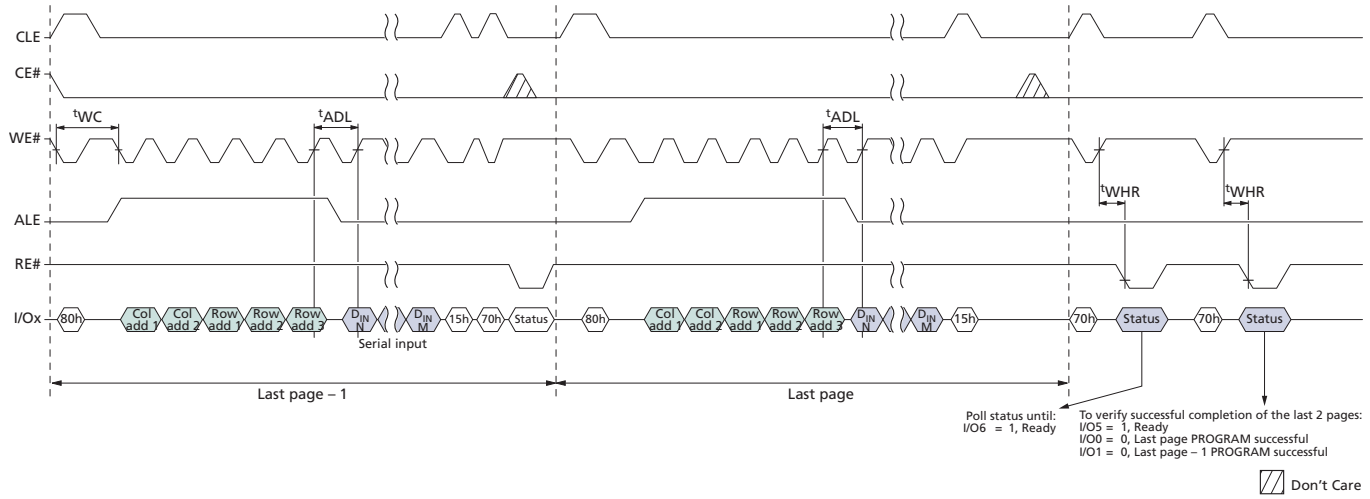


Figure 88: INTERNAL DATA MOVE

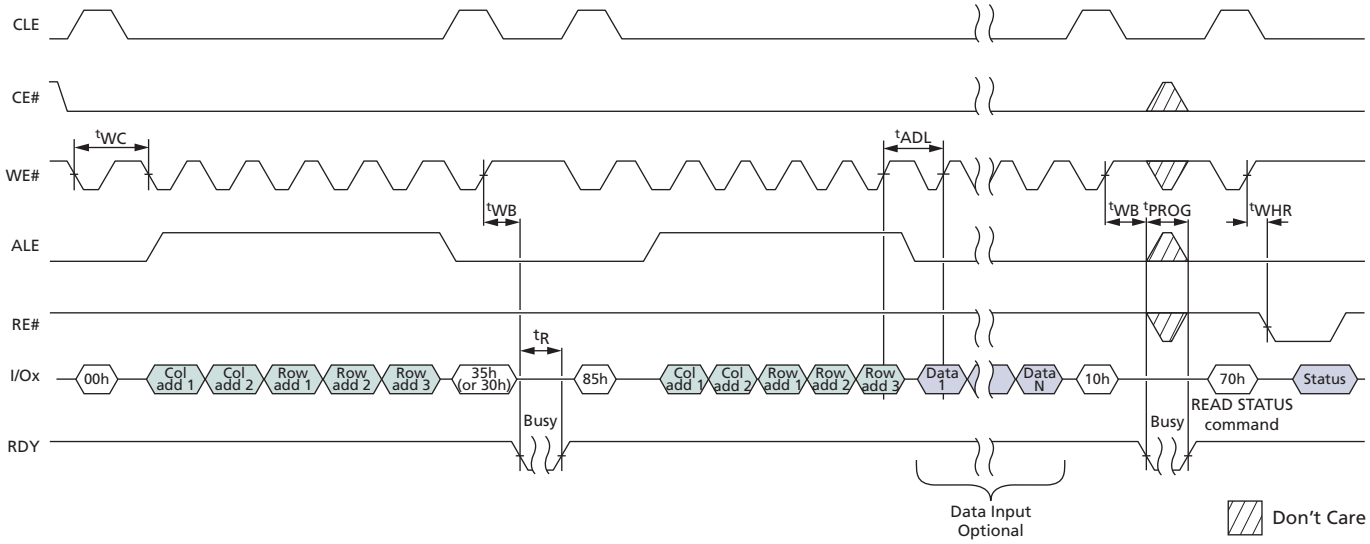
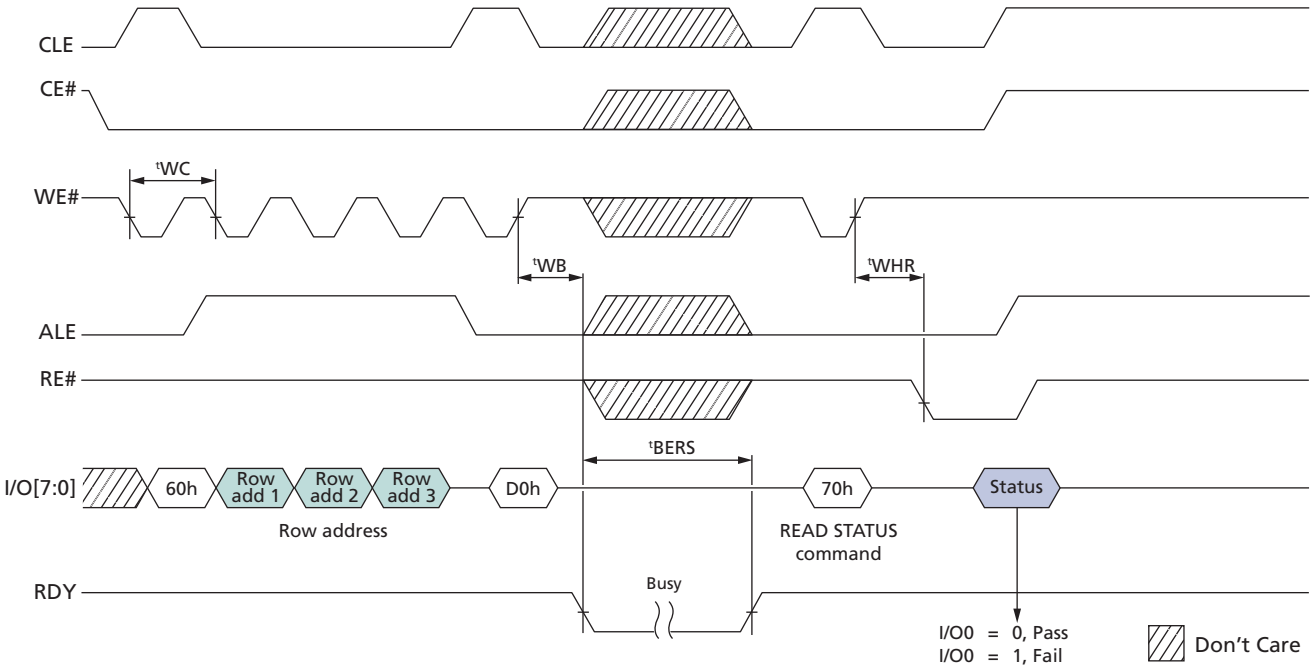


Figure 89: ERASE BLOCK Operation



1Gb: x16, x32 Mobile LPDDR2 SDRAM

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability

Table 39: S4 Configuration Addressing

Architecture	64 Meg x 16	32 Meg x 32	64 Meg x 32	64 Meg x 64
Die configuration	8 Meg x 16 x 8 banks	4 Meg x 32 x 8 banks	2 x 8 Meg x 16 x 8 banks	4 x 4 Meg x 32 x 8 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	512 (A[8:0])	1K (A[9:0])	512 (A[8:0])
Number of die	1	1	2	4
Die per rank	1	1	2	2
Ranks per channel[1]	1	1	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

General Description

The 1Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

LPDDR2 Array Configuration

The 1Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 40: I_{DD} Specifications (32 Meg x 32)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	180	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	200	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	

Table 40: I_{DD} Specifications (32 Meg x 32) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 41: I_{DD} Specifications (64 Meg x 16)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	

Table 41: I_{DD} Specifications (64 Meg x 16) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	140	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	155	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 42: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1])

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	12	mA
I_{DD02}	V_{DD2}	60	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	2	

Table 42: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1]) (Continued)

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD2P1}	V_{DD1}	1200	µA
I_{DD2P2}	V_{DD2}	3200	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2PS1}	V_{DD1}	1200	µA
I_{DD2PS2}	V_{DD2}	3200	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2N1}	V_{DD1}	1.2	mA
I_{DD2N2}	V_{DD2}	40	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD2NS1}	V_{DD1}	1.2	mA
I_{DD2NS2}	V_{DD2}	24	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD3P1}	V_{DD1}	2.8	mA
I_{DD3P2}	V_{DD2}	10	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3PS1}	V_{DD1}	2.8	mA
I_{DD3PS2}	V_{DD2}	10	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3N1}	V_{DD1}	3	mA
I_{DD3N2}	V_{DD2}	44	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD3NS1}	V_{DD1}	3	mA
I_{DD3NS2}	V_{DD2}	28	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD4R1}	V_{DD1}	4	mA
I_{DD4R2}	V_{DD2}	280	
$I_{DD4R,in}$	V_{DDCA}	4	
I_{DD4W1}	V_{DD1}	4	mA
I_{DD4W2}	V_{DD2}	310	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD51}	V_{DD1}	40	mA
I_{DD52}	V_{DD2}	140	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD5PB1}	V_{DD1}	4	mA
I_{DD5PB2}	V_{DD2}	46	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	2	

Table 42: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1]) (Continued)

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD5AB1}	V_{DD1}	4	mA
I_{DD5AB2}	V_{DD2}	46	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD81}	V_{DD1}	100	µA
I_{DD82}	V_{DD2}	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	40	

Note: 1. Actual I_{DD} for the 64M x 64 QDP device is dependant on the specific states in which the memory controller operates each of the two ranks. Consult Micron's Power Calculator for LPDDR2.

Table 43: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	I_{DD6} Partial-Array Self Refresh Current			Unit
		32 Meg x 32 64 Meg x 16	64 Meg x 32	64 Meg x 64	
Full array	V_{DD1}	230	460	920	µA
	V_{DD2}	700	1400	2800	
	V_{DDi}	20	40	80	
1/2 array	V_{DD1}	200	400	800	
	V_{DD2}	500	1000	2000	
	V_{DDi}	20	40	80	
1/4 array	V_{DD1}	190	380	760	
	V_{DD2}	400	800	1600	
	V_{DDi}	20	40	80	
1/8 array	V_{DD1}	185	370	740	
	V_{DD2}	360	720	1440	
	V_{DDi}	20	40	80	

Note: 1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I_{DD6} PASR currents are measured using bank-masking only.

Figure 90: V_{DD1} Typical Self-Refresh Current vs. Temperature (Per Die)

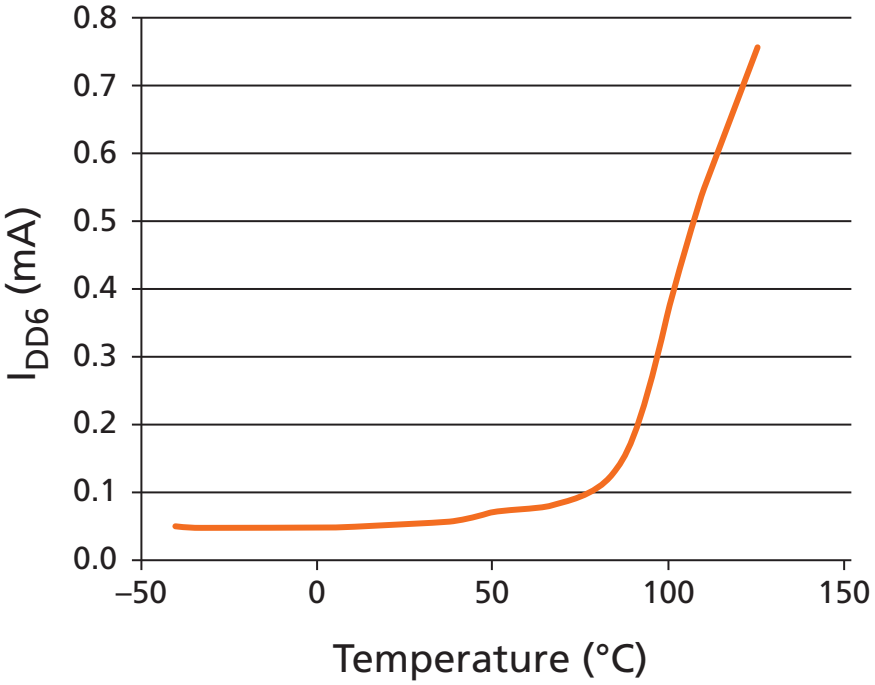
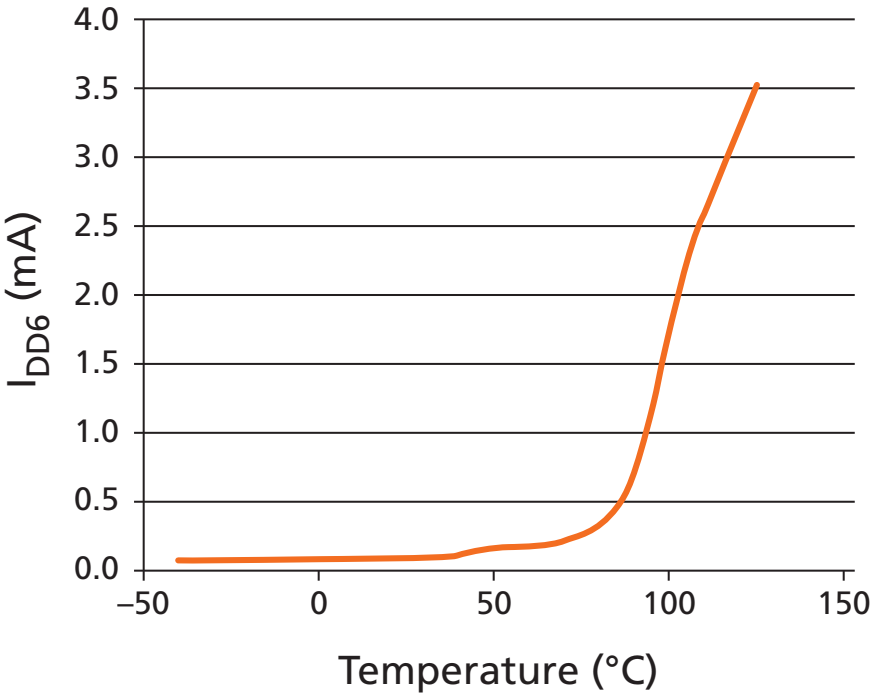


Figure 91: V_{DD2} Typical Self-Refresh Current vs. Temperature (Per Die)



Functional Description

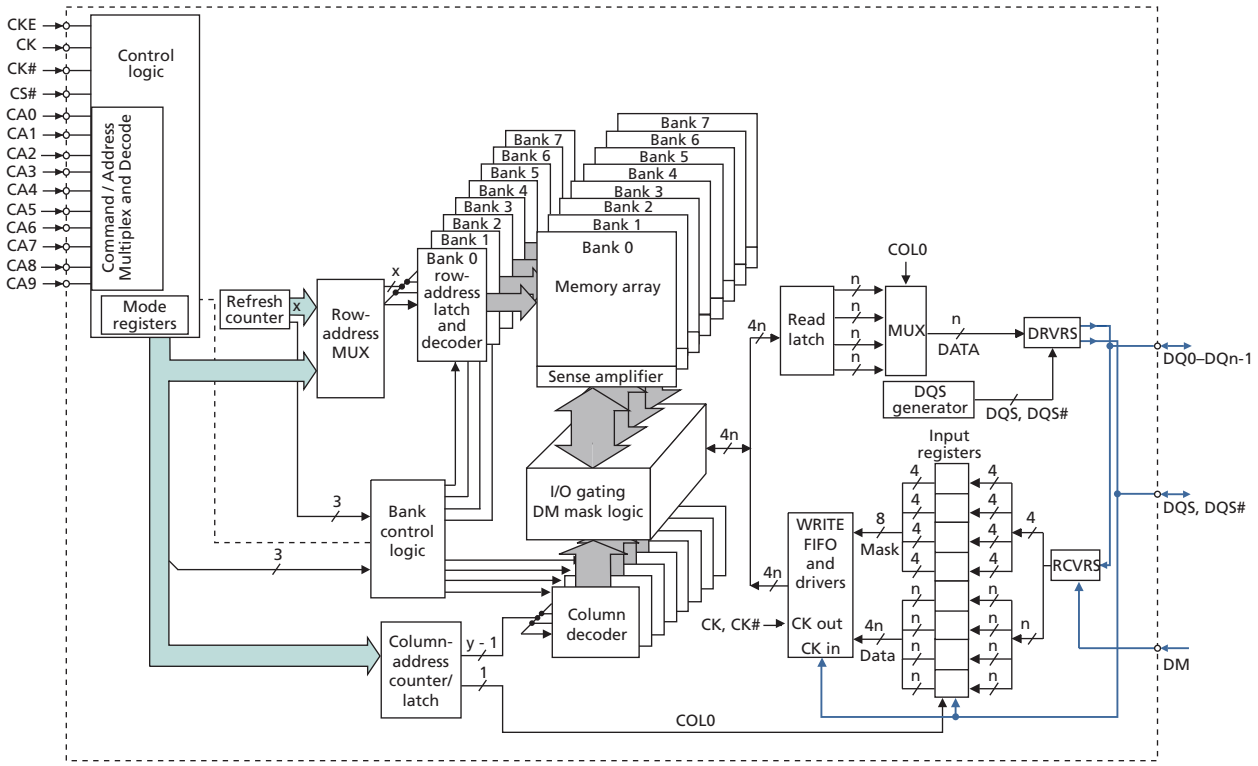
Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Figure 92: Functional Block Diagram



Power-Up

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see Figure 93 (page 139)). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$), and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply between Ta and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration ^{t}INIT0 (Tb - Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Voltage Ramp Completion

After Ta is reached:

- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least ^{t}INIT1 = 100ns, after which CKE can be asserted HIGH. The clock must be stable at least ^{t}INIT2 = 5 × ^{t}CK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (^{t}IS, ^{t}IH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for ^{t}CKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least ^{t}INIT3 = 200µs (Td).

2. RESET Command

After ^{t}INIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command.

Wait at least ^{t}INIT4 while keeping CKE asserted and issuing NOP commands.

3. MRRs and Device Auto Initialization (DAI) Polling

After ^{t}INIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down (page 191)).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of ^{t}INIT5, or until the DAI bit is set, before proceeding.

Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than ^{t}INIT5 after the RESET command. The controller must wait at least ^{t}INIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration

After ^{t}INIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).

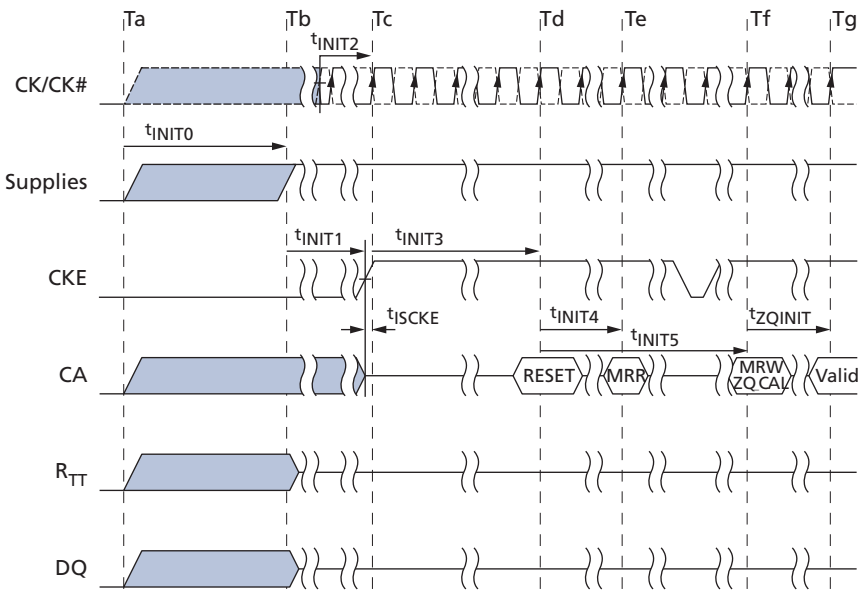
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after ^{t}ZQINIT.

5. Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH (page 200).

Figure 93: Voltage Ramp and Initialization Sequence



Note: 1. High-Z on the CA bus indicates valid NOP.

Table 44: Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	–	20	ms	Maximum voltage ramp time
tINIT1	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
tINIT2	5	–	tCK	Minimum stable clock before first CKE HIGH
tINIT3	200	–	µs	Minimum idle time after first CKE assertion
tINIT4	1	–	µs	Minimum idle time after RESET command
tINIT5	–	10	µs	Maximum duration of device auto initialization
tZQINIT	1	–	µs	ZQ initial calibration (S4 devices only)
tCKb	18	100	ns	Clock cycle time during boot

Note: 1. The tINIT0 maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding tINIT0 MAX, please contact the factory.

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latchup. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during the power-off sequence to avoid latchup.

Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Required Power Supply Conditions Between Tx and Tz:

- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} must be greater than V_{DDCA} - 200mV
- V_{DD1} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

The voltage difference between V_{SS}, V_{SSQ}, and V_{SSCA} must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed ^{t}POFF. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 45: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	^{t}POFF	–	2	sec

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

The MRR command is used to read from a register. The MRW command is used to write to a register. An "R" in the access column of the mode register assignment table indicates read-only; a "W" indicates write-only; "R/W" indicates read or write capable or enabled.

Table 46: Mode Register Assignments

Notes 1–5 apply to all parameters and conditions

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI		DNVI	DI	DAI	go to MR0
1	01h	Device feature 1	W	*n*WR (for AP)			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU					RL and WL			go to MR2
3	03h	I/O config-1	W	RFU					DS			go to MR3
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate			go to MR4
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		go to MR8
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11–15	0Bh ≈ 0Fh	Reserved	–	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18–19	12h–13h	Reserved	–	RFU								go to MR18
20–31	14h–1Fh	Reserved for NVM										MR20–MR30
32	20h	DQ calibration pattern A	R	See Table 83 (page 187).								go to MR32
33–39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Table 83 (page 187).								go to MR40
41–47	29h–2Fh	Do not use										go to MR41
48–62	30h–3Eh	Reserved	–	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64–126	40h–7Eh	Reserved	–	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128–190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192–254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

Notes:
1. RFU bits must be set to 0 during MRW.
2. RFU bits must be read as 0 during MRR.
3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.
4. RFU mode registers must not be written.
5. WRITEs to read-only registers must have no impact on the functionality of the device.

Table 47: MR0 Device Information (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI		DNVI	DI	DAI

Table 48: MR0 Op-Code Bit Definitions

Notes 1–4 apply to all parameters and conditions

Register Information	Tag	Type	OP	Definition
Device auto initialization status	DAI	Read-only	OP0	0b: DAI complete
				1b: DAI in progress
Device information	DI	Read-only	OP1	0b
				1b: NVM
Data not valid information	DNVI	Read-only	OP2	0b: DNVI not supported
Built-in self test for RZQ information	RZQI	Read-only	OP[4:3]	00b: RZQ self test not supported
				01b: ZQ pin might be connected to V_{DDCA} or left floating
				10b: ZQ pin might be shorted to ground
				11b: ZQ pin self test complete; no error condition detected

Notes:
1. If RZQI is supported, it will be set upon completion of the MRW ZQ initialization calibration.
2. If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3] = 01 or OP[4:3] = 10 could indicate a ZQ-pin assembly error. It is recommended that the assembly error be corrected.
3. In the case of a possible assembly error (either OP[4:3] = 01 or OP[4:3] = 10, as defined above), the device will default to factory trim settings for R_{ON} and will ignore ZQ calibration commands. In either case, the system might not function as intended.
4. If a ZQ self test returns a value of 11b, this indicates that the device has detected a resistor connection to the ZQ pin. Note that this result cannot be used to validate the ZQ resistor value, nor does it indicate that the ZQ resistor tolerance meets the specified limits (240 ohms ±1%).

Table 49: MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
*n*WR (for AP)			WC	BT	BL		

Table 50: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL = burst length	Write-only	OP[2:0]	010b: BL4 (default)	
			011b: BL8	
			100b: BL16	
			All others: Reserved	
BT = burst type	Write-only	OP3	0b: Sequential (default)	
			1b: Interleaved	
WC = wrap control	Write-only	OP4	0b: Wrap (default)	
			1b: No wrap	
*n*WR = number of ^{t}WR clock cycles	Write-only	OP[7:5]	001b: *n*WR = 3 (default)	1
			010b: *n*WR = 4	
			011b: *n*WR = 5	
			100b: *n*WR = 6	
			101b: *n*WR = 7	
			110b: *n*WR = 8	
			All others: Reserved	

Note: 1. The programmed value in *n*WR register is the number of clock cycles that determines when to start internal precharge operation for a WRITE burst with AP enabled. It is determined by RU (^{t}WR/^{t}CK).

Table 51: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC)

Notes 1–5 apply to all parameters and conditions

							Burst Cycle Number and Burst Address Sequence															
BL	BT	C3	C2	C1	C0	WC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
4	Any	X	X	0b	0b	Wrap	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
	Any	X	X	X	0b	No wrap	*y*	*y* + 1	*y* + 2	*y* + 3												
8	Seq	X	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	Any	X	X	X	0b	No wrap	Illegal (not supported)															

Table 51: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC) (Continued)

Notes 1–5 apply to all parameters and conditions

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
16	Seq	0b	0b	0b	0b	Wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b		Illegal (not supported)															
	Any	X	X	X	0b	No wrap	Illegal (not supported)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL = 4, the burst address represents C[1:0].
3. For BL = 8, the burst address represents C[2:0].
4. For BL = 16, the burst address represents C[3:0].
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown in the following table.

Table 52: No-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full-page boundary				
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

Note:
1. No-wrap BL = 4 data orders shown are prohibited.

Table 53: MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			

Table 54: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition
RL and WL	Write-only	OP[3:0]	0001b: RL3/WL1 (default)
			0010b: RL4/WL2
			0011b: RL5/WL2
			0100b: RL6/WL3
			0101b: RL7/WL4
			0110b: RL8/WL4
			All others: Reserved

Table 55: MR3 I/O Configuration 1 (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

Table 56: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition
DS	Write-only	OP[3:0]	0000b: Reserved
			0001b: 34.3 ohm typical
			0010b: 40 ohm typical (default)
			0011b: 48 ohm typical
			0100b: 60 ohm typical
			0101b: Reserved
			0110b: 80 ohm typical
			0111b: 120 ohm typical
			All others: Reserved

Table 57: MR4 Device Temperature (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM refresh rate		

Table 58: MR4 Op-Code Bit Definitions

Notes 1–10 apply to all parameters and conditions

Feature	Type	OP	Definition
SDRAM refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded
			001b: 4 × ^{t}REFI, 4 × ^{t}REFIpb, 4 × ^{t}REFW
			010b: 2 × ^{t}REFI, 2 × ^{t}REFIpb, 2 × ^{t}REFW
			011b: 1 × ^{t}REFI, 1 × ^{t}REFIpb, 1 × ^{t}REFW (≤85°C)
			100b: Reserved
			101b: 0.25 × ^{t}REFI, 0.25 × ^{t}REFIpb, 0.25 × ^{t}REFW, do not derate SDRAM AC timing
			110b: 0.25 × ^{t}REFI, 0.25 × ^{t}REFIpb, 0.25 × ^{t}REFW, derate SDRAM AC timing
			111b: SDRAM high temperature operating limit exceeded
Temperature update flag (TUF)	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4
			1b: OP[2:0] value has changed since last read of MR4

Notes:
1. A MODE REGISTER READ from MR4 will reset OP7 to 0.
2. OP7 is reset to 0 at power-up.
3. If OP2 = 1, the device temperature is greater than 85°C.
4. OP7 is set to 1 if OP[2:0] has changed at any time since the last MR4 read.
5. The device might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: ^{t}RCD, ^{t}RC, ^{t}RAS, ^{t}RP, and ^{t}RRD. The ^{t}DQSCK parameter must be derated as specified in AC Timing. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in Temperature Sensor (page 184).
9. While the AT grade product is guaranteed to operate from T_{CASE} –40°C to 105°C, the temperature sensor accuracy relative to this is not guaranteed. The temperature sensor embedded in the LPDDR2 device is not an accurate reflection of the DRAM T_{CASE} operating temperature. Sampling of the sensor has shown up to a ±7°C variance from actual T_{CASE}.
10. The temperature sensor does not work above 105°C, but the functionalities here described in this datasheet are guaranteed for products range up to 125°C (AUT).

Table 59: MR5 Basic Configuration 1 (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

Table 60: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	0000 0011b:
			All others: Reserved

Table 61: MR6 Basic Configuration 2 (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 62: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	0000 0000b: Version A
			0000 0001b: Version B
			0000 0010b: Version C
			0000 0011b: Version D

Table 63: MR7 Basic Configuration 3 (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 64: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	0000 0000b: Version A

Note: 1. MR7 is vendor-specific.

Table 65: MR8 Basic Configuration 4 (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 66: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b
			01b
			10b: NVM
			11b: Reserved

Table 66: MR8 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition
Density	Read-only	OP[5:2]	0000b: 64Mb
			0001b: 128Mb
			0010b: 256Mb
			0011b: 512Mb
			0100b: 1Gb
			0101b: 2Gb
			0110b: 4Gb
			0111b: 8Gb
			1000b: 16Gb
			1001b: 32Gb
			All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x32
			01b: x16
			10b: x8
			11b: not used

Table 67: MR9 Test Mode (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 68: MR10 Calibration (MA[7:0] = 0Ah)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4	Calibration code							

Table 69: MR10 Op-Code Bit Definitions

Notes 1–4 apply to all parameters and conditions

Feature	Type	OP	Definition
Calibration code	Write-only	OP[7:0]	0xFF: Calibration command after initialization
			0xAB: Long calibration
			0x56: Short calibration
			0xC3: ZQRESET
			All others: Reserved

Notes:
1. Host processor must not write MR10 with reserved values.
2. The device ignores calibration commands when a reserved value is written into MR10.
3. See AC timing table for the calibration latency.

4. If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see MRW ZQ Calibration Commands (page 189)) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

Table 70: MR[11:15] Reserved (MA[7:0] = 0Bh–0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table 71: MR16 PASR Bank Mask (MA[7:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank mask (4-bank or 8-bank)							

Table 72: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the bank = unmasked (default)
			1b: refresh blocked = masked

Note: 1. For 4-bank devices, only OP[3:0] are used.

Table 73: MR17 PASR Segment Mask (MA[7:0] = 011h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment mask							

Note: 1. This table applies for 1Gb to 8Gb devices only.

Table 74: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: refresh enable to the segment: = unmasked (default)
			1b: refresh blocked: = masked

Table 75: MR17 PASR Row Address Ranges in Masked Segments

Segment	OP	Segment Mask	1Gb	2Gb, 4Gb	8Gb
			R[12:10]	R[13:11]	R[14:12]
0	0	XXXXXXX1	000b		
1	1	XXXXXX1X	001b		
2	2	XXXXX1XX	010b		
3	3	XXXX1XXX	011b		

Table 75: MR17 PASR Row Address Ranges in Masked Segments (Continued)

Segment	OP	Segment Mask	1Gb	2Gb, 4Gb	8Gb
			R[12:10]	R[13:11]	R[14:12]
4	4	XXX1XXXX	100b		
5	5	XX1XXXXX	101b		
6	6	X1XXXXXX	110b		
7	7	1XXXXXXX	111b		

Note: 1. X is "Don't Care" for the designated segment.

Table 76: Reserved Mode Registers

Mode Register	MA	Address	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[18:19]	MA[7:0]	12h–13h	RFU	Reserved							
MR[20:31]		14h–1Fh	NVM[1]								
MR[33:39]		21h–27h	DNU[1]								
MR[41:47]		29h–2Fh									
MR[48:62]		30h–3Eh	RFU								
MR[64:126]		40h–7Eh	RFU								
MR127		7Fh	DNU								
MR[128:190]		80h–BEh	RVU[1]								
MR191		BFh	DNU								
MR[192:254]		C0h–FEh	RVU								
MR255		FFh	DNU								

Note: 1. NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

Table 77: MR63 RESET (MA[7:0] = 3Fh) – MRW Only

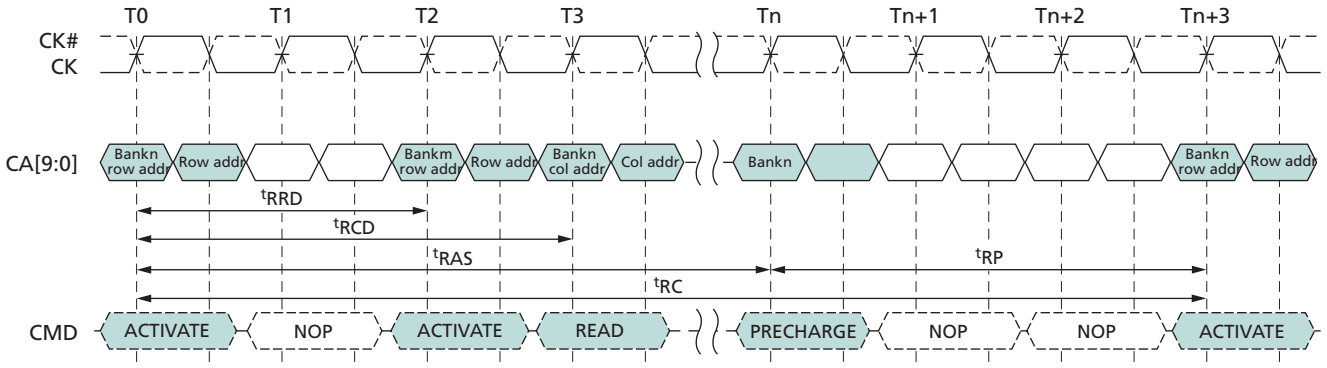
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: 1. For additional information on MRW RESET see MODE REGISTER WRITE Command (page 188).

ACTIVATE Command

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at ^{t}RCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (^{t}RC). The minimum time interval between ACTIVATE commands to different banks is ^{t}RRD.

Figure 94: ACTIVATE Command



Notes:
1. ^{t}RCD = 3, ^{t}RP = 3, ^{t}RRD = 2.
2. A PRECHARGE ALL command uses ^{t}RPab timing, and a single-bank PRECHARGE command uses ^{t}RPpb timing. In this figure, ^{t}RP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

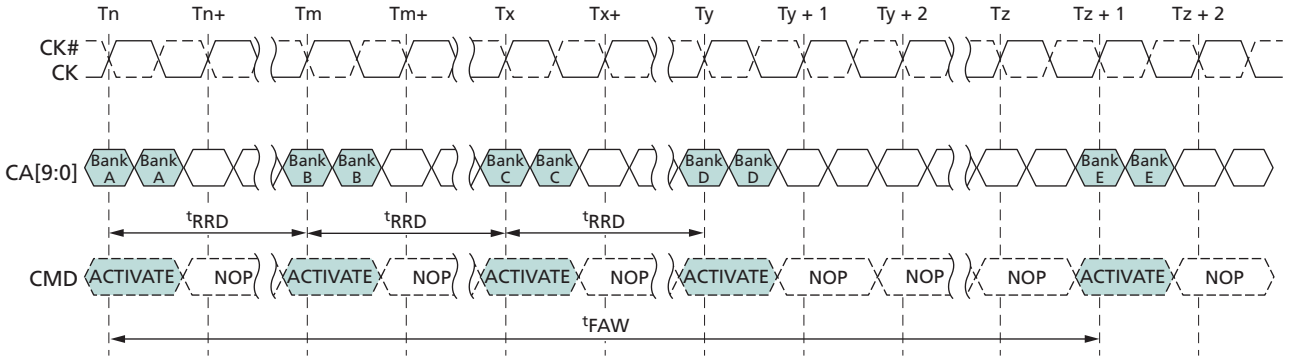
8-Bank Device Operation

Two rules regarding 8-bank device operation must be observed. One rule restricts the number of sequential ACTIVATE commands that can be issued; the second provides additional RAS precharge time for a PRECHARGE ALL command.

The 8-Bank Device Sequential Bank Activation Restriction: No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling ^{t}FAW window. To convert to clocks, divide ^{t}FAW[ns] by ^{t}CK[ns], and round up to the next integer value. For example, if RU(^{t}FAW/^{t}CK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock *n* + 1 and *n* + 9. REFpb also counts as bank activation for purposes of ^{t}FAW.

The 8-Bank Device PRECHARGE ALL Provision: ^{t}RP for a PRECHARGE ALL command must equal ^{t}RPab, which is greater than ^{t}RPpb.

Figure 95: tFAW Timing (8-Bank Devices)



Note: 1. Exclusively for 8-bank devices.

Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles.

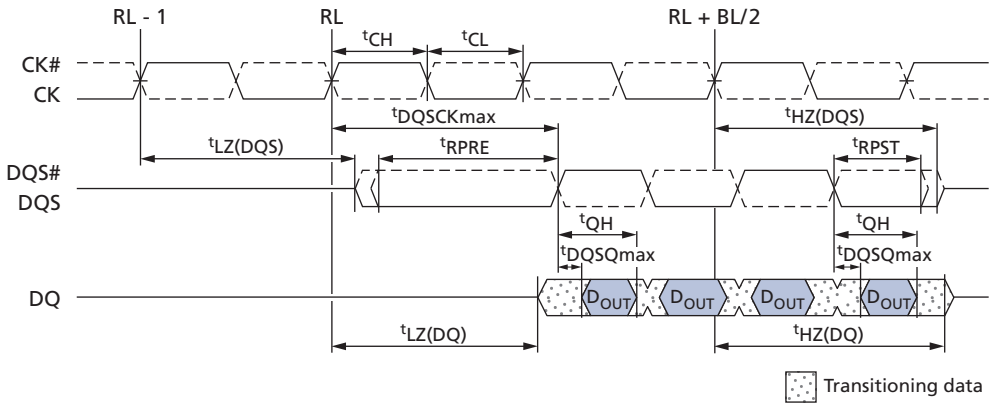
A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, READs can be interrupted by READs and WRITEs can be interrupted by WRITEs, provided that the interrupt occurs on a 4-bit boundary and that tCCD is met.

Burst READ Command

The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW tRPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers.

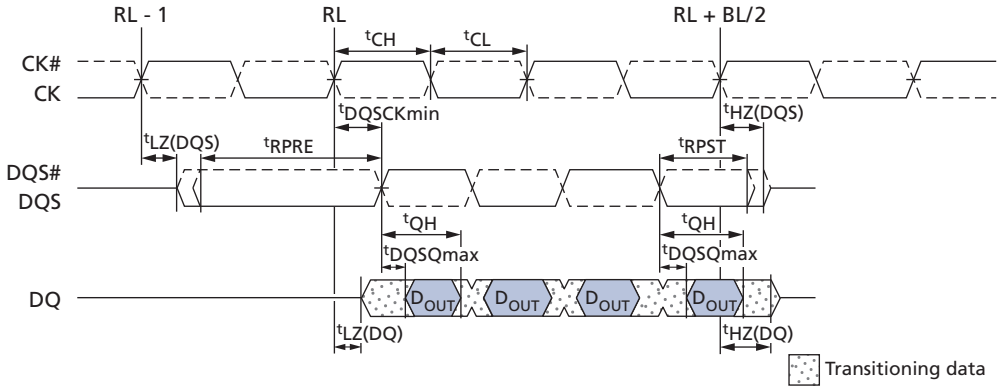
Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 96: READ Output Timing – tDQSCK (MAX)



Notes: 1. tDQSCK can span multiple clock periods.
2. An effective burst length of 4 is shown.

Figure 97: READ Output Timing – tDQSCK (MIN)



Note: 1. An effective burst length of 4 is shown.

Figure 98: Burst READ – RL = 5, BL = 4, ^{t}DQSCK > ^{t}CK

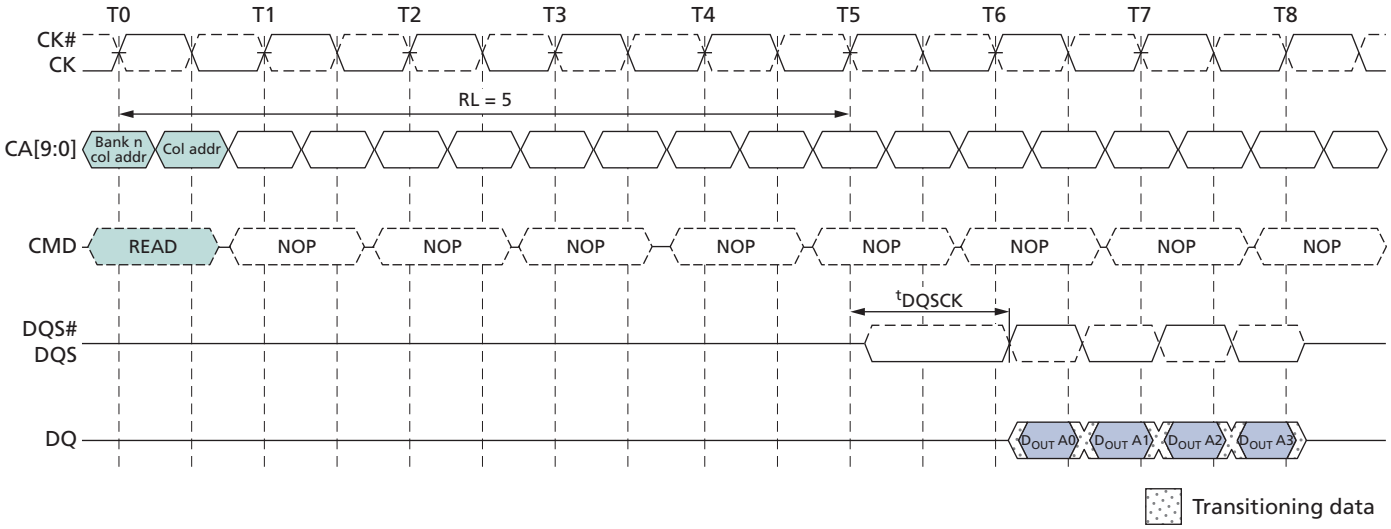


Figure 99: Burst READ – RL = 3, BL = 8, ^{t}DQSCK < ^{t}CK

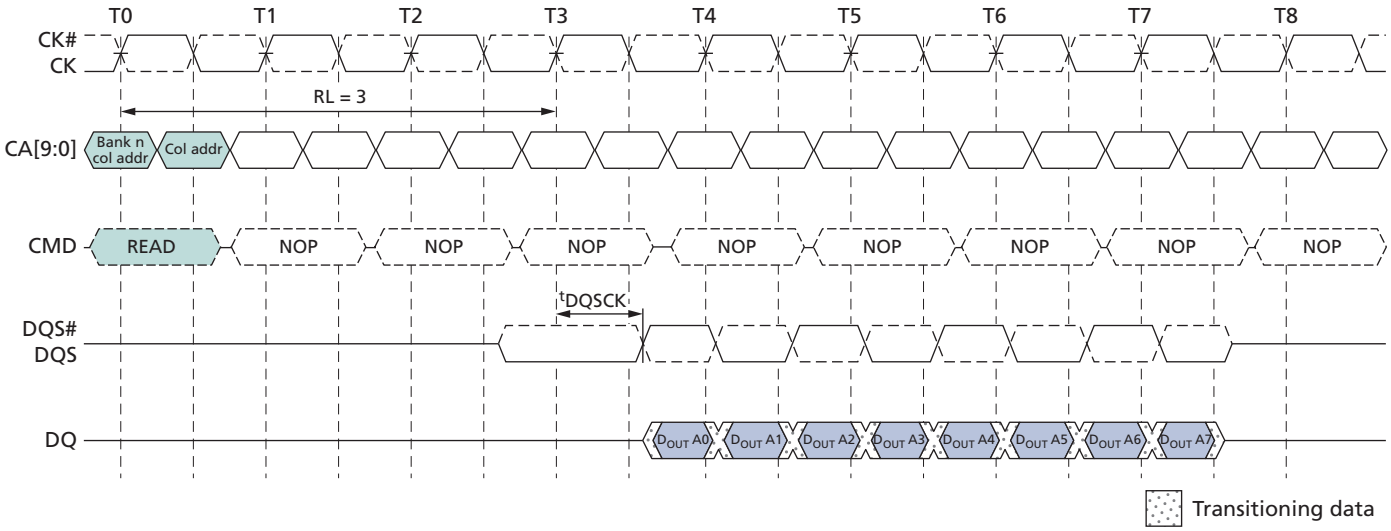
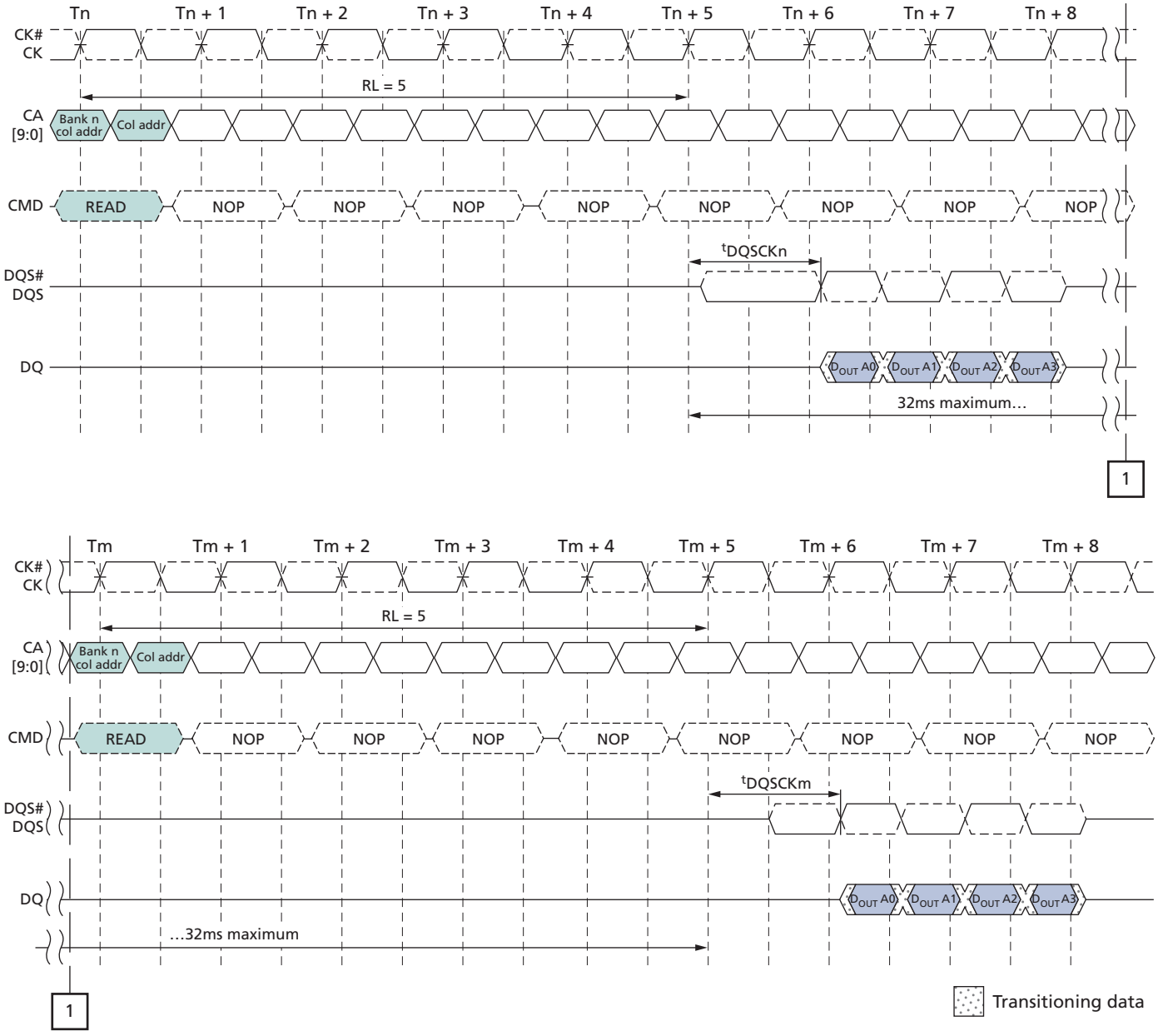
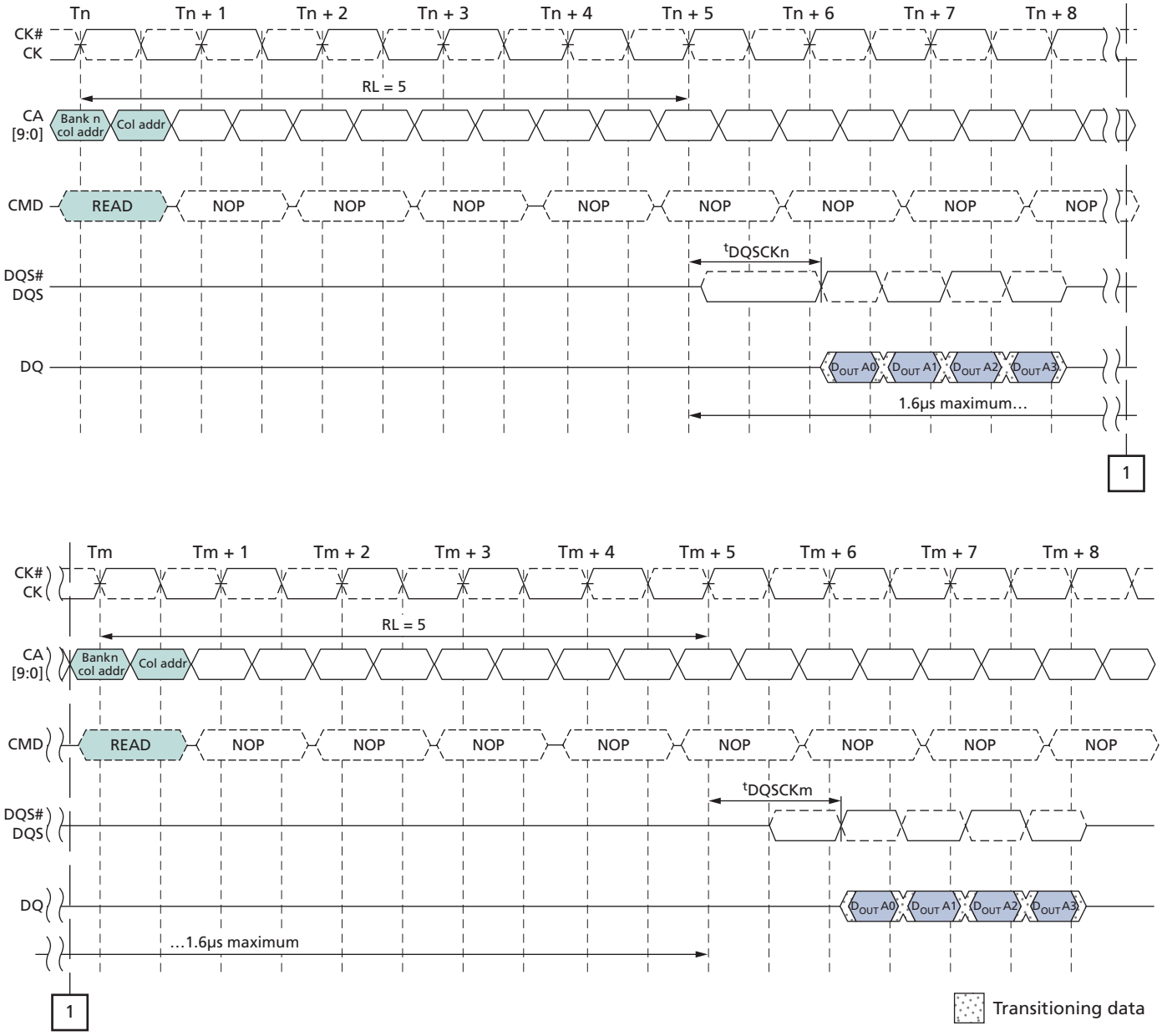


Figure 100: tDQSCKDL Timing



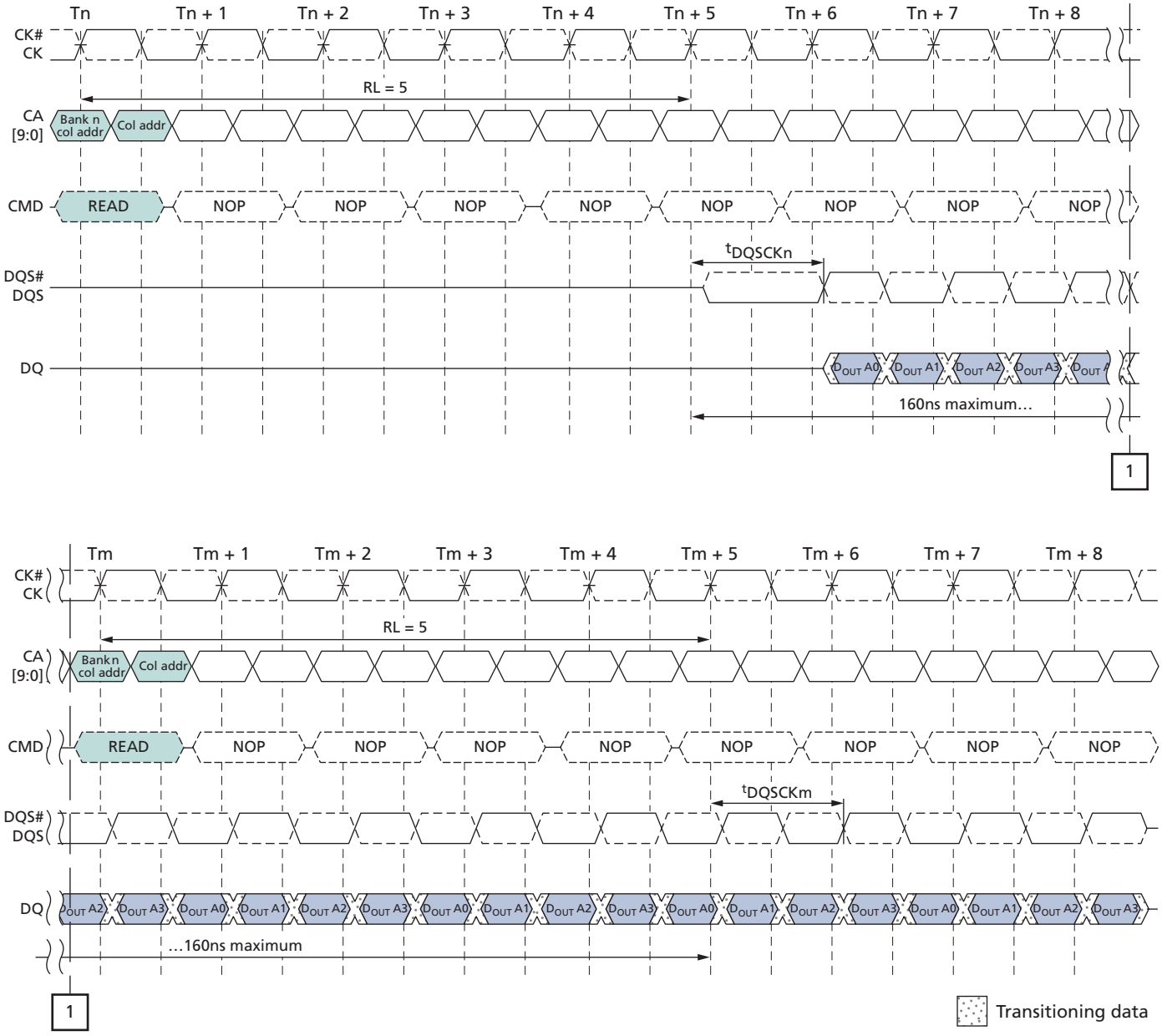
Notes:
1. tDQSCKDL = (tDQSCK*n* - tDQSCK*m*).
2. tDQSCKDL (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 32ms rolling window.

Figure 101: tDQSCKDM Timing



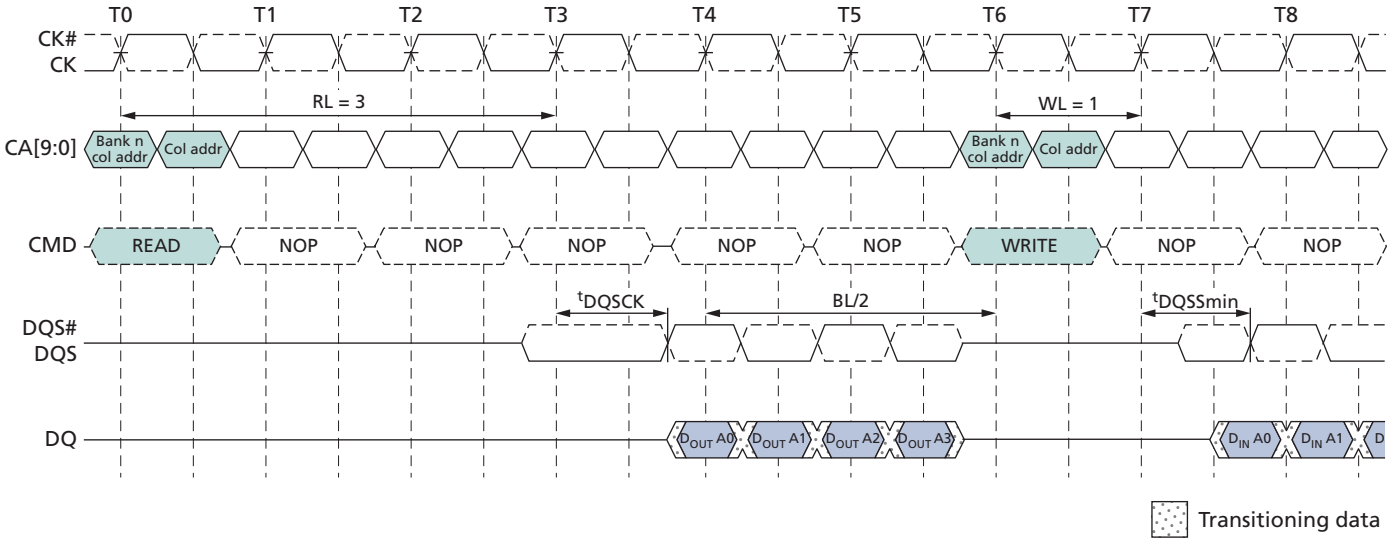
Notes:
1. tDQSCKDM = (tDQSCK*n* - tDQSCK*m*).
2. tDQSCKDM (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair within any 1.6µs rolling window.

Figure 102: tDQSCKDS Timing



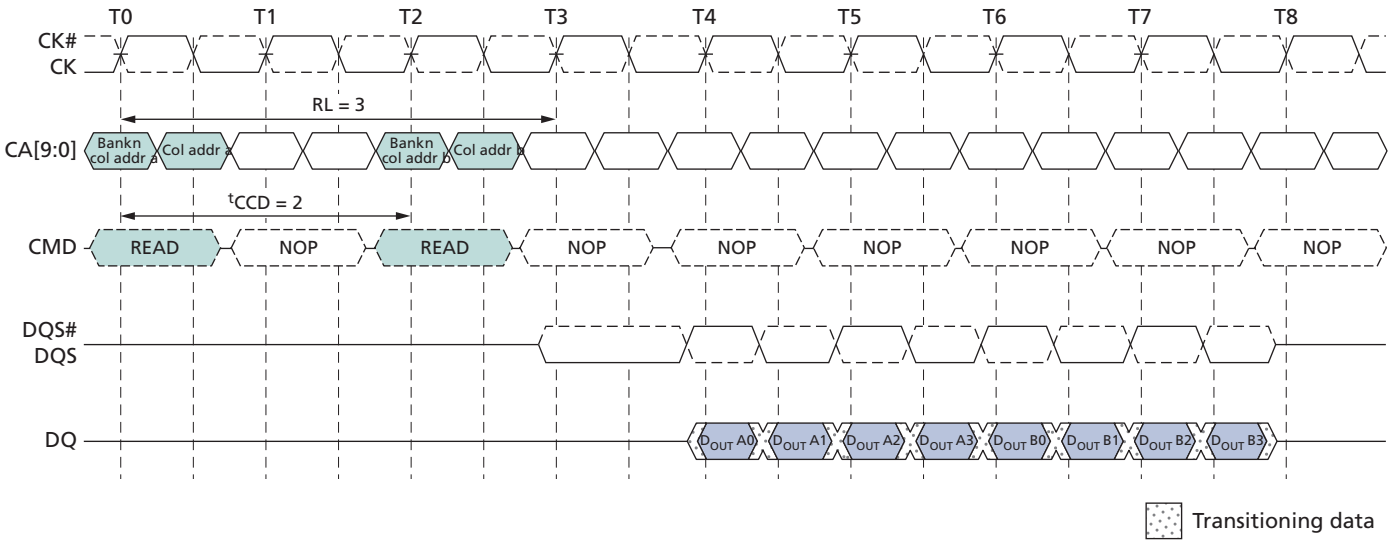
Notes:
1. tDQSCKDS = (tDQSCK*n* - tDQSCK*m*).
2. tDQSCKDS (MAX) is defined as the maximum of ABS (tDQSCK*n* - tDQSCK*m*) for any (tDQSCK*n*, tDQSCK*m*) pair for READs within a consecutive burst, within any 160ns rolling window.

Figure 103: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 1 - WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

Figure 104: Seamless Burst READ – RL = 3, BL = 4, ^{t}CCD = 2

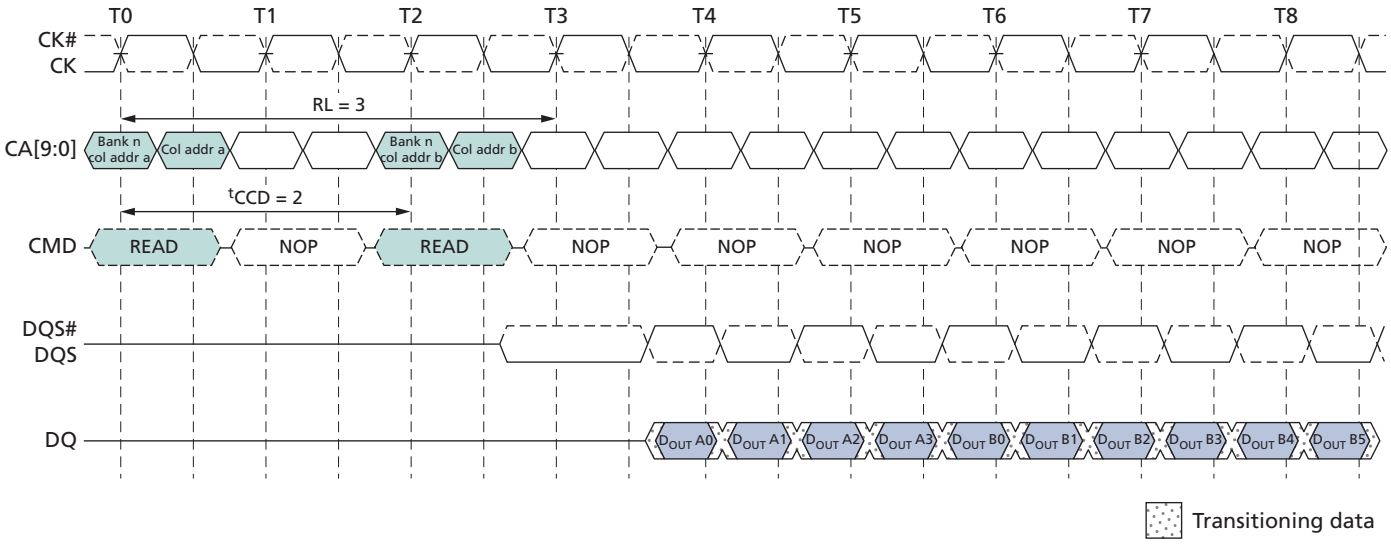


A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL = 16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

READs Interrupted by a READ

A burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that tCCD is met.

Figure 105: READ Burst Interrupt Example – RL = 3, BL = 8, tCCD = 2



Note: 1. READs can only be interrupted by other READs or the BST command.

Burst WRITE Command

The burst WRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW tWPRE prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued.

Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 106: Data Input (WRITE) Timing

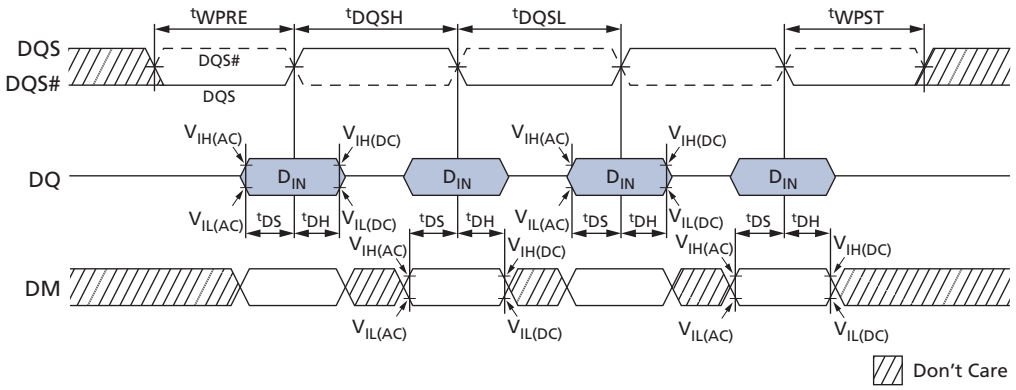


Figure 107: Burst WRITE – WL = 1, BL = 4

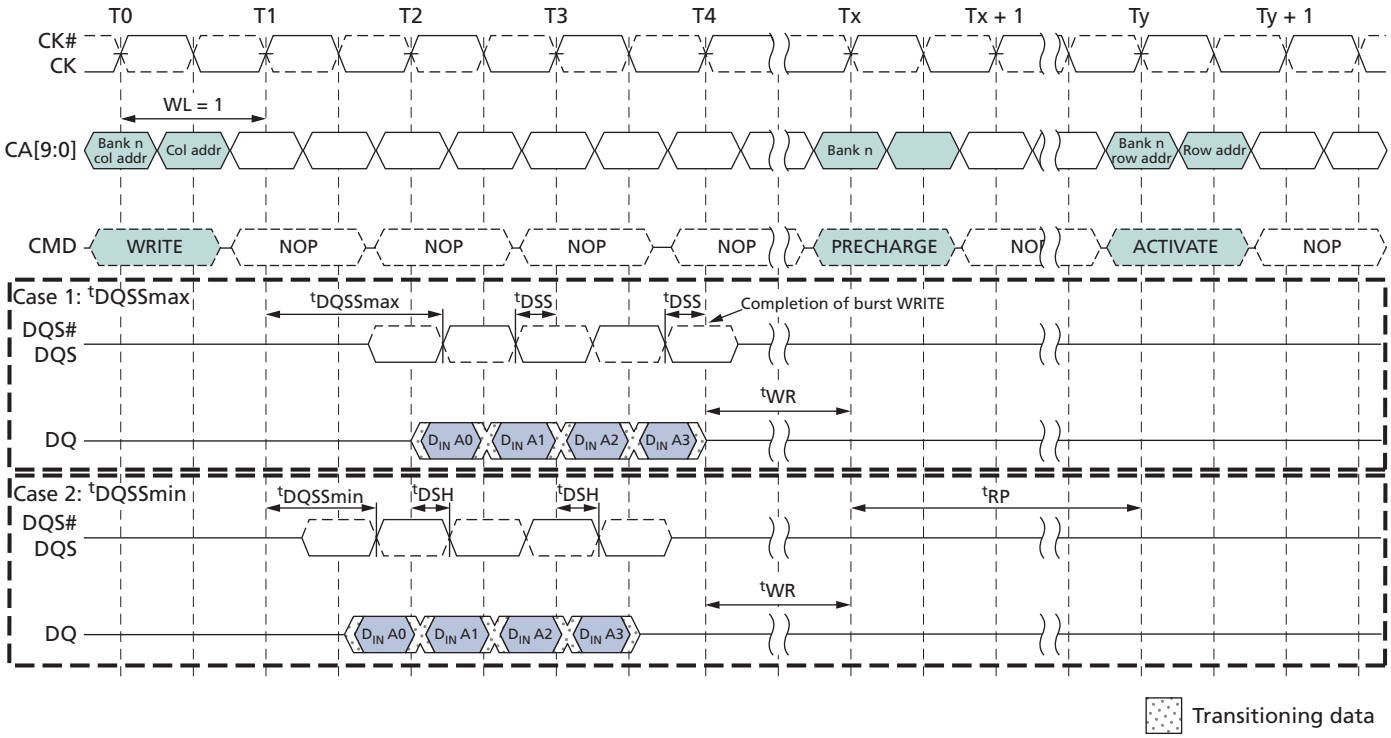
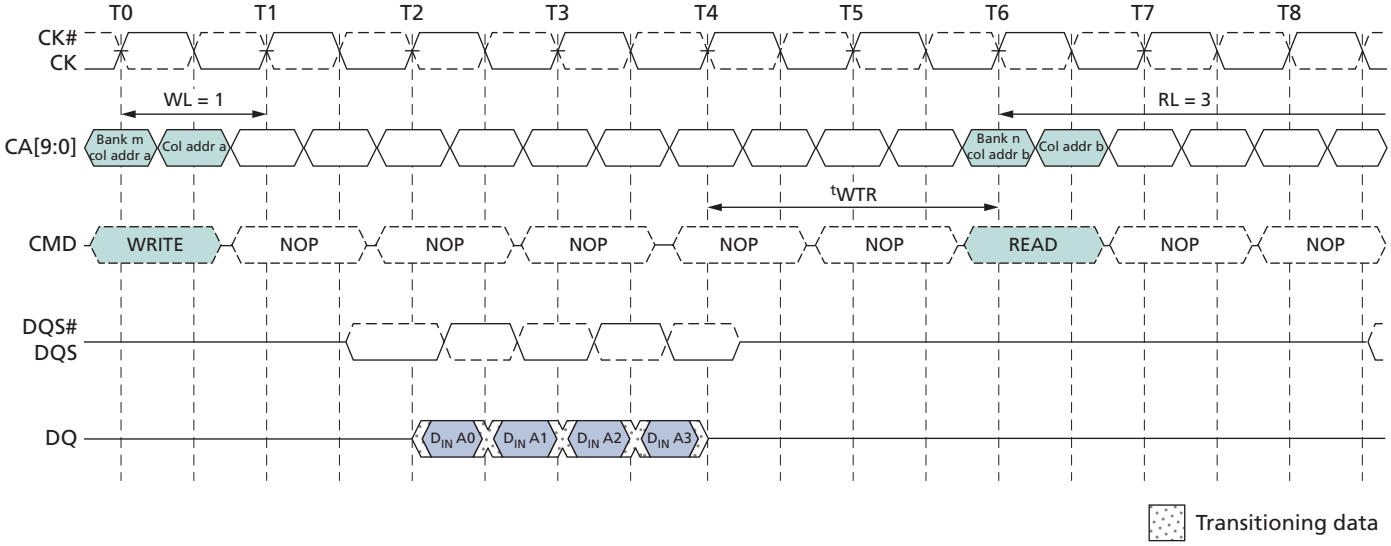
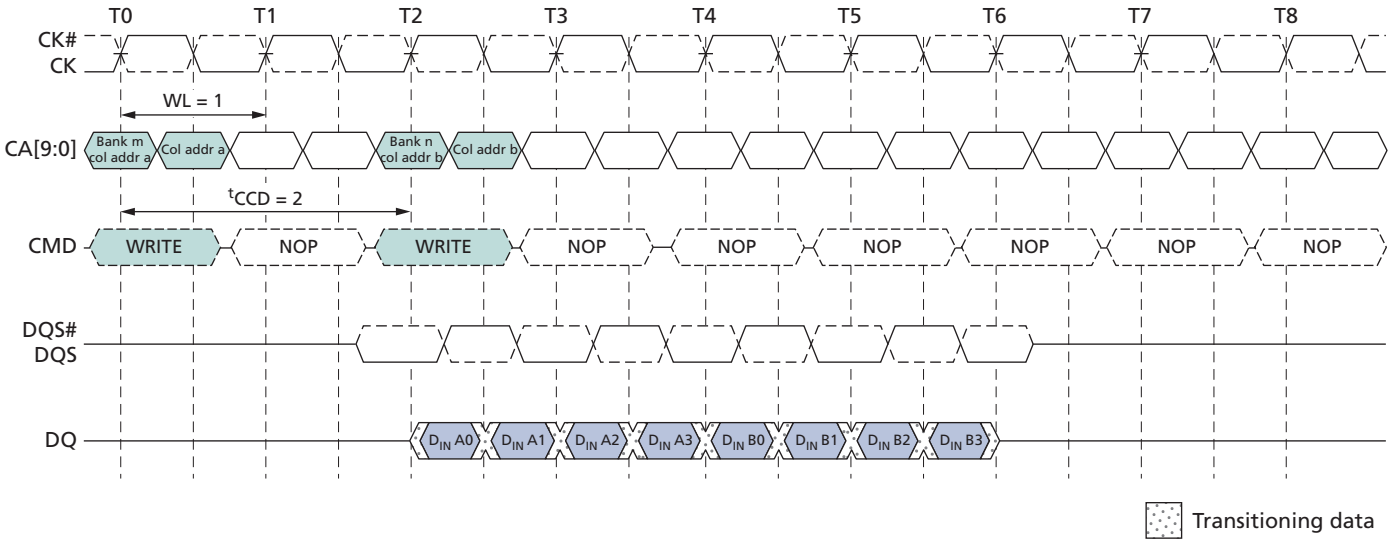


Figure 108: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)].
2. ^{t}WTR starts at the rising edge of the clock after the last valid input data.
3. If a WRITE burst is truncated with a BST command, the effective burst length of the truncated WRITE burst should be used as BL to calculate the minimum WRITE-to-READ delay.

Figure 109: Seamless Burst WRITE – WL = 1, BL = 4, ^{t}CCD = 2



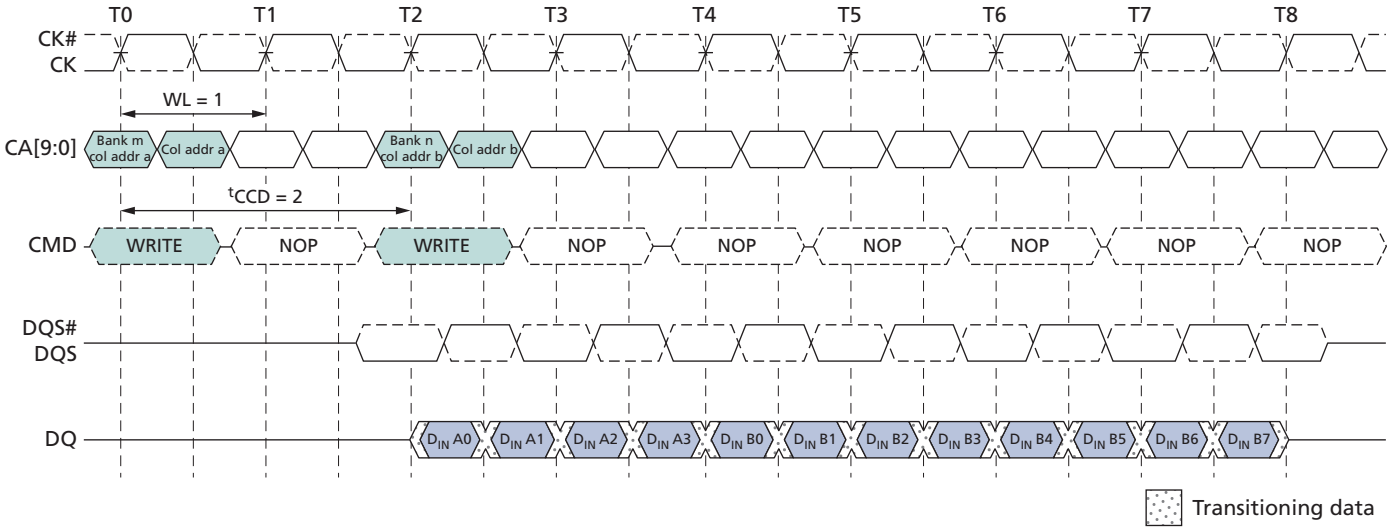
Note:
1. The seamless burst WRITE operation is supported by enabling a WRITE command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is supported for any activated bank.

WRITEs Interrupted by a WRITE

A burst WRITE can only be interrupted by another WRITE with a 4-bit burst boundary, provided that tCCD (MIN) is met.

A WRITE burst interrupt can occur on even clock cycles after the initial WRITE command, provided that tCCD (MIN) is met.

Figure 110: WRITE Burst Interrupt Timing – WL = 1, BL = 8, tCCD = 2



Notes:
1. WRITEs can only be interrupted by other WRITEs or the BST command.
2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

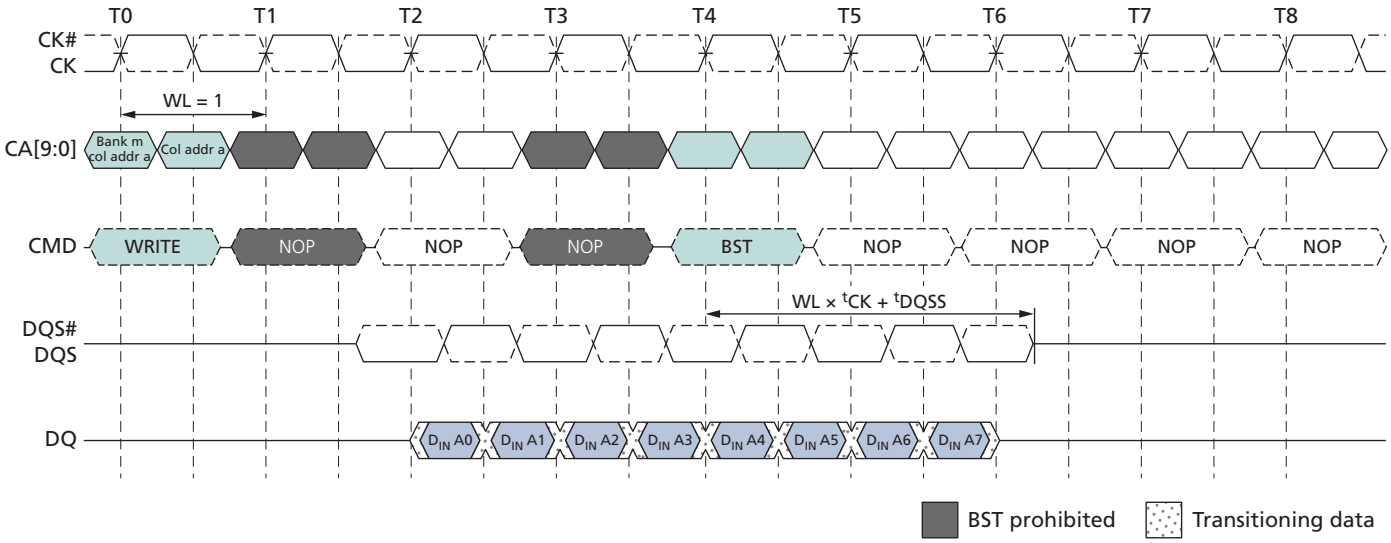
BURST TERMINATE Command

The BURST TERMINATE (BST) command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

- Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ-to-WRITE or WRITE-to-READ delay.
- The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock where the BST command is issued. The BST command truncates an ongoing WRITE burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.

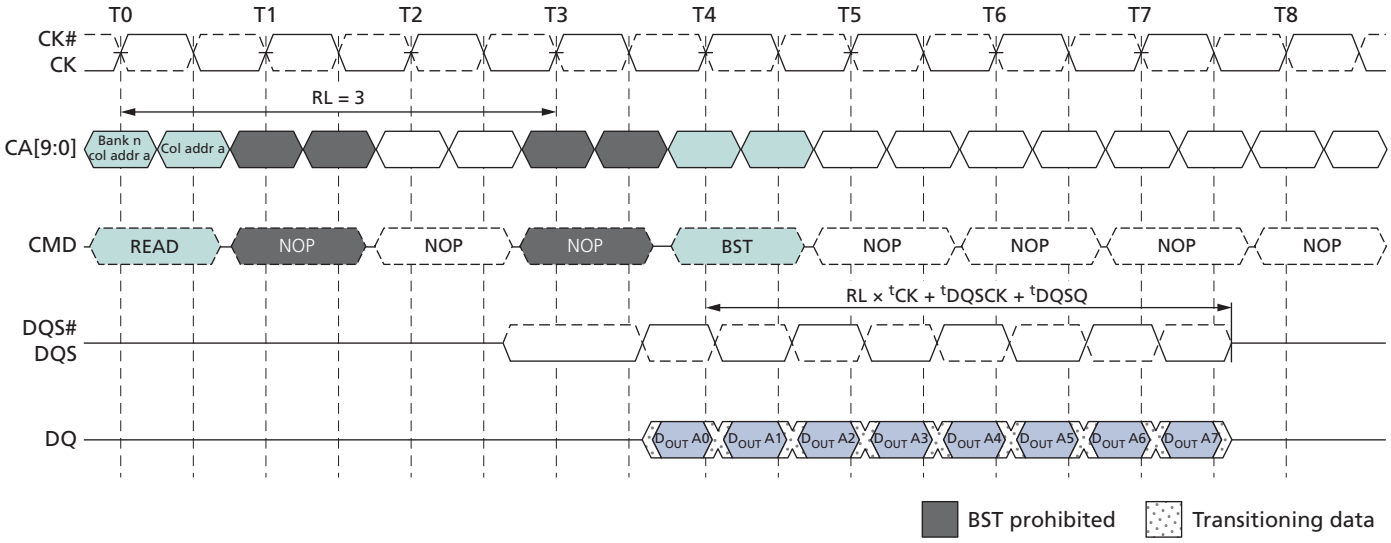
- The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

Figure 111: Burst WRITE Truncated by BST – WL = 1, BL = 16



Notes:
1. The BST command truncates an ongoing WRITE burst WL × ^{t}CK + ^{t}DQSS after the rising edge of the clock where the BST command is issued.
2. BST can only be issued an even number of clock cycles after the WRITE command.
3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Figure 112: Burst READ Truncated by BST – RL = 3, BL = 16



Notes:
1. The BST command truncates an ongoing READ burst (RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ) after the rising edge of the clock where the BST command is issued.
2. BST can only be issued an even number of clock cycles after the READ command.
3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Write Data Mask

On LPDDR2 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

Figure 113: Data Mask Timing

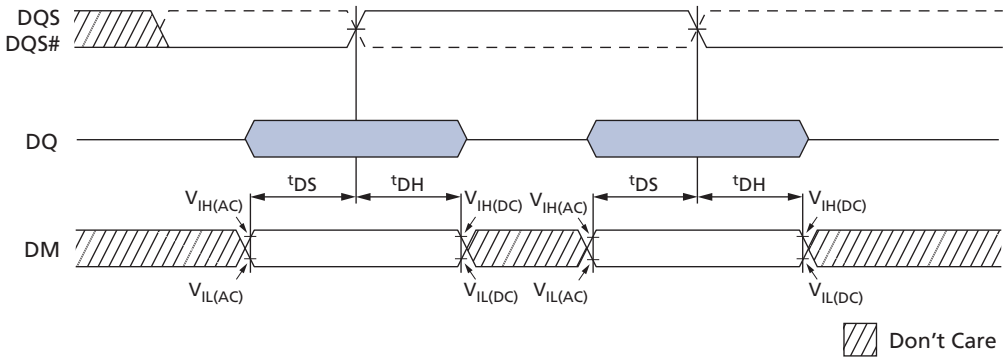
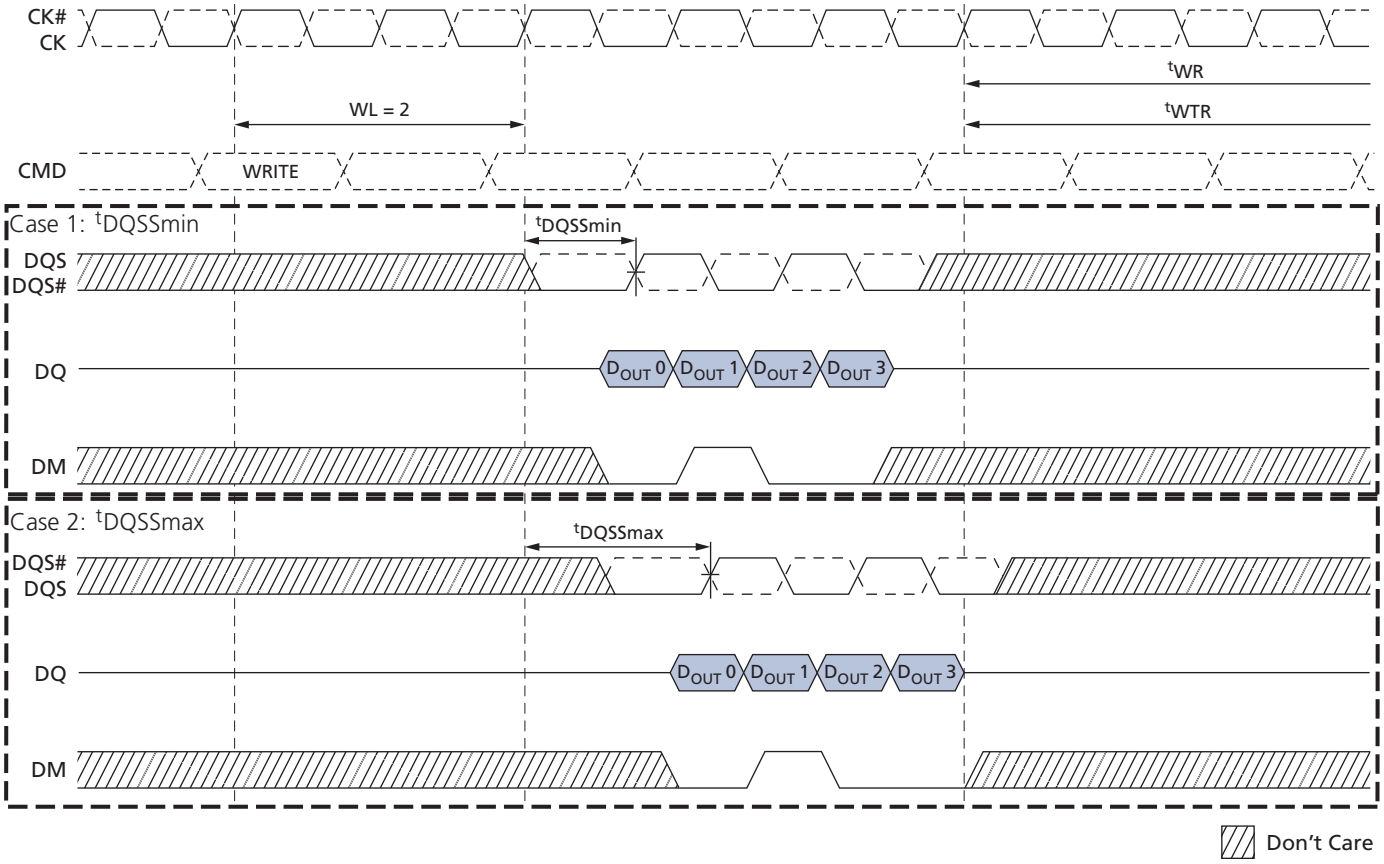


Figure 114: Write Data Mask – Second Data Bit Masked



Note: 1. For the data mask function, WL = 2, BL = 4 is shown; the second data bit is masked.

PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access ^{t}RPab after an all bank PRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE command is issued.

To ensure that 8-bank devices can meet the instantaneous current demand required to operate, the row precharge time (^{t}RP) for an all bank PRECHARGE in 8-bank devices (^{t}RPab) will be longer than the row precharge time for a single-bank PRECHARGE (^{t}RPpb). For 4-bank devices, ^{t}RPab is equal to ^{t}RPpb.

ACTIVATE to PRECHARGE timing is shown in ACTIVATE Command.

Table 78: Bank Selection for PRECHARGE by Address Bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-Bank Device	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks	All banks

READ Burst Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (^{t}RP) has elapsed. A PRECHARGE command cannot be issued until after ^{t}RAS is satisfied.

The minimum READ-to-PRECHARGE time (^{t}RTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command. ^{t}RTP begins BL/2 - 2 clock cycles after the READ command.

If the burst is truncated by a BST command, the effective BL value is used to calculate when ^{t}RTP begins.

Figure 115: READ Burst Followed by PRECHARGE – RL = 3, BL = 8, RU(^{t}RTP(MIN)/^{t}CK) = 2

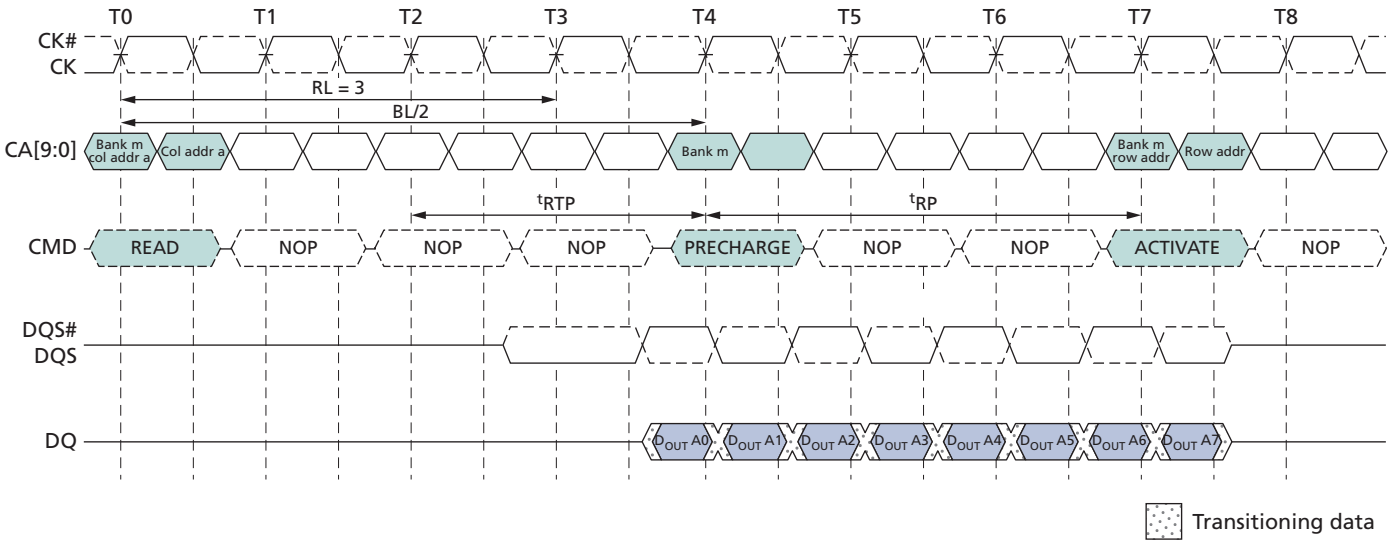
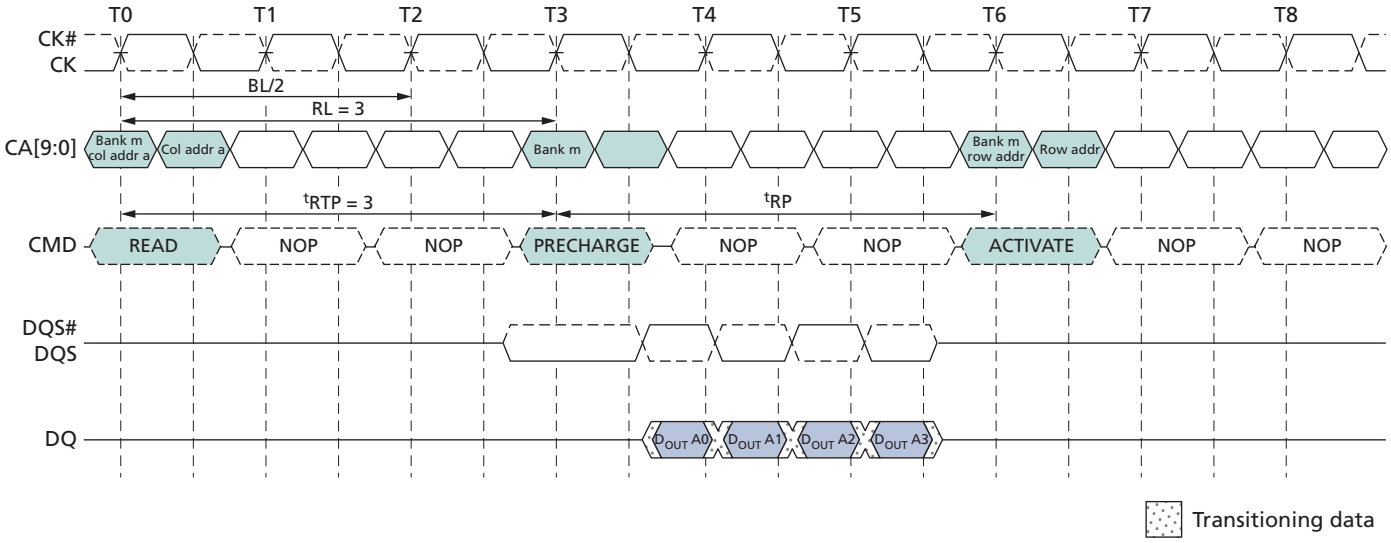


Figure 116: READ Burst Followed by PRECHARGE – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 3



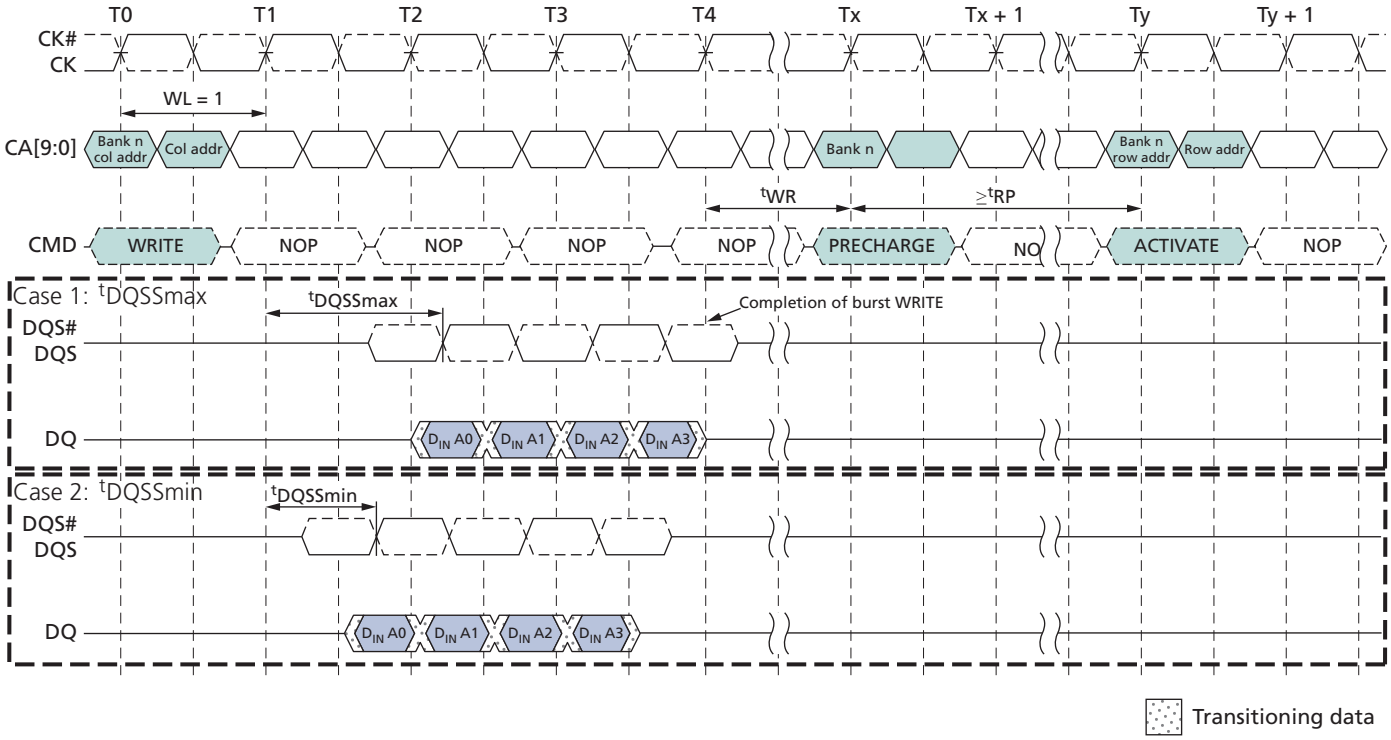
WRITE Burst Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. tWR delay is referenced from the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the tWR delay. For WRITE-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.

Figure 117: WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

READ Burst with Auto Precharge

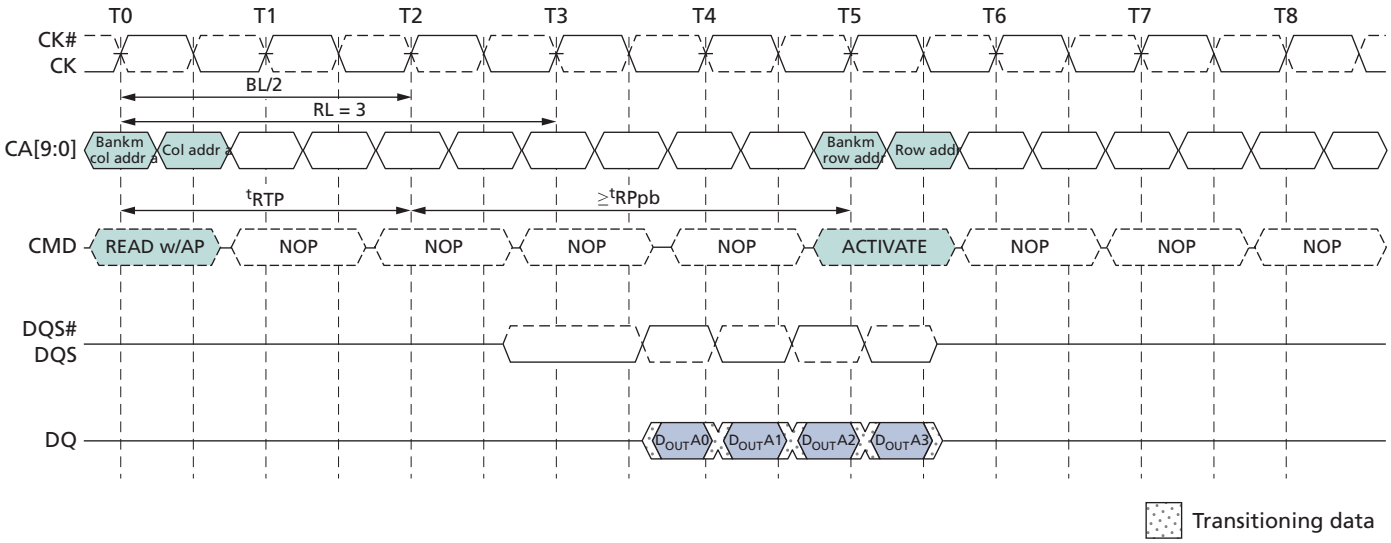
If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.

These devices start an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU(^{t}RTP/^{t}CK) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations, see the PRECHARGE and Auto Precharge Clarification table.

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Figure 118: READ Burst with Auto Precharge – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 2



WRITE Burst with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge tWR cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Figure 119: WRITE Burst with Auto Precharge – WL = 1, BL = 4

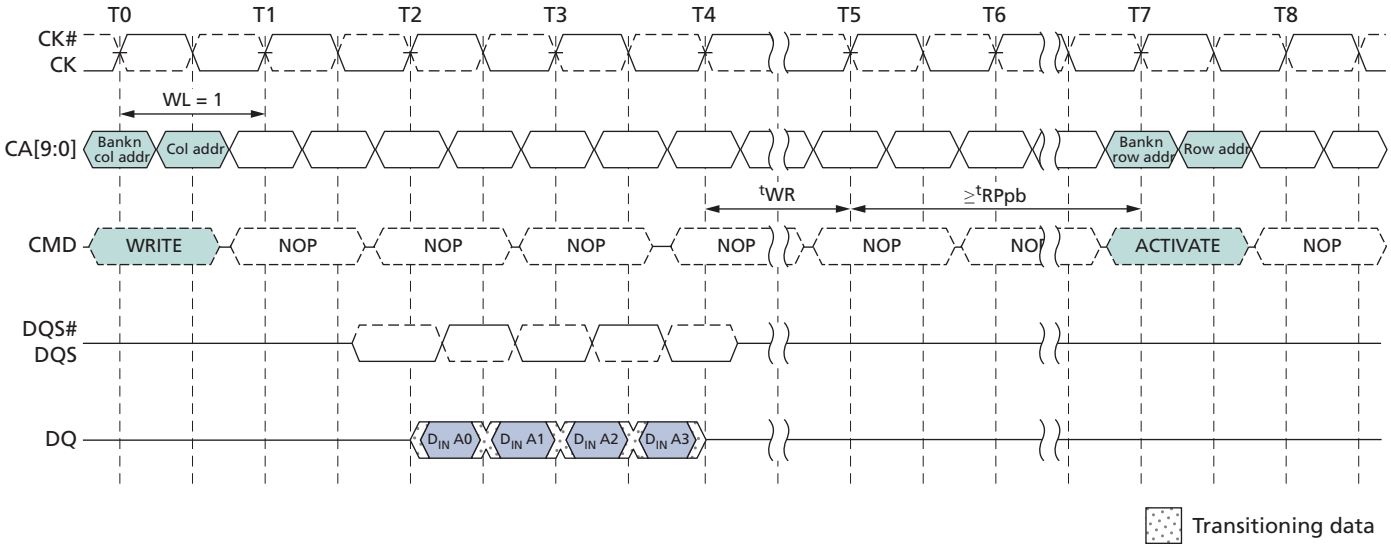


Table 79: PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	PRECHARGE to same bank as READ	BL/2 + MAX(2, RU(^{t}RTP/^{t}CK)) - 2	CLK	1
	PRECHARGE ALL	BL/2 + MAX(2, RU(^{t}RTP/^{t}CK)) - 2	CLK	1
BST	PRECHARGE to same bank as READ	1	CLK	1
	PRECHARGE ALL	1	CLK	1
READ w/AP	PRECHARGE to same bank as READ w/AP	BL/2 + MAX(2, RU(^{t}RTP/^{t}CK)) - 2	CLK	1, 2
	PRECHARGE ALL	BL/2 + MAX(2, RU(^{t}RTP/^{t}CK)) - 2	CLK	1
	ACTIVATE to same bank as READ w/AP	BL/2 + MAX(2, RU(^{t}RTP/^{t}CK)) - 2 + RU(^{t}RPpb/^{t}CK)	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCKmax/^{t}CK) - WL + 1	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	BL/2	CLK	3
WRITE	PRECHARGE to same bank as WRITE	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
BST	PRECHARGE to same bank as WRITE	WL + RU(^{t}WR/^{t}CK) + 1	CLK	1
	PRECHARGE ALL	WL + RU(^{t}WR/^{t}CK) + 1	CLK	1

Table 79: PRECHARGE and Auto Precharge Clarification (Continued)

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1, 2
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	ACTIVATE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RPpb/^{t}CK)	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	BL/2	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	CLK	3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1
PRECHARGE ALL	PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1

Notes:
1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command—either a one-bank PRECHARGE or PRECHARGE ALL—issued to that bank. The PRECHARGE period is satisfied after ^{t}RP, depending on the latest PRECHARGE command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock. Per-bank REFRESH is only supported in devices with eight banks.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank

- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command.

When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE commands

After an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command

Table 80: REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From	To	Notes
tRFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	

Table 80: REFRESH Command Scheduling Separation Requirements (Continued)

Symbol	Minimum Delay From	To	Notes
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed, so REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Mobile LPDDR2 devices provide significant flexibility in scheduling REFRESH commands as long as the required boundary conditions are met (see the ^{t}SRF Definition figure).

In the most straightforward implementations, a REFRESH command should be scheduled every ^{t}REFI. In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 1Gb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by ^{t}REFBW), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: ^{t}REFW - (R/8) × ^{t}REFBW = ^{t}REFW - R × 4 × ^{t}RFCab.

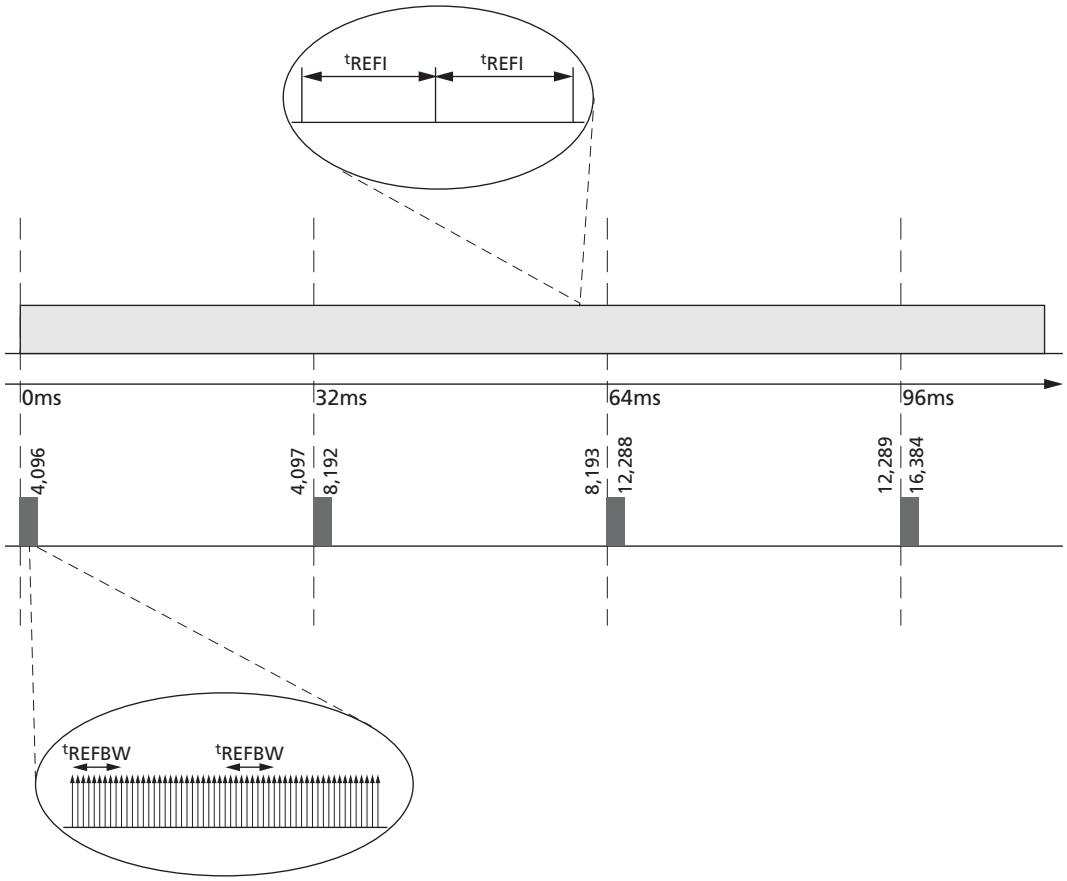
For example, a 1Gb device at $T_C \leq 85^{\circ}C$ can be operated without a refresh for up to 32ms - 4096 × 4 × 130ns ≈ 30ms.

Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in *every* rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in the Supported Transition from Repetitive REFRESH Burst figure. If this transition occurs immediately after the burst refresh phase, all rolling ^{t}REFW intervals will meet the minimum required number of REFRESH commands.

A nonsupported transition is shown in Figure 122 (page 176). In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling ^{t}REFW intervals, the minimum number of REFRESH commands is not satisfied.

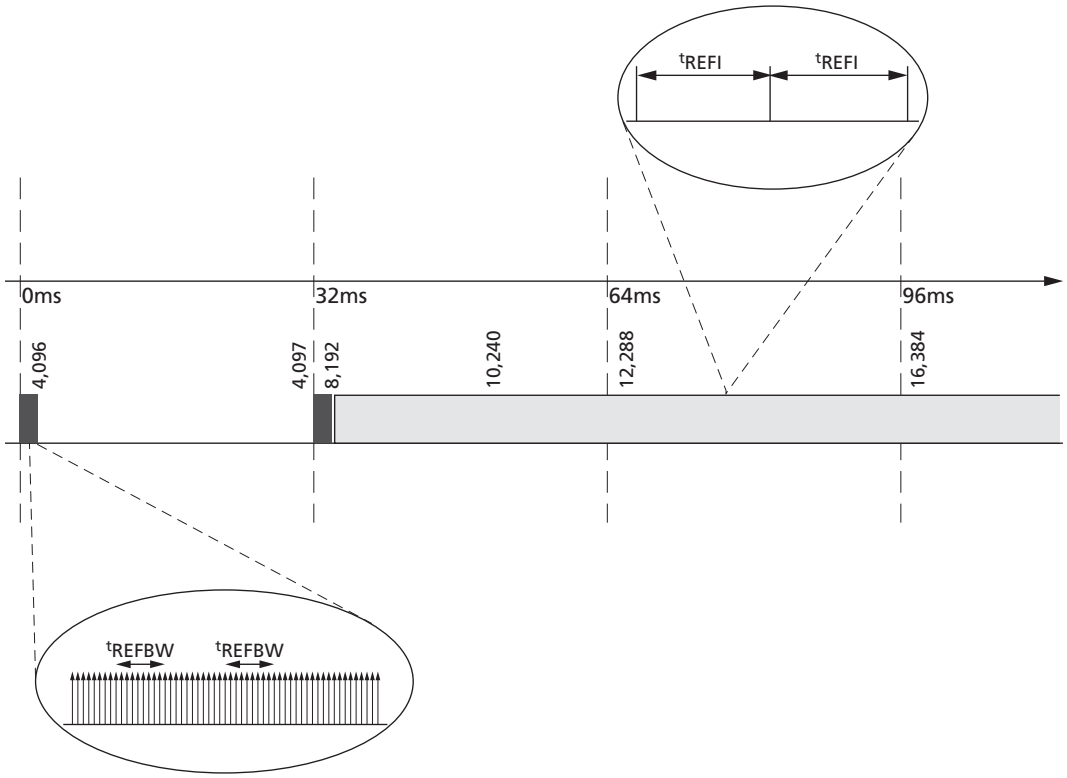
Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed. Micron recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see the Recommended Self Refresh Entry and Exit figure).

Figure 120: Regular Distributed Refresh Pattern



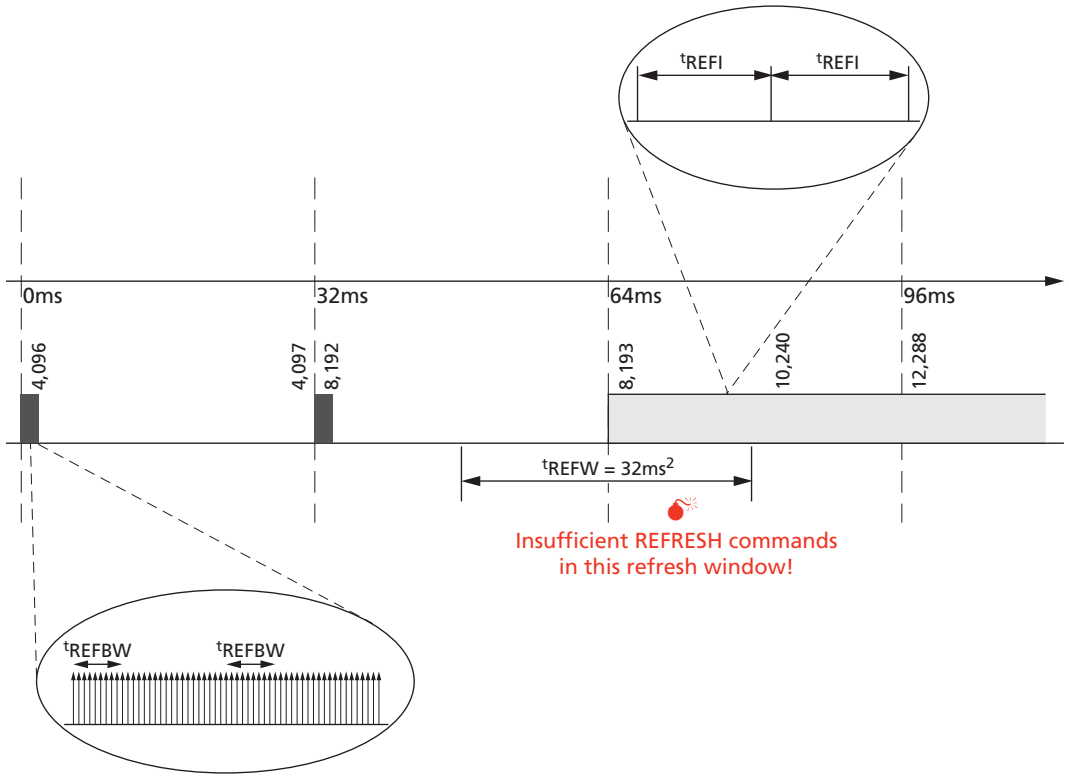
Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
2. As an example, in a 1Gb LPDDR2 device at $T_C \leq 85^{\circ}C$, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 30ms without any REFRESH command.

Figure 121: Supported Transition from Repetitive REFRESH Burst



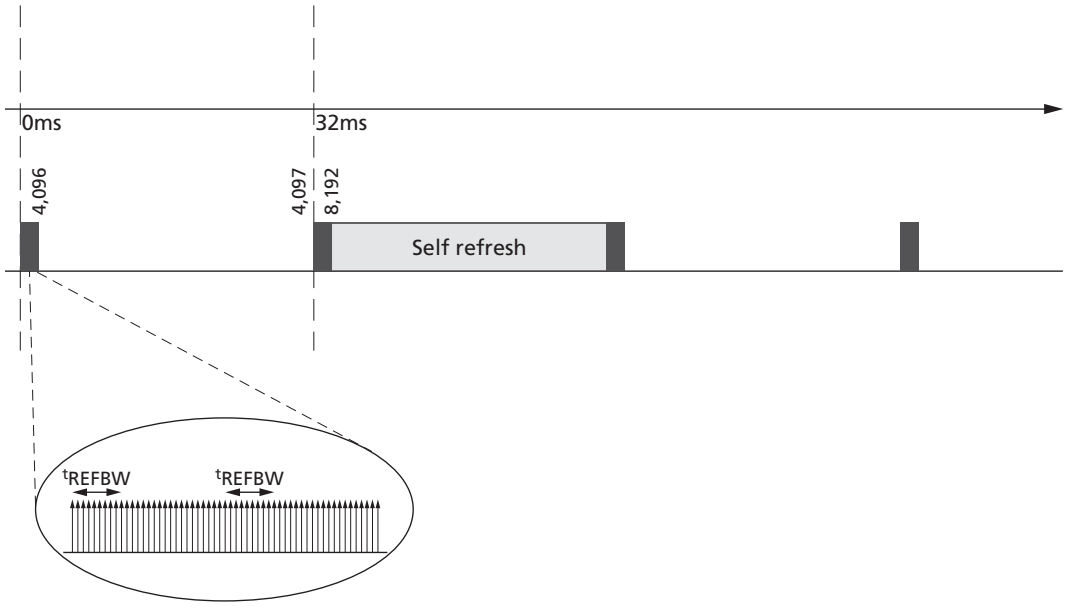
Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
2. As an example, in a 1Gb LPDDR2 device at $T_C \leq 85^{\circ}C$, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 30ms without any REFRESH command.

Figure 122: Nonsupported Transition from Repetitive REFRESH Burst



Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
2. There are only ≈ 2048 REFRESH commands in the indicated tREFW window. This does not provide the required minimum number of REFRESH commands (R).

Figure 123: Recommended Self Refresh Entry and Exit



Note: 1. In conjunction with a burst/pause refresh pattern.

REFRESH Requirements

1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (^{t}REFW = 32 ms @ MR4[2:0] = 011 or $T_C \leq 85^{\circ}C$). For actual values per density and the resulting average refresh interval (^{t}REFI), see Refresh Requirements.

For ^{t}REFW and ^{t}REFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REFab commands can be issued in any rolling ^{t}REFBW (^{t}REFBW = 4 × 8 × ^{t}RFCab). This condition does not apply if REFpb commands are used.

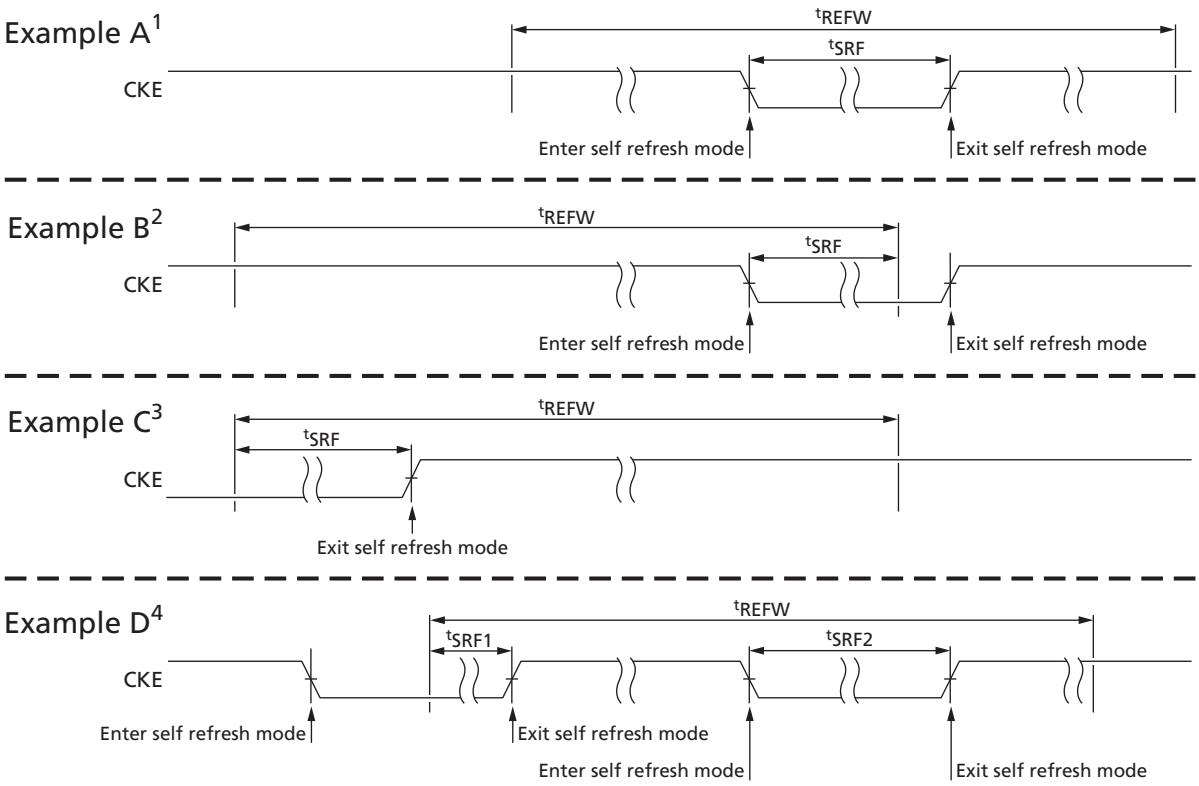
3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

$$R' = RU\left(\frac{t_{SRF}}{t_{REFI}}\right) = R - RU\left(R \times \frac{t_{SRF}}{t_{REFW}}\right)$$

Where RU represents theround-up function.

Figure 124: tSRF Definition



Notes:
1. Time in self refresh mode is fully enclosed in the refresh window (tREFW).
2. At self refresh entry.
3. At self refresh exit.
4. Several intervals in self refresh during one tREFW interval. In this example, tSRF = tSRF1 + tSRF2.

Figure 125: All-Bank REFRESH Operation

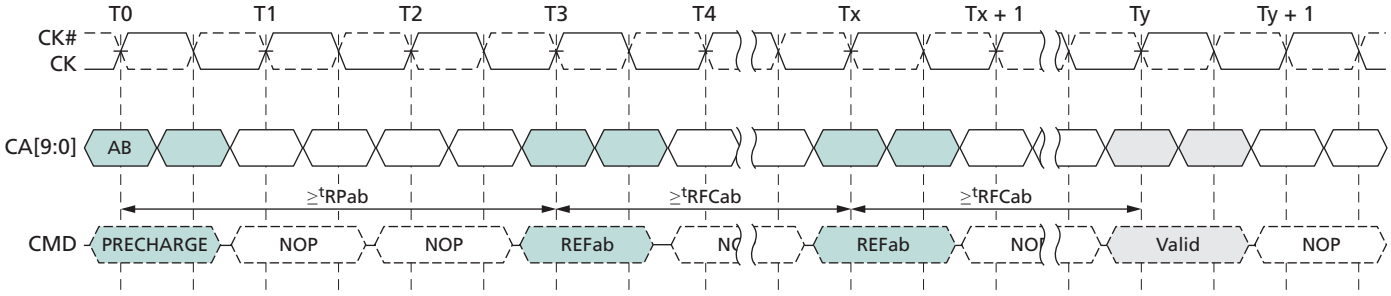
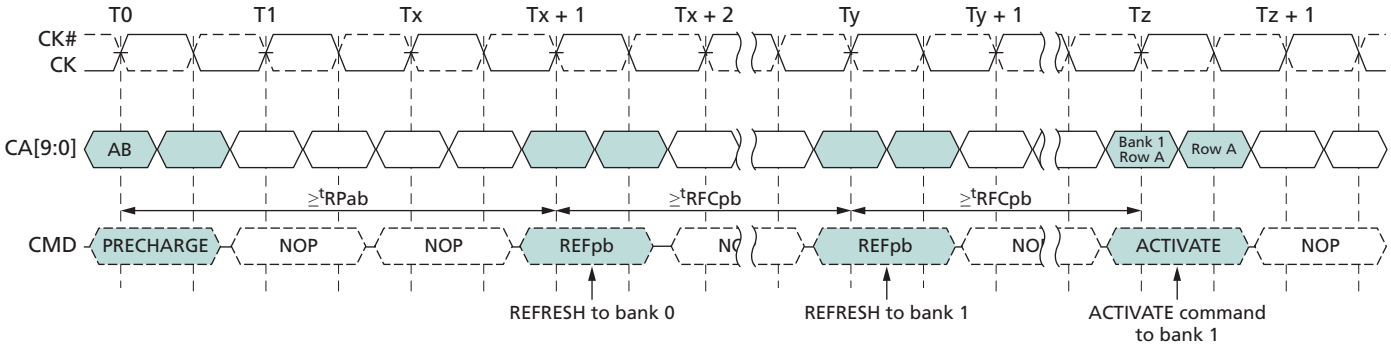


Figure 126: Per-Bank REFRESH Operation



Notes:
1. Prior to T0, the REFpb bank counter points to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the ^{t}RFCpb period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock.

CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. A NOP command must be driven in the clock cycle following the SELF REFRESH command. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.

Mobile LPDDR2 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range. See Table 95 (page 213) for details.

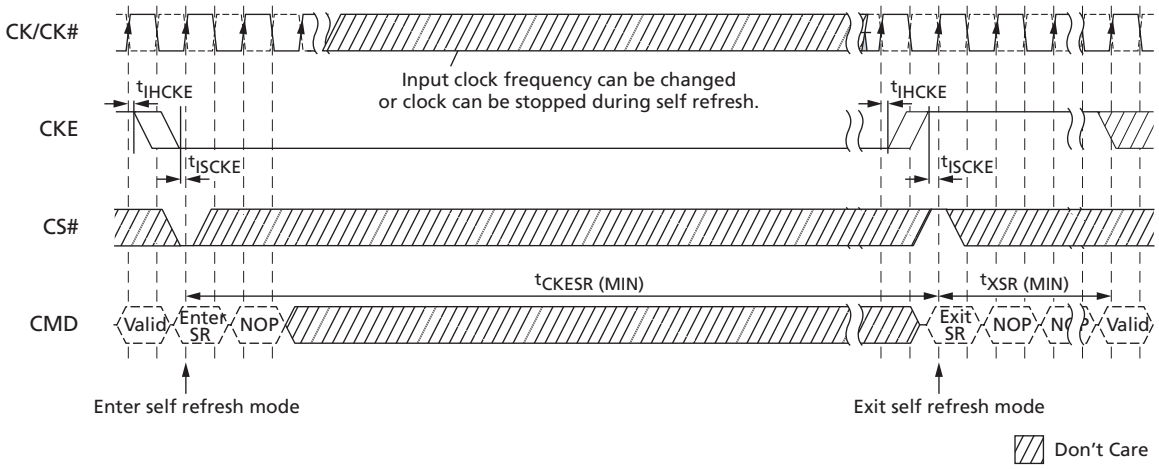
After the device has entered self refresh mode, all external signals other than CKE are "Don't Care." For proper self refresh operation, power supply pins (V_{DD1}, V_{DD2}, V_{DDQ}, and V_{DDCA}) must be at valid levels. V_{DDQ} can be turned off during self refresh. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting self refresh, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see the Single-Ended AC and DC Input Levels for DQ and DM table). V_{REFDQ} can be at any level between 0 and V_{DDQ}; V_{REFCA} can be at any level between 0 and V_{DDCA} during self refresh.

Before exiting self refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (see AC and DC Logic Input Measurement Levels for Single-Ended Signals (page 216)). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during ^{t}CKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least ^{t}CKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (^{t}XSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout ^{t}XSR. NOP commands must be registered on each rising clock edge during ^{t}XSR.

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

Figure 127: SELF REFRESH Operation



Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
2. The device must be in the all banks idle state prior to entering self refresh mode.
3. ^{t}XSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after ^{t}XSR is satisfied. NOPs must be issued during ^{t}XSR.

Partial-Array Self Refresh – Bank Masking

Devices in densities of 64Mb–512Mb are comprised of four banks; densities of 1Gb and higher are comprised of eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks. For bank masking bit assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as "unmasked." When a bank mask bit is unmasked, the array

space being refreshed within that bank is determined by the programmed status of the segment mask bits.

Partial-Array Self Refresh – Segment Masking

Programming segment mask bits is similar to programming bank mask bits. For densities 1Gb and higher, eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment mask bits up to eight bits. For densities less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as "masked," a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment masking scheme can be used in place of or in combination with a bank masking scheme. Each segment mask bit setting is applied across all banks. For segment masking bit assignments, see the tables noted above.

Table 81: Bank and Segment Masking Example

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
Segment 0	0	–	M	–	–	–	–	–	M
Segment 1	0	–	M	–	–	–	–	–	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	–	M	–	–	–	–	–	M
Segment 4	0	–	M	–	–	–	–	–	M
Segment 5	0	–	M	–	–	–	–	–	M
Segment 6	0	–	M	–	–	–	–	–	M
Segment 7	1	M	M	M	M	M	M	M	M

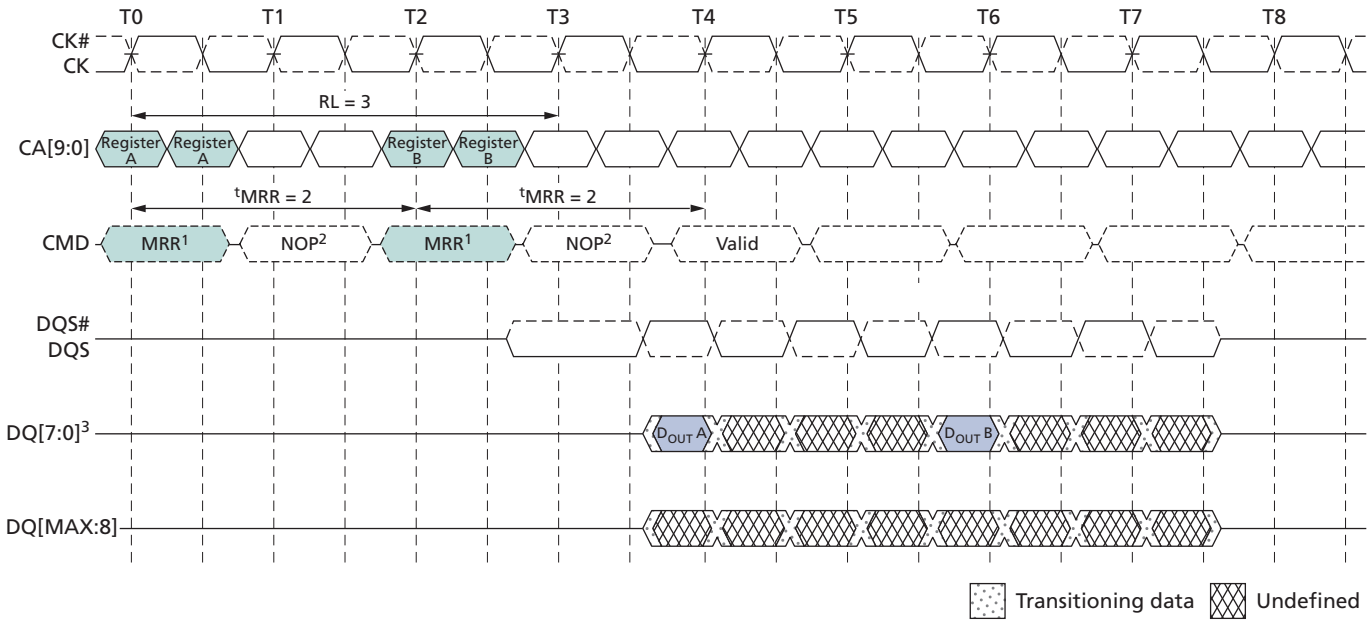
Note: 1. This table provides values for an 8-bank device with REFRESH operations masked to banks 1 and 7, and segments 2 and 7.

MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the Data Calibration Pattern Description table. All DQS are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (^{t}MRR) is two clock cycles.

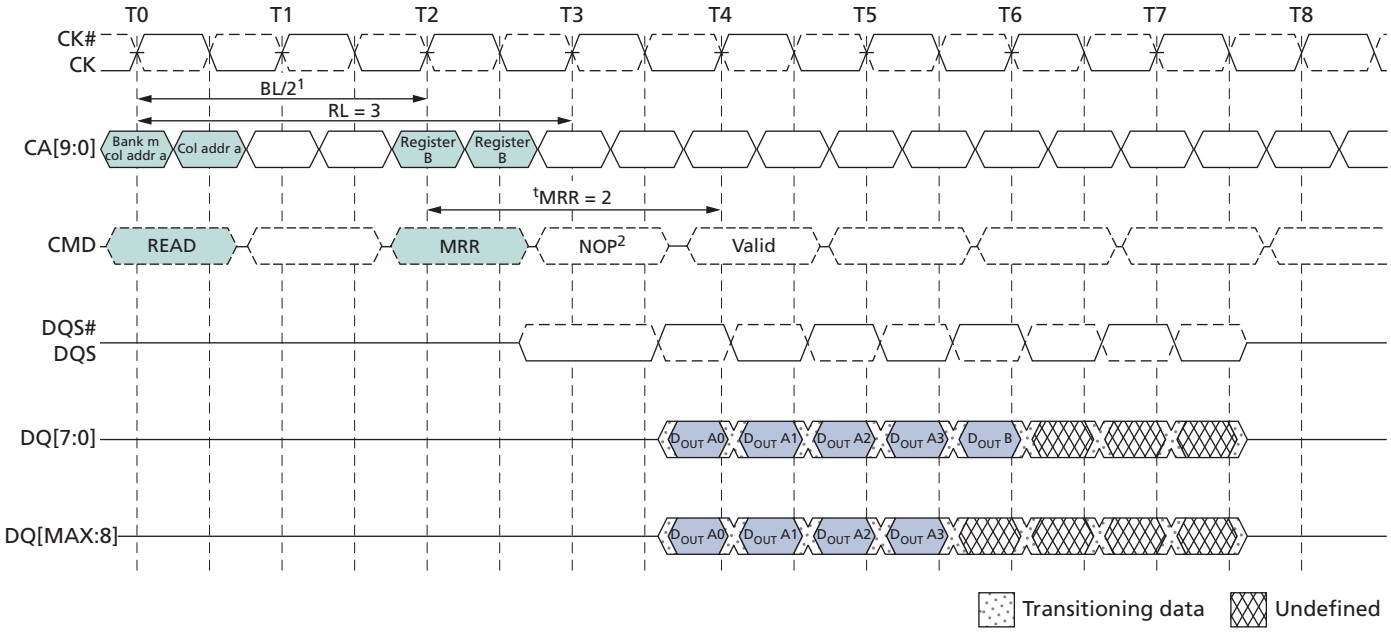
Figure 128: MRR Timing – RL = 3, ^{t}MRR = 2



Notes:
1. MRRs to DQ calibration registers MR32 and MR40 are described in Data Calibration.
2. Only the NOP command is supported during ^{t}MRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum MRR to write latency is RL + RU(^{t}DQSCKmax/^{t}CK) + 4/2 + 1 - WL clock cycles.
5. Minimum MRR to MRW latency is RL + RU(^{t}DQSCKmax/^{t}CK) + 4/2 + 1 clock cycles.

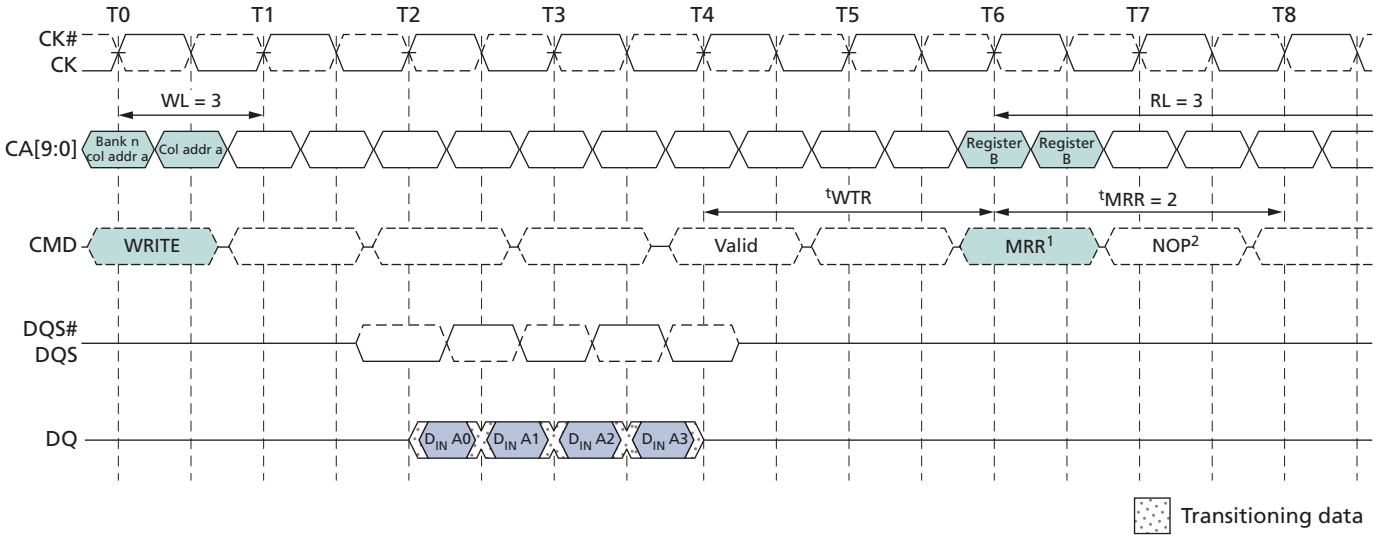
READ bursts and WRITE bursts cannot be truncated by MRR. Following a READ command, the MRR command must not be issued before BL/2 clock cycles have completed. Following a WRITE command, the MRR command must not be issued before WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK) clock cycles have completed. If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the BL value.

Figure 129: READ to MRR Timing – RL = 3, ^{t}MRR = 2



Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Only the NOP command is supported during ^{t}MRR.

Figure 130: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)].
2. Only the NOP command is supported during ^{t}MRR.

Temperature Sensor

Mobile LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see Operating Temperature Range table).

Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than ^{t}TSI.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see table noted above). For example, T_{CASE} could be above 85°C when MR4[2:0] equals 011b.

To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.

Table 82: Temperature Sensor Definitions and Operating Conditions

Parameter	Description	Symbol	Min/Max	Value	Unit
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2˚C	TempGradient	MAX	System-dependent	˚C/s
MR4 READ interval	Time period between MR4 READs from the system	ReadInterval	MAX	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of MR4	^{t}TSI	MAX	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	MAX	System-dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	˚C

Mobile LPDDR2 devices accommodate the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

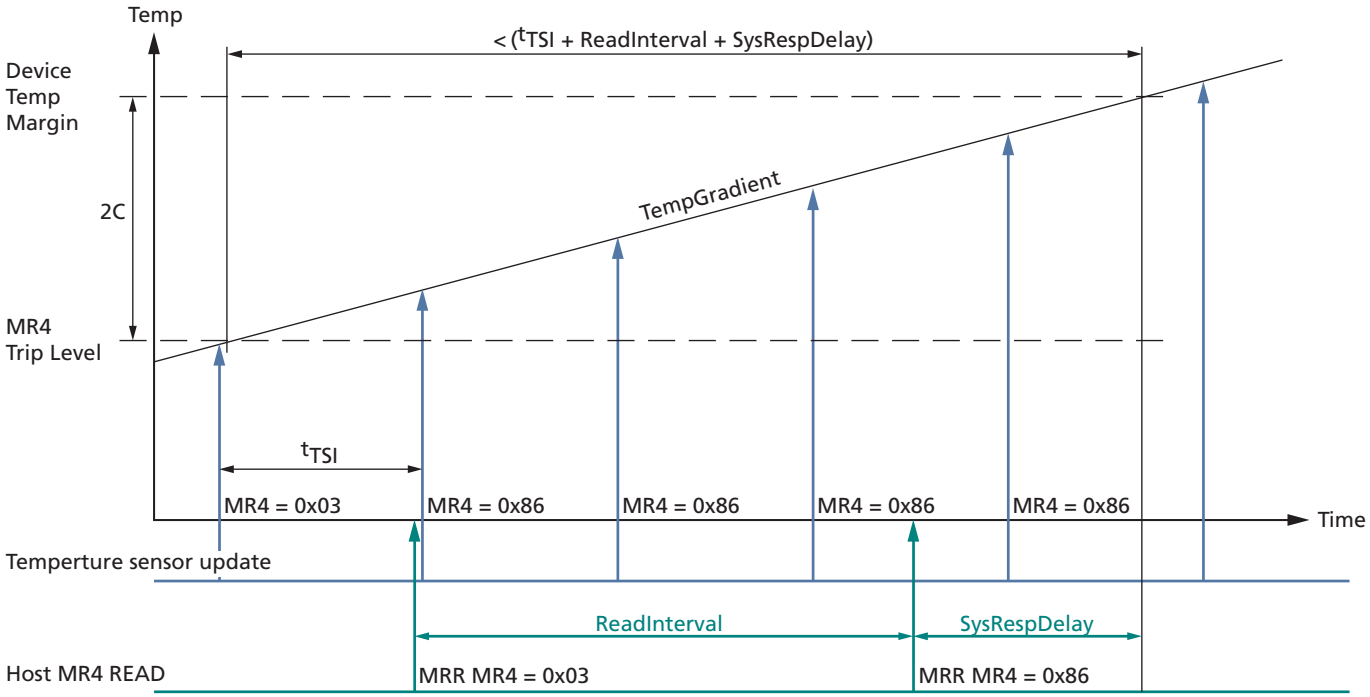
$$\text{TempGradient} \times (\text{ReadInterval} + {}^{t}\text{TSI} + \text{SysRespDelay}) \leq 2°\text{C}$$

For example, if TempGradient is 10˚C/s and the SysRespDelay is 1ms:

$$\frac{10°\text{C}}{\text{s}} \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2°\text{C}$$

In this case, ReadInterval must not exceed 167ms.

Figure 131: Temperature Sensor Timing

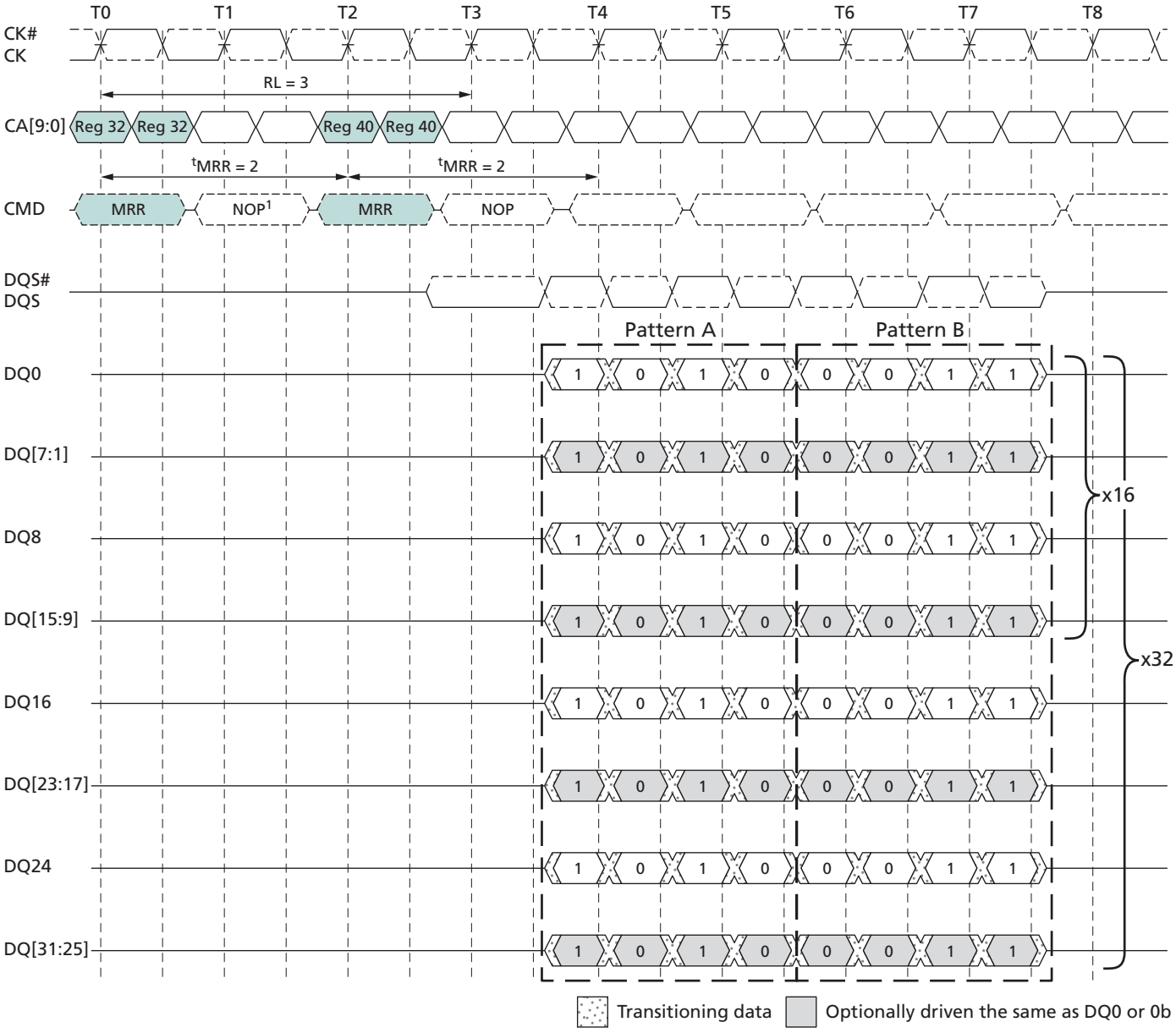


DQ Calibration

Mobile LPDDR2 devices feature a DQ calibration function that outputs one of two pre-defined system timing calibration patterns. For x16 devices, pattern A (MRR to MRR32), and pattern B (MRR to MRR40), will return the specified pattern on DQ0 and DQ8; x32 devices return the specified pattern on DQ0, DQ8, DQ16, and DQ24.

For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Figure 132: MR32 and MR40 DQ Calibration Timing – RL = 3, tMRR = 2



Note: 1. Only the NOP command is supported during tMRR.

Table 83: Data Calibration Pattern Description

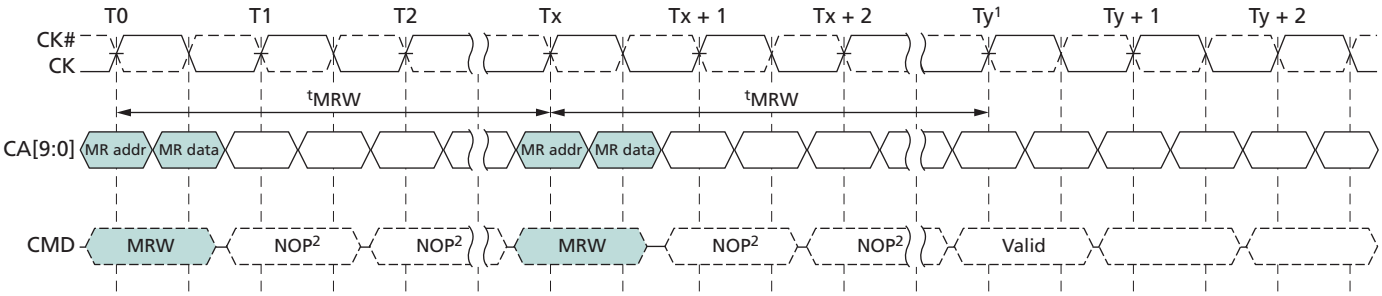
Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Reads to MR40 return DQ calibration pattern B

MODE REGISTER WRITE Command

The MODE REGISTER WRITE (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f–CA0f, CA9r–CA4r. The data to be written to the mode register is contained in CA9f–CA2f. The MRW command period is defined by ^{t}MRW. MRWs to read-only registers have no impact on the functionality of the device.

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

Figure 133: MODE REGISTER WRITE Timing – RL = 3, ^{t}MRW = 5



Notes: 1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during ^{t}MRW.

Table 84: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
	MRW (RESET)	Resetting, device auto initialization	All banks idle
Bank(s) active	MRR	Reading mode register, bank(s) idle	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see 2. RESET Command under Power-Up (page 137)). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during ^{t}INIT4. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed.

For MRW RESET timing, see Figure 93 (page 139).

MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration. To achieve tighter tolerances, proper ZQ calibration must be performed.

There are four ZQ calibration commands and related timings: ^{t}ZQINIT, ^{t}ZQRESET, ^{t}ZQCL, and ^{t}ZQCS. ^{t}ZQINIT is used for initialization calibration; ^{t}ZQRESET is used for resetting ZQ to the default output impedance; ^{t}ZQCL is used for long calibration(s); and ^{t}ZQCS is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.

ZQINIT must be performed for LPDDR2 devices. ZQINIT provides an output impedance accuracy of ±15%. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15%. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

ZQRESET resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within ^{t}ZQCS for all speed bins, assuming the maximum sensitivities specified in Table 115 and Table 116 (page 231) are met. The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.

Mobile LPDDR2 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ_{correction}}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where T_{sens} = MAX ($dR_{ON}dT$) and V_{sens} = MAX ($dR_{ON}dV$) define temperature and voltage sensitivities.

For example, if T_{sens} = 0.75%/°C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1°C/sec, and $V_{driftrate}$ = 15 mV/sec, then the interval between ZQCS commands is calculated as:

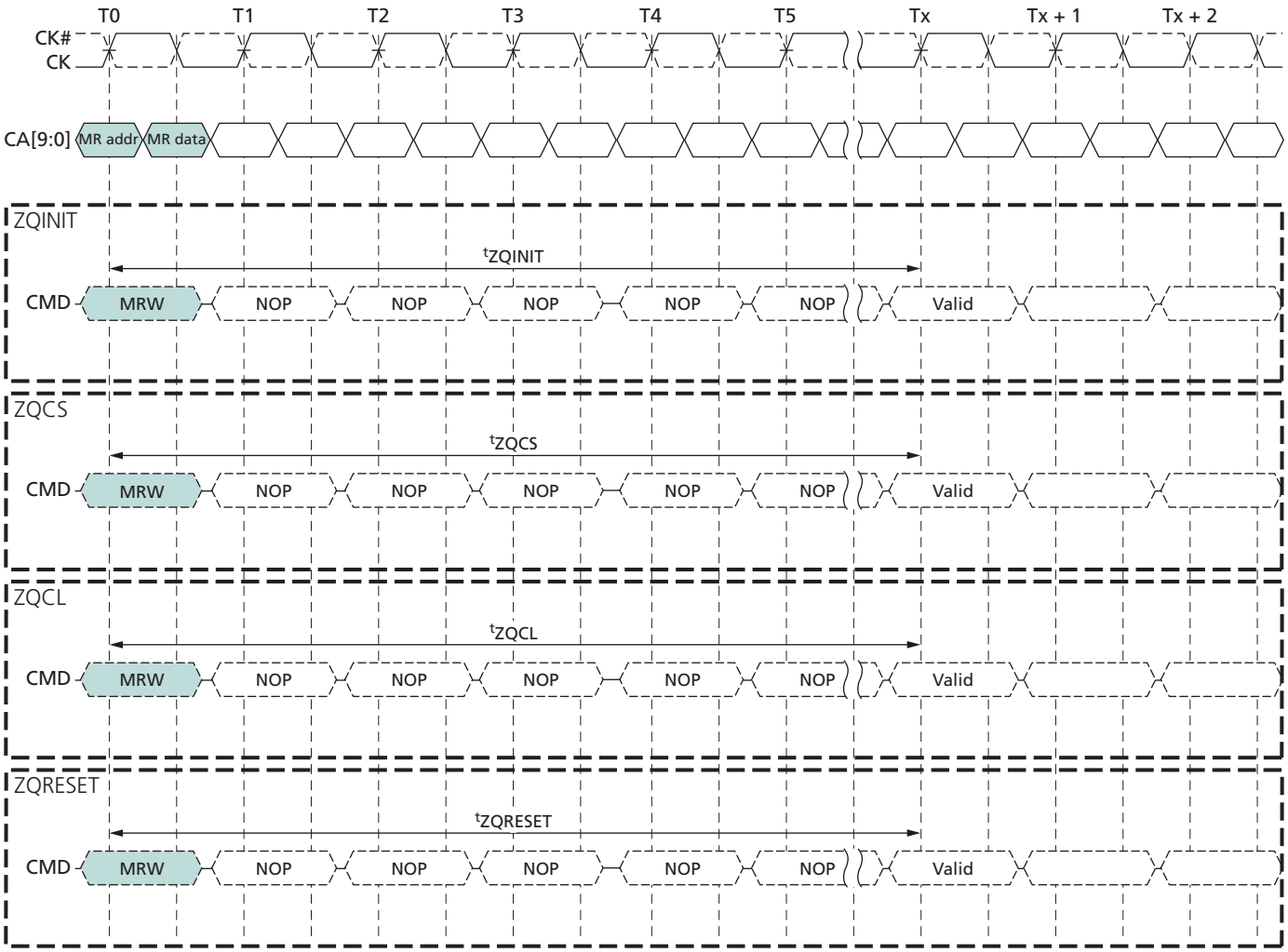
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods (^{t}ZQINIT, ^{t}ZQCL, or ^{t}ZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent ^{t}ZQINIT, ^{t}ZQCS, and ^{t}ZQCL overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to V_{DDCA}. In this situation, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Figure 134: ZQ Timings



Notes:
1. Only the NOP command is supported during ZQ calibrations.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm (±1% tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS# is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down I_{DD} specification will not be applied until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

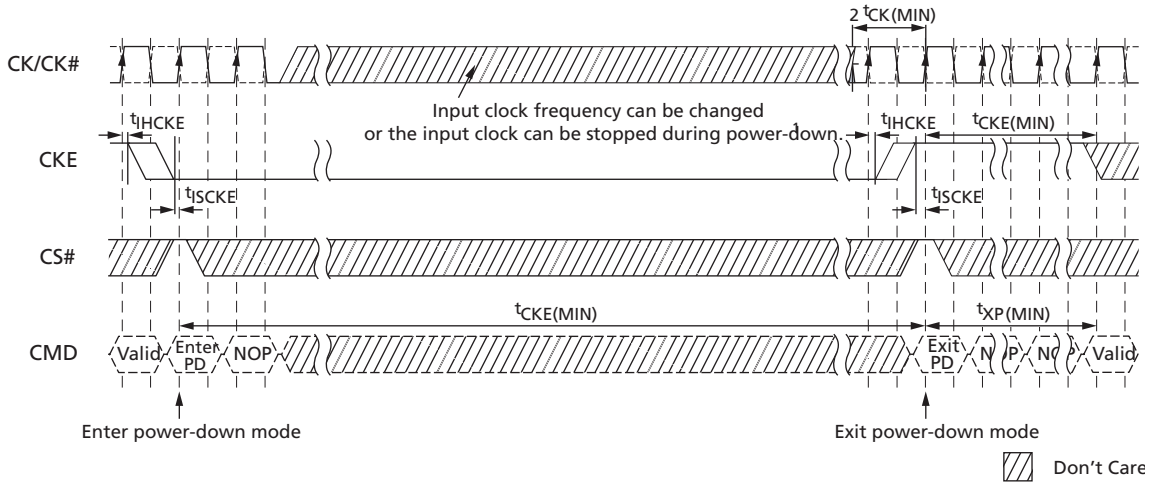
Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until ^{t}CKE is satisfied. V_{REFCA} must be maintained at a valid level during power-down.

V_{DDQ} can be turned off during power-down. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting power-down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions).

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in REFRESH Command.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until ^{t}CKE is satisfied. A valid, executable command can be applied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing section.

Figure 135: Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 136: CKE Intensive Environment

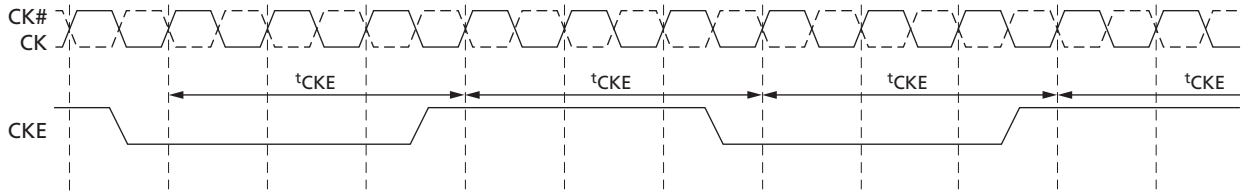
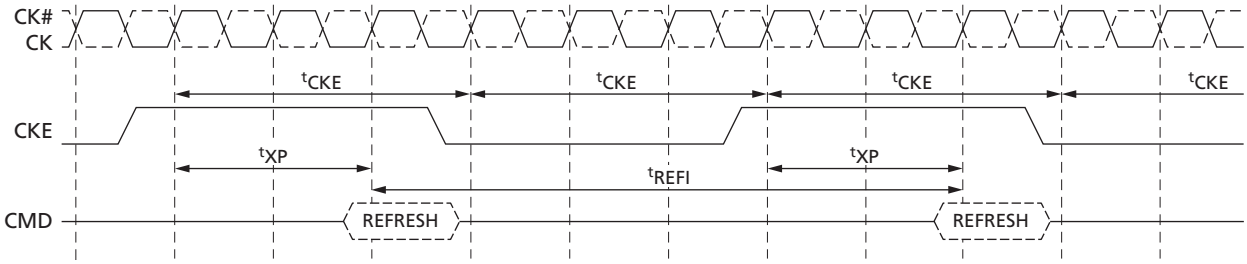
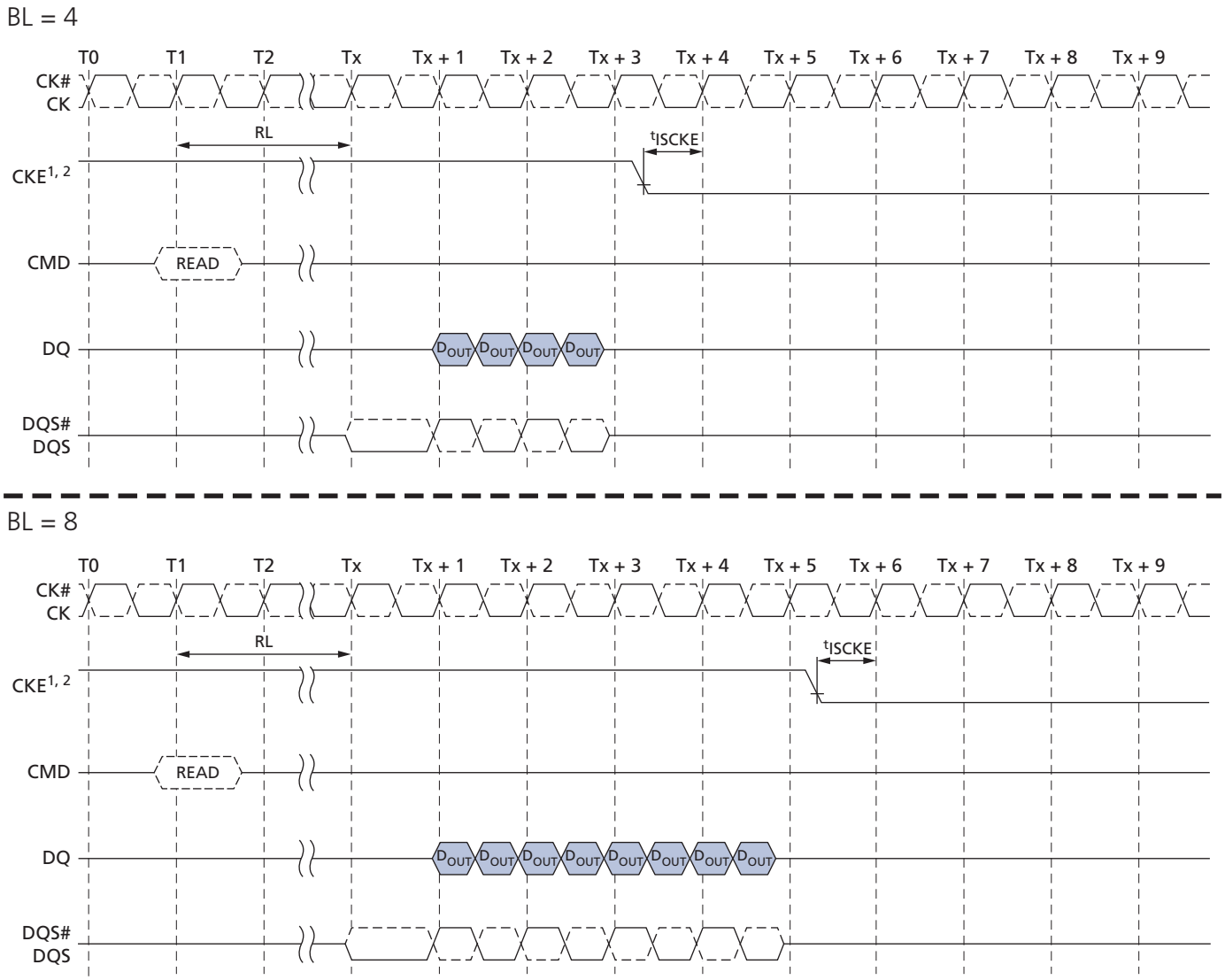


Figure 137: REFRESH-to-REFRESH Timing in CKE Intensive Environments



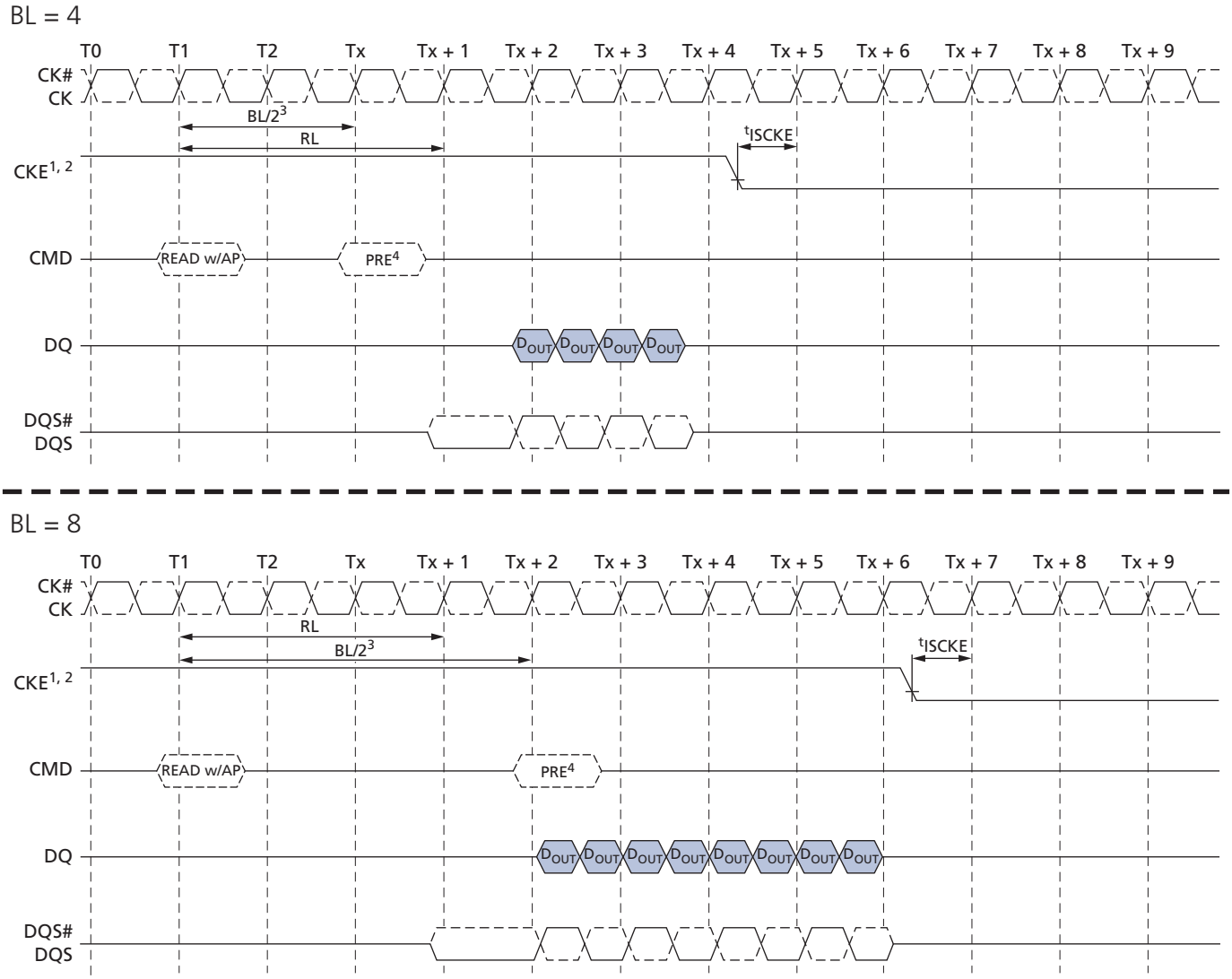
Note: 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure 138: READ to Power-Down Entry



Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at (RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 1) clock cycles after the clock on which the READ command is registered.

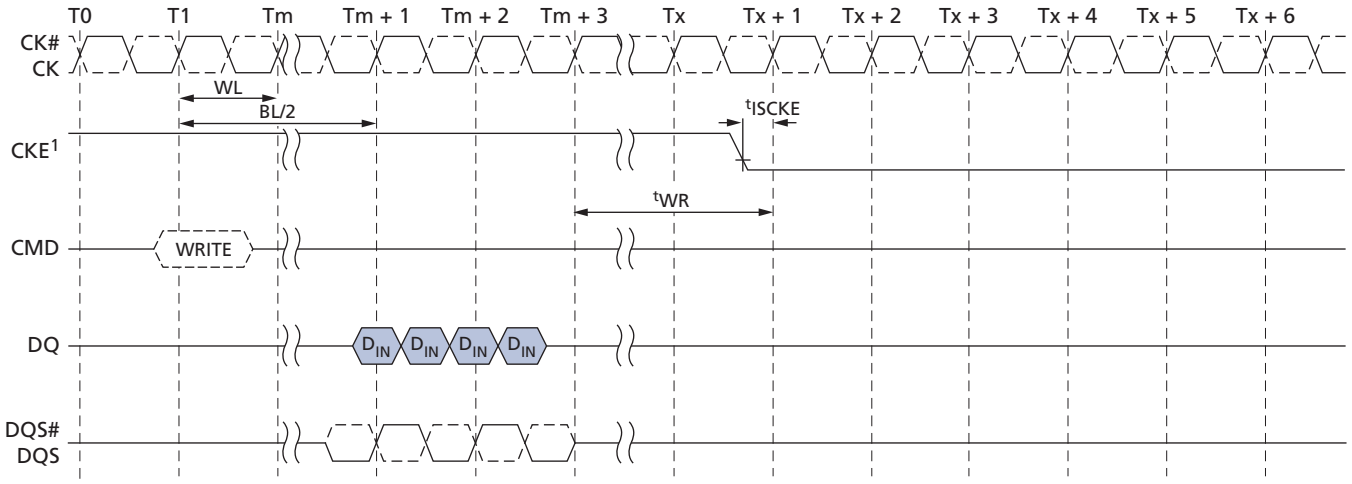
Figure 139: READ with Auto Precharge to Power-Down Entry



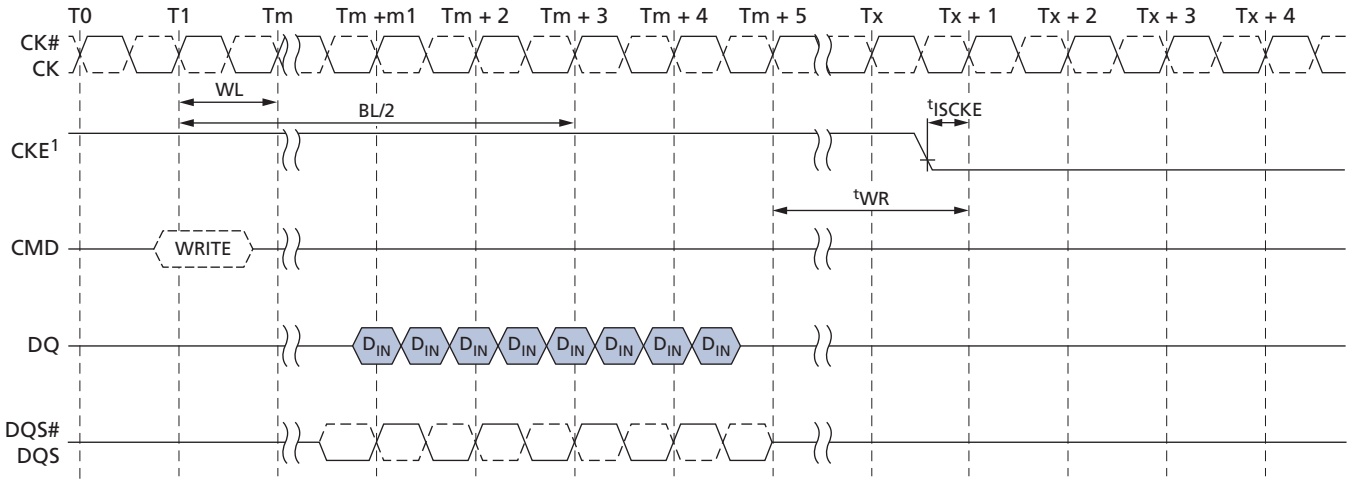
Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at (RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1) clock cycles after the clock on which the READ command is registered.
3. BL/2 with ^{t}RTP = 7.5ns and ^{t}RAS (MIN) is satisfied.
4. Start internal PRECHARGE.

Figure 140: WRITE to Power-Down Entry

BL = 4

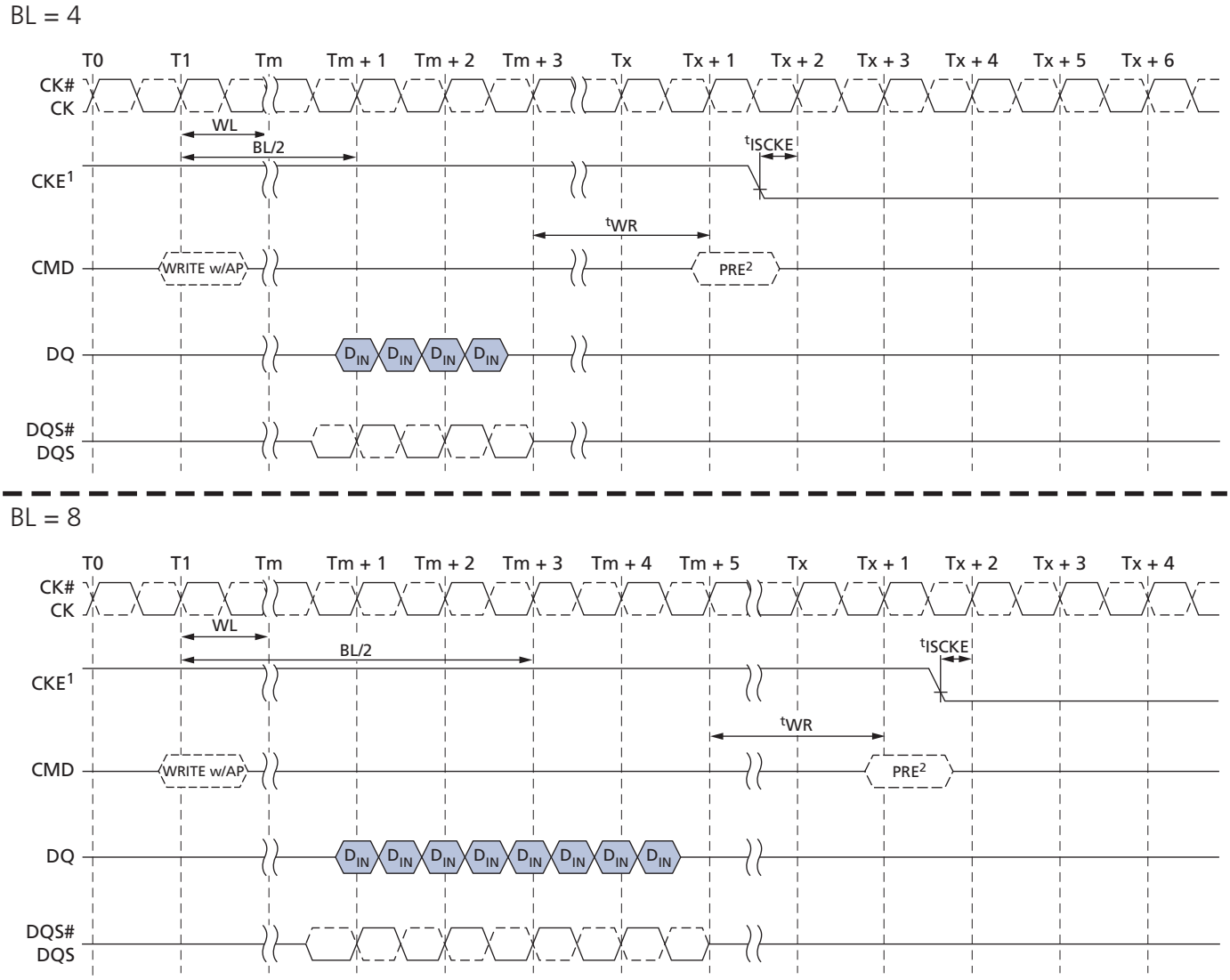


BL = 8



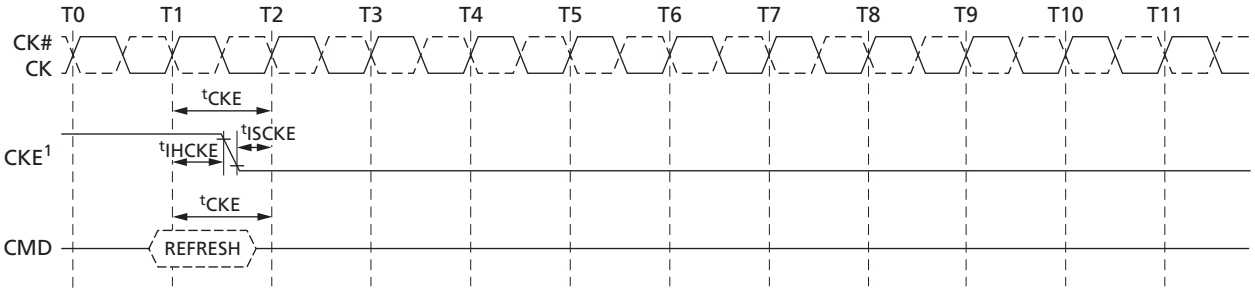
Note: 1. CKE can be registered LOW at (WL + 1 + BL/2 + RU(^{t}WR/^{t}CK)) clock cycles after the clock on which the WRITE command is registered.

Figure 141: WRITE with Auto Precharge to Power-Down Entry



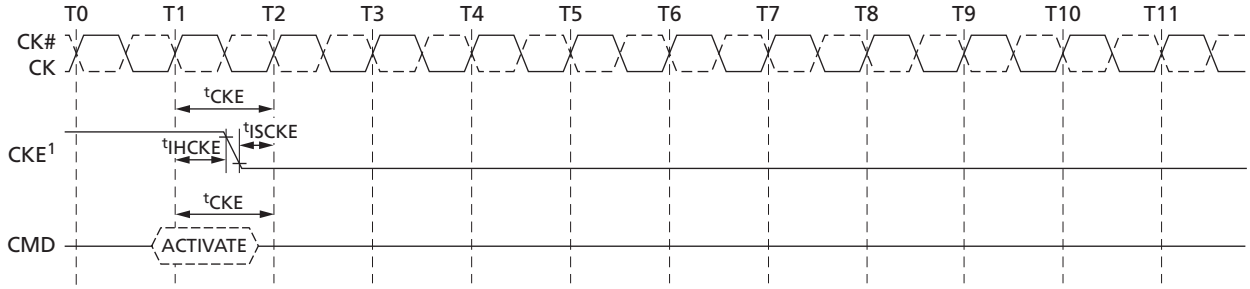
Notes:
1. CKE can be registered LOW at (WL + 1 + BL/2 + RU(^{t}WR/^{t}CK + 1) clock cycles after the WRITE command is registered.
2. Start internal PRECHARGE.

Figure 142: REFRESH Command to Power-Down Entry



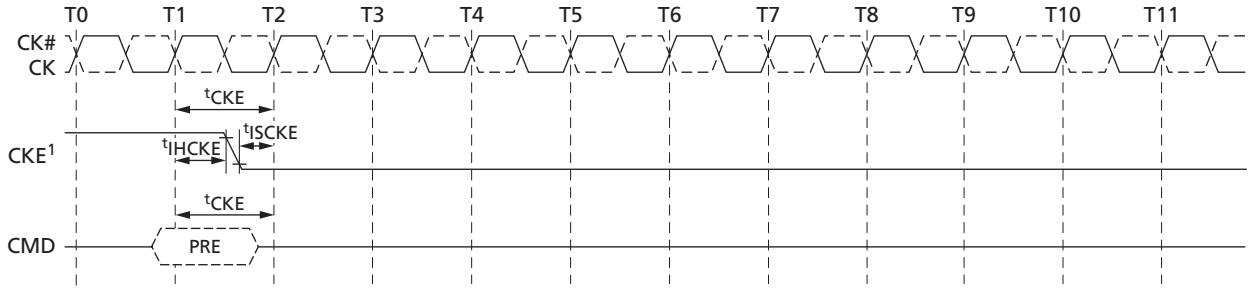
Note: 1. CKE can go LOW ^{t}IHCKE after the clock on which the REFRESH command is registered.

Figure 143: ACTIVATE Command to Power-Down Entry



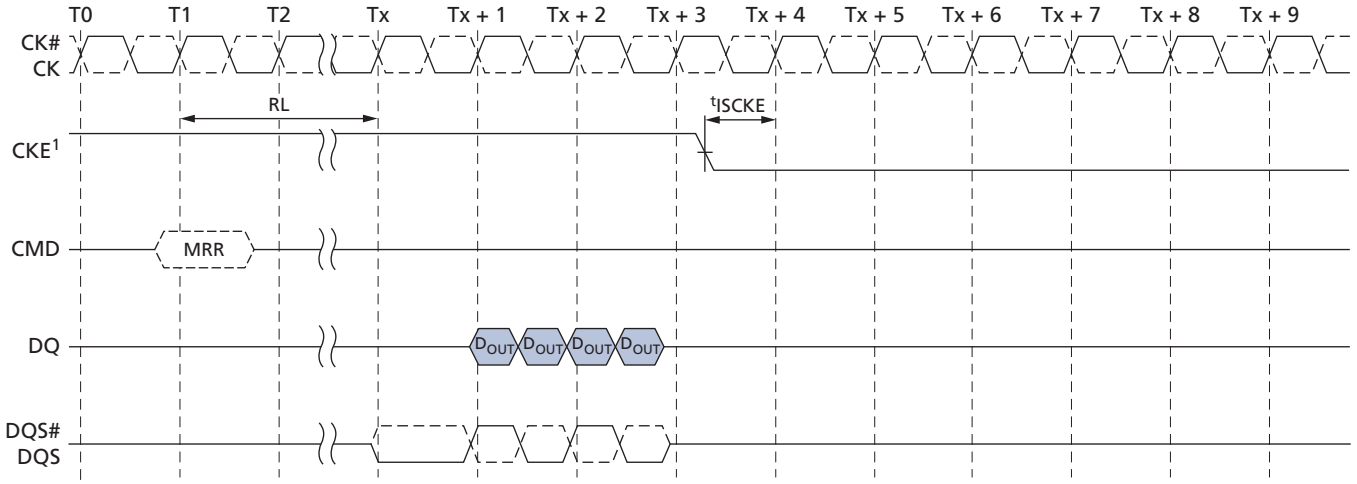
Note: 1. CKE can go LOW at ^{t}IHCKE after the clock on which the ACTIVATE command is registered.

Figure 144: PRECHARGE Command to Power-Down Entry



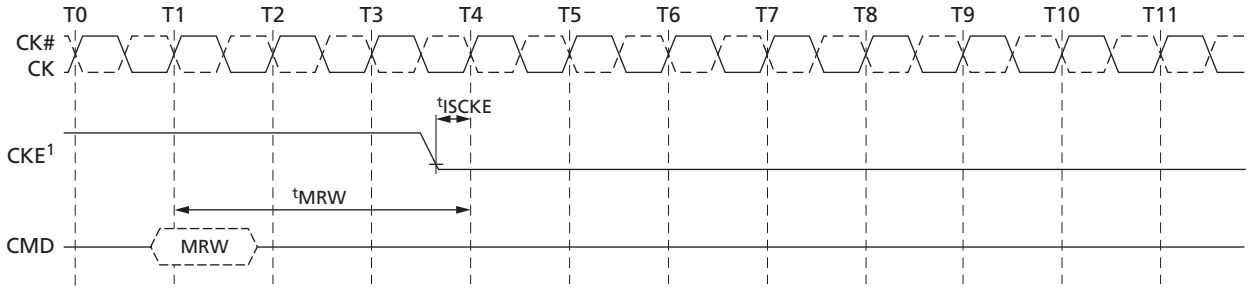
Note: 1. CKE can go LOW ^{t}IHCKE after the clock on which the PRECHARGE command is registered.

Figure 145: MRR Command to Power-Down Entry



Note: 1. CKE can be registered LOW at (RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1) clock cycles after the clock on which the MRR command is registered.

Figure 146: MRW Command to Power-Down Entry



Note: 1. CKE can be registered LOW ^{t}MRW after the clock on which the MRW command is registered.

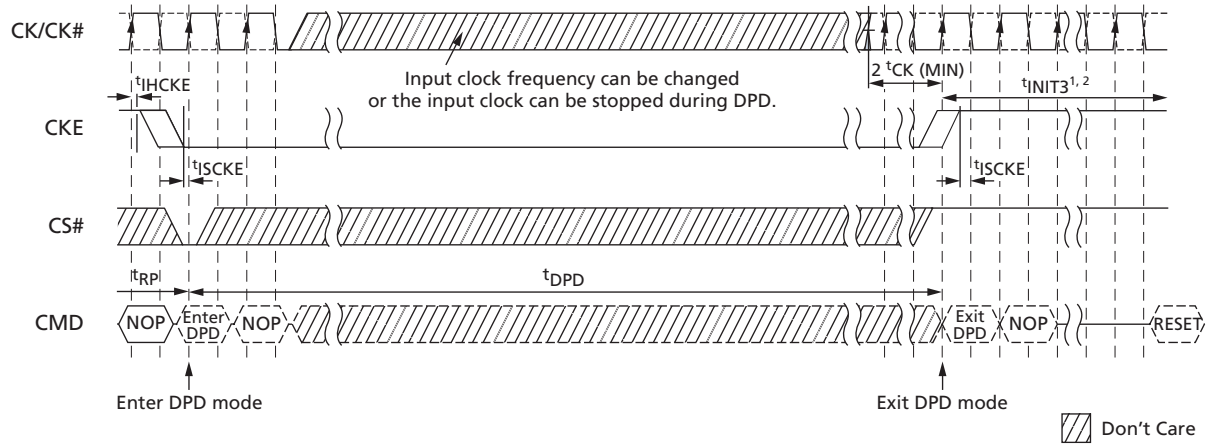
Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress, however, deep power-down I_{DD} specifications will not be applied until those operations complete. The contents of the array will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. V_{REFDQ} can be at any level between 0 and V_{DDQ}, and V_{REFCA} can be at any level between 0 and V_{DDCA} during DPD. All power supplies (including V_{REF}) must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

To exit DPD, CKE must be HIGH, ^{t}ISCKE must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

Figure 147: Deep Power-Down Entry and Exit Timing



Notes: 1. The initialization sequence can start at any time after Tx + 1.
2. ^{t}INIT3 and Tx + 1 refer to timings in the initialization sequence. For details, see Mode Register Definition.

Input Clock Frequency Changes and Stop Events

Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, Mobile LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,^{t}RCD and ^{t}RP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, ^{t}CK(MIN) and ^{t}CK(MAX) must be met for each clock cycle.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- REFRESH requirements are met
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands must have completed, including any associated data bursts, prior to changing the frequency
- Related timing conditions, ^{t}RCD, ^{t}WR, ^{t}WRA, ^{t}RP, ^{t}MRW, and ^{t}MRR, etc., are met
- CS# must be held HIGH
- Only REFab or REFpb commands can be in process

The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of 2 × ^{t}CK + ^{t}XP.

For input clock frequency changes, ^{t}CK(MIN) and ^{t}CK(MAX) must be met for each clock cycle.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has two possible encodings: CS# HIGH at the clock rising edge N; and CS# LOW with CA0, CA1, CA2 HIGH at the clock rising edge N.

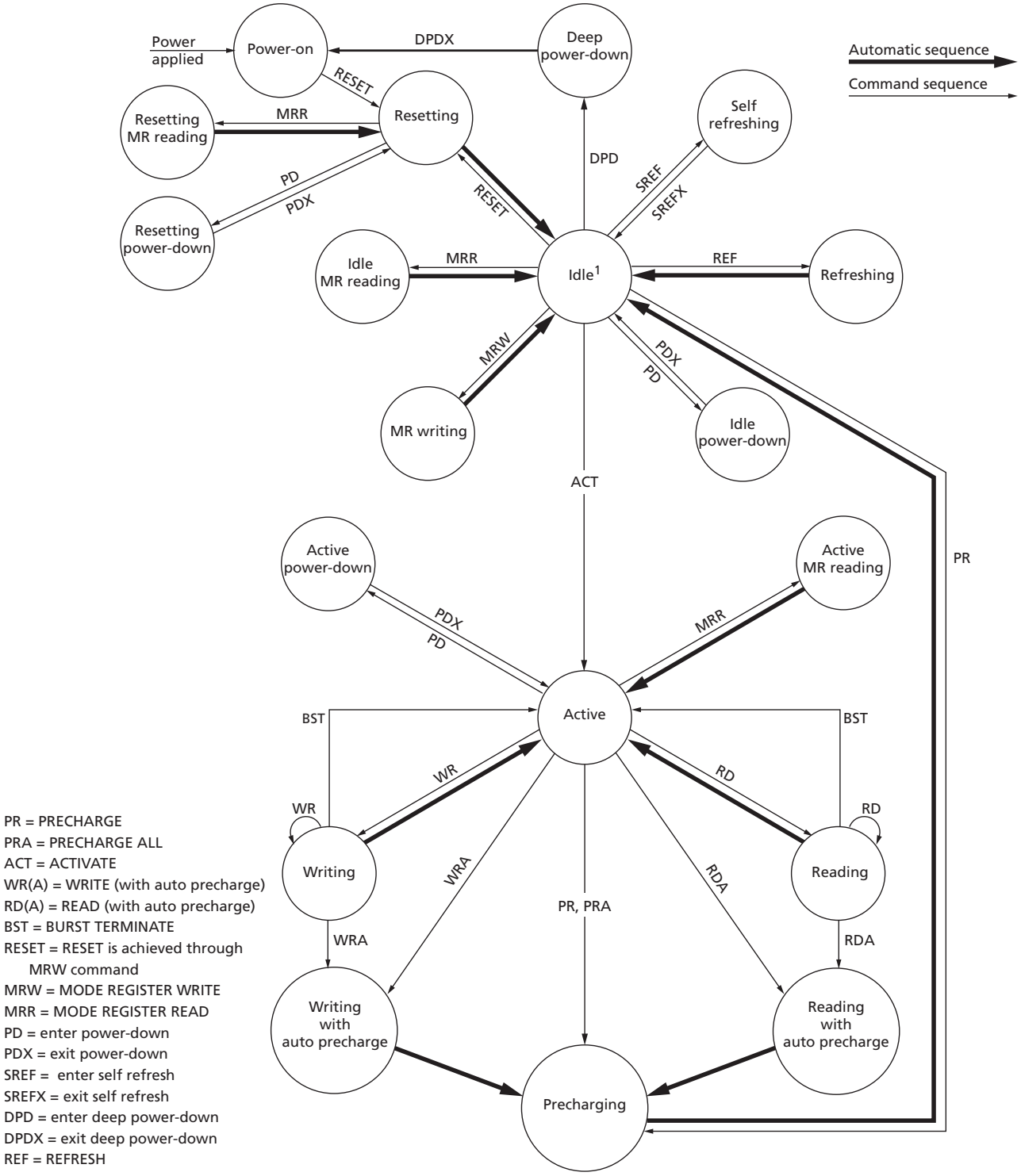
The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

Simplified Bus Interface State Diagram

The state diagram (see Figure 148 (page 201)) provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications.

The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks.

Figure 148: Simplified Bus Interface State Diagram



Note: 1. All banks are precharged in the idle state.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Table 85: Command Truth Table

Notes 1–11 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE													
	CK(*n*-1)	CK(*n*)	CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	X								↓
REFRESH (per bank)	H	H	L	L	L	H	L	X						↑
	H	H	X	X										↓
REFRESH (all banks)	H	H	L	L	L	H	H	X						↑
	H	H	X	X										↓
Enter self refresh	H	L	L	L	L	H	X							↑
	X	L	X	X										↓
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
	H	H	X	X										↓
BST	H	H	L	H	H	L	L	X						↑
	H	H	X	X										↓
Enter DPD	H	L	L	H	H	L	X							↑
	X	L	X	X										↓
NOP	H	H	L	H	H	H	X							↑
	H	H	X	X										↓
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							↑
	L	L	X	X										↓

Table 85: Command Truth Table (Continued)

Notes 1–11 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE													
	CK(*n*-1)	CK(*n*)	CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
NOP	H	H	H	X										
	H	H	X	X										
Maintain PD, SREF, DPD, (NOP)	L	L	H	X										
	L	L	X	X										
Enter power-down	H	L	H	X										
	X	L	X	X										
Exit PD, SREF, DPD	L	H	H	X										
	X	H	X	X										

Notes:
1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses (BA) determine which bank will be operated upon.
3. AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
4. X indicates a "Don't Care" state, with a defined logic level, either HIGH (H) or LOW (L).
5. Self refresh exit and DPD exit are asynchronous.
6. V_{REF} must be between 0 and V_{DDQ} during self refresh and DPD operation.
7. CAxr refers to command/address bit "x" on the rising edge of clock.
8. CAxf refers to command/address bit "x" on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. Per-bank refresh is only supported in devices with eight banks.
11. The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.

Table 86: CKE Truth Table

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = "Don't Care"

Current State	CKE*n*-1	CKE*n*	CS#	Command *n*	Operation *n*	Next State	Notes
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, 7
Idle power-down	L	L	X	X	Maintain idle power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8

Table 86: CKE Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions; L = LOW, H = HIGH, X = "Don't Care"

Current State	CKE*n*-1	CKE*n*	CS#	Command *n*	Operation *n*	Next State	Notes
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank(s) active	H	L	H	NOP	Enter active power-down	Active power-down	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down	
	H	L	L	Enter self refresh	Enter self refresh	Self refresh	
	H	L	L	DPD	Enter deep power-down	Deep power-down	
Resetting	H	L	H	NOP	Enter resetting power-down	Resetting power-down	
Other states	H	H	Refer to the command truth table				

Notes:
1. Current state = the state of the device immediately prior to the clock rising edge *n*.
2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
3. CKE*n* = the logic state of CKE at clock rising edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
4. CS#= the logic state of CS# at the clock rising edge *n*.
5. Command *n* = the command registered at clock edge *n*, and operation *n* is a result of command *n*.
6. Power-down exit time (^{t}XP) must elapse before any command other than NOP is issued.
7. The clock must toggle at least twice prior to the ^{t}XP period.
8. Upon exiting the resetting power-down state, the device will return to the idle state if ^{t}INIT5 has expired.
9. The DPD exit procedure must be followed as described in Deep Power Down.
10. Self refresh exit time (^{t}XSR) must elapse before any command other than NOP is issued.
11. The clock must toggle at least twice prior to the ^{t}XSR time.

Table 87: Current State Bank *n* to Command to Bank *n* Truth Table

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current state	

Table 87: Current State Bank *n* to Command to Bank *n* Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (per bank)	Begin to refresh	Refreshing (per bank)	6
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	7
	MRW	Load value to mode register	MR writing	7
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	7, 8
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9, 10
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9
Reading	READ	Select column and start new read burst	Reading	11, 12
	WRITE	Select column and start write burst	Writing	11, 12, 13
	BST	Read burst terminate	Active	14
Writing	WRITE	Select column and start new write burst	Writing	11, 12
	READ	Select column and start read burst	Reading	11, 12, 15
	BST	Write burst terminate	Active	14
Power-on	MRW RESET	Begin device auto initialization	Resetting	7, 9
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:

1. Values in this table apply when both CKE*n* -1 and CKE*n* are HIGH, and after ^{t}XSR or ^{t}XP has been met, if the previous state was power-down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

   Idle: The bank or banks have been precharged, and ^{t}RP has been met.

   Active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts or accesses and no register accesses are in progress.

   Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

   Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
4. The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in the following table.

   Precharge: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. After ^{t}RP is met, the bank is in the idle state.

   Row activate: Starts with registration of an ACTIVATE command and ends when ^{t}RCD is met. After ^{t}RCD is met, the bank is in the active state.

READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP is met. After ^{t}RP is met, the bank is in the idle state.

WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP is met. After ^{t}RP is met, the bank is in the idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states.

   Refresh (per bank): Starts with registration of a REFRESH (per bank) command and ends when ^{t}RFCpb is met. After ^{t}RFCpb is met, the bank is in the idle state.

   Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when ^{t}RFCab is met. After ^{t}RFCab is met, the device is in the all banks idle state.

   Idle MR reading: Starts with registration of the MRR command and ends when ^{t}MRR is met. After ^{t}MRR is met, the device is in the all banks idle state.

   Resetting MR reading: Starts with registration of the MRR command and ends when ^{t}MRR is met. After ^{t}MRR is met, the device is in the all banks idle state.

   Active MR reading: Starts with registration of the MRR command and ends when ^{t}MRR is met. After ^{t}MRR is met, the bank is in the active state.

   MR writing: Starts with registration of the MRW command and ends when ^{t}MRW is met. After ^{t}MRW is met, the device is in the all banks idle state.

   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, the device is in the all banks idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, ^{t}RP still applies.
11. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Table 88: Current State Bank *n* to Command to Bank *m* Truth Table

Notes 1–6 apply to all parameters and conditions

Current State of Bank *n*	Command to Bank *m*	Operation	Next State for Bank *m*	Notes
Any	NOP	Continue previous operation	Current state of bank *m*	
Idle	Any	Any command supported to bank *m*	–	7

Table 88: Current State Bank *n* to Command to Bank *m* Truth Table (Continued)

Notes 1–6 apply to all parameters and conditions

Current State of Bank *n*	Command to Bank *m*	Operation	Next State for Bank *m*	Notes
Row activating, active, or pre-charging	ACTIVATE	Select and activate row in bank *m*	Active	8
	READ	Select column and start READ burst from bank *m*	Reading	9
	WRITE	Select column and start WRITE burst to bank *m*	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or active MR reading	11, 12, 13
	BST	READ or WRITE burst terminates an on-going READ/WRITE from/to bank *m*	Active	7
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank *m*	Reading	9
	WRITE	Select column and start WRITE burst to bank *m*	Writing	9, 14
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank *m*	Reading	9, 15
	WRITE	Select column and start WRITE burst to bank *m*	Writing	9
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank *m*	Reading	9, 16
	WRITE	Select column and start WRITE burst to bank *m*	Writing	9, 14, 16
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank *m*	Reading	9, 15, 16
	WRITE	Select column and start WRITE burst to bank *m*	Writing	9, 16
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	MRW RESET	Begin device auto initialization	Resetting	17, 18
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:
1. This table applies when: the previous state was self refresh or power-down; after ^{t}XSR or ^{t}XP has been met; *and* both CKE*n* -1 and CKE*n* are HIGH.
2. All states and sequences not shown are illegal or reserved.

3. Current state definitions:

   Idle: The bank has been precharged and ^{t}RP has been met.

   Active: A row in the bank has been activated, ^{t}RCD has been met, no data bursts or accesses and no register accesses are in progress.

   Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.
4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.
5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.
6. The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

   Idle MRR: Starts with registration of the MRR command and ends when ^{t}MRR has been met. After ^{t}MRR is met, the device is in the all banks idle state.

   Reset MRR: Starts with registration of the MRR command and ends when ^{t}MRR has been met. After ^{t}MRR is met, the device is in the all banks idle state.

   Active MRR: Starts with registration of the MRR command and ends when ^{t}MRR has been met. After ^{t}MRR is met, the bank is in the active state.

   MRW: Starts with registration of the MRW command and ends when ^{t}MRW has been met. After ^{t}MRW is met, the device is in the all banks idle state.
7. BST is supported only if a READ or WRITE burst is ongoing.
8. ^{t}RRD must be met between the ACTIVATE command to bank *n* and any subsequent ACTIVATE command to bank *m*.
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank *m* depends on the current state of bank *m* (idle, row-activating, precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

Table 89: DM Truth Table

Functional Name	DM	DQ	Notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Note: 1. Used to mask write data, and is provided simultaneously with the corresponding input data.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 90: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	+2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2} (1.2V)	–0.4	+1.6	V	1
V_{DDCA} supply voltage relative to V_{SSCA}	V_{DDCA}	–0.4	+1.6	V	1, 2
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	+1.6	V	1, 3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.6	V	
Storage temperature	T_{STG}	–55	+125	°C	4

Notes:
1. See 1. Voltage Ramp under Power-Up (page 137).
2. V_{REFCA} 0.6 ≤ V_{DDCA}; however, V_{REFCA} may be ≥ V_{DDCA} provided that V_{REFCA} ≤ 300mV.
3. V_{REFDQ} 0.6 ≤ V_{DDQ}; however, V_{REFDQ} may be ≥ V_{DDQ} provided that V_{REFDQ} ≤ 300mV.
4. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input/Output Capacitance

Table 91: Input/Output Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		MIN	MAX	MIN	MAX		
Input capacitance, CK and CK#	C_{CK}	1.0	2.0	1.0	2.0	pF	2, 3
Input capacitance delta, CK and CK#	C_{DCK}	0	0.20	0	0.25	pF	2, 3, 4
Input capacitance, all other input-only pins	C_I	1.0	2.0	1.0	2.0	pF	2, 3, 5
Input capacitance delta, all other input-only pins	C_{DI}	–0.40	+0.40	–0.50	+0.50	pF	2, 3, 6
Input/output capacitance, DQ, DM, DQS, DQS#	C_{IO}	1.25	2.5	1.25	2.5	pF	2, 3, 7, 8
Input/output capacitance delta, DQS, DQS#	C_{DDQS}	0	0.25	0	0.30	pF	2, 3, 8, 9
Input/output capacitance delta, DQ, DM	C_{DIO}	–0.5	+0.5	–0.6	+0.6	pF	2, 3, 8, 10

Table 91: Input/Output Capacitance (Continued)

Note 1 applies to all parameters and conditions

Parameter	Symbol	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		MIN	MAX	MIN	MAX		
Input/output capacitance ZQ	C_{ZQ}	0	2.5	0	2.5	pF	2, 3, 11

Notes:
1. T_C –40°C to +105°C; V_{DDQ} = 1.14–1.3V; V_{DDCA} = 1.14–1.3V; V_{DD1} = 1.7–1.95V; V_{DD2} = 1.14–1.3V.
2. This parameter applies to die devices only (does not include package capacitance).
3. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, and V_{SSQ} applied; all other pins are left floating.
4. Absolute value of C_{CK} - $C_{CK\#}$.
5. C_I applies to CS#, CKE, and CA[9:0].
6. $C_{DI} = C_I - 0.5 \times (C_{CK} + C_{CK}\#)$.
7. DM loading matches DQ and DQS.
8. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).
9. Absolute value of C_{DQS} and $C_{DQS\#}$.
10. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS} + C_{DQS\#})$ in byte-lane.
11. Maximum external load capacitance on ZQ pin: 5pF.

Electrical Specifications – I_{DD} Specifications and Conditions

The following definitions and conditions are used in the I_{DD} measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)max}$
- HIGH: $V_{IN} \geq V_{IH(DC)min}$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table 92: Switching for CA Input Signals

Notes 1–3 apply to all parameters and conditions

	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising
Cycle	N		N + 1		N + 2		N + 3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H

Table 92: Switching for CA Input Signals (Continued)

Notes 1–3 apply to all parameters and conditions

	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:
1. CS# must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 93: Switching for I_{DD4R}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N +1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	LHLLHLH	L
Rising	H	L	N + 2	Read_Rising	HLH	LHLLHLH	H
Falling	H	L	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4R}.

Table 94: Switching for I_{DD4W}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	LLH	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N +1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	LHLLHLH	L
Rising	H	L	N + 2	Write_Rising	LLH	LHLLHLH	H
Falling	H	L	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4W}.

Table 95: I_{DD} Specification Parameters and Operating Conditions

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current (SDRAM): $^{t}CK = {}^{t}CKmin$; $^{t}RC = {}^{t}RCmin$; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	I_{DD0in}	V_{DDCA}, V_{DDQ}	4
Idle power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	4
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	4
Idle non-power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	4
Idle non-power-down standby current with clock stopped: CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	4
Active power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	4
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	4
Operating burst READ current: $^{t}CK = {}^{t}CKmin$; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: $^{t}CK = {}^{t}CKmin$; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	4
All-bank REFRESH burst current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH between valid commands; $^{t}RC = {}^{t}RFCabmin$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	4

Table 95: I_{DD} Specification Parameters and Operating Conditions (Continued)

Notes 1–3 apply to all parameters and conditions

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: ^{t}CK = ^{t}CKmin; CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI; CA bus inputs are switching; Data bus inputs are stable	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	4
Per-bank REFRESH average current: ^{t}CK = ^{t}CKmin; CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI/8; CA bus inputs are switching; Data bus inputs are stable	I_{DD5PB1}	V_{DD1}	6
	I_{DD5PB2}	V_{DD2}	6
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	4, 6
Self refresh current (–25˚C to +85˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	I_{DD61}	V_{DD1}	7
	I_{DD62}	V_{DD2}	7
	I_{DD6IN}	V_{DDCA}, V_{DDQ}	4, 7
Self refresh current (+85˚C to +105˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD6ET1}	V_{DD1}	7, 8
	I_{DD6ET2}	V_{DD2}	7, 8
	$I_{DD6ET,in}$	V_{DDCA}, V_{DDQ}	4, 7, 8
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD81}	V_{DD1}	8
	I_{DD82}	V_{DD2}	8
	I_{DD8IN}	V_{DDCA}, V_{DDQ}	4, 8

Notes:
1. I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the sum of V_{DDQ} and V_{DDCA}.
5. Guaranteed by design with output reference load and R_{ON} = 40 ohm.
6. Per-bank REFRESH is only applicable for LPDDR2-S4 device densities 1Gb or higher.
7. This is the general definition that applies to full-array self refresh.
8. I_{DD6ET} and I_{DD8} are typical values, are sampled only, and are not tested.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 96: Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			Power Supply	Unit
	Min	Typ	Max		
V_{DD1}[1]	1.70	1.80	1.95	Core power 1	V
V_{DD2}	1.14	1.20	1.30	Core power 2	V
V_{DDCA}	1.14	1.20	1.30	Input buffer power	V
V_{DDQ}	1.14	1.20	1.30	I/O buffer power	V

Note:
1. V_{DD1} uses significantly less power than V_{DD2}.

Table 97: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current: For CA, CKE, CS#, CK, CK#; Any input 0V ≤ V_{IN} ≤ V_{DDCA}; (All other pins not under test = 0V)	I_L	–2	2	µA	1
V_{REF} supply leakage current: V_{REFDQ} = V_{DDQ}/2, or V_{REFCA} = V_{DDCA}/2; (All other pins not under test = 0V)	I_{VREF}	–1	1	µA	2

Notes:
1. Although DM is for input only, the DM leakage must match the DQ and DQS/DQS# output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Table 98: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
IT temperature range	T_{CASE}[1]	–40	+85	˚C
AT temperature range		–40	+105	˚C

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. Some applications require operation in the maximum case temperature range, between 85˚C and 105˚C. For some LPDDR2 devices, derating may be necessary to operate in this range (see the MR4 Device Temperature (MA[7:0] = 04h) table).
3. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the operating temperature range. For example, T_{CASE} could be above 85˚C when the temperature sensor indicates a temperature of less than 85˚C.

AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 99: Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC input logic HIGH	V_{REF} + 0.220	Note 2	V_{REF} + 0.300	Note 2	V	1, 2
$V_{ILCA(AC)}$	AC input logic LOW	Note 2	V_{REF} - 0.220	Note 2	V_{REF} - 0.300	V	1, 2
$V_{IHCA(DC)}$	DC input logic HIGH	V_{REF} + 0.130	V_{DDCA}	V_{REF} + 0.200	V_{DDCA}	V	1
$V_{ILCA(DC)}$	DC input logic LOW	V_{SSCA}	V_{REF} - 0.130	V_{SSCA}	V_{REF} - 0.200	V	1
$V_{REFCA(DC)}$	Reference voltage for CA and CS# inputs	0.49 × V_{DDCA}	0.51 × V_{DDCA}	0.49 × V_{DDCA}	0.51 × V_{DDCA}	V	3, 4

Notes:
1. For CA and CS# input-only pins. $V_{REF} = V_{REFCA(DC)}$.
2. See Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFCA} could prevent V_{REFCA} from deviating more than ±1% V_{DDCA} from $V_{REFCA(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately $V_{DDCA}/2$ ±12mV.

Table 100: Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE input HIGH level	0.8 × V_{DDCA}	Note 1	V	1
V_{ILCKE}	CKE input LOW level	Note 1	0.2 × V_{DDCA}	V	1

Note:
1. See Overshoot and Undershoot Definition.

Table 101: Single-Ended AC and DC Input Levels for DQ and DM

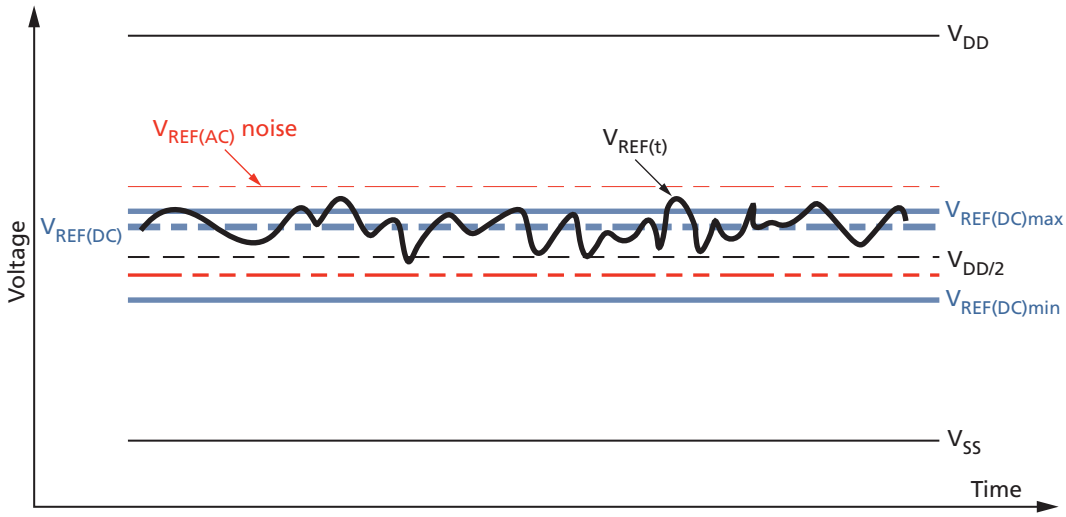
Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHDQ(AC)}$	AC input logic HIGH	V_{REF} + 0.220	Note 2	V_{REF} + 0.300	Note 2	V	1, 2
$V_{ILDQ(AC)}$	AC input logic LOW	Note 2	V_{REF} - 0.220	Note 2	V_{REF} - 0.300	V	1, 2
$V_{IHDQ(DC)}$	DC input logic HIGH	V_{REF} + 0.130	V_{DDQ}	V_{REF} + 0.200	V_{DDQ}	V	1
$V_{ILDQ(DC)}$	DC input logic LOW	V_{SSQ}	V_{REF} - 0.130	V_{SSQ}	V_{REF} - 0.200	V	1
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	0.49 × V_{DDQ}	0.51 × V_{DDQ}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	3, 4

Notes:
1. For DQ input-only pins. $V_{REF} = V_{REFDQ(DC)}$.
2. See Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFDQ} could prevent V_{REFDQ} from deviating more than ±1% V_{DDQ} from $V_{REFDQ(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately. $V_{DDQ}/2$ ±12mV.

V_{REF} Tolerances

The DC tolerance limits and AC noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated below. This figure shows a valid reference voltage $V_{REF}(t)$ as a function of time. V_{DD} is used in place of V_{DDCA} for V_{REFCA}, and V_{DDQ} for V_{REFDQ}. $V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (for example, 1 second) and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA}, also over a very long period of time (for example, 1 second). This average must meet the MIN/MAX requirements in Table 99 (page 216). Additionally, $V_{REF}(t)$ can temporarily deviate from $V_{REF(DC)}$ by no more than ±1% V_{DD}. $V_{REF}(t)$ cannot track noise on V_{DDQ} or V_{DDCA} if doing so would force V_{REF} outside these specifications.

Figure 149: V_{REF} DC Tolerance and V_{REF} AC Noise Limits



The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{REF}.

V_{REF} DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When V_{REF} is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

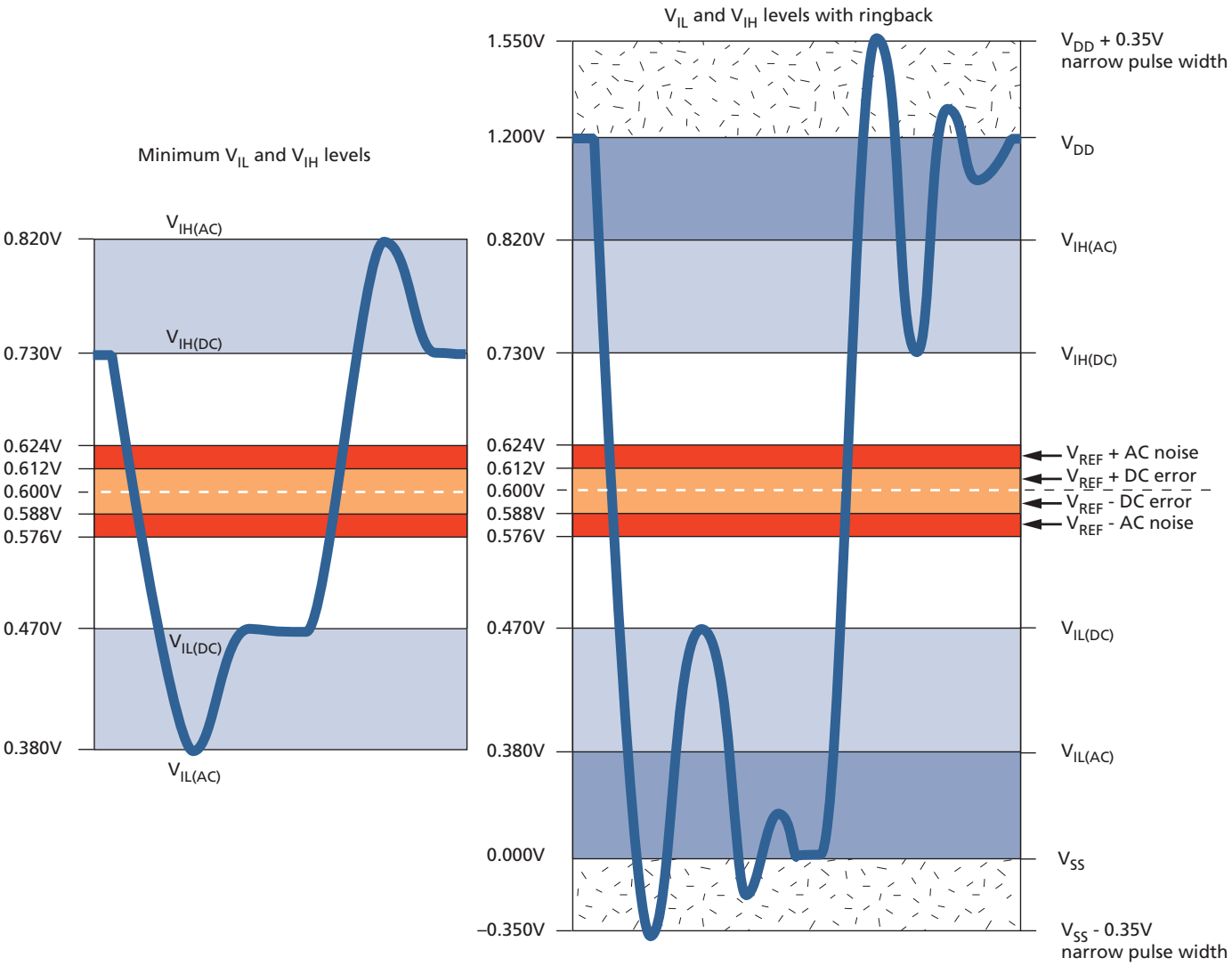
- V_{REF} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}), *and*
- the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF} (see Table 99 (page 216)).

System timing and voltage budgets must account for V_{REF} deviations outside this range.

The setup/hold specification and derating values must include time and voltage associated with V_{REF} AC noise. Timing and voltage effects due to AC noise on V_{REF} up to the specified limit (±1% V_{DD}) are included in LPDDR2 timings and their associated deratings.

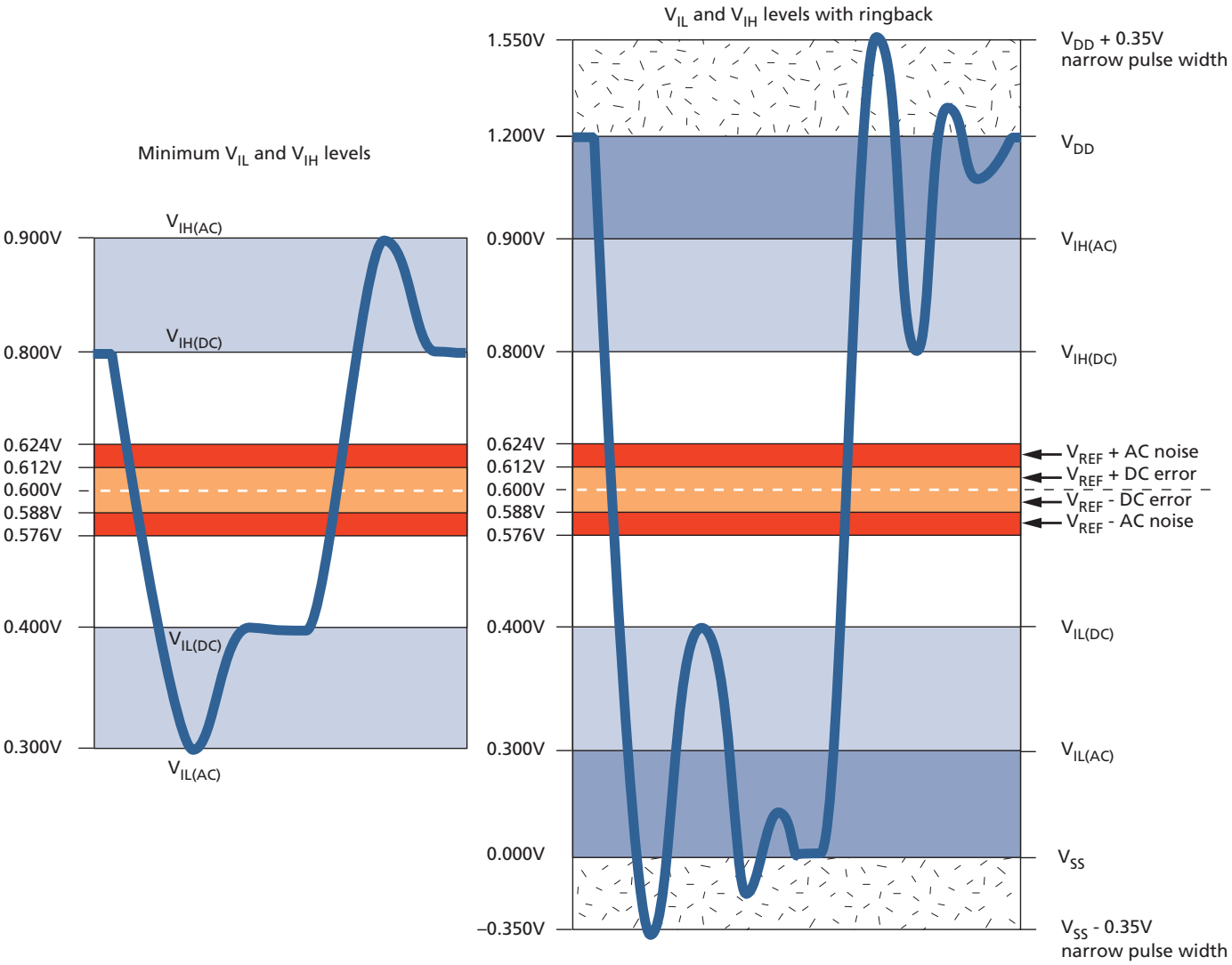
Input Signal

Figure 150: LPDDR2-466 to LPDDR2-1066 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, CK#, and CS# V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.
3. For CA[9:0], CK, CK#, and CS# V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.

Figure 151: LPDDR2-200 to LPDDR2-400 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, CK#, and CS# V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.
3. For CA[9:0], CK, CK#, and CS# V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.

AC and DC Logic Input Measurement Levels for Differential Signals

Figure 152: Differential AC Swing Time and ^{t}DVAC

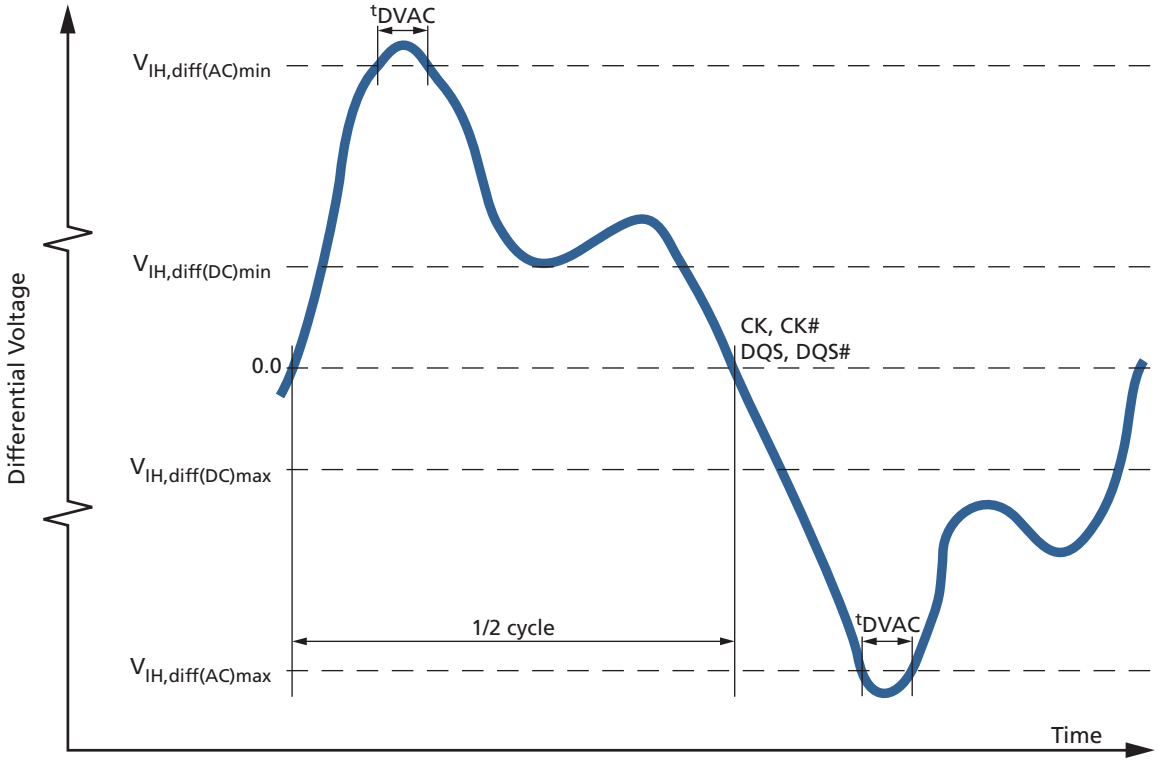


Table 102: Differential AC and DC Input Levels

For CK and CK#, $V_{REF} = V_{REFCA(DC)}$; For DQS and DQS# $V_{REF} = V_{REFDQ(DC)}$

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IH,diff(AC)}$	Differential input HIGH AC	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	V	2
$V_{IL,diff(AC)}$	Differential input LOW AC	Note 1	$2 \times (V_{REF} - V_{IL(AC)})$	Note 1	$2 \times (V_{REF} - V_{IL(AC)})$	V	2
$V_{IH,diff(DC)}$	Differential input HIGH	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	V	3
$V_{IL,diff(DC)}$	Differential input LOW	Note 1	$2 \times (V_{REF} - V_{IL(DC)})$	Note 1	$2 \times (V_{REF} - V_{IL(DC)})$	V	3

Notes: 1. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals and must comply with the specified limitations for overshoot and undershoot (see Overshoot and Undershoot Definition).

2. For CK and CK#, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS and DQS#, use $V_{IH}/V_{IL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. Used to define a differential signal slew rate.

Table 103: CK/CK# and DQS/DQS# Time Requirements Before Ringback (^{t}DVAC)

Slew Rate (V/ns)	^{t}DVAC (ps) at $V_{IH}/V_{ILdiff(AC)}$ = 440mV	^{t}DVAC (ps) at $V_{IH}/V_{ILdiff(AC)}$ = 600mV
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

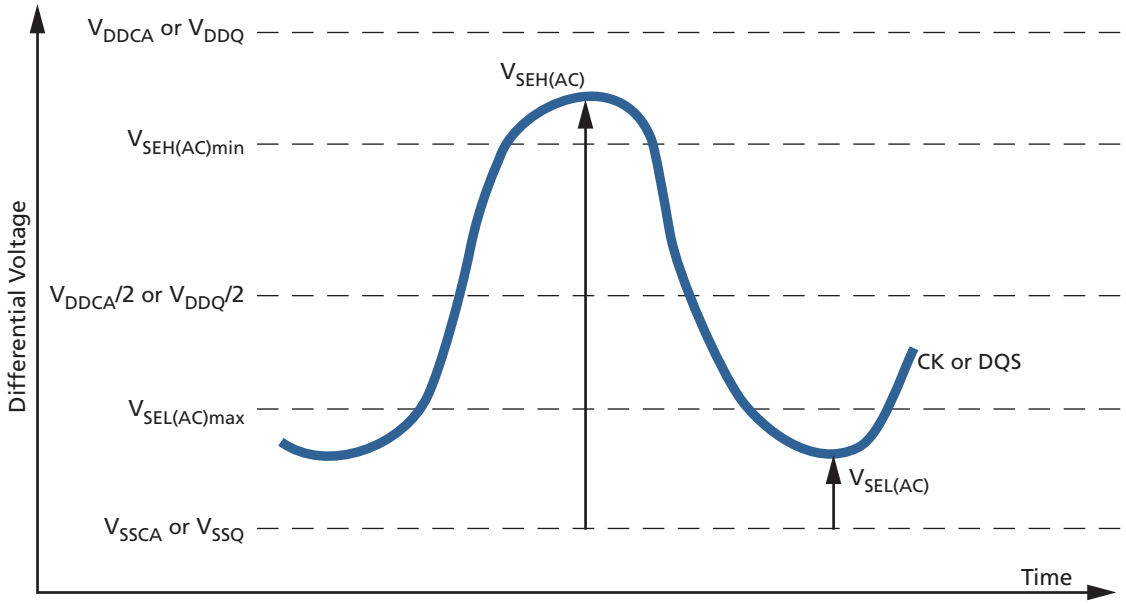
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, CK#, DQS, and DQS#) must also comply with certain requirements for single-ended signals.

CK and CK# must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle. DQS, DQS# must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.

Figure 153: Single-Ended Requirements for Differential Signals



Note that while CA and DQ signal requirements are referenced to V_{REF}, the single-ended components of differential signals also have a requirement with respect to $V_{DDQ}/2$ for DQS, and $V_{DDCA}/2$ for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)max}$ or $V_{SEH(AC)min}$ has no bearing on timing. This requirement does, however, add a restriction on the common mode characteristics of these signals (see "Single-Ended AC and DC Input Levels for CA and CS# Inputs" for CK/CK# single-ended requirements, and "Single-Ended AC and DC Input Levels for DQ and DM" for DQ and DQM single-ended requirements).

Table 104: Single-Ended Levels for CK, CK#, DQS, DQS#

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	$(V_{DDQ}/2) + 0.220$	Note 1	$(V_{DDQ}/2) + 0.300$	Note 1	V	2, 3
	Single-ended HIGH level for CK, CK#	$(V_{DDCA}/2) + 0.220$	Note 1	$(V_{DDCA}/2) + 0.300$	Note 1	V	2, 3
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 1	$(V_{DDQ}/2) - 0.220$	Note 1	$(V_{DDQ}/2) – 0.300$	V	2, 3
	Single-ended LOW level for CK, CK#	Note 1	$(V_{DDCA}/2) - 0.220$	Note 1	$(V_{DDCA}/2) – 0.300$	V	2, 3

Notes: 1. These values are not defined, however, the single-ended signals CK, CK#, DQS0, DQS#0, DQS1, DQS#1, DQS2, DQS#2, DQS3, DQS#3 must be within the respective limits ($V_{IH(DC)max}$/ $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (See Overshoot and Undershoot Definition).

2. For CK and CK#, use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and DQS#[3:0]), use $V_{IH}/V_{IL(AC)}$ of DQ.
3. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK, CK#, DQS, and DQS#) must meet the specifications in Table 104 (page 222). The differential input crosspoint voltage (V_{IX}) is measured from the actual crosspoint of the true signal and its and complement to the midlevel between V_{DD} and V_{SS}.

Figure 154: V_{IX} Definition

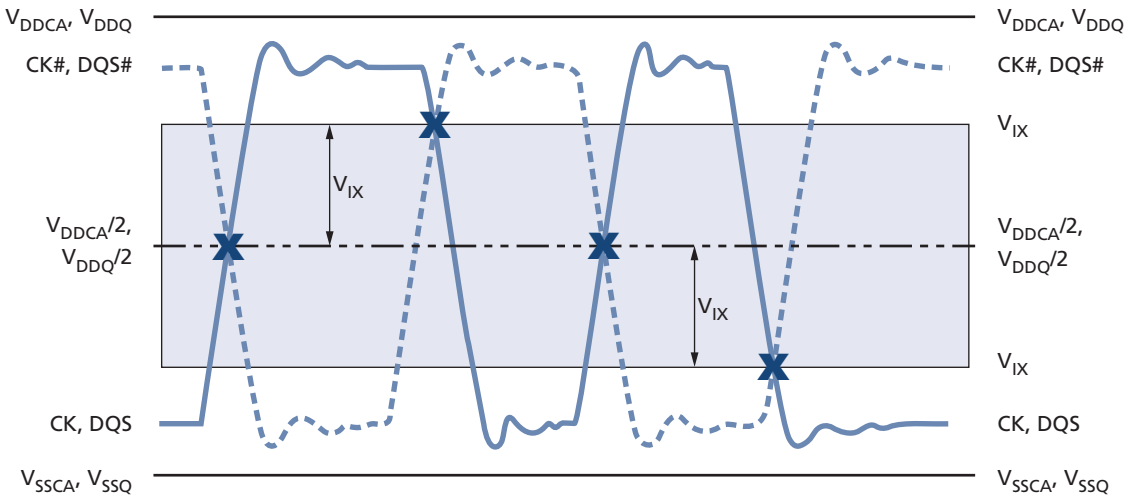


Table 105: Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input crosspoint voltage relative to $V_{DDCA}/2$ for CK and CK#	–120	120	mV	1, 2
$V_{IXDQ(AC)}$	Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS and DQS#	–120	120	mV	1, 2

Notes:
1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK and CK#, $V_{REF} = V_{REFCA(DC)}$. For DQS and DQS#, $V_{REF} = V_{REFDQ(DC)}$.

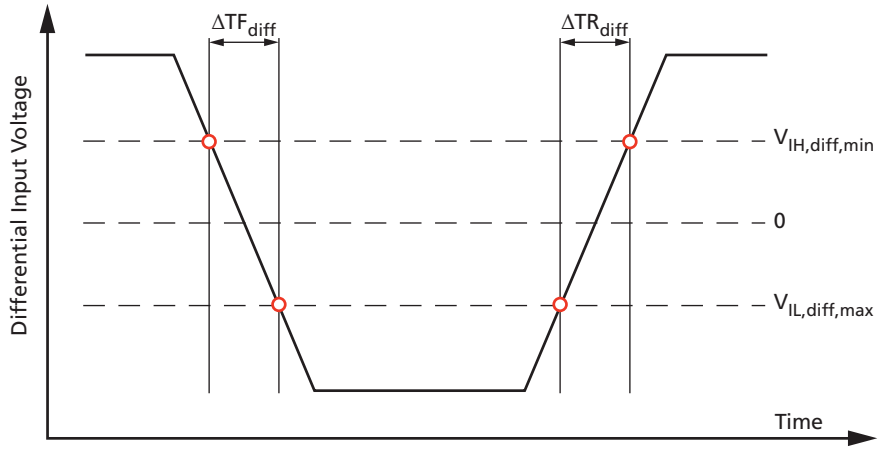
Input Slew Rate

Table 106: Differential Input Slew Rate Definition

Description	Measured[1]		Defined by
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TF_{diff}$

Note: 1. The differential signals (CK/CK# and DQS/DQS#) must be linear between these thresholds.

Figure 155: Differential Input Slew Rate Definition for CK, CK#, DQS, and DQS#



Output Characteristics and Operating Conditions

Table 107: Single-Ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)		V_{REF} + 0.12	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)		V_{REF} - 0.12	V	
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)		0.1 x V_{DDQ}	V	2
I_{OZ}	Output leakage current (DQ, DM, DQS, DQS#); DQ, DQS, DQS# are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	MIN	–5	µA	
		MAX	+5	µA	
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	MIN	–15	%	
		MAX	+15	%	

Notes: 1. I_{OH} = –0.1mA.
2. I_{OL} = 0.1mA.

Table 108: Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level (for output SR)	+ 0.2 x V_{DDQ}	V
$V_{OLdiff(AC)}$	AC differential output LOW measurement level (for output SR)	- 0.2 x V_{DDQ}	V

Single-Ended Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 109: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 156: Single-Ended Output Slew Rate Definition

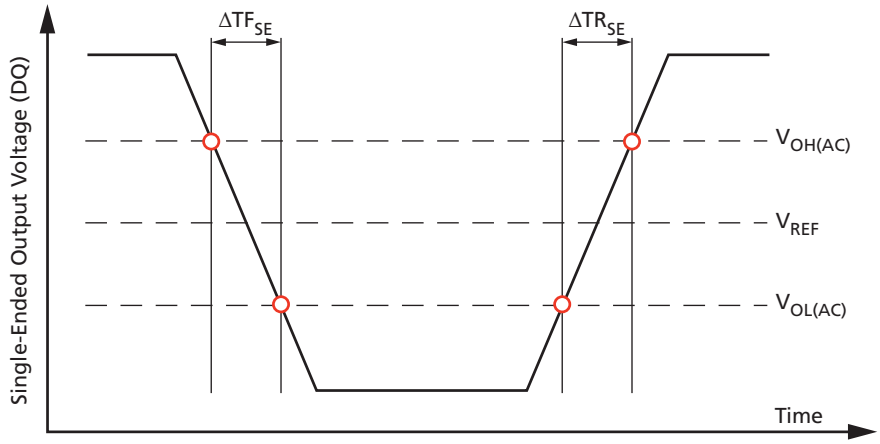


Table 110: Single-Ended Output Slew Rate

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended output slew rate (output impedance = 40Ω ±30%)	SRQ_{SE}	1.5	3.5	V/ns
Single-ended output slew rate (output impedance = 60Ω ±30%)	SRQ_{SE}	1.0	2.5	V/ns

Table 110: Single-Ended Output Slew Rate (Continued)

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Output slew-rate-matching ratio (pull-up to pull-down)		0.7	1.4	–

Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 111: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TF_{diff}$

Note:
1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 157: Differential Output Slew Rate Definition

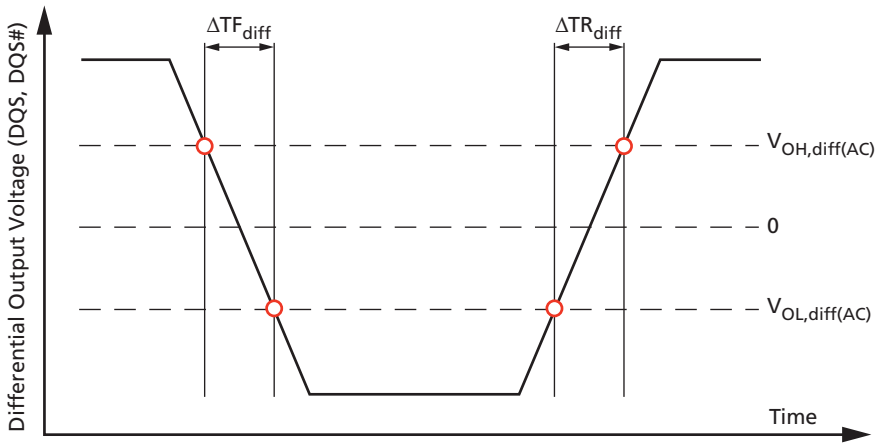


Table 112: Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate (output impedance = 40Ω ±30%)	SRQ_{diff}	3.0	7.0	V/ns
Differential output slew rate (output impedance = 60Ω ±30%)	SRQ_{diff}	2.0	5.0	V/ns

Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = single-ended signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

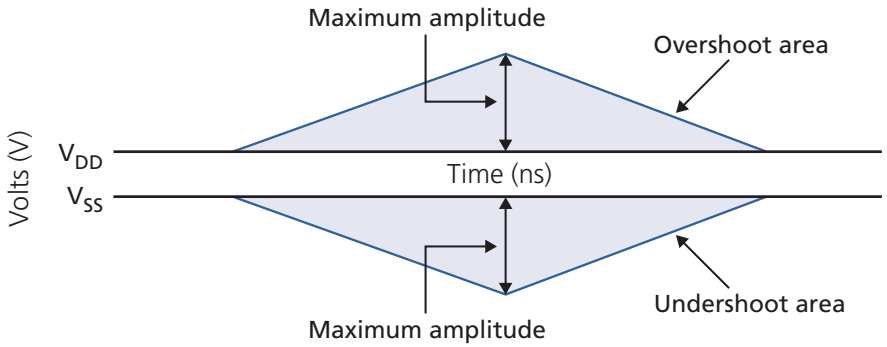
Table 113: AC Overshoot/Undershoot Specification

Applies for CA[9:0], CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM

Parameter	1066	933	800	667	533	400	333	Unit
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum area above V_{DD}[1]	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns
Maximum area below V_{SS}[2]	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns

Notes:
1. V_{DD} stands for V_{DDCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS, and DQS#.
2. V_{SS} stands for V_{SSCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS, and DQS#.

Figure 158: Overshoot and Undershoot Definition

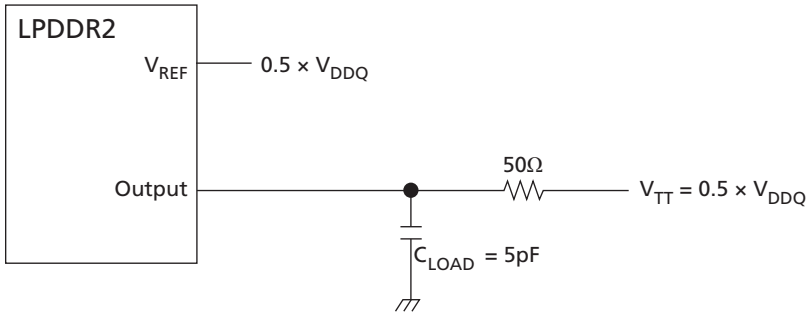


Notes:
1. V_{DD} stands for V_{DDCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS, and DQS#.
2. V_{SS} stands for V_{SSCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS, and DQS#.

HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.

Figure 159: HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note: 1. All output timing parameter values (^{t}DQSCK, ^{t}DQSQ, ^{t}QHS, ^{t}HZ, ^{t}RPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance

Output driver impedance is selected by a mode register during initialization. To achieve tighter tolerances, ZQ calibration is required. Output specifications refer to the default output drive unless specifically stated otherwise. The output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

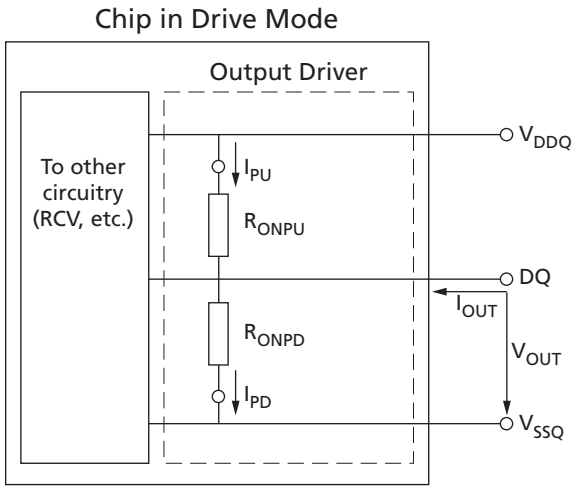
$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPD} is turned off.

$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPU} is turned off.

Figure 160: Output Driver



Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor R_{ZQ}. Typical R_{ZQ} is 240 ohms.

Table 114: Output Driver DC Electrical Characteristics with ZQ Calibration

Notes 1–4 apply to all parameters and conditions

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit	Notes
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/7$	
	R_{ON34PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/7$	
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/6$	
	R_{ON40PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/6$	
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/5$	
	R_{ON48PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/5$	
60.0Ω	R_{ON60PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/4$	
	R_{ON60PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/4$	
80.0Ω	R_{ON80PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/3$	
	R_{ON80PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/3$	
120.0Ω	$R_{ON120PD}$	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/2$	
	$R_{ON120PU}$	0.5 × V_{DDQ}	0.85	1.00	1.15	$R_{ZQ}/2$	
Mismatch between pull-up and pull-down	MM_{PUPD}		–15.00		+15.00	%	5

Notes:
1. Applies across entire operating temperature range after calibration.
2. $R_{ZQ} = 240Ω$.
3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see Output Driver Temperature and Voltage Sensitivity.
4. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x V_{DDQ}.
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}:

Measure R_{ONPU} and R_{ONPD}, both at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

For example, with MM_{PUPD} (MAX) = 15% and R_{ONPD} = 0.85, RON_{PU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen.

Table 115: Output Driver Sensitivity Definition

Resistor	V_{OUT}	Min	Max	Unit
R_{ONPD}	0.5 × V_{DDQ}	$85 - (dR_{ON}dT \cdot \lvert\Delta T\rvert) - (dR_{ON}dV \cdot \lvert\Delta V\rvert)$	$115 + (dR_{ON}dT \cdot \lvert\Delta T\rvert) - (dR_{ON}dV \cdot \lvert\Delta V\rvert)$	%
R_{ONPU}				

Notes:
1. $\Delta T = T - T$ (at calibration). $\Delta V = V - V$ (at calibration).
2. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production testing; they are verified by design and characterization.

Table 116: Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
R_{ONdT}	R_{ON} temperature sensitivity	0.00	0.75	%/°C
R_{ONdV}	R_{ON} voltage sensitivity	0.00	0.20	%/mV

Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Table 117: Output Driver DC Electrical Characteristics Without ZQ Calibration

RON_{nom}	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/7$
	R_{ON34PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/7$
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/6$
	R_{ON40PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/6$
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/5$
	R_{ON48PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/5$
60.0Ω	R_{ON60PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/4$
	R_{ON60PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/4$
80.0Ω	R_{ON80PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/3$
	R_{ON80PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	$R_{ZQ}/3$

Table 117: Output Driver DC Electrical Characteristics Without ZQ Calibration (Continued)

RON_{nom}	Resistor	V_{OUT}	Min	Typ	Max	Unit
120.0Ω	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$

Notes: 1. Applies across entire operating temperature range without calibration.
2. $R_{ZQ} = 240\Omega$.

Table 118: I-V Curves

	$R_{ON} = 240\Omega$ (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current (mA) / R_{ON} (ohms)				Current (mA) / R_{ON} (ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
Voltage (V)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	–0.19	–0.32	–0.21	–0.26
0.10	0.38	0.64	0.40	0.53	–0.38	–0.64	–0.40	–0.53
0.15	0.56	0.94	0.60	0.78	–0.56	–0.94	–0.60	–0.78
0.20	0.74	1.26	0.79	1.04	–0.74	–1.26	–0.79	–1.04
0.25	0.92	1.57	0.98	1.29	–0.92	–1.57	–0.98	–1.29
0.30	1.08	1.86	1.17	1.53	–1.08	–1.86	–1.17	–1.53
0.35	1.25	2.17	1.35	1.79	–1.25	–2.17	–1.35	–1.79
0.40	1.40	2.46	1.52	2.03	–1.40	–2.46	–1.52	–2.03
0.45	1.54	2.74	1.69	2.26	–1.54	–2.74	–1.69	–2.26
0.50	1.68	3.02	1.86	2.49	–1.68	–3.02	–1.86	–2.49
0.55	1.81	3.30	2.02	2.72	–1.81	–3.30	–2.02	–2.72
0.60	1.92	3.57	2.17	2.94	–1.92	–3.57	–2.17	–2.94
0.65	2.02	3.83	2.32	3.15	–2.02	–3.83	–2.32	–3.15
0.70	2.11	4.08	2.46	3.36	–2.11	–4.08	–2.46	–3.36
0.75	2.19	4.31	2.58	3.55	–2.19	–4.31	–2.58	–3.55
0.80	2.25	4.54	2.70	3.74	–2.25	–4.54	–2.70	–3.74
0.85	2.30	4.74	2.81	3.91	–2.30	–4.74	–2.81	–3.91
0.90	2.34	4.92	2.89	4.05	–2.34	–4.92	–2.89	–4.05
0.95	2.37	5.08	2.97	4.23	–2.37	–5.08	–2.97	–4.23
1.00	2.41	5.20	3.04	4.33	–2.41	–5.20	–3.04	–4.33
1.05	2.43	5.31	3.09	4.44	–2.43	–5.31	–3.09	–4.44
1.10	2.46	5.41	3.14	4.52	–2.46	–5.41	–3.14	–4.52
1.15	2.48	5.48	3.19	4.59	–2.48	–5.48	–3.19	–4.59
1.20	2.50	5.55	3.23	4.65	–2.50	–5.55	–3.23	–4.65

Figure 161: Output Impedance = 240 Ohms, I-V Curves After ZQRESET

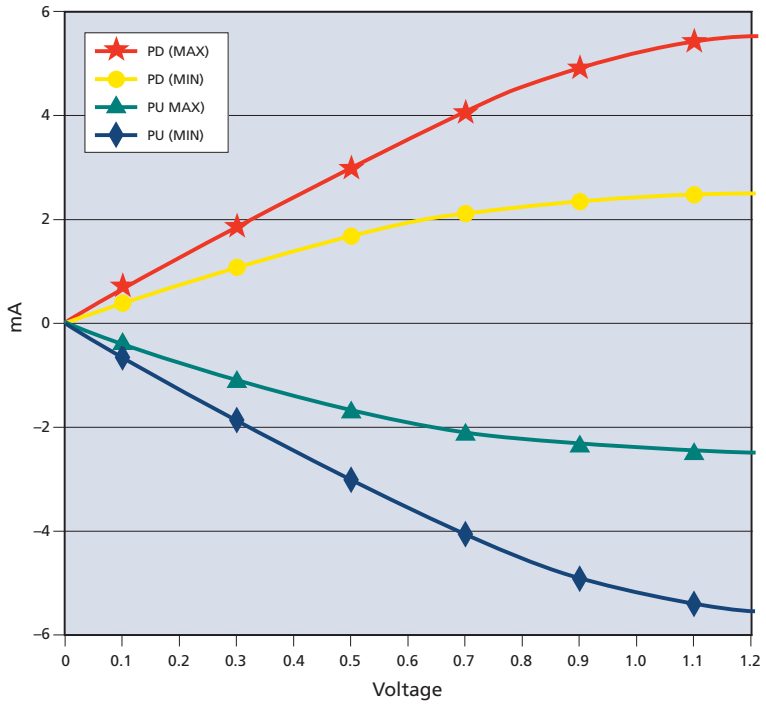
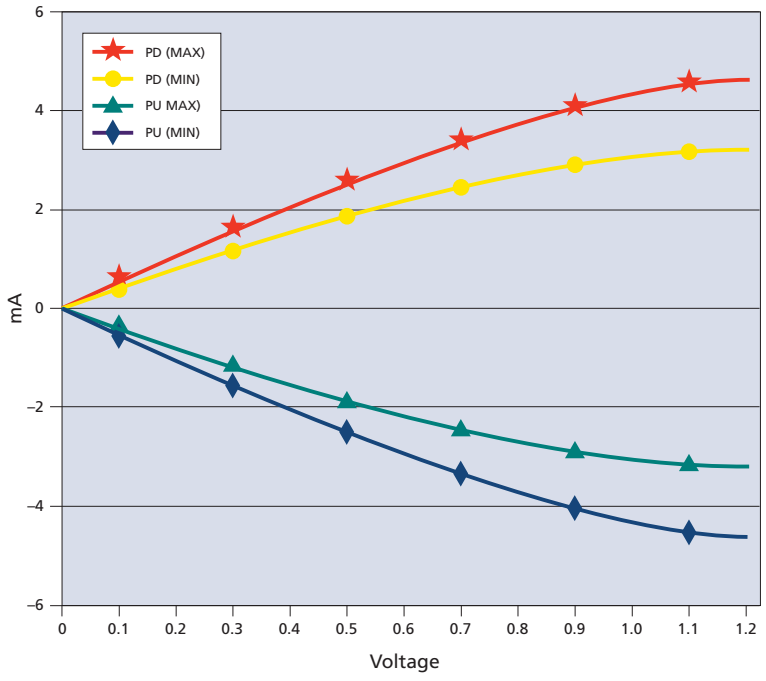


Figure 162: Output Impedance = 240 Ohms, I-V Curves After Calibration



Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 119: Definitions and Calculations

Symbol	Description	Calculation	Notes
^{t}CK(avg) and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit ^{t}CK(avg) represents the actual clock average ^{t}CK(avg)of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. ^{t}CK(avg)can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CK_{j}\right)/N$ Where N = 200	
^{t}CK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
^{t}CH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$^{t}CH(avg) = \left(\sum_{j=1}^{N} {}^{t}CH_{j}\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
^{t}CL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$^{t}CL(avg) = \left(\sum_{j=1}^{N} {}^{t}CL_{j}\right)/(N \times {}^{t}CK(avg))$ Where N = 200	
^{t}JIT(per)	The single-period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).	$^{t}JIT(per) = \text{min/max of } \left({}^{t}CK_{i} - {}^{t}CK(avg)\right)$ Where i = 1 to 200	1
^{t}JIT(per),act	The actual clock jitter for a given system.		
^{t}JIT(per), allowed	The specified clock period jitter allowance.		
^{t}JIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. ^{t}JIT(cc) defines the cycle-to-cycle jitter.	$^{t}JIT(cc) = \text{max of } \left({}^{t}CK_{i+1} - {}^{t}CK_{i}\right)$	1
^{t}ERR(nper)	The cumulative error across *n* multiple consecutive cycles from ^{t}CK(avg).	$^{t}ERR(nper) = \left(\sum_{j=i}^{i+n-1} {}^{t}CK_{j}\right) - (n \times {}^{t}CK(avg))$	1
^{t}ERR(nper),act	The actual cumulative error over *n* cycles for a given system.		
^{t}ERR(nper), allowed	The specified cumulative error allowance over *n* cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	$^{t}ERR(nper),min = (1 + 0.68LN(n)) \times {}^{t}JIT(per),min$	2

Table 119: Definitions and Calculations (Continued)

Symbol	Description	Calculation	Notes
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	^{t}ERR(nper),max = (1 + 0.68LN(n)) × ^{t}JIT(per),max	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	^{t}JIT(duty),min = MIN((^{t}CH(abs),min – ^{t}CH(avg),min), (^{t}CL(abs),min – ^{t}CL(avg),min)) × ^{t}CK(avg) ^{t}JIT(duty),max = MAX((^{t}CH(abs),max – ^{t}CH(avg),max), (^{t}CL(abs),max – ^{t}CL(avg),max)) × ^{t}CK(avg)	

Notes:
1. Not subject to production testing.
2. Using these equations, ^{t}ERR(nper) tables can be generated for each ^{t}JIT(per),act value.

^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 120: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)

Notes:
1. ^{t}CK(avg),min is expressed in ps for this table.
2. ^{t}JIT(duty),min is a negative value.

Clock Period Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing section. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(^{t}nPARAM),act exceed ^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{^{t}\text{PARAM} + ^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - ^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{nPARAM}} - ^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cycle derating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceed the supported cumulative ^{t}ERR(^{t}nPARAM),allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^{t}CORE), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{^{t}\text{PARAM} + ^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - ^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{CK(avg)}}\right\} - ^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (^{t}IS, ^{t}IH, ^{t}ISCKE, ^{t}IHCKE, ^{t}ISb, ^{t}IHb, ^{t}ISCKEb, ^{t}IHCKEb) are measured from a command/address signal (CKE, CS, or CA[9:0]) transition edge to its respective clock signal (CK/CK#) crossing. The specification values are not affected by the ^{t}JIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

^{t}RPRE

When the device is operated with input clock jitter, ^{t}RPRE must be derated by the ^{t}JIT(per),act,max of the input clock that exceeds ^{t}JIT(per),allowed,max. Output deratings are relative to the input clock:

$$^{t}\text{RPRE(min,derated)} = 0.9 - \left(\frac{^{t}\text{JIT(per)},\text{act,max} - ^{t}\text{JIT(per)},\text{allowed,max}}{^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR2-800 device has ^{t}CK(avg) = 2500ps, ^{t}JIT(per),act,min = –172ps, and ^{t}JIT(per),act,max = +193ps, then ^{t}RPRE,min,derated = 0.9 - (^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) = 0.9 - (193 - 100)/2500 = 0.8628 ^{t}CK(avg).

^{t}LZ(DQ), ^{t}HZ(DQ), ^{t}DQSCK, ^{t}LZ(DQS), ^{t}HZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where: *n* = 0, 1, 2, or 3; and *m* = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by ^{t}JIT(per).

^{t}QSH, ^{t}QSL

These parameters are affected by duty cycle jitter, represented by ^{t}CH(abs)min and ^{t}CL(abs)min. These parameters determine the absolute data valid window at the device pin. The absolute minimum data valid window at the device pin = min [(^{t}QSH(abs)min × ^{t}CK(avg)min - ^{t}DQSQmax - ^{t}QHSmax), (^{t}QSL(abs)min × ^{t}CK(avg)min - ^{t}DQSQmax - ^{t}QHSmax)]. This minimum data valid window must be met at the target frequency regardless of clock jitter.

^{t}RPST

^{t}RPST is affected by duty cycle jitter, represented by ^{t}CL(abs). Therefore, ^{t}RPST(abs)min can be specified by ^{t}CL(abs)min. ^{t}RPST(abs)min = ^{t}CL(abs)min - 0.05 = ^{t}QSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

^{t}DS, ^{t}DH

These parameters are measured from a data signal (DM*n* *or* DQ*m*, where *n* = 0, 1, 2, 3; and *m* = DQ[31:0]) transition edge to its respective data strobe signal (DQS*n*, DQS*n*#: *n* = 0,1,2,3) crossing. The specification values are not affected by the amount of ^{t}JIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DSS, ^{t}DSH

These parameters are measured from a data strobe signal crossing (DQS*x*, DQS*x*#) to its clock signal crossing (CK/CK#). The specification values are not affected by the amount of ^{t}JIT(per)) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DQSS

^{t}DQSS is measured from the clock signal crossing (CK/CK#) to the first latching data strobe signal crossing (DQS*x*, DQS*x*#). When the device is operated with input clock jitter, this parameter must be derated by the actual ^{t}JIT(per),act of the input clock in excess of ^{t}JIT(per),allowed.

$$^{t}\text{DQSS(min,derated)} = 0.75 - \left(\frac{^{t}\text{JIT(per),act,min} - ^{t}\text{JIT(per),allowed, min}}{^{t}\text{CK(avg)}}\right)$$

$$^{t}\text{DQSS(max,derated)} = 1.25 - \left(\frac{^{t}\text{JIT(per),act,max} - ^{t}\text{JIT(per),allowed, max}}{^{t}\text{CK(avg)}}\right)$$

For example, if the measured jitter into an LPDDR2-800 device has ^{t}CK(avg) = 2500ps, ^{t}JIT(per),act,min = -172ps, and ^{t}JIT(per),act,max = +193ps, then:

^{t}DQSS,(min,derated) = 0.75 - (^{t}JIT(per),act,min - ^{t}JIT(per),allowed,min)/^{t}CK(avg) = 0.75 - (-172 + 100)/2500 = 0.7788 ^{t}CK(avg), *and*

^{t}DQSS,(max,derated) = 1.25 - (^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) =

1.25 - (193 - 100)/2500 = 1.2128 ^{t}CK(avg).

Refresh Requirements

Table 121: Refresh Requirement Parameters (Per Density)

Parameter		Symbol	64Mb	128Mb	256Mb	512Mb	1Gb	2Gb	4Gb	8Gb	Unit
Number of banks			4	4	4	4	8	8	8	8	
Refresh window: T_{CASE} ≤ 85°		^{t}REFW	32	32	32	32	32	32	32	32	ms
Refresh window: 85°C < T_{CASE} ≤ 105°C		^{t}REFW	8	8	8	8	8	8	8	8	ms
Required number of REFRESH commands (MIN)		R	2048	2048	4096	4096	4096	8192	8192	8192	
Average time between REFRESH commands (for reference only) T_{CASE} ≤ 85°C	REFab	^{t}REFI	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	µs
	REFpb	^{t}REFIpb	(REFpb not supported below 1Gb)				0.975	0.4875	0.4875	0.4875	µs
Refresh cycle time		^{t}RFCab	90	90	90	90	130	130	130	210	ns
Per-bank REFRESH cycle time		^{t}RFCpb	na				60	60	60	90	ns
Burst REFRESH window = 4 × 8 × ^{t}RFCab		^{t}REFBW	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	µs

AC Timing

Table 122: AC Timing

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the ^{t}CK minimum conditions (in multiples of ^{t}CK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	^{t}CK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Maximum frequency		–	–	533	466	400	333	266	200	166	MHz	
Clock Timing												
Average clock period	^{t}CK(avg)	MIN	–	1.875	2.15	2.5	3	3.75	5	6	ns	
		MAX	–	100	100	100	100	100	100	100		
Average HIGH pulse width	^{t}CH(avg)	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	^{t}CK (avg)	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Average LOW pulse width	^{t}CL(avg)	MIN	–	0.45	0.45	0.45	0.45	0.45	0.45	0.45	^{t}CK (avg)	
		MAX	–	0.55	0.55	0.55	0.55	0.55	0.55	0.55		
Absolute clock period	^{t}CK(abs)	MIN	–	^{t}CK(avg)min ± ^{t}JIT(per)min							ps	
Absolute clock HIGH pulse width	^{t}CH(abs)	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	^{t}CK (avg)	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Absolute clock LOW pulse width	^{t}CL(abs)	MIN	–	0.43	0.43	0.43	0.43	0.43	0.43	0.43	^{t}CK (avg)	
		MAX	–	0.57	0.57	0.57	0.57	0.57	0.57	0.57		
Clock period jitter (with supported jitter)	^{t}JIT(per), allowed	MIN	–	-90	-95	-100	-110	-120	-140	-150	ps	
		MAX	–	90	95	100	110	120	140	150		
Maximum clock jitter between two consecutive clock cycles (with supported jitter)	^{t}JIT(cc), allowed	MAX	–	180	190	200	220	240	280	300	ps	
Duty cycle jitter (with supported jitter)	^{t}JIT(duty), allowed	MIN	–	MIN ((^{t}CH(abs),min - ^{t}CH(avg),min), (^{t}CL(abs),min - ^{t}CL(avg),min)) × ^{t}CK(avg)							ps	
		MAX	–	MAX ((^{t}CH(abs),max - ^{t}CH(avg),max), (^{t}CL(abs),max - ^{t}CL(avg),max)) × ^{t}CK(avg)								
Cumulative errors across 2 cycles	^{t}ERR(2per), allowed	MIN	–	-132	-140	-147	-162	-177	-206	-221	ps	
		MAX	–	132	140	147	162	177	206	221		
Cumulative errors across 3 cycles	^{t}ERR(3per), allowed	MIN	–	-157	-166	-175	-192	-210	-245	-262	ps	
		MAX	–	157	166	175	192	210	245	262		
Cumulative errors across 4 cycles	^{t}ERR(4per), allowed	MIN	–	-175	-185	-194	-214	-233	-272	-291	ps	
		MAX	–	175	185	194	214	233	272	291		
Cumulative errors across 5 cycles	^{t}ERR(5per), allowed	MIN	–	-188	-199	-209	-230	-251	-293	-314	ps	
		MAX	–	188	199	209	230	251	293	314		
Cumulative errors across 6 cycles	^{t}ERR(6per), allowed	MIN	–	-200	-211	-222	-244	-266	-311	-333	ps	
		MAX	–	200	211	222	244	266	311	333		
Cumulative errors across 7 cycles	^{t}ERR(7per), allowed	MIN	–	-209	-221	-232	-256	-279	-325	-348	ps	
		MAX	–	209	221	232	256	279	325	348		

Table 122: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the tCK minimum conditions (in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Cumulative errors across 8 cycles	tERR(8per), allowed	MIN	–	-217	-229	-241	-266	-290	-338	-362	ps	
		MAX	–	217	229	241	266	290	338	362		
Cumulative errors across 9 cycles	tERR(9per), allowed	MIN	–	-224	-237	-249	-274	-299	-349	-374	ps	
		MAX	–	224	237	249	274	299	349	374		
Cumulative errors across 10 cycles	tERR(10per), allowed	MIN	–	-231	-244	-257	-282	-308	-359	-385	ps	
		MAX	–	231	244	257	282	308	359	385		
Cumulative errors across 11 cycles	tERR(11per), allowed	MIN	–	-237	-250	-263	-289	-316	-368	-395	ps	
		MAX	–	237	250	263	289	316	368	395		
Cumulative errors across 12 cycles	tERR(12per), allowed	MIN	–	-242	-256	-269	-296	-323	-377	-403	ps	
		MAX	–	242	256	269	296	323	377	403		
Cumulative errors across *n* = 13, 14, 15…, 49, 50 cycles	tERR(nper), allowed	MIN	tERR(nper),allowed,min = (1 + 0.68ln(n)) × tJIT(per),allowed,min								ps	
		MAX	tERR(nper), allowed,max = (1 + 0.68ln(n)) × tJIT(per),allowed,max									
ZQ Calibration Parameters												
Initialization calibration time	tZQINIT	MIN	–	1	1	1	1	1	1	1	µs	
Long calibration time	tZQCL	MIN	6	360	360	360	360	360	360	360	ns	
Short calibration time	tZQCS	MIN	6	90	90	90	90	90	90	90	ns	
Calibration RESET time	tZQRESET	MIN	3	50	50	50	50	50	50	50	ns	
READ Parameters[3]												
DQS output access time from CK/CK#	tDQSCK	MIN	–	2500	2500	2500	2500	2500	2500	2500	ps	
		MAX	–	5500	5500	5500	5500	5500	5500	5500		
DQSCK delta short	tDQSCKDS	MAX	–	330	380	450	540	670	900	1080	ps	4
DQSCK delta medium	tDQSCKDM	MAX	–	680	780	900	1050	1350	1800	1900	ps	5
DQSCK delta long	tDQSCKDL	MAX	–	920	1050	1200	1400	1800	2400	–	ps	6
DQS-DQ skew	tDQSQ	MAX	–	200	220	240	280	340	400	500	ps	
Data-hold skew factor	tQHS	MAX	–	230	260	280	340	400	480	600	ps	
DQS output HIGH pulse width	tQSH	MIN	–	tCH(abs) - 0.05							tCK (avg)	
DQS output LOW pulse width	tQSL	MIN	–	tCL(abs) - 0.05							tCK (avg)	
Data half period	tQHP	MIN	–	MIN (tQSH, tQSL)							tCK (avg)	
DQ/DQS output hold time from DQS	tQH	MIN	–	tQHP - tQHS							ps	

Table 122: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the ^{t}CK minimum conditions (in multiples of ^{t}CK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	^{t}CK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
READ preamble	^{t}RPRE	MIN	–	0.9	0.9	0.9	0.9	0.9	0.9	0.9	^{t}CK (avg)	7
READ postamble	^{t}RPST	MIN	–	^{t}CL(abs) - 0.05							^{t}CK (avg)	8
DQS Low-Z from clock	^{t}LZ(DQS)	MIN	–	^{t}DQSCK (MIN) - 300							ps	
DQ Low-Z from clock	^{t}LZ(DQ)	MIN	–	^{t}DQSCK(MIN) - (1.4 × ^{t}QHS(MAX))							ps	
DQS High-Z from clock	^{t}HZ(DQS)	MAX	–	^{t}DQSCK (MAX) - 100							ps	
DQ High-Z from clock	^{t}HZ(DQ)	MAX	–	^{t}DQSCK(MAX) + (1.4 × ^{t}DQSQ(MAX))							ps	
WRITE Parameters[3]												
DQ and DM input hold time (V_{REF} based)	^{t}DH	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input setup time (V_{REF} based)	^{t}DS	MIN	–	210	235	270	350	430	480	600	ps	
DQ and DM input pulse width	^{t}DIPW	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	^{t}CK (avg)	
Write command to first DQS latching transition	^{t}DQSS	MIN	–	0.75	0.75	0.75	0.75	0.75	0.75	0.75	^{t}CK (avg)	
		MAX	–	1.25	1.25	1.25	1.25	1.25	1.25	1.25	^{t}CK (avg)	
DQS input high-level width	^{t}DQSH	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	^{t}CK (avg)	
DQS input low-level width	^{t}DQSL	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	^{t}CK (avg)	
DQS falling edge to CK setup time	^{t}DSS	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	^{t}CK (avg)	
DQS falling edge hold time from CK	^{t}DSH	MIN	–	0.2	0.2	0.2	0.2	0.2	0.2	0.2	^{t}CK (avg)	
Write postamble	^{t}WPST	MIN	–	0.4	0.4	0.4	0.4	0.4	0.4	0.4	^{t}CK (avg)	
Write preamble	^{t}WPRE	MIN	–	0.35	0.35	0.35	0.35	0.35	0.35	0.35	^{t}CK (avg)	
CKE Input Parameters												
CKE minimum pulse width (HIGH and LOW pulse width)	^{t}CKE	MIN	3	3	3	3	3	3	3	3	^{t}CK (avg)	
CKE input setup time	^{t}ISCKE	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	^{t}CK (avg)	9
CKE input hold time	^{t}IHCKE	MIN	–	0.25	0.25	0.25	0.25	0.25	0.25	0.25	^{t}CK (avg)	10

Table 122: AC Timing (Continued)

Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the tCK minimum conditions (in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Command Address Input Parameters[3]												
Address and control input setup time	tIS	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input hold time	tIH	MIN	–	220	250	290	370	460	600	740	ps	11
Address and control input pulse width	tIPW	MIN	–	0.40	0.40	0.40	0.40	0.40	0.40	0.40	tCK (avg)	
Boot Parameters (10 MHz–55 MHz)[12, 13, 14]												
Clock cycle time	tCKb	MAX	–	100	100	100	100	100	100	100	ns	
		MIN	–	18	18	18	18	18	18	18		
CKE input setup time	tISCKEb	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
CKE input hold time	tIHCKEb	MIN	–	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns	
Address and control input setup time	tISb	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
Address and control input hold time	tIHb	MIN	–	1150	1150	1150	1150	1150	1150	1150	ps	
DQS output data access time from CK/CK#	tDQSCKb	MIN	–	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	
		MAX	–	10.0	10.0	10.0	10.0	10.0	10.0	10.0		
Data strobe edge to output data edge	tDQSQb	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Data hold skew factor	tQHSb	MAX	–	1.2	1.2	1.2	1.2	1.2	1.2	1.2	ns	
Mode Register Parameters												
MODE REGISTER WRITE command period	tMRW	MIN	3	3	3	3	3	3	3	3	tCK (avg)	
MODE REGISTER READ command period	tMRR	MIN	2	2	2	2	2	2	2	2	tCK (avg)	
Core Parameters[15]												
READ latency	RL	MIN	3	8	7	6	5	4	3	3	tCK (avg)	
WRITE latency	WL	MIN	1	4	4	3	2	2	1	1	tCK (avg)	
ACTIVATE-to-ACTIVATE command period	tRC	MIN	–	tRAS + tRPab (with all-bank precharge), tRAS + tRPpb (with per-bank precharge)							ns	17
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	tCKESR	MIN	3	15	15	15	15	15	15	15	ns	
SELF REFRESH exit to next valid command delay	tXSR	MIN	2	tRFCab + 10							ns	

Table 122: AC Timing (Continued)

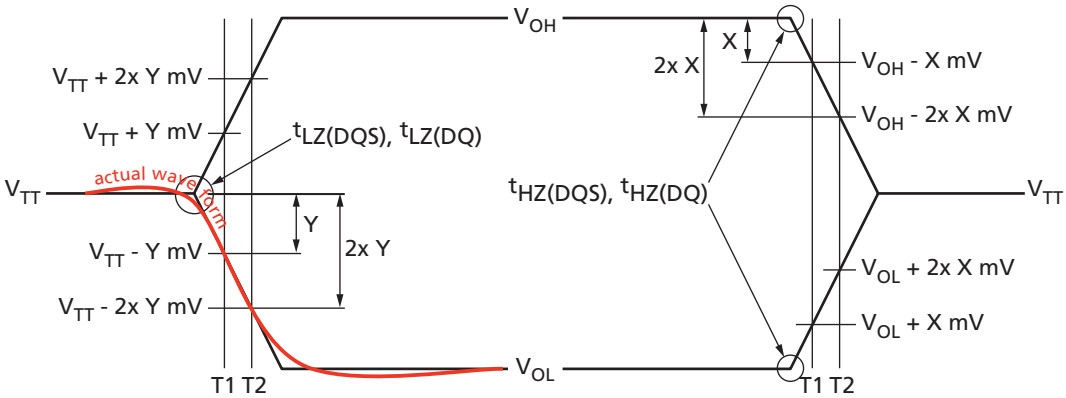
Notes 1–2 apply to all parameters and conditions. AC timing parameters must satisfy the tCK minimum conditions (in multiples of tCK) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min/ Max	tCK Min	Data Rate							Unit	Notes
				1066	933	800	667	533	400	333		
Exit power-down to next valid command delay	tXP	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
CAS-to-CAS delay	tCCD	MIN	2	2	2	2	2	2	2	2	tCK (avg)	
Internal READ to PRECHARGE command delay	tRTP	MIN	2	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns	
RAS-to-CAS delay	tRCD	Fast	3	15	15	15	15	15	15	15	ns	
		TYP	3	18	18	18	18	18	18	18		
Row precharge time (single bank)	tRPpb	Fast	3	15	15	15	15	15	15	15	ns	
		TYP	3	18	18	18	18	18	18	18		
Row precharge time (all banks)	tRPab 4-bank	Fast	3	15	15	15	15	15	15	15	ns	
		TYP	3	18	18	18	18	18	18	18		
Row precharge time (all banks)	tRPab 8-bank	Fast	3	18	18	18	18	18	18	18	ns	
		TYP	3	21	21	21	21	21	21	21		
Row active time	tRAS	MIN	3	42	42	42	42	42	42	42	ns	
		MAX	–	70	70	70	70	70	70	70	µs	
WRITE recovery time	tWR	MIN	3	15	15	15	15	15	15	15	ns	
Internal WRITE-to-READ command delay	tWTR	MIN	2	7.5	7.5	7.5	7.5	7.5	10	10	ns	
Active bank *a* to active bank *b*	tRRD	MIN	2	10	10	10	10	10	10	10	ns	
Four-bank activate window	tFAW	MIN	8	50	50	50	50	50	50	60	ns	
Minimum deep power-down time	tDPD	MIN	–	500	500	500	500	500	500	500	µs	
Temperature Derating[16]												
tDQSCK derating	tDQSCK (derated)	MAX	–	5620	6000	6000	6000	6000	6000	6000	ps	
Core timing temperature derating	tRCD (derated)	MIN	–	tRCD + 1.875							ns	
	tRC (derated)	MIN	–	tRC + 1.875							ns	
	tRAS (derated)	MIN	–	tRAS + 1.875							ns	
	tRP (derated)	MIN	–	tRP + 1.875							ns	
	tRRD (derated)	MIN	–	tRRD + 1.875							ns	

Notes: 1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.

2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to V_{REF}.
4. ^{t}DQSCKDS is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. ^{t}DQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
5. ^{t}DQSCKDM is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a 1.6µs rolling window. ^{t}DQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
6. ^{t}DQSCKDL is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a 32ms rolling window. ^{t}DQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
   For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). ^{t}HZ and ^{t}LZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for ^{t}RPST, ^{t}HZ(DQS) and ^{t}HZ(DQ)), or begins driving (for ^{t}RPRE, ^{t}LZ(DQS), ^{t}LZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ) or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters ^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as single-ended. The timing parameters ^{t}RPRE and ^{t}RPST are determined from the differential signal DQS/DQS#.

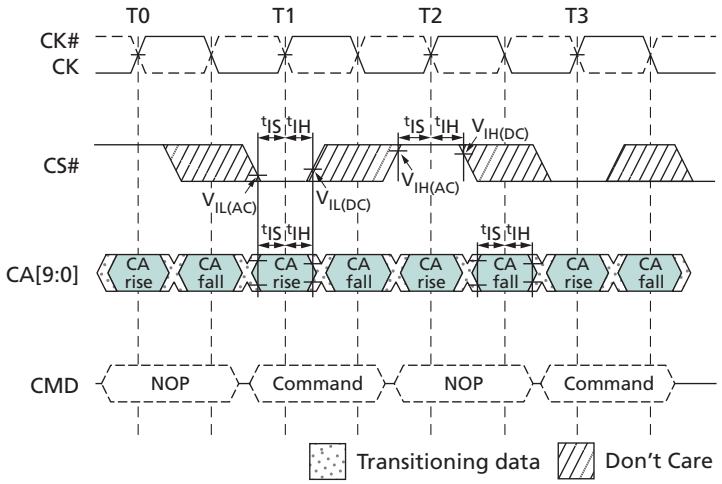
Output Transition Timing



7. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.
8. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal.
9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/CK# crossing.
10. CKE input hold time is measured from CK/CK# crossing to CKE reaching a HIGH/LOW voltage level.
11. Input setup/hold time for signal (CA[9:0], CS#).
12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, ^{t}CK during boot is ^{t}CKb).

13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
14. The output skew parameters are measured with default output impedance settings using the reference load.
15. The minimum ^{t}CK column applies only when ^{t}CK is greater than 6ns.
16. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] = 04h) table).
17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

Figure 163: Command Input Setup and Hold Timing



Notes:
1. The setup and hold timing shown applies to all commands.
2. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see Power-Down (page 191).

CA and CS# Setup, Hold, and Derating

For all input signals (CA and CS#), the total required setup time (^{t}IS) and hold time (^{t}IH) is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) values to the Δ^{t}IS and Δ^{t}IH derating values, respectively. Example: ^{t}IS (total setup time) = ^{t}IS(base) + Δ^{t}IS. (See the series of tables following this section.)

The typical setup slew rate (^{t}IS) for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. The typical setup slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is consistently earlier than the typical slew rate line between the shaded $V_{REF(DC)}$-to-(AC) region, use the typical slew rate for the derating value (see the Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock figure). If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see the Tangent Line – ^{t}IS for CA and CS# Relative to Clock figure).

The hold (^{t}IH) typical slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The hold (^{t}IH) typical slew

rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is consistently later than the typical slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value (see the Typical Slew Rate – ^{t}IH for CA and CS# Relative to Clock figure). If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see the Tangent Line – ^{t}IH for CA and CS# Relative to Clock figure).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for a specified time, ^{t}VAC (see the Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ and < $V_{IL(AC)}$ table).

For slow slew rates the total setup time could be a negative value (that is, a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the AC220 table, the derating values are obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 123: CA and CS# Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
^{t}IS (base)	0	30	70	150	240	300	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±220mV
^{t}IH (base)	90	120	160	240	330	390	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±130mV

Note: 1. AC/DC referenced for 1 V/ns CA and CS# slew rate, and 2 V/ns differential CK/CK# slew rate.

Table 124: CA and CS# Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	255	200	
^{t}IS (base)	300	440	600	850	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±300mV
^{t}IH (base)	400	540	700	950	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±200mV

Note: 1. AC/DC referenced for 1 V/ns CA and CS# slew rate, and 2 V/ns differential CK/CK# slew rate.

Table 125: Derating Values for AC/DC-Based $^{t}IS/^{t}IH$ (AC220)

$\Delta^{t}IS$, $\Delta^{t}IH$ derating in ps

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
CA, CS# slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.

Table 126: Derating Values for AC/DC-Based $^{t}IS/^{t}IH$ (AC300)

$\Delta^{t}IS$, $\Delta^{t}IH$ derating in ps

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
CA, CS# slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

Table 127: Required Time for Valid Transition – $^{t}VAC > V_{IH(AC)}$ and $< V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 300mV (ps)		^{t}VAC at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–

Table 127: Required Time for Valid Transition – $^{t}VAC > V_{IH(AC)}$ and $< V_{IL(AC)}$ (Continued)

Slew Rate (V/ns)	^{t}VAC at 300mV (ps)		^{t}VAC at 220mV (ps)	
	Min	Max	Min	Max
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–

Figure 164: Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock

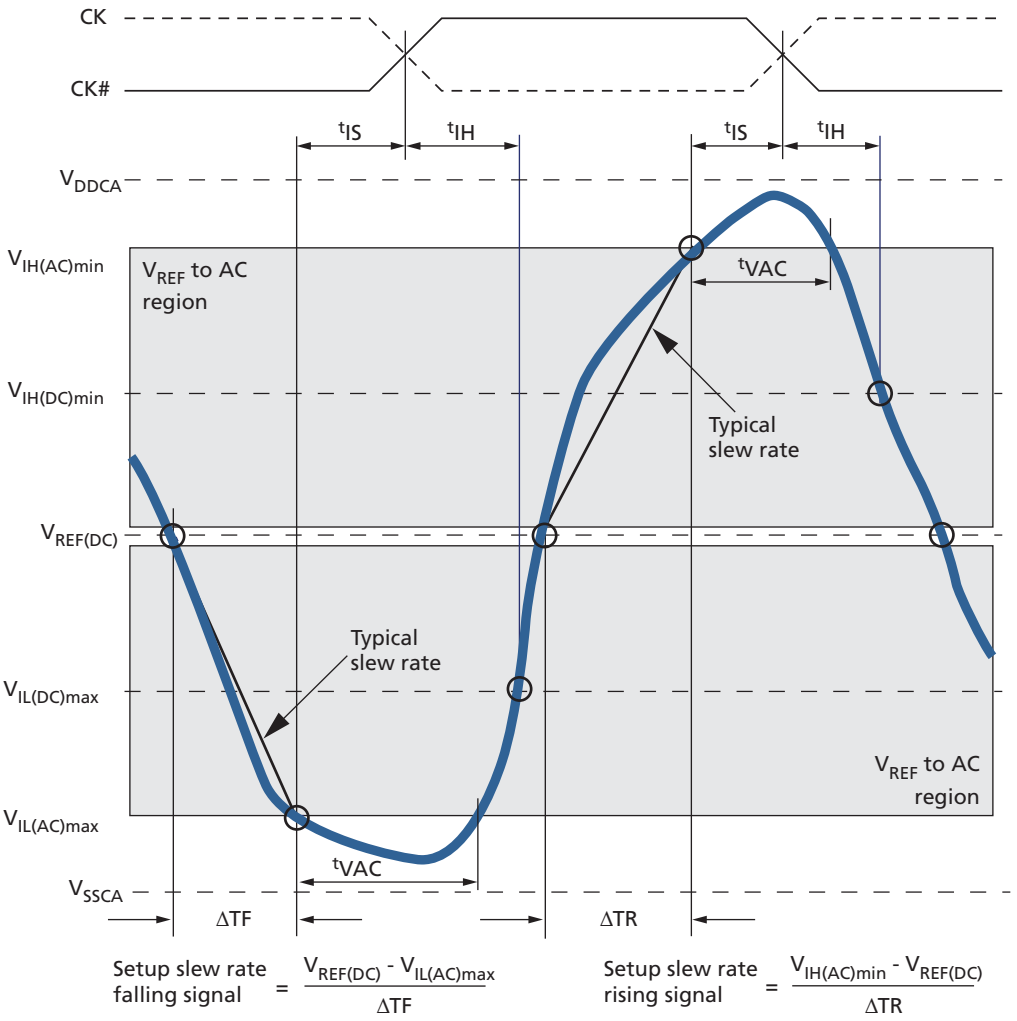
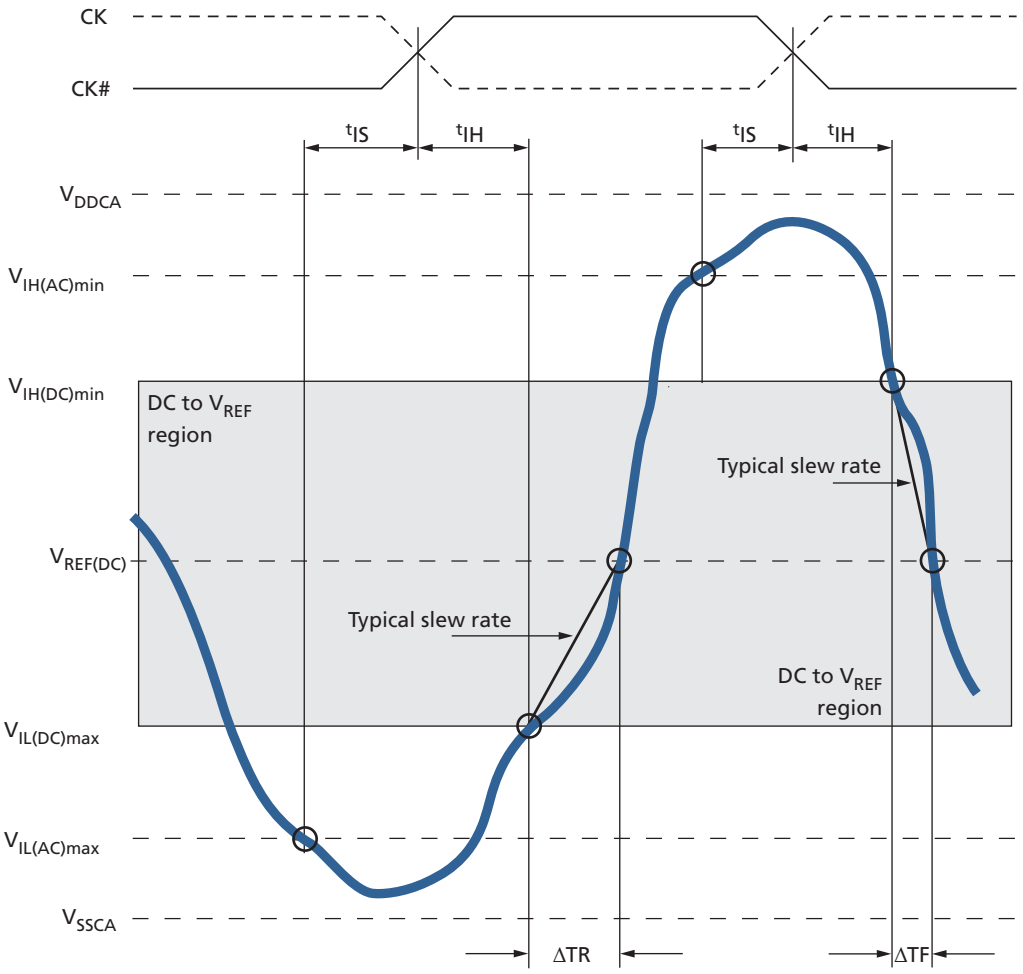


Figure 165: Typical Slew Rate – ^{t}IH for CA and CS# Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Figure 166: Tangent Line – ^{t}IS for CA and CS# Relative to Clock

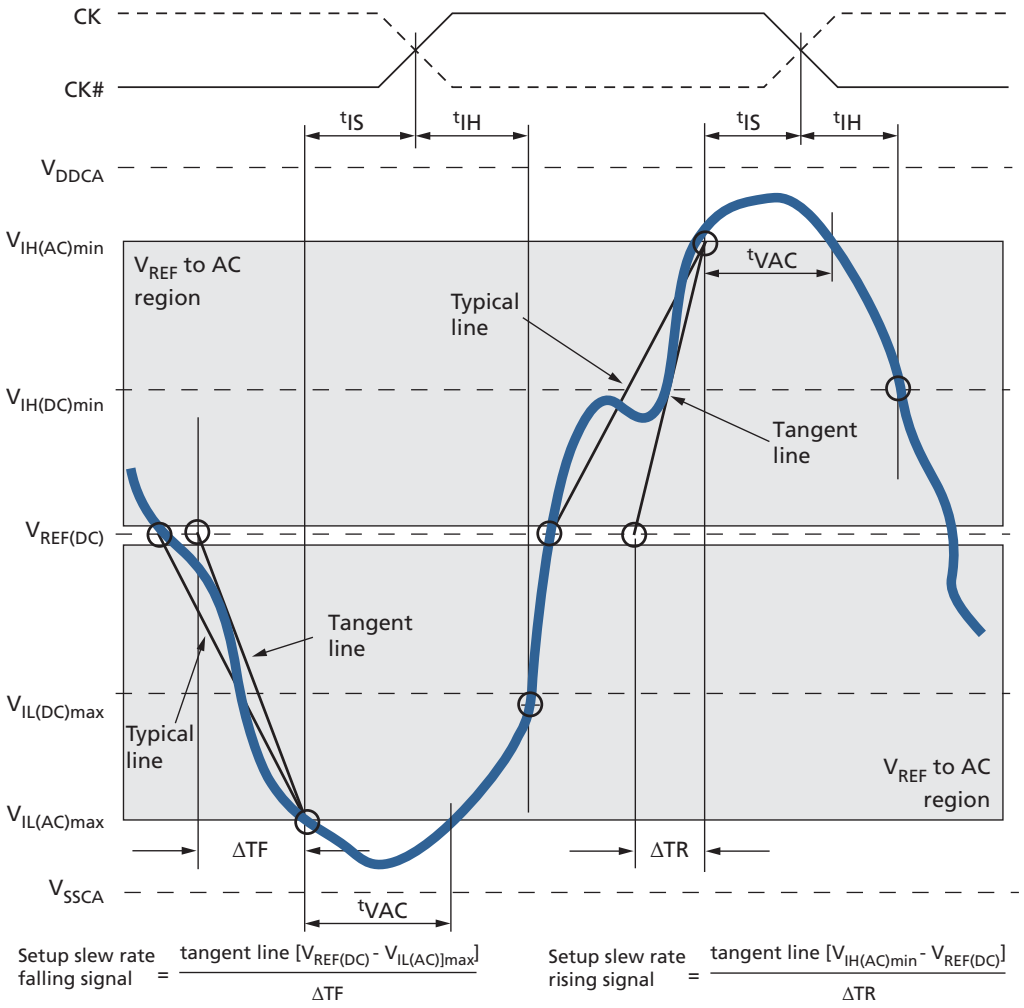
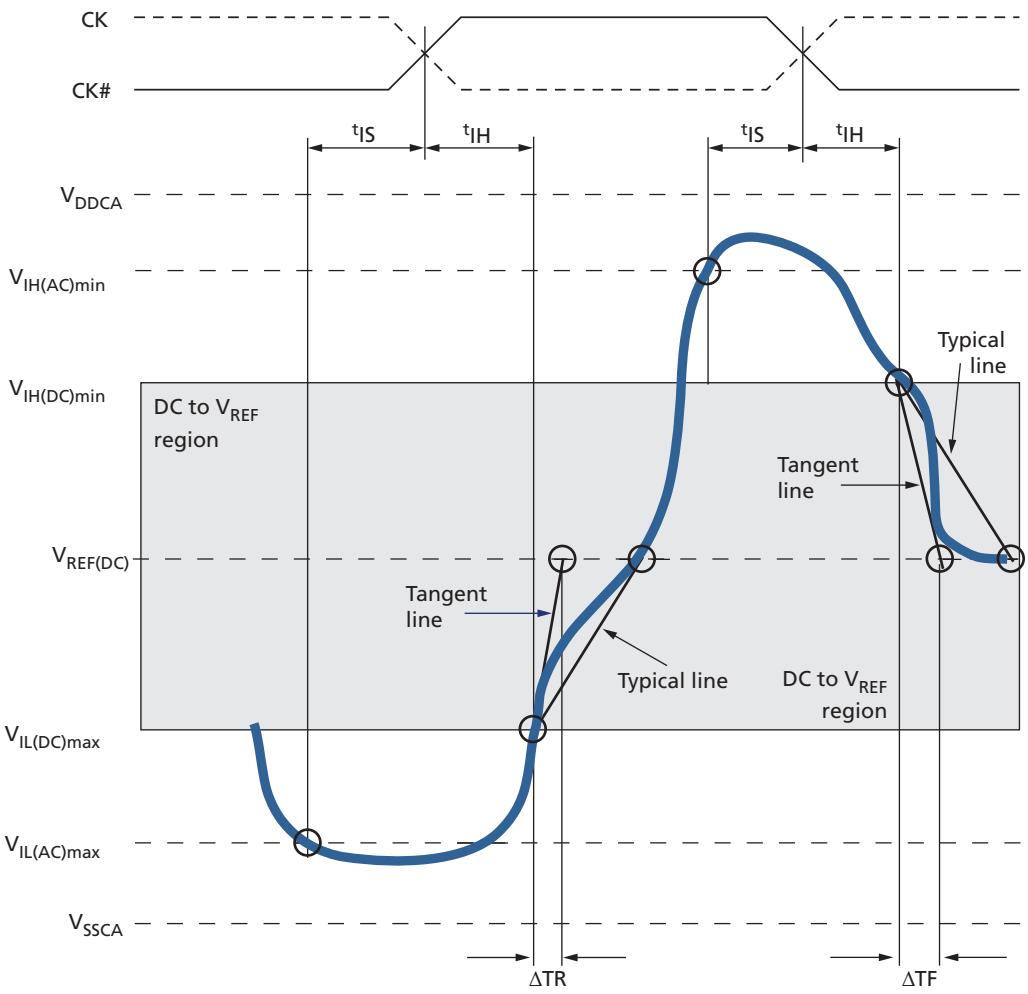


Figure 167: Tangent Line – ^{t}IH for CA and CS# Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (^{t}DS) and hold time (^{t}DH) by adding the data sheet ^{t}DS(base) and ^{t}DH(base) values (see the following table) to the Δ^{t}DS and Δ^{t}DH derating values, respectively (see the following derating tables). Example: ^{t}DS = ^{t}DS(base) + Δ^{t}DS.

The typical ^{t}DS slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. The typical ^{t}DS slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$ (see the Typical Slew Rate and ^{t}VAC – ^{t}DS for DQ Relative to Strobe figure).

If the actual signal is consistently earlier than the typical slew rate line in the figure, "Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock (CA and CS# Setup, Hold, and Derating), the area shaded gray between the $V_{REF(DC)}$ region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$ region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see figure "Tangent Line – ^{t}IS for CA and CS# Relative to Clock" in CA and CS# Setup, Hold, and Derating).

Th^{t}e typical ^{t}DH slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The typical ^{t}DH slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$ (see the Typical Slew Rate – DH for DQ Relative to Strobe figure).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for the derating value (see the Tangent Line – ^{t}DH for DQ with Respect to Strobe figure).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for the specified time, ^{t}VAC (see the Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$ table).

The total setup time for slow slew rates could be negative (that is, a valid input signal may not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the following tables, the derating values can be obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 128: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
^{t}DS (base)	-10	15	50	130	210	230	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±220mV

Table 128: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) (Continued)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
^{t}DH (base)	80	105	140	220	300	320	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±130mV

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate.

Table 129: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate				Reference
	400	333	255	200	
^{t}DS (base)	180	300	450	700	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±300mV
^{t}DH (base)	280	400	550	800	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±200mV

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate.

Table 130: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC220)

Δ^{t}DS, Δ^{t}DH derating in ps

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: 1. Shaded cells are not supported.

Table 131: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC300)

Δ^{t}DS, Δ^{t}DH derating in ps

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	**0**	**0**	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4												4	-35	-40	-11	-8

Note: 1. Shaded cells are not supported.

Table 132: Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 300mV (ps)		^{t}VAC at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–

Figure 168: Typical Slew Rate and ^{t}VAC – ^{t}DS for DQ Relative to Strobe

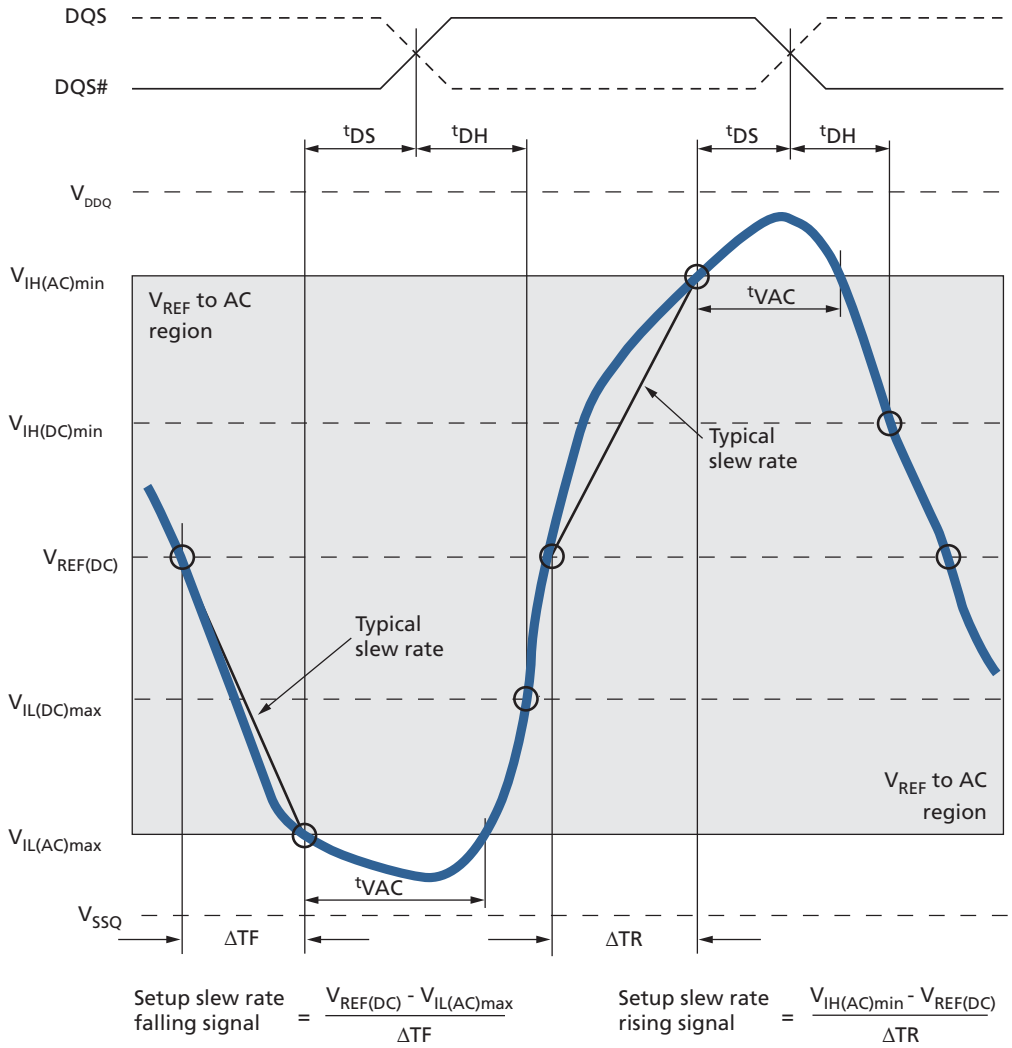


Figure 169: Typical Slew Rate – ^{t}DH for DQ Relative to Strobe

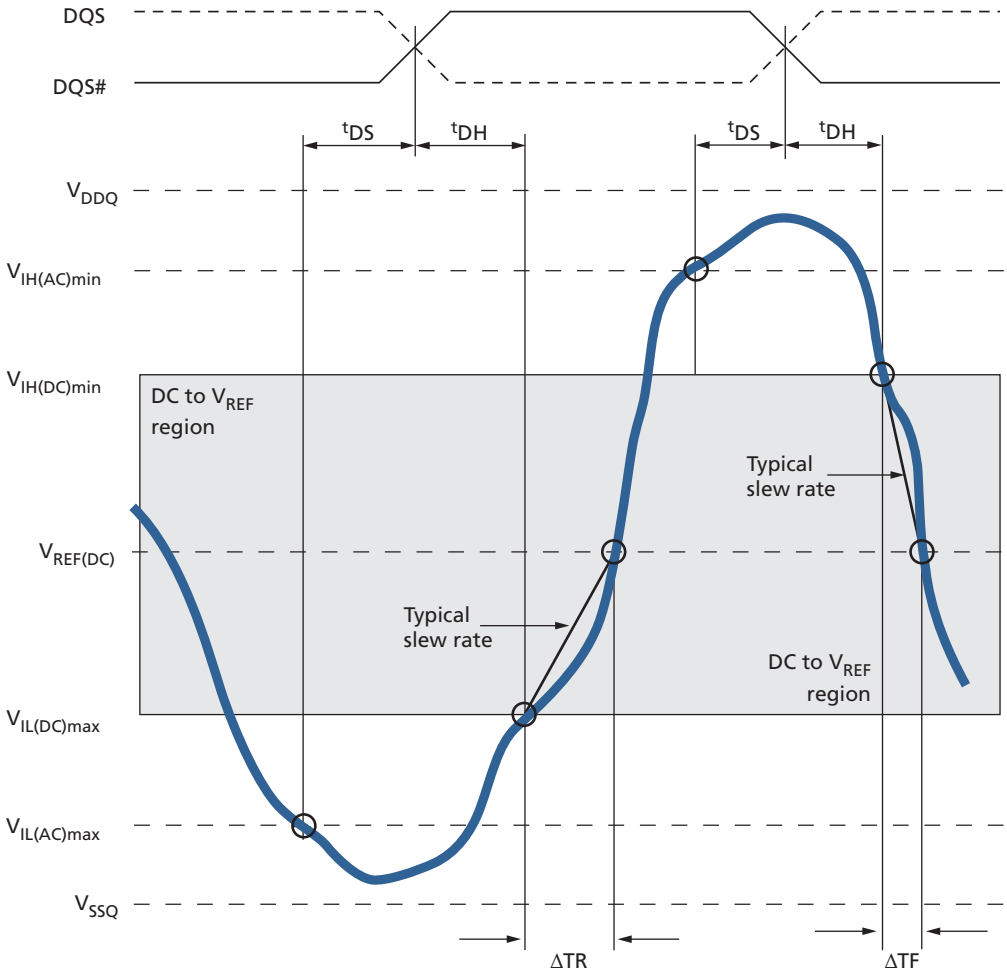


Figure 170: Tangent Line – ^{t}DS for DQ with Respect to Strobe

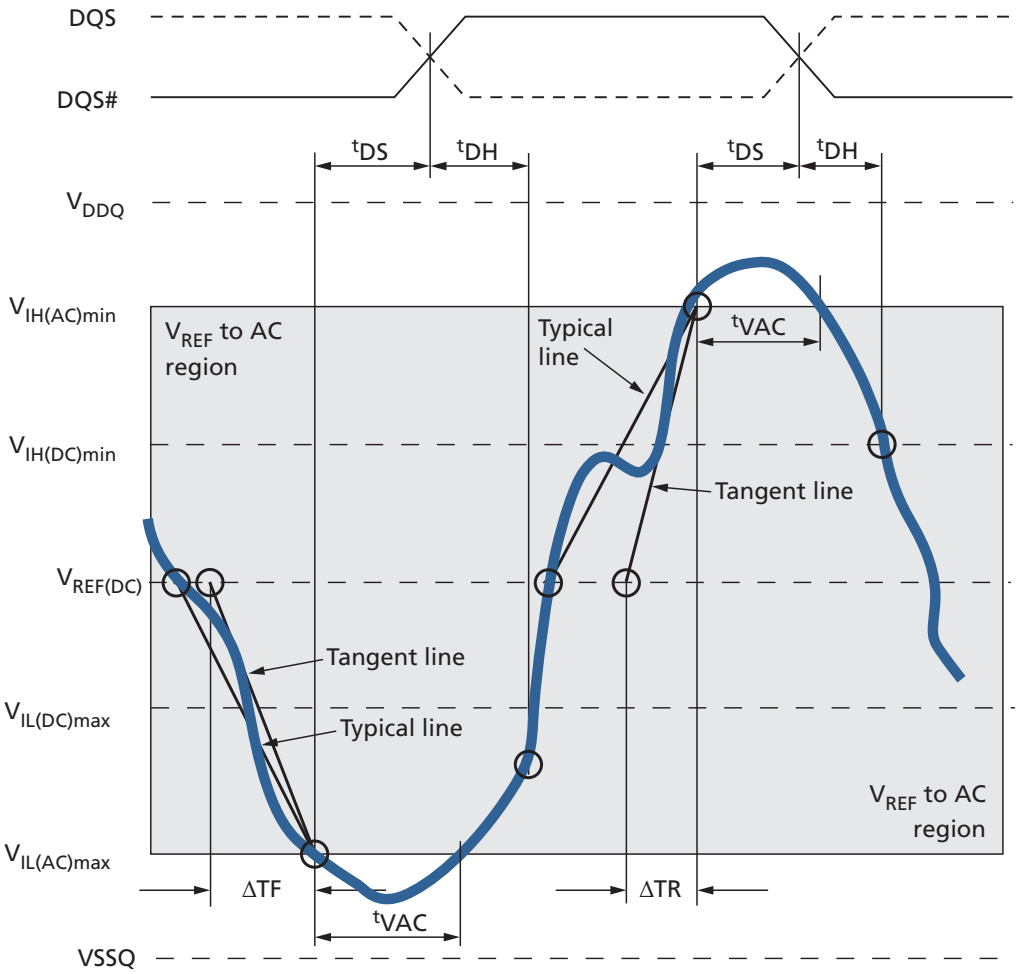
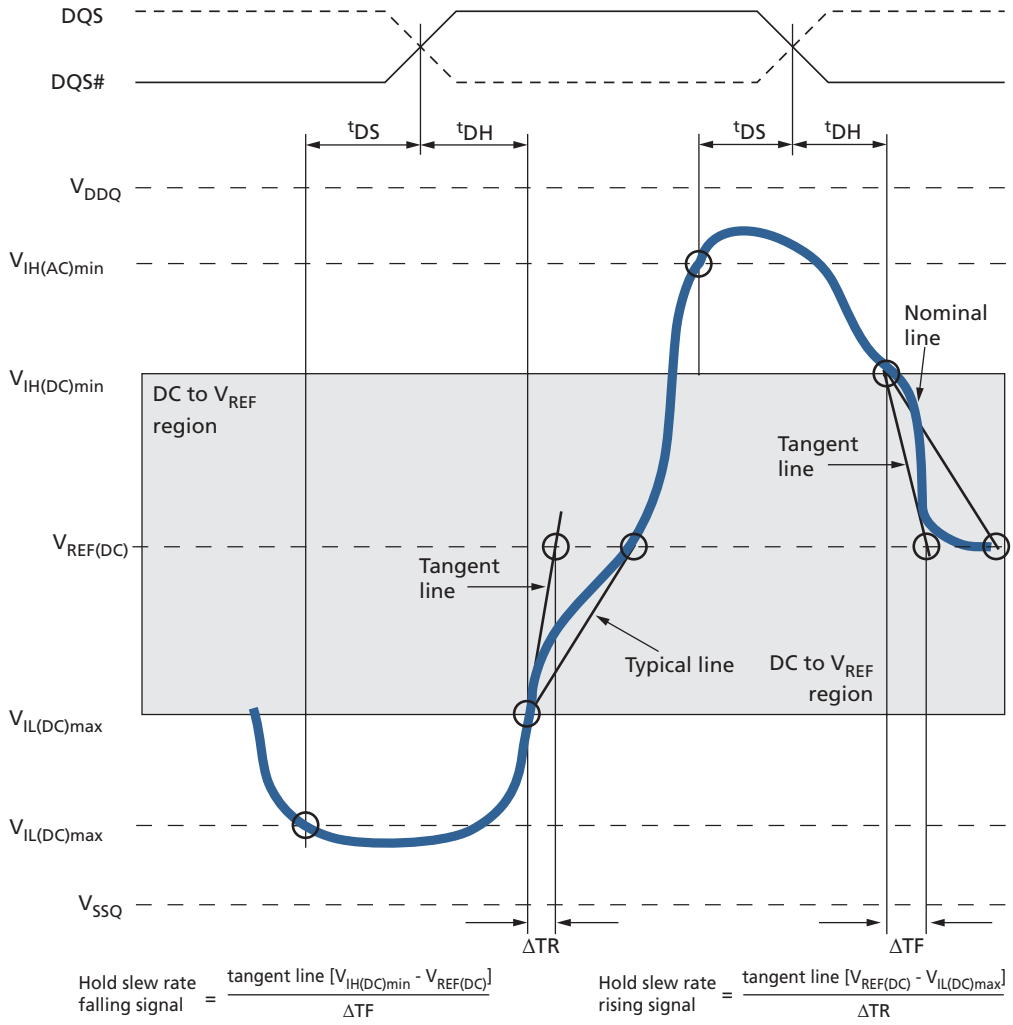


Figure 171: Tangent Line – ^{t}DH for DQ with Respect to Strobe



Revision History

Rev. E – 06/16

- Updated legal status to Production

Rev. D – 05/16

- Added industrial temperature range part number
- Added Key Timing parameters table and Configuration Addressing table to Features
- Corrected Ball Assignments table in Ball Assignments and Descriptions section (added ZQ1 to ball F3)
- Corrected Device Diagrams (added ZQ1)

Rev. C – 01/16

- Added part number table to Features

Rev. B – 02/15

- Updated x16 NAND to x8 NAND

Rev. A – 01/15

- Initial release

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