MT312

Satellite Channel Decoder Design Manual

Part Number: MT312

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ZARLINK™ SEMICONDUCTOR

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Overview

The MT312 is a QPSK/BPSK 1 to 45MS/s demodulator and channel decoder for digital satellite television transmissions compliant to both DVB-S and DSS standards and other systems, such as LMDS, that use the same architecture.

A Command Driven Control (CDC) system is provided making the MT312 very simple to program. After the tuner has been programmed to the required frequency to acquire a DVB transmission, the MT312 requires a minimum of five registers to be written.

The MT312 provides a monitor of bit error rate after the QPSK module and also after the Viterbi module. For receiver installation, a high speed scan or 'blind search' mode is available. This allows all signals from a given satellite to be evaluated for frequency, symbol rate and convolutional coding scheme. The phase of the IQ signals can be automatically determined.

Full DiSEqC™ v2.2 is provided for both writing and reading DiSEqC™ messages. Storage in registers for up to eight data bytes sent and eight data bytes received is provided.

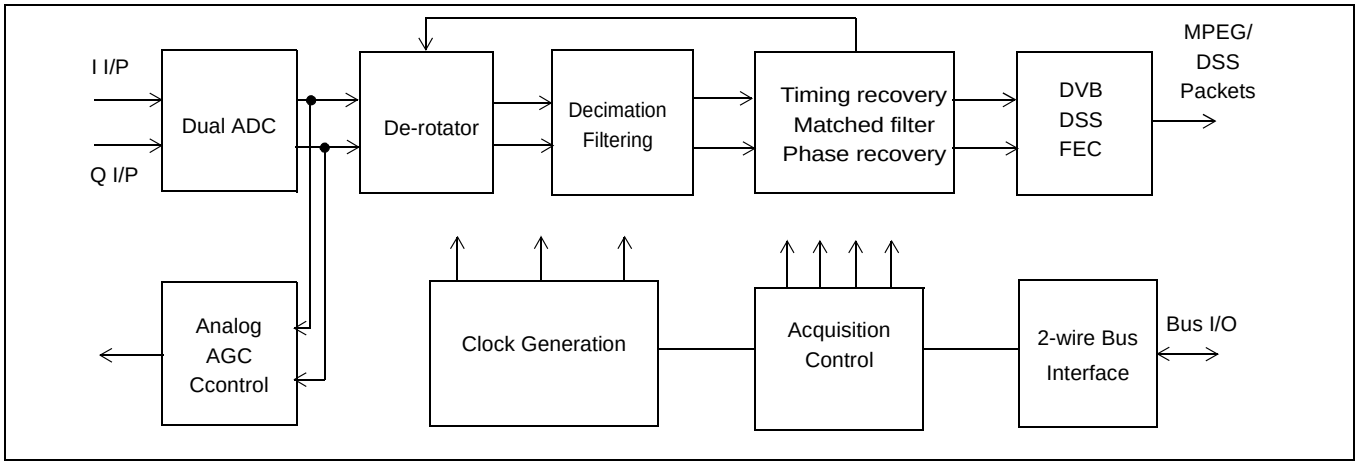

Figure 1 - MT312 functional block diagram

Additional Features

- 2-wire bus microprocessor interface.
- All-digital clock and carrier recovery.
- On-chip PLL clock generation using a low cost 10 to 15MHz crystal.
- 3.3V operation.
- 80 pin MQFP package.
- Low external component count.
- Commercial temperature range 0 to 70°C.

Demodulator

- BPSK or QPSK programmable.
- Optional fast acquisition mode for low symbol rates.

Viterbi

- Programmable decoder rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8.
- Automatic spectrum resolution of IQ phase.
- Constraint length k=7.
- Trace back depth 128.
- Extensive SNR and BER monitors.

De-Interleaver

- Compliant with DVB and DSS standards.

Reed-Solomon

- (204, 188) for DVB and (146,130) for DSS.
- Reed-Solomon bit-error-rate monitor to indicate Viterbi performance.

De-Scrambler

- EBU specification de-scrambler for DVB mode.

Outputs

- MPEG transport parallel & serial output.
- MPEG clock input for external synchronising of MPEG data output.
- Integrated MPEG2 TEI bit processing for DVB only.

Application Support

- Channel decoder system evaluation board.
- Windows based evaluation software.
- ANSI-C generic software.

1.0 Application Diagram

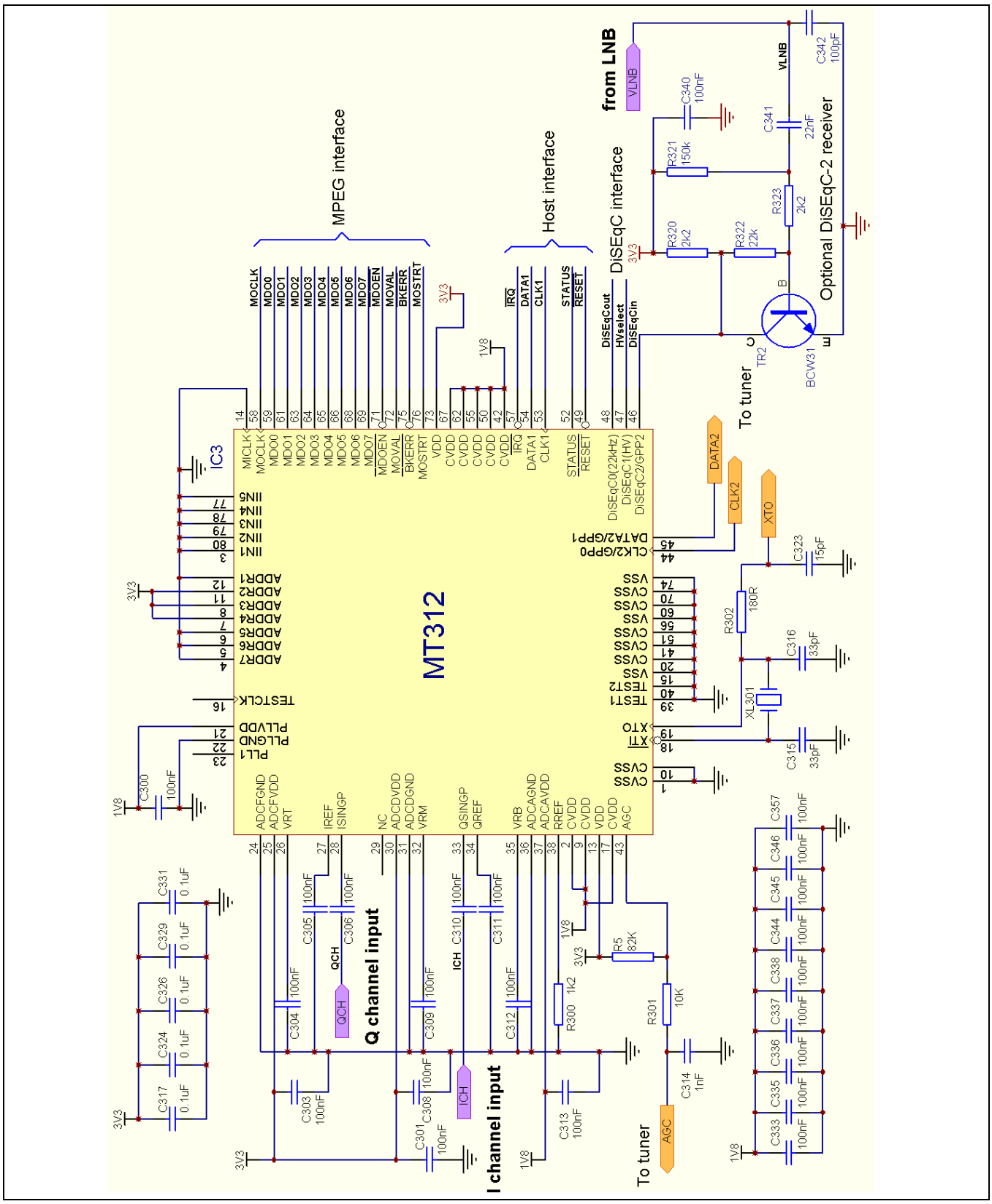

Figure 2 - Application schematic

2.0 Functional Overview

2.1 Introduction

MT312 is a single-chip variable rate digital QPSK/BPSK satellite demodulator and channel decoder. The MT312 accepts baseband in-phase and quadrature analogue signals and delivers an MPEG or DSS packet data stream. Digital filtering in MT312 removes the need for programmable external anti-alias filtering for all symbol rates from 1 to 45MS/s. Frequency, timing and carrier phase recovery are all digital and the only feedback to the analogue front-end is for automatic gain control. The digital phase-recovery loop enables very fine bandwidth control that is needed to overcome performance degradation due to phase and thermal noise.

All acquisition algorithms are built into the MT312 controller. The MT312 can be operated in a Command Driven Control (CDC) mode by specifying the symbol rate and Viterbi code rate. There is also a provision for a search for unknown symbol rates and Viterbi code rates.

2.2 Analogue-to-Digital converter

The MT312 contains dual 6-bit A/D converters which each sample a 500mVpp single-ended analogue input at up to 91MHz. The fixed rate sampling clock is provided on-chip using a programmable PLL needing only a low cost 10 to 15MHz crystal. Different crystal frequencies can be combined with different PLL ratios, depending on the maximum symbol rate, allowing a flexible approach to clock generation.

2.3 QPSK demodulator

The demodulator in the MT312 consists of signal amplitude offset compensation, frequency offset compensation, decimation filtering, carrier recovery, symbol recovery and matched filtering. The decimation filters give continuous operation from 2Mbits/s to 90Mbits/s allowing one receiver to cover the needs of the consumer market as well as the single carrier per channel (SCPC) market with the same components without compromising performance, that is, the channel reception is within 0.5dB from theory. For a given symbol rate, control algorithms on the chip detect the number of decimation stages needed and switch them in automatically.

The frequency offset compensation circuitry is capable of tracking out up to ±15MHz frequency offset. This allows the system to cope with relatively large frequency uncertainties introduced by the Low Noise Block (LNB). Full control of the LNB is provided by the DiSEqC™ outputs from the MT312. Horizontal/vertical polarisation and an instruction modulated 22kHz signal are available under register control. All DiSEqC™v2.2 functions are implemented on the MT312. An internal state machine that handles all the demodulator functions controls the signal tracking and acquisition. Various preset modes are available as well as blind acquisition where the receiver has no prior knowledge of the received signal. Fast acquisition algorithms have been provided for low symbol rate applications. Full interactive control of the acquisition function is possible for debug purposes. In the event of a signal fade or a cycle slip, the QPSK demodulator allows sufficient time for the FEC to reacquire lock, for example, via a phase rotation in the Viterbi decoder. This is to minimise the loss of signal due to the signal fade. Only if the FEC fails to re-acquire lock for a long period (which is programmable) the QPSK will try to re-acquire the signal.

The matched filter is a root-raised-cosine filter with either 0.20 or 0.35 roll-off, compliant with DSS and DVB standards. Although not a part of the DVB standard, MT312 allows a roll-off of 0.20 to be used with other DVB parameters. An AGC signal is provided to control the signal levels in the tuner section of the receiver and ensure the signal level fed to the MT312 is set at an optimal value under all reception conditions.

The MT312 provides comprehensive information on the input signal and the state of the various parts of the device. This information includes Signal to Noise Ratio (SNR), signal level, AGC lock, timing and carrier lock signals. A maskable interrupt output is available to inform the host controller when events occur.

2.4 Forward error correction

The MT312 contains FEC blocks to enable error correction for DVB-S and DSS transmissions. The Viterbi decoder block can decode the convolutional code with rates 1/2, 2/3, 3/4, 5/6, 6/7 or 7/8. The block features automatic synchronisation, automatic IQ phase resolution and automatic code rate detection. The trace back depth of 128 provides better performance at high code rates and the built-in synchronisation algorithm allows the Viterbi decoder to lock onto signals with very poor signal-to-noise ratios. A Viterbi bit error rate monitor provides an indication of the error rate at the QPSK output.

The 24-bit error count register in the Viterbi decoder allows the bit error rate at the output of the QPSK demodulator to be monitored. The 24-bit bit error count register in the Reed-Solomon decoder allows the Viterbi output bit error rate to be monitored. The 16-bit uncorrectable packet counter yields information about the output packet error rate. These three monitors and the QPSK SNR register allow the performance of the device and its individual components, such as the QPSK demodulator and the Viterbi decoder, to be monitored extensively by the external microprocessor. The frame/byte align block features a sophisticated synchronisation algorithm to ensure reliable recovery of DVB and DSS framed data streams under worst case signal conditions. The de-interleaver uses on-chip RAM and is compatible with the DVB and DSS algorithms. The Reed-Solomon decoder is a truncated version of the (255, 239) code. The code block size is 204 for DVB and 146 for DSS. The decoder provides a count of the number of uncorrectable blocks as well as the number of bit errors corrected. The latter gives an indication of the bit error rate at the output of the Viterbi decoder. In DVB mode, spectrum de-scrambling is performed compatible with the DVB specification. The final output is a parallel or serial transport data stream, packet sync, data clock, and a block error signal. The data clock may be inverted under software control.

2.4.1 Viterbi error count measurement

A method of estimating the bit error rate at the output of the QPSK block has been provided in the Viterbi decoder. The incoming data bit stream is delayed and compared with the re-encoded and punctured version of the decoded bit stream to obtain a count of errors, see Figure 3. The measurement system has a programmable register to determine the number of data bits (the error count period) over which the count is being recorded. A read register indicates the error count result and an interrupt can be generated to inform the host microprocessor that a new count is available.

The VIT_ERRPER_H-M-L group of three registers is programmed with the required number of data bits (the error count period) (VIT_ERRPER[23:0]). The actual value is four times VIT_ERRPER[23:0]. The count of errors found during this period is loaded by the MT312 into the VIT_ERRCNT_H-M-L trio of registers when the bit count VIT_ERRPER[23:0] is reached. At the same time an interrupt is generated on the $\overline{IRQ}$ line. Setting the IE_FEC[2] bit in the IE_FEC register enables the interrupt. Reading the register does not clear VIT_ERRCNT [23:0], it is only loaded with the error count.

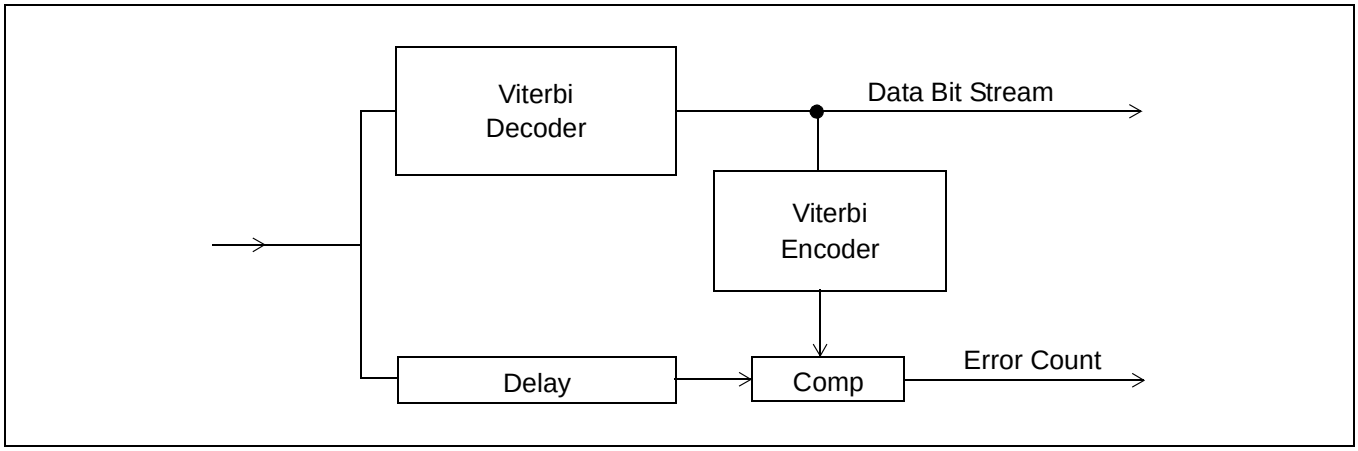

Figure 3 - Viterbi block diagram

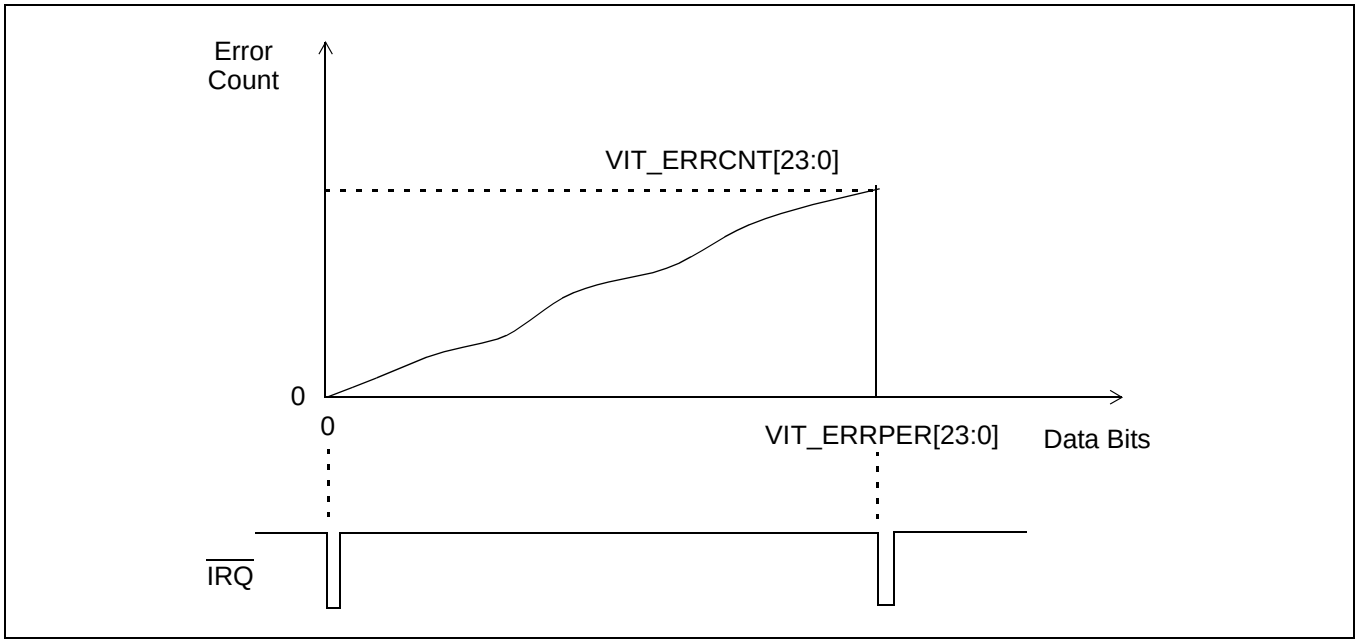

Figure 4 - Viterbi error count measurement

Figure 4 shows the bit errors rising until the maximum programmed value of VIT_ERRPER[23:0] is reached, when an interrupt is generated on the IRQ line to advise the host microprocessor that a new value of bit error count has been loaded into the VIT_ERRCNT [23:0] register. The IRQ line will go high when the IE_FEC register is read by the host microprocessor. The error count may be expressed as a ratio:

$$\frac{\text{VIT\_ERRCNT[23:0]}}{\text{VIT\_ERRPER[23:0]*4}}$$

2.4.1.1 Viterbi error count coarse indication

To assist in the process of aligning the receiver dish aerial, a coarse indication of the number of bit errors being received can be provided by monitoring the STATUS line with the following set up conditions.

The frequency of the output waveform will be a function of the bit error count (triggering the maximum value programmed into the VIT_MAXERR[7:0] register and the dish alignment on the satellite. This VIT_MAXERR mode is enabled by setting the FEC_STAT_EN register bit-0. Figure 5 below shows the bit errors rising to the maximum value programmed and triggering a change of state on the STATUS line.

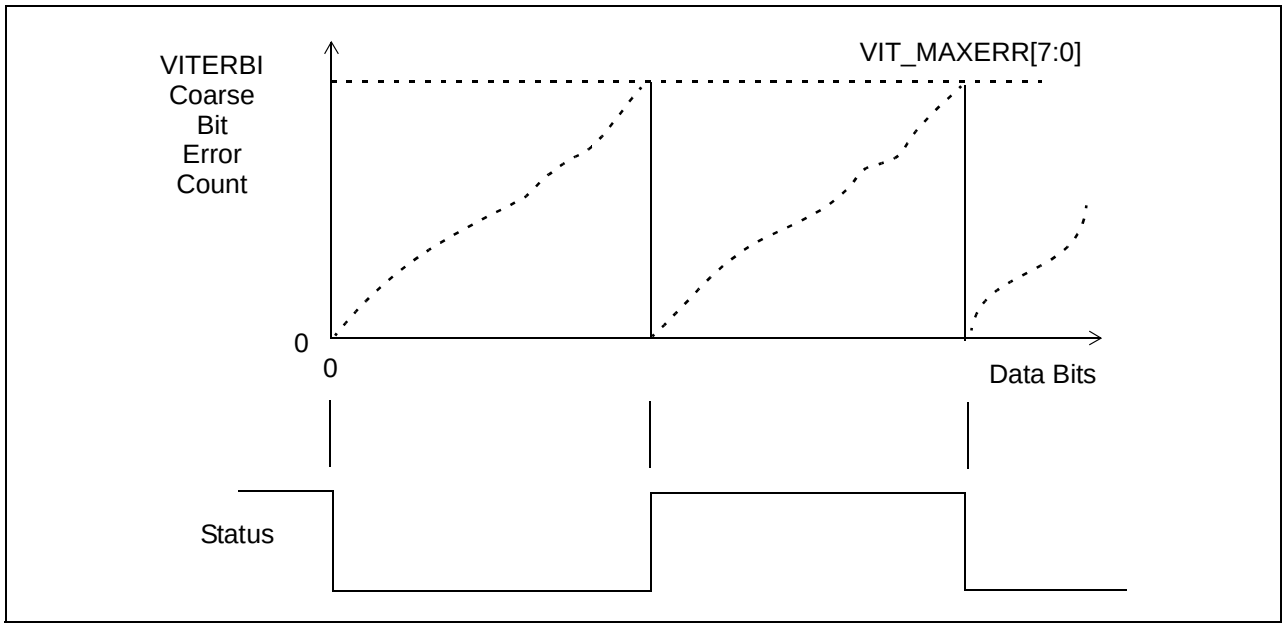

Figure 5 - Viterbi error count coarse indication

2.4.2 The frame alignment block

The frame alignment algorithm detects a sequence of correctly spaced synchronising bytes in the Viterbi decoded bit-stream and arranges the input into blocks of data bytes. Each block consists of 204 bytes for DVB and 147 bytes for DSS. In the DSS mode, the synchronising byte is removed from the data stream, so only 146 bytes of a block are passed to the next stage. The frame alignment block also removes the 180° phase ambiguity not removed by the Viterbi decoder.

2.4.3 The De-interleaver block

2.4.3.1 DVB

Before transmission, the data bytes are interleaved with each other in a cyclic pattern of twelve. This ensures the bytes are spaced out to avoid the possibility of a noise spike corrupting a group of consecutive message bytes. Figure 6 below shows conceptually how the convolutional de-interleaving system works. The synchronisation byte is always loaded into the First-In-First-Out (FIFO) memory in branch 0. The switch is operated at regular byte intervals to insert successively received bytes into successive branches. After 12 bytes have been received, byte 13 is written next to the synchronisation byte in branch 0, etc. In the MT312, this de-interleaving function is realised using on-chip Random Access Memory (RAM).

2.4.3.2 DSS

Before transmission, the data bytes are interleaved with each other in a cyclic pattern of thirteen. This ensures the bytes are spaced out to avoid the possibility of a noise spike corrupting a group of consecutive message bytes. Figure 7 below shows conceptually how the convolutional de-interleaving system works. On the MT312, this function is realised in the same Random Access Memory (RAM) as used for DVB, but utilising a different addressing algorithm.

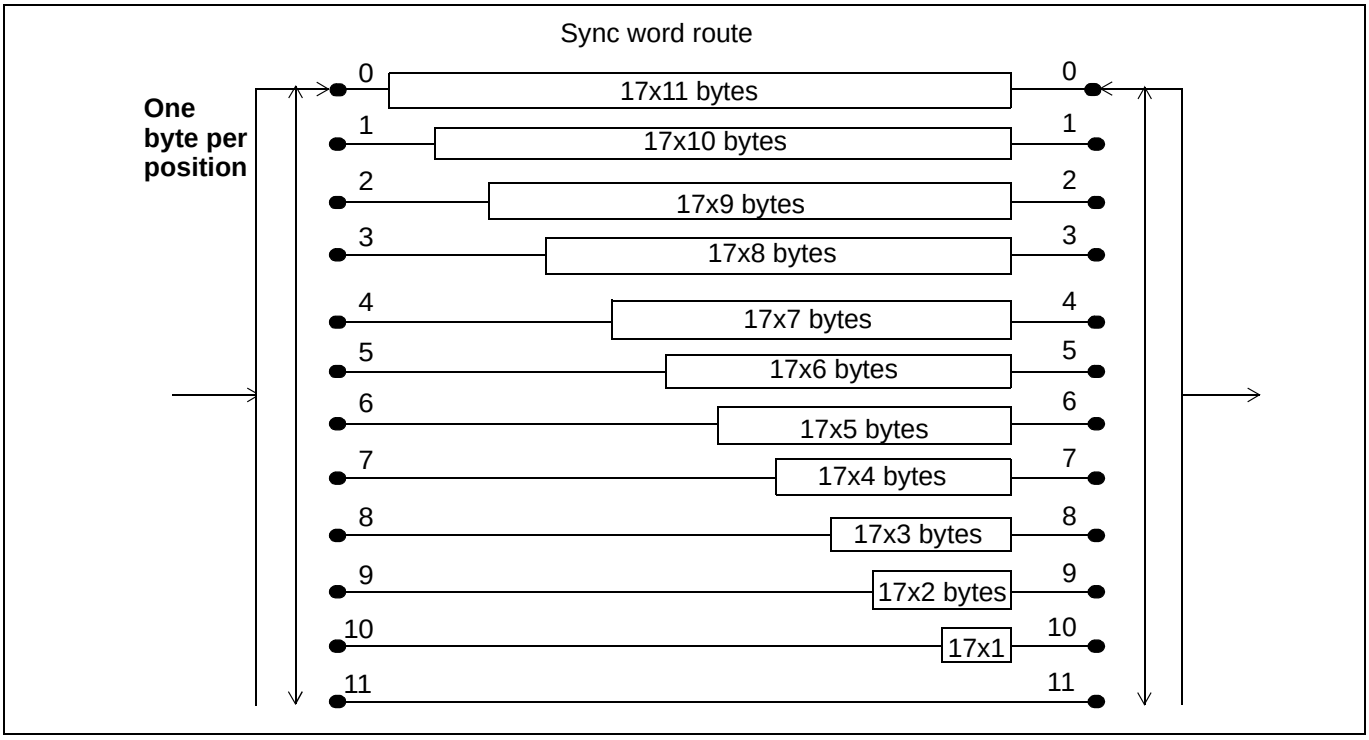

Figure 6 - DVB conceptual diagram of the convolutional de-interleaver block

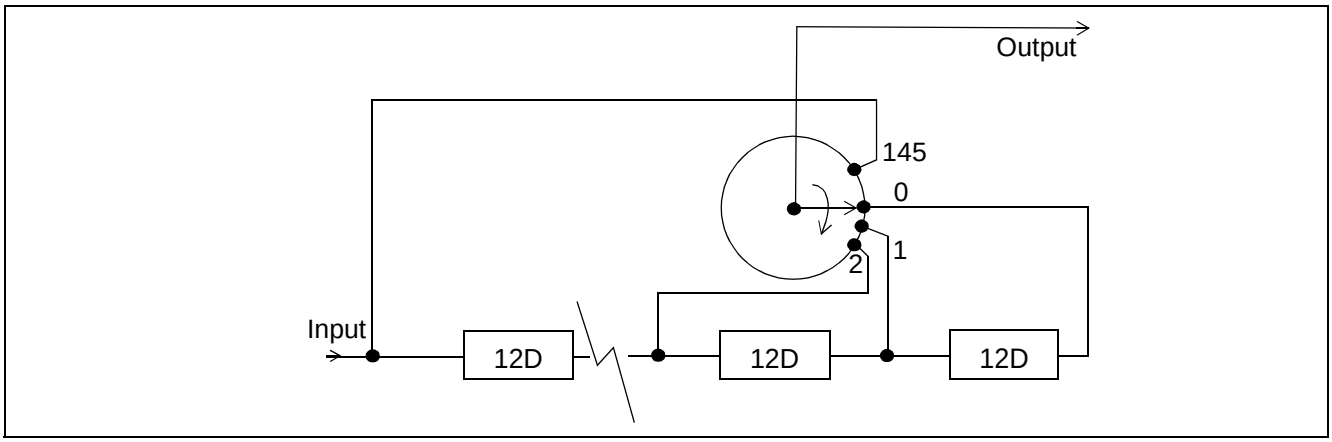

Figure 7 - DSS conceptual diagram of the convolutional de-interleaver block

2.4.4 The Reed-Solomon decoder block

DVB and DSS data are encoded using shortened versions of the Reed-Solomon code of block length 255, containing 239 message bytes and 16 check bytes, that is (255,239) with T = 8. Both encoders use the same generator polynomial. The code block size for DVB is 204 and that for DSS is 146. Hence DVB code is (204, 188) and DSS code is (146, 130), with both having T = 8. The block structure of the DVB and DSS Reed-Solomon codes are as shown in Figure 8 and Figure 9 below.

The Reed-Solomon decoder can correct up to eight byte errors per packet. If there are more than eight bytes containing errors, the packet is flagged as uncorrectable using the pin $\overline{\text{BKERR}}$. In the case of DVB the Transport Error Indicator (TEI) bit of the MPEG packet is set to 1, if setting of TEI is enabled.

2.4.5 The energy dispersal (de-scrambler) block, DVB only

Before Reed-Solomon encoding in the DVB transmission system, the MPEG2 data stream is randomised using the configuration shown in Figure 10 below. This is a Pseudo Random Binary Sequence (PRBS) generator, with the polynomial:

$$1 + X^{14} + X^{15}$$

The PRBS registers are loaded with the initialization sequence as shown, at the start of the first transport packet in a group of eight packets. This point is indicated by the inverted sync byte B8hex (the normal DVB sync byte is 47hex). The data starting with the first byte after the sync byte are randomised by exclusive-ORing data bits with the PRBS (the sync bytes themselves are not randomised). In the decoder, the process of de-randomising or de-scrambling the data is exactly the same as described above. The de-scrambler also inverts the sync byte B8hex so that all MPEG output packets have the same sync byte 47hex.

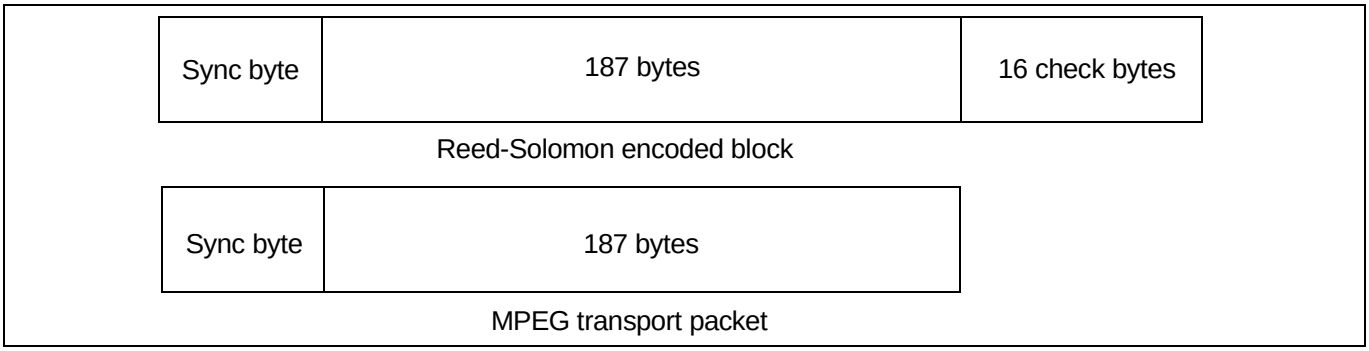

Figure 8 - DVB Block Structure

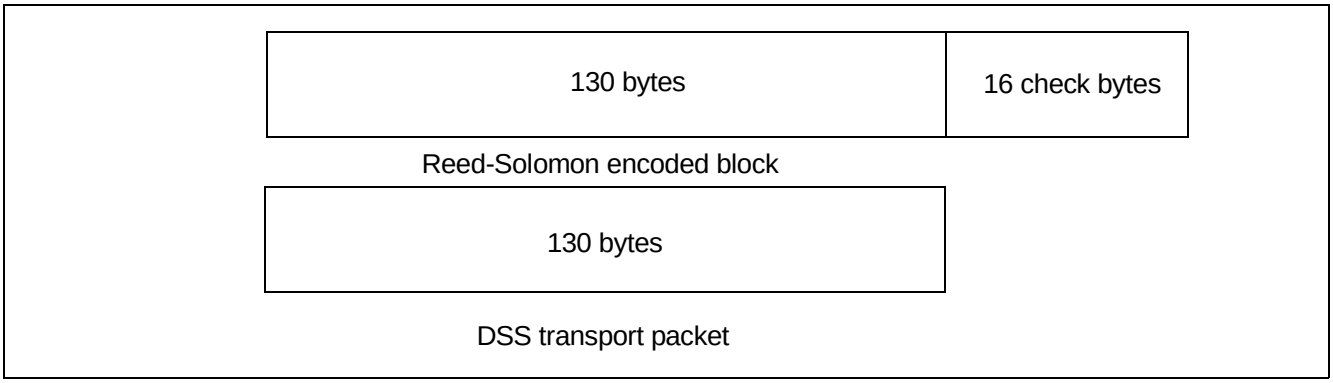

Figure 9 - DVB energy dispersal conceptual diagram

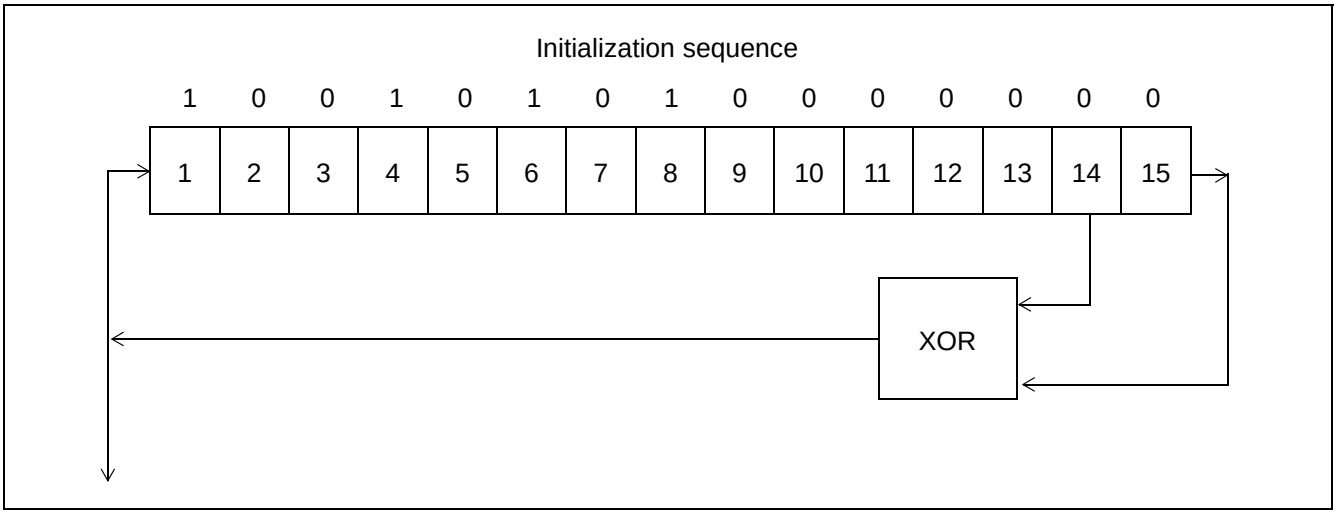

Figure 10 - DVB energy dispersal conceptual diagram

2.4.6 Output stage

The transport stream can be output in a byte-parallel or bit-serial mode. The output interface consists of an 8-bit output, output clock, a packet validation level, a packet start pulse and a block error indicator.

The output clock rate depends on the symbol rate, QPSK/BPSK choice, convolutional (Viterbi) coding rate, DVB/DSS choice and byte-parallel or bit-serial output mode. This rate is computed by MT312 to be very close to the minimum required to output packet data without packet overlap. Furthermore, the packets at the output of MT312 are as evenly spaced as possible to minimise packet position movement in the transport layer. The maximum movement in the packet synchronisation byte position is limited to ±1 output clock period.

An external MPEG clock can be input to synchronise the MPEG data output to MPEG decoders.

2.5 Control

Automatic symbol rate search, code rate search, signal acquisition and signal tracking algorithms are built into the MT312 using a sophisticated on-chip controller. The software interaction with the device is via a simple Command Driven Control (CDC) interface. This CDC maps high level inputs such as symbol rates in MS/s and frequencies in MHz, to low level on-chip register settings. The on-chip control state machine and the CDC significantly reduces the software overhead as well as the channel search times. There is also an option for the host processor to by-pass both the CDC as well as the on-chip controller and take direct control of the QPSK demodulator. Once the MT312 has locked to the signal, any frequency offset can be read from the LNB_FREQ error registers 7 and 8. The frequency synthesiser under the software control can be re-tuned in frequency to optimise the received signal within the SAW bandwidth. Note that MT312 compensates for any frequency offsets before QPSK demodulation. Hence a frequency offset will not necessarily lead to a performance loss. Performance loss will occur only if a significant part of the signal is cut off by the base-band filter, due to this frequency offset. This will happen only if the symbol rate is close to the maximum supported by that filter. In such an event it is recommended that front-end be re-tuned to neutralise this error before the filter. It is then necessary for the MT312 to re-acquire the signal.

The MT312 can generate control signals to enable full control of the dish and LNB. The chip implements the signals needed for the full DiSEqC™ v2.2 specification. This includes high/low band selection, polarisation and dish position. In this mode, the symbol rate in MS/s and Viterbi code rate are the only values needed to start the MT312 searching for the signal. The CDC module maps the high level parameters into the various low level register settings needed to acquire and track the signal. The low level registers may be read and directly modified to suit very specific requirements. However, this is not recommended.

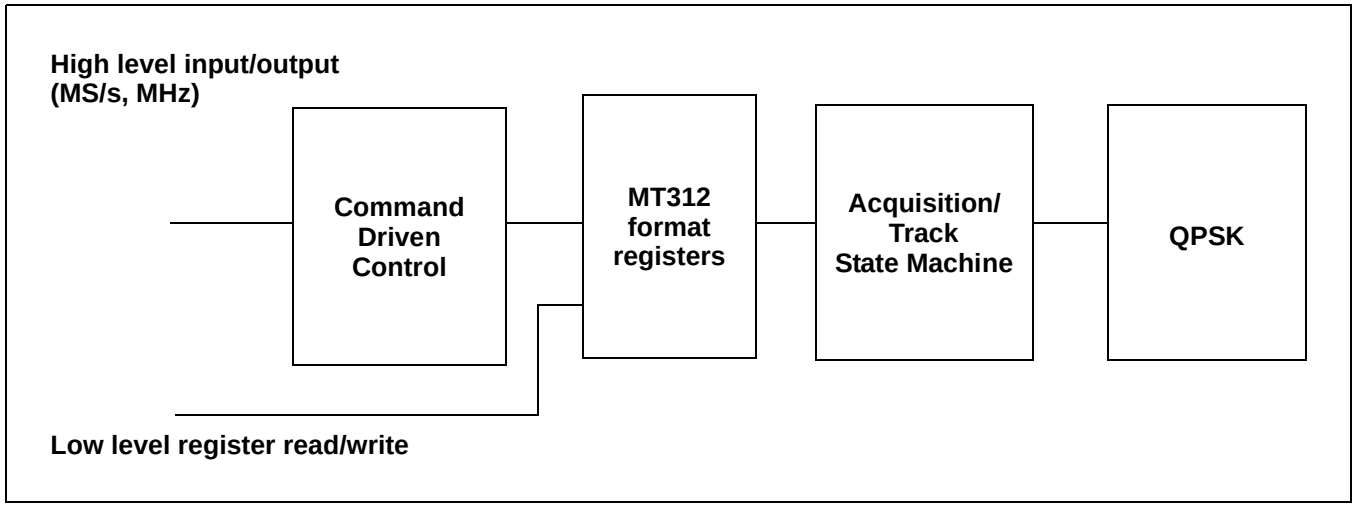

Figure 11 - MT312 control structure

2.5.1 Symbol Rate and Code Rate Search Mode

Where the symbol rate and/or the Viterbi code rate are unknown, the MT312 can be programmed to search for QPSK/BPSK signals. The user should define the range(s) over which the search is required. The MT312 will then locate and track any signal detected. Failure to find a QPSK signal in the specified frequency and specified symbol rate ranges will be indicated by interrupts (see section 7.2 “QPSK Demodulator Read Registers” on page 45). MT312 will carry on searching these ranges after issuing these interrupts. When the MT312 has locked onto a signal, the symbol rate in MS/s may be read from the MONITOR registers. The Viterbi code rate may be read from the FEC_STATUS register. This search facility is primarily for the initial installation of a set top box.

2.6 DiSEqC™ Transmit and Receive Messages

The MT312 has the capability to send and receive DiSEqC™ messages. Eight registers are provided to store a message for transmission and a further eight registers are provided to store a received message. The received bytes have a parity bit and a parity error bit in addition to the eight data bits. These additional bits are read out in sequence following the data bits, so two byte reads are required for each data byte.

2.6.1 DiSEqC™ transmitting messages

The sequence of events to send a message are as follows:

1. Load the required message bytes into the DiSEqC™ instruction register 36, see page 34. Sequential writes to the same register are achieved by setting the Inhibit Auto Incrementing (IAI) bit 7 in RADD, the register address byte.
2. Load the number of bytes (less one) in the DiSEqC™ instruction in the register DISEQC_MODE[5:3], see page 33.
3. Set DISEQC_MODE[2:0] = 4 to command the MT312 to encode the data and transmit the message.
4. Reset DISEQC_MODE[2:0] to either 0 or 1 depending on previous setting of 22kHz off or on. The data loaded into the DISEQC_INSTR register is retained, so that if the same message is to be repeated, stage 1 above can be omitted.

2.6.2 DiSEqC™ receiving messages

The MT312 will automatically listen for DiSEqC™ messages 5ms after a message has been transmitted. If a return message is expected, the DISEQC_MODE[2:0] must be set to zero in order to leave the LNB control signal free for another DiSEqC™ transmitter to respond. The sequence of events to receive a message are as follows:

1. Enable DISEQC2/GPP2 pin 46 as an input by setting GPP_CTRL register address-20 bit-5 to zero.
2. Enable interrupts if the $\overline{\text{IRQ}}$ pin is being used to interrupt the host processor in DISEQC2_CTRL1 register 121.
3. Monitor DISEQC2_INT register.
4. If bit-3 = 1 and bit-1 = 0, there has been no message received.
5. If a message has been received, bit-0 will be set. If bit-1 is also set the message is complete. DISEQC2_INT register bits-7-4 indicate how many bytes have been received.
6. Read the received message from DISEQC2_FIFO register 120 by setting the Inhibit Auto Incrementing (IAI) bit-7 in RADD, the register address byte and sequentially reading DISEQC2_FIFO for the indicated number of bytes. Each data byte read requires two 2-wire bus reads. The second or the pair of bytes contains the parity bit and a parity bit error indicator.

The user may choose to wait for the end of message indication, before reading the message, if it is known that the message is not greater than eight bytes. However, if the length of message is not known, the message should be read out of the FIFO by the host as it is being received. Care must be taken to avoid a FIFO buffer overflow. DISEQC2_INT register bits-7-4 will indicate how many bytes remain in the FIFO.

3.0 MT312 software control

This section describes the sequences of register operations needed to acquire DVB and DSS channels with known or unknown parameters. Communication with the MT312 is via a standard 2-wire bus and the first byte following the chip address, in write mode, is the register address (RADD). The register map is organised to group important read registers at the lowest addresses, then the main control write registers in the next block of addresses. The first register to be written must be the configuration register, which has been placed at the highest register address, because it is only written once during the initialization sequence. The CONFIG register can only be reset by the hardware reset. The MT312 is held in a power saving mode following the hardware reset.

After a hardware reset, the MT312 must be taken out of the power save mode by writing a one to the MSB of the CONFIG register (see “The configuration register (127)” on page 21). When MT312 is not being used it can be put back into the power save mode by writing a zero to the MSB of CONFIG.

3.1 MT312 register map overview

Address	Description	Type
00 - 06	Interrupt and Status	read
07 - 19, 108 - 117, 123, 124	Primary signal monitors	read
20 - 39, 41, 96, 103	Primary control parameters	write/read
40, 42 - 49, 50 - 106, 125	Secondary parameters	write/read
107, 118 - 122	Secondary monitors	read
126	Chip identification	read
127	Chip configuration	write/read

Table 1 - MT312 register map overview

All write/read registers take on default values on full software reset, except for the configuration register (127), which is only reset to the default value by a hardware reset.

3.2 Register usage overview

Section Title	Register Addresses	Starting Page
4.0 MT312 Initialization	21, 127, 34, 126	20
5.0 Tuner Control	20, 37, 38, 7-8, 111-115	25
6.0 DiSEqC Control	22, 35-36, 121-122, 118-120	32
7.0 QPSK demodulator	23-30, 32, 0-2, 4-5, 116-117, 123-124	39
8.0 Forward Error Correction	31, 33, 97, 3, 6, 9-18	49
9.0 Automatic Gain Control	39, 41, 19, 108-110	54
10.0 MPEG Packet Data Output	93, 103	56

Table 2 - Register usage overview

4.0 MT312 Initialization

4.1 Initialization sequence

MT312 will be in the power save mode after a hardware reset. The first command to be written must be to the CONFIGURATION register at address 127. After loading this register, wait 150µs before writing to the RESET register. During this wait, the tuner can programmed to the required channel frequency via the General Purpose Port (register 20). Note that the GPP register occupies the address space before the RESET register. If the AGC slope control bit of AGC_CTRL(39) or the AGC_REF(41) are to be changed, it is best to write to these registers after writing to the RESET register. This will allow the front-end AGC loop to settle while the other registers are being written.

Next write 128 to the RESET register (21) to reset the MT312 state machine and all parameter registers to the default settings. It is then necessary to change the default setting of register 49 (see 11.2.9, SNR_HIGH threshold value register 49 (R/W)) to 50 (decimal).

If necessary, other default parameters may need to be changed. These may include:

- Slope of AGC control signal - See AGC control register 39 (R/W) [bit-0] AGC_SL bit
- AGC Reference value - See AGC_REF Reference Value register 41 (R/W)
- Relative phase the of IQ spectrum - See Viterbi mode register 25 (R/W) [bit-6]
- LNB frequency search range, default ±6MHz See FR_LIM frequency limit register 37 (R/W)
- For low Baud rates only, set fast frequency acquisition mode - See QPSK control register 26 (R/W) [bit-2] = 1

To invert MOCLK or $\overline{\text{BKERR}}$ output signals - See Output data control register 96 (R/W)

After this, the LNB controls are defined, in the DISEQC mode control register 22 (R/W).

The signal parameters should then be written to the MT312. The symbol rate (Symbol rate registers 23 - 24 (R/W)) may be specified within ±2% of the required value, absolute precision is not required to achieve successful lock and tracking. If the symbol rate is unknown, a search mode is available.

Selecting the correct bit of Viterbi mode register 25 (R/W), if known, programs the convolutional code rate. If the code rate is unknown, some or all of the bits of VIT_MODE may be set to force a search for the code rate.

Finally, the MT312 is given a GO command, register (27) GO =1, to release the state machine and to start the signal acquisition sequence. This is summarised as an example in Figure 13 Initialization sequence in DVB mode.

4.2 The configuration register (127)

CONFIG[bits 7-0]: This register is for setting up the MT312. It must be loaded first before any other register. It can only be reset to the default value by the RESET pin being pulled low.

CONFIG[bit-7]: 312_EN High = MT312 enable.
Low = MT312 disable to save power.

CONFIG[bits 6-5]:

DSS_B	DSS_A	Mode
0	0	DVB mode
0	1	DSS mode 1 - code rate 2/3
1	0	DSS mode 2 - code rate 6/7
1	1	DSS Code Rate search

If both DSS_A and DSS_B are set high, the MT312 will search for the code rate in DSS mode. If either of the DSS_A or DSS_B are set high, the symbol rate is automatically set to 20MS/s and SYM_RATE registers (23 & 24) are ignored. The matched filter root-raised-cosine roll-off is set to 0.20 and bit-0 of QPSK_CTRL (26) is ignored. Also, any code rate programmed into VIT_MODE register (25) and VIT_SETUP register (86) will be ignored.

Also in DSS mode, the TS_SW_RATE register (50) must be set to 20, see “Timing Synchronisation Sweep Rate register 50 (R/W)” on page 67.

CONFIG[bit-4]: BPSK High = BPSK
Low = QPSK

CONFIG[bits3-2]: PLL_FACTOR[1:0]:

bit-3	bit-2	Multiplication factor
0	0	3
0	1	4
1	0	6
1	1	9

CONFIG[bit-1]: CRYS15 High = 15MHz crystal.
Low = 10MHz crystal.

CONFIG[bit-0]: ADCEXT High = ADC external.
Low = ADC internal.

e.g. For a crystal frequency of 10MHz, a system clock frequency of 60MHz, the PLL ratio will be 6, requiring the PLL_FACTOR[1:0] = 2.

For QPSK reception and ADC internal, the MT312 is enabled by writing 88hex to register 127.

MT312 computes the System clock frequency using bit-3 to bit-1 above. This frequency is used internally for computing parameters needed for acquiring the QPSK signal.

It is possible to use a crystal frequency other than 10 or 15 MHz. As an example, if the crystal frequency is 10.25MHz and the PLL multiplication factor is 6. Then bit-3 is set to 1 and bit-2 to 0. Bit-1 may be given an arbitrary value (0 or 1). The external software must compute the system clock frequency and load this value (multiplied by 2) to the SYS_CLK register (address 34). In the above example, the system clock frequency is 61.5 MHz and hence the value 123 has to be loaded into SYS_CLK register.

The QPSK demodulator checks the SYS_CLK register and if this is non-zero, it uses the contents of this as the system clock frequency, for internal calculations mentioned above. If this register is zero (which is the default setting), QPSK demodulator works out the system clock frequency from bits-3- bit-1 of the CONFIG register assuming that the crystal frequency is either 10 or 15 MHz, as defined by bit-1.

4.3 Power Supplies

To avoid the possibility of destructive latch-up, the CV_{DD} supply must never, at any time during power-up, exceed 0·5V above the V_{DD} supply and must also remain within the absolute maximum ratings, see section 13.2 “Absolute Maximum Ratings” on page 80. In general therefore, the V_{DD} supply should be established ahead of, or simultaneously with the CV_{DD} supply.

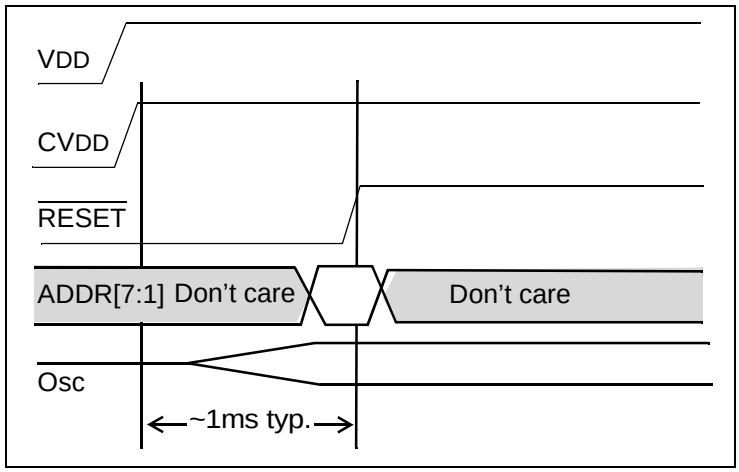

Figure 12 - MT312 Power-up Sequence

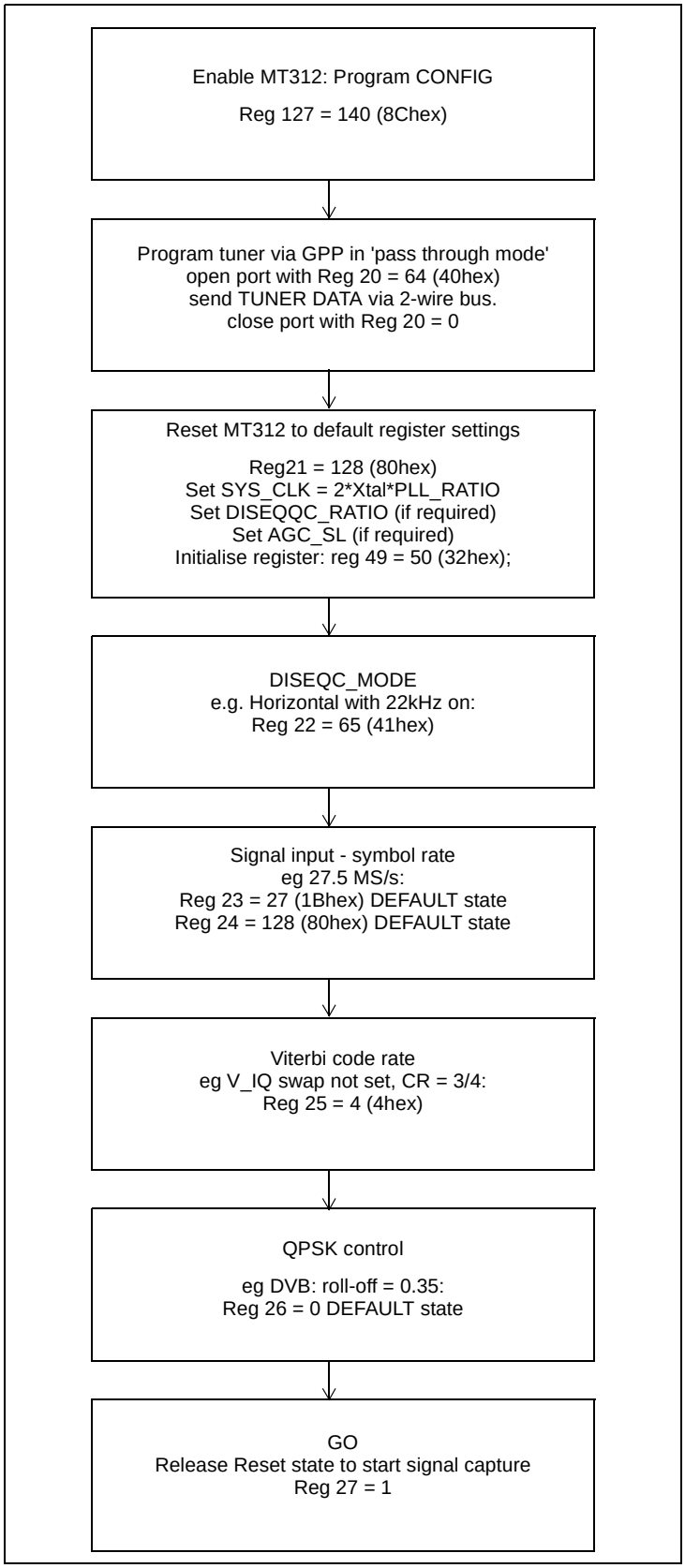

Figure 13 - Initialization sequence in DVB mode.

4.4 Spectral inversion

Spectral inversion of the QPSK signal can be caused by the transmitter or the receiver front-end. In the latter case, this could happen due to the way I-Q conversion is carried out or because the I and Q connections are swapped between the I-Q converter and the MT312. If spectral inversion is caused by the receiver front-end, then this must be removed by swapping I and Q (within MT312) before QPSK demodulation, by setting the Q_IQ_SP bit-6 of QPSK control register 26 (R/W) to 1. If no spectral inversion is caused by the receiver front-end design, then bit-6 of QPSK_CTRL should be set to zero.

If the transmitted signal is known to be spectrally inverted, then V_IQ_SP bit-6 of the Viterbi mode register 25 (R/W) may be set to 1, or if the spectral inversion status of the transmitted signal is not known, then the AUT_IQ bit-7 of the same register may be set to 1 to allow the MT312 to determine the spectral inversion automatically.

4.5 Read/write registers

Also see “The configuration register (127)” on page 21

4.5.1 Reset register 21 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
RESET	21	FR_312	PR_312	FR_QP	PR_QP	FR_VIT	PR_VIT	PR_BA	PR_DS	R/W	00

bit-7: FR_312 High = Full reset of MT312 device.

bit-6: PR_312 High = Partial reset of MT312 device.

bit-5: FR_QP High = Full reset of QPSK block.

bit-4: PR_QP High = Partial reset of QPSK block.

bit-3: FR_VIT High = Full reset of Viterbi block.

bit-2: PR_VIT High = Partial reset of Viterbi block.

bit-1: PR_BA High = Partial reset of Byte Align block.

bit-0: PR_DS High = Partial reset of De-scrambler block.

- Writing a one to these register locations generates a reset pulse three crystal clock periods wide.
- The register automatically resets to zero after use.
- A full reset resets the registers to their default values.
- A partial reset does not reset the registers to their default values.

4.5.2 System clock frequency register 34 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
SYS_CLK	34	SYS_CLK[7:0] - System clock frequency x2 in MHz								R/W	00

SYS_CLK[7:0] = System clock frequency * 2 in MHz.

If the reference frequency (a crystal or external clock) is other than 10.000MHz or 15.000MHz the SYS_CLK register must be programmed to indicate the system clock frequency to the calculation unit. The maximum system clock frequency allowed is 91MHz.

e.g. for a crystal frequency = 10.111MHz, if the PLL multiplication ratio is 9, the system clock frequency = 91MHz and SYS_CLK[7:0] = 182 (B6hex).

The system clock frequency is NOT affected by the setting of SYS_CLK[7:0] register. For 10MHz and 15MHz frequencies, the MT312 calculates the system frequency from bits 3-1 in the CONFIG register (see “The configuration register (127)” on page 21) and this register may be left at the default of 00.

4.6 Read registers

4.6.1 Identification register 126 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
ID	126	ID[7:0] Chip identification.								R	03

ID[7:0]: This register provides an identification number related to the MT312 version

5.0 Tuner Control

5.1 Simple channel change sequence

If the MT312 is running, to change channel keeping the same signal conditions, it is only necessary to change the tuner data and possibly the DiSEqC™ data. NO reset is necessary.

5.2 Channel change sequence with a new symbol rate

If the MT312 is running, to change channel and symbol rate but not Viterbi coding rate, change the tuner data and possibly the DiSEqC™ data and symbol rate. NO reset is necessary.

5.3 Channel change sequence with search mode

If the signal parameters are unknown, it is possible to instruct the MT312 to find a digital signal and report the parameters found. Registers 23 and 24 are programmed with the expected range(s) and the search mode bit SYM_RATE[bit-15] is set high. A code rate search is forced by programming more than one bit in VIT_MODE (25) register. The IQ spectrum phase can be automatically determined by setting bit-7 in the Viterbi mode register 25 (R/W).

Note: code rate 6/7 is not searched for in DVB mode.

If a signal with the specified symbol rate range (or ranges) is not found in the frequency range searched, a QPSK Baud End interrupt (bit-6, QPSK_INT_L (2)) is issued. When the MT312 QPSK section has locked to the signal, this is indicated in register (6) by QPSK_STAT_H[bit-0] = 1. The symbol rate found can be read from registers (123 - 124) MONITOR, provided the register (103) MON_CTRL = 3. The tolerance of the result is ±0.25%. The 14 MSBs

of this result (discarding two LSBs) may be written as the 14 LSBs of the 16-bit register pair (23 and 24) SYM_RATE in the non-search mode for re-acquisition of the same channel.

The FEC is locked to the signal, when byte align lock in FEC_STATUS[bit-2] = 1. The code rate found can then be read from FEC_STATUS[bits 6-4], see section 8.2.2 “FEC status register 6 (R)” on page 51 for details.

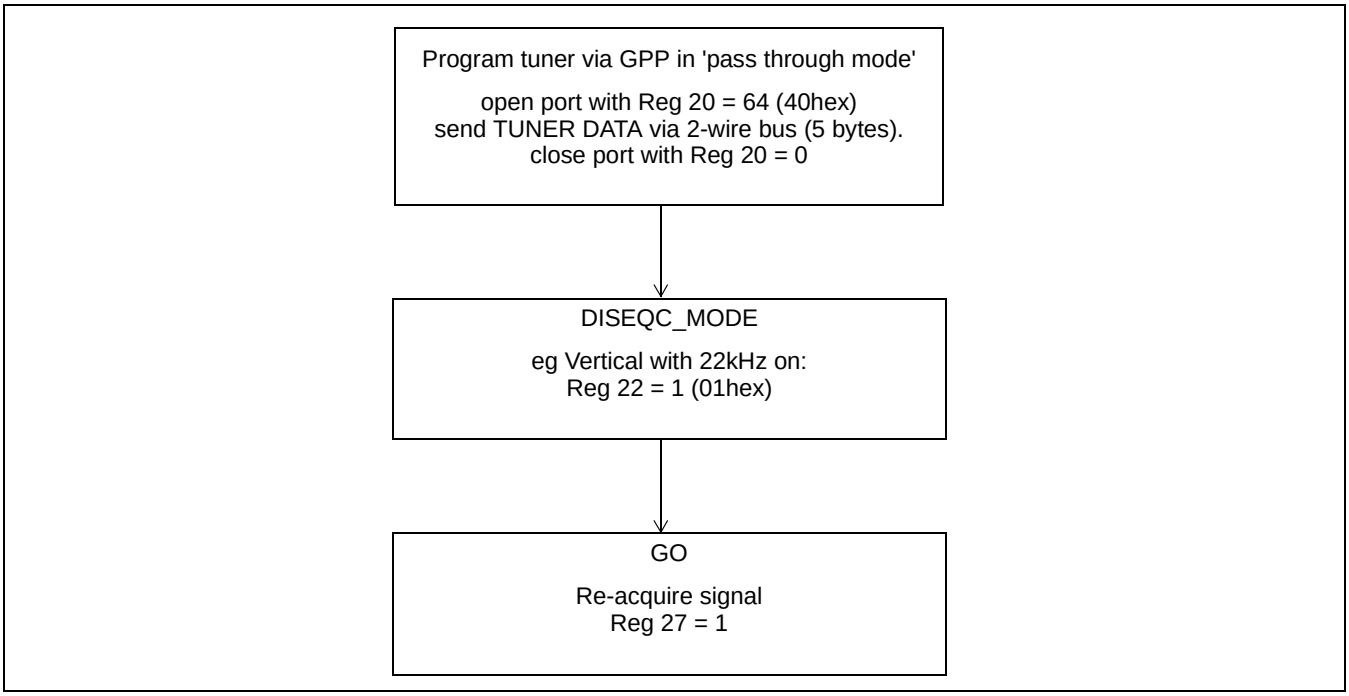

Figure 14 - Simple channel change sequence

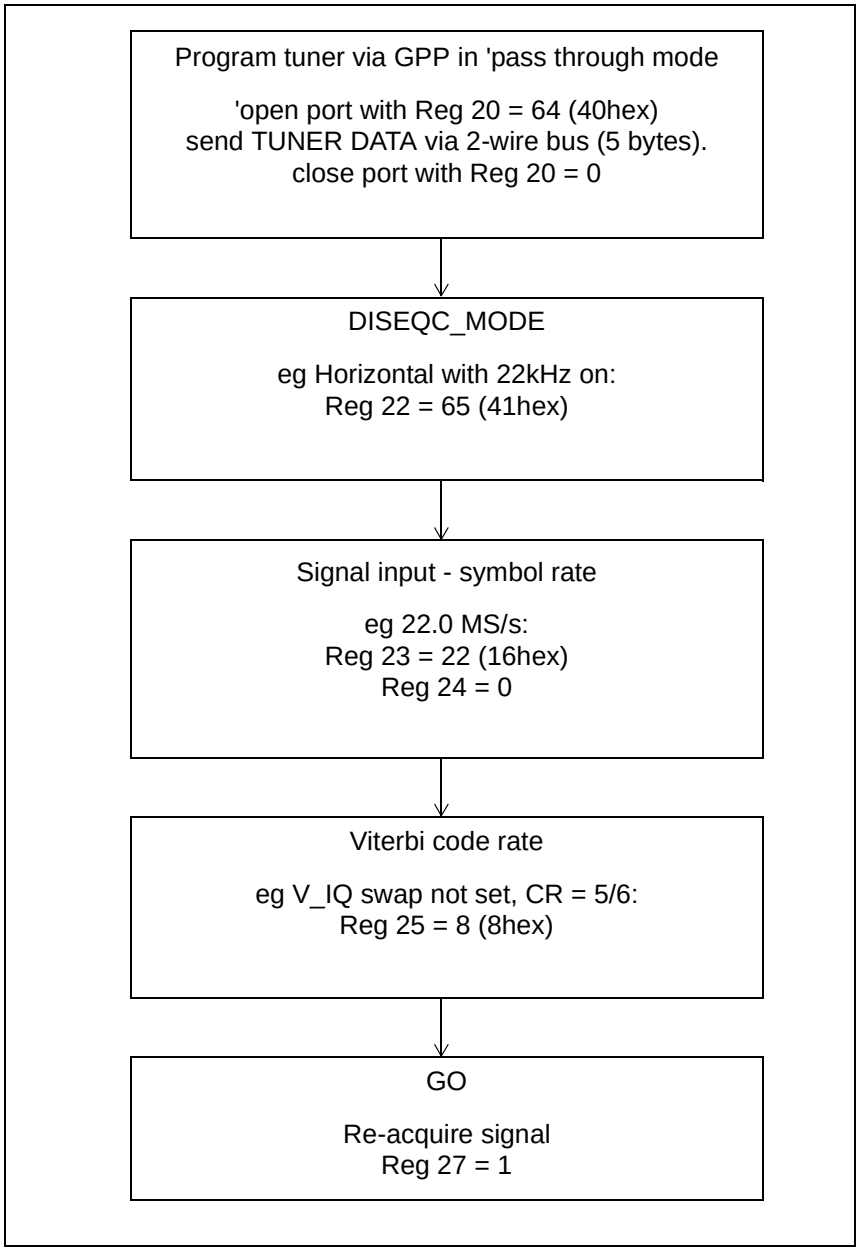

Figure 15 - Channel change sequence with new symbol rate, DVB mode

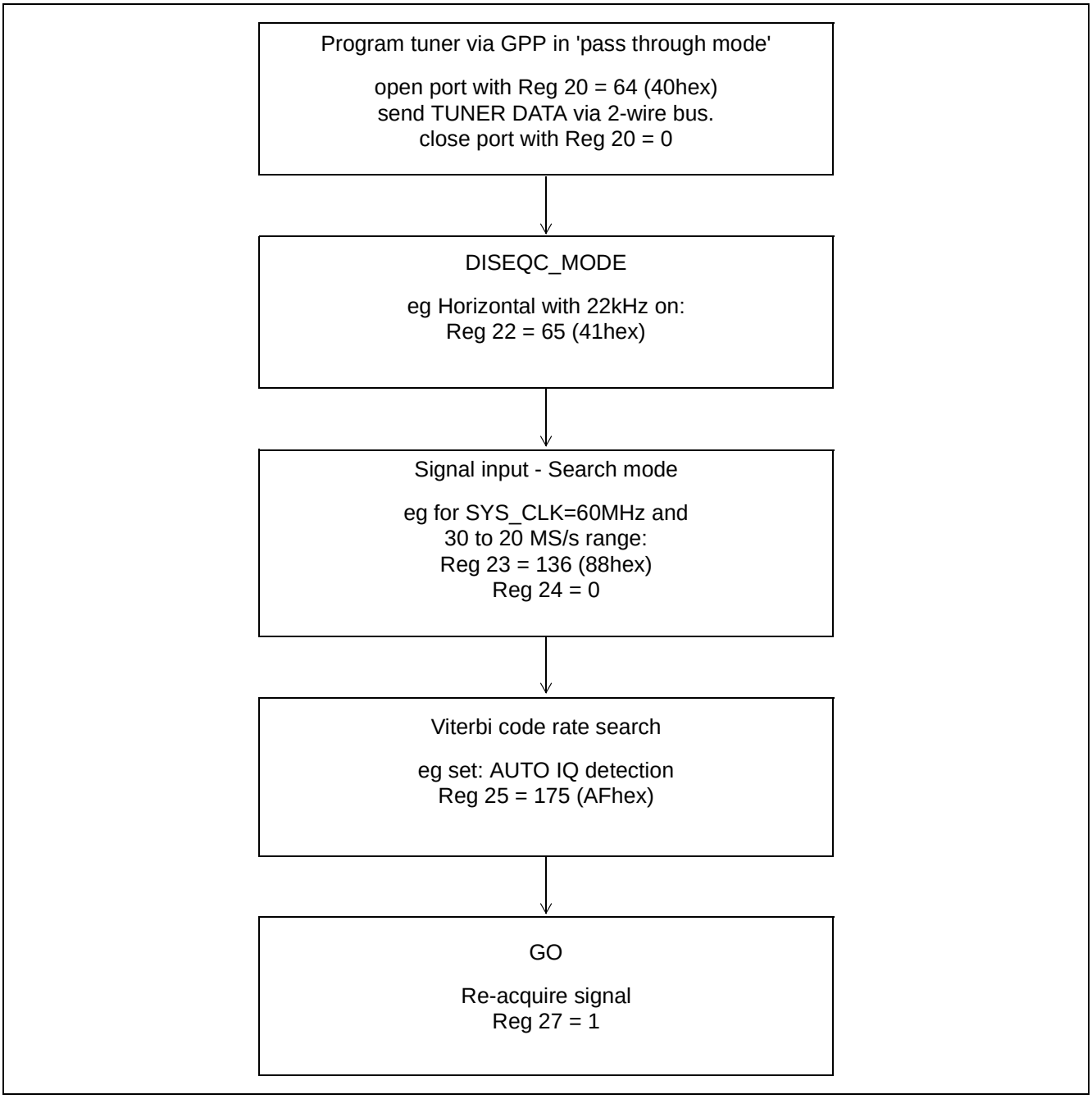

Figure 16 - Channel change sequence with search mode, DVB mode

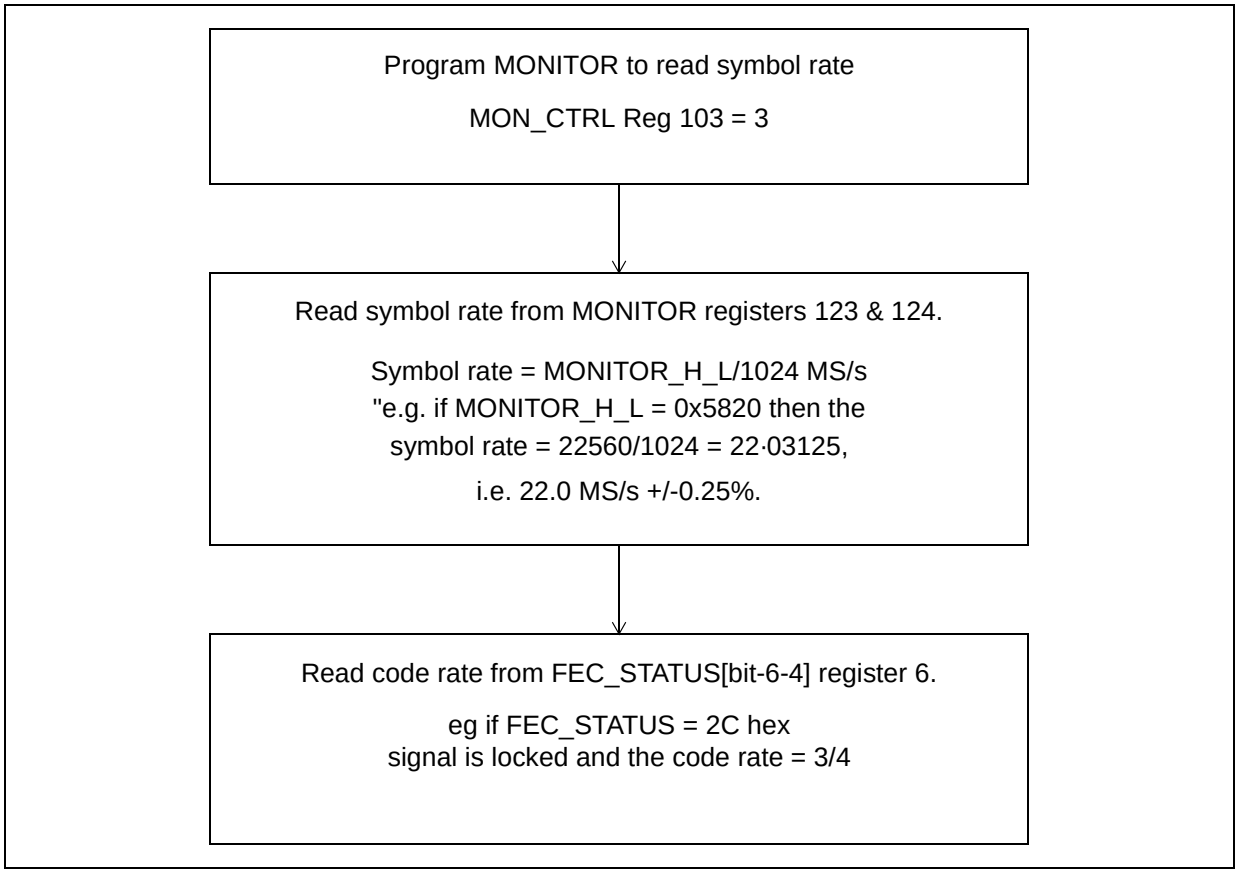

Figure 17 - Results of symbol rate and code rate search, DVB or DSS mode

5.4 Tuner Control Read/Write Registers

5.4.1 General purpose port control register 20 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
GPP_CTRL	20	Reserved	2W_PAS	GPP_DIR[2:0]			GPP_PIN[2:0]			R/W	20

bit-7: Reserved. Must be set low.

bit-6: 2W_PAS: High = 2-wire bus pass-through.
Low = GPP pin I/O direction set by GPP_DIR[2:0].

bit-5-3: GPP_DIR[2:0] Any bit set high configures the corresponding GPP[2:0] pin as an output
Any bit set low configures the corresponding GPP[2:0] pin as an input
Mixed use of pins as inputs and outputs is allowed.

If bit-6 = 1, pass-through mode, then:
GPP_DIR[1:0] are ignored,
bit-2: = Input or output set by GPP_DIR[2] - relating to pin 46.
Pin 45 = DATA2, this is a transparent, bi-directional connection to the primary DATA1.
Pin 44 = CLK2, this is a transparent, bi-directional connection to the primary CLK1.

If bit-6 = 0 then: GPP_DIR[2:0] defines the input/output conditions of the GPP pins and:

If a pin[n] is defined as output then:

GPP_PIN[n] high forces GPP[n] pin high

GPP_PIN[n] low forces GPP[n] pin low

If a pin[n] is defined as input then:

GPP[n] pin high sets bit GPP_PIN[n] high

GPP[n] pin low sets bit GPP_PIN[n] low

Allocation of the GPP[2:0] pins is:

GPP[2] pin = DiSEqC™ v2.2 input, 3-wire bus enable or can be used for any other application

GPP[1] pin = DATA2 or 3-wire bus data

GPP[0] pin = CLK2 or 3-wire bus clock

The register default state of 20 hex allows the GPP[2] pin to be used for the 3-wire bus enable line and to be kept low at all times, except when programming the synthesiser.

When GPP[2] pin is used for DiSEqC™ v2.2 input, the GPP_CTRL register will need to be set to zero after every full reset to make GPP[2] an input.

5.4.2 FR_LIM frequency limit register 37 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FR_LIM	37	Reserved	FR_LIM[6:0] - Freq. limit in MHz							R/W	30

bit-7: Reserved. Must be set low.

FR_LIM[6:0] frequency search range 125kHz steps (MHz/8).

This unsigned 7 bit number represents a search range of +/-0 to +/- 15.875MHz.

Default value 30 (hex) = +/- 6.00MHz.

5.4.3 FR_OFF frequency offset register 38 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FR_OFF	38	FR_OFF[7:0] 2's comp. freq. offset in MHz/32								R/W	00

FR_OFF[7:0] Frequency offset correction value in 31.25kHz steps (MHz/32). This 2's complement 8 bit number represents an offset from -4MHz to +3.96875MHz. Default value 0.

The frequency search is carried out in the range [(-FR_LIM + FR_OFF), (FR_LIM + FR_OFF)]. The frequency offset register can be useful in reducing the frequency search during channel hopping, especially with low symbol rates. If the location of the wanted channel with respect to the current channel is known and if the synthesiser step size is too large to set the precise frequency of that channel, then the FR_OFF register can be used to take up any residual frequency offset.

5.5 Tuner Control Read Registers

5.5.1 Measured LNB frequency error registers 7 - 8 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
LNB_FREQ H	07	LNB_FREQ[15:8] Measured LNB frequency error (high byte)								R	00
LNB_FREQ L	08	LNB_FREQ[7:0] Measured LNB frequency error (low byte)								R	00

LNB_FREQ[15:0] Frequency offset in steps of 1·953125kHz (MHz/512). This is a 2's complement 16 bit number. e.g. a hex value of F680 (= -2432) represents an offset of -4.75MHz.

Once the chip is in lock, these two registers provide a measurement of the frequency of the signal at the input to MT312. Ideally, this frequency is zero. Due to LNB frequency uncertainty this frequency may take a positive or negative value. The analogue front-end may then be re-tuned to bring this offset close to zero. Note that MT312 indicates the frequency location of the QPSK spectrum with respect to zero frequency. The direction in which the synthesiser frequency has to be stepped depends on the design of the analogue front-end. Also note that in many instances it will not be necessary to re-tune even when there is a relatively large frequency offset. This is because MT312 compensates for this frequency offset before it demodulates the signal. Re-tune only if a substantial part of the QPSK spectrum is affected by the base-band filter which precedes MT312. This will be the case only for symbol rates which are close to the maximum symbol rate supported by the above mentioned filters.

When MT312 locks, part of the frequency offset is taken up by the frequency compensation mixer and part by the carrier synchroniser. LNB_FREQ gives only the value in the frequency compensation mixer. Over a short period of about one second after lock, the carrier synchroniser will transfer all the frequency compensation to the mixer. Hence the LNB_FREQ reading will have an error less than ±5% of the symbol rate during this short period after lock. If an accurate frequency reading is needed immediately after lock, the calculation given in section on FREQ_ERR2 has to be performed by external software.

5.5.2 Frequency error 1 and 2 registers 111 - 115 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FREQ_ERR1 H	111	FREQ_ERR1[23:16] Input frequency error coarse (high byte)								R	00
FREQ_ERR1 M	112	FREQ_ERR1[15:8] Input frequency error coarse (middle byte)								R	00
FREQ_ERR1 L	113	FREQ_ERR1[7:0] Input frequency error coarse (low byte)								R	00

FREQ_ERR1[23:0] is the ratio of frequency compensation mixer offset to system clock x 2^{24}. It is a 24-bit signed number.

For most purposes the LS byte can be ignored hence the alternative definition is more useful: FREQ_ERR1[23:8] is the ratio of frequency compensation mixer offset to system clock x 2^{16}. A 16-bit signed number.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FREQ_ERR2 H	114	FREQ_ERR2[15:8] Input frequency error fine (high byte)								R	00
FREQ_ERR2 L	115	FREQ_ERR2[7:0] Input frequency error fine (low byte)								R	00

FREQ_ERR2 [16:0] is the ratio of carrier synchroniser offset to symbol rate x 2^{8}. It is a 16-bit signed number. This value drops to near zero within about a second of signal lock. To obtain an accurate value for the frequency offset at

any time, especially immediately after lock, the error from each of these registers can be calculated and added together. In practice only the two most significant bytes of FREQ_ERR1 are required, so that the net offset can be calculated as:

$$f_{OFF} = -\left(\frac{ERR1 \times PLL}{65536} + \frac{ERR2 \times Rs}{262144}\right)$$

Where:

f_{OFF}	=	the frequency offset to be applied to the tuner in MHz
ERR1	=	FREQ_ERR1[23:8]
PLL	=	the PLL frequency in MHz
ERR2	=	FREQ_ERR2[15:0]
Rs	=	the symbol rate in MS/s calculated from the value in the “Symbol Rate Output registers 116 - 117 (R)” on page 48

Any frequency error in FREQ_ERR2 transfers to FREQ_ERR1 very rapidly after lock, so that any delay between reading the two values will cause an error in the calculation. It is therefore recommended that the five bytes above are read as a block, especially if the 2-wire bus is subject to congestion or other delays.

6.0 DiSEqC Control

6.1 Screen printouts of DiSEqC™ waveforms

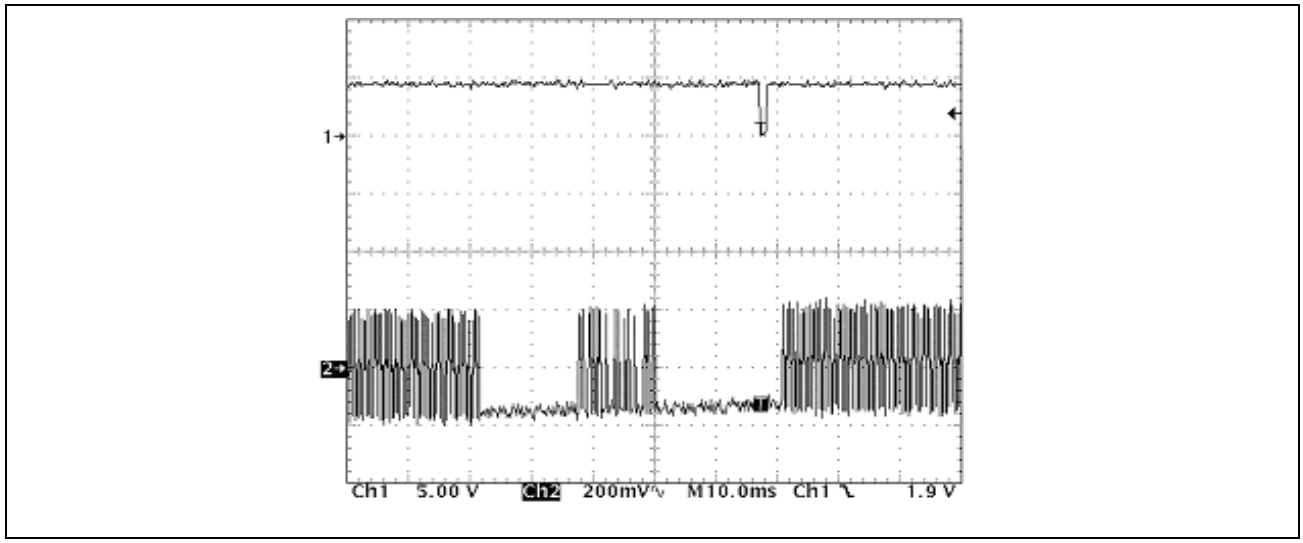

Figure 18 - A DiSEqC™ data byte interrupting a continuous 22kHz tone

The timing periods of the 16ms before the data byte and 16ms afterwards to the interrupt being asserted are clearly shown. The restoration of the 22kHz after the interrupt is controlled by software.

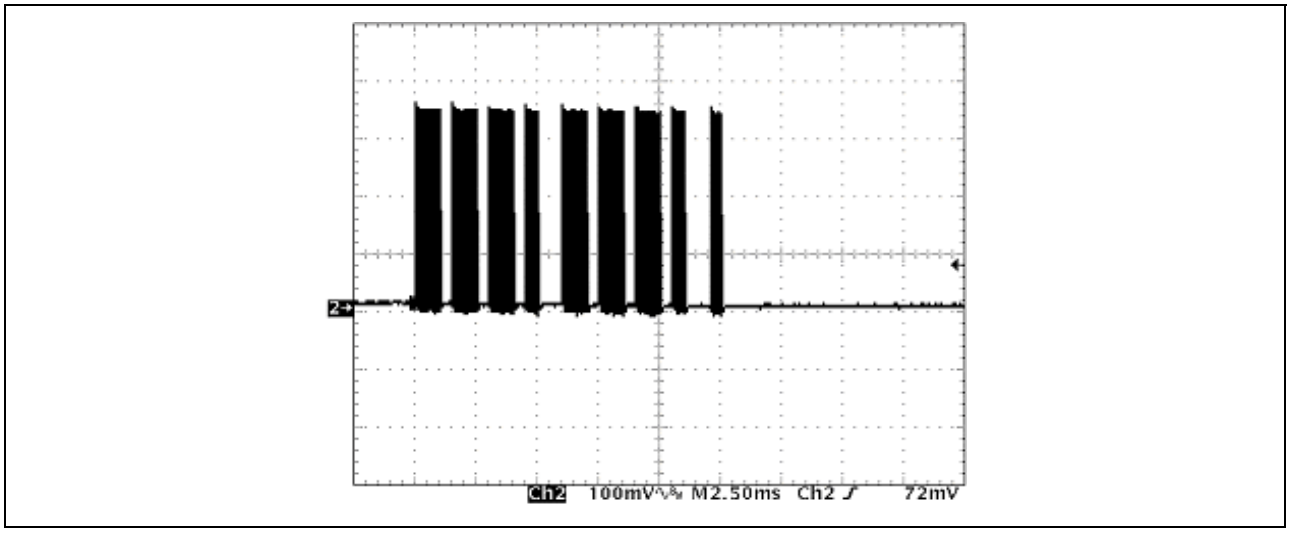

Figure 19 - One DiSEqC™ data byte - 0x11 (hex) plus parity bit

30

A 'zero' comprises 22kHz on for 1ms then off for 0.5ms. A 'one' comprises 22kHz on for 0.5ms then off for 1ms. The ninth bit is an odd parity bit.

6.2 DiSEqC™ control read/write registers

6.2.1 DISEQC mode control register 22 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC_MODE	22	Reserved	HV	DISEQC instruction length			22kHz mode			R/W	00

bit-7: Reserved. Must be set low.

bit-6: HV H/V polarisation control: High = Horizontal, DISEQC[1] pin = high
Low = Vertical, DISEQC[1] pin = low
The DISEQC[1] pin controls the externally generated 13/18V LNB voltage.

bits5-3: Number of bytes in DiSEqC™ instruction minus 1 to output on the DISEQC[0] pin, i.e. if the message contains four bytes, program bits 5-3 with the value three.

bits2-0: DISEQC mode:

0:	22kHz off
1:	22kHz on continuous
2:	Burst mode - on for 12.5ms = '0'
3:	Burst mode - modulated 1:2 for 12.5ms = '1'
4:	Modulated with bytes from DISEQC_INSTR
5-7:	Reserved.

Note: for modes 2 and 3, an interrupt is generated 16ms (see FEC interrupt register 3 (R)) after the '0' or '1' burst. For mode 4, there is a 16ms delay before the message bytes, then an interrupt is generated 16ms after the last message byte has been sent (see FEC interrupt register 3 (R)). The requisite number of bytes must be pre-loaded into the DISEQC instruction register 36 (R/W) before this bit is set, see page 34.

6.2.2 DISEQC ratio register 35 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC_RATIO	35	DISEQC_RATIO[7:0]								R/W	00

DISEQC_RATIO[7:0] must be programmed to set the DiSEqC™ output tone frequency.

$$F_{out} = \frac{F_{xtal}}{4*DISEQC\_RATIO[7:0]}$$

Where F_{out} is in kHz and F_{xtal} is in MHz

For a 22kHz output tone, DISEQC_RATIO[7:0] = 11.364 * F_{xtal} e.g. with F_{xtal} = 10MHz, DISEQC_RATIO[7:0] = 114, or for 15 MHz 170.

For this example, the DISEQC frequency $= \frac{10^7}{4 \times 114} = 21.93kHz$

For a 10MHz crystal, the tone frequency range is from 9.8kHz with DISEQC_RATIO = 255 to 250kHz with DISEQC_RATIO = 10. A lower value than 10 causes the tone frequency to become unstable, until the DISEQC RATIO = 0, the default, value giving a 22kHz tone frequency. This range is not guaranteed, the maximum tone frequency should be used with caution.

6.2.3 DISEQC instruction register 36 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC_INSTR	36	DISEQC_INSTR[7:0]								R/W	00

Up to eight instruction data bytes are first loaded into a bank of registers through this register. The 2-wire automatic register address incrementing is turned off during this loading by setting bit-7: IAI = 1 in RADD, (register address). The number of bytes (less one) must be defined in the DiSEqC™ instruction register DISEQC_MODE[5:3].

i.e. DISEQC_MODE[5:3] = (number of bytes in the DiSEqC™ instruction) - 1

When the DiSEqC™ instruction data bytes have been loaded, set DISEQC_MODE[2:0] = 4. At the same time program DISEQC_MODE[5:3] as required. The instruction data bytes are modulated onto the 22kHz signal and output from the DISEQC[0] pin.

An interrupt is generated 16ms after all the data bytes have been sent and the MT312 then resets DISEQC_MODE[5:0] to zero, see Figure 18 - “A DiSEqC™ data byte interrupting a continuous 22kHz tone,” on page 32.

6.2.4 DISEQC2 control 1 registers 121 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_CTRL1	121	DISEQC2_CTRL1[7:0]								R/W	00

bits7-6: MIN_TONE_PER Minimum Tone Period, for controlling (or fine tuning) the DiSEqC™ 2 receive algorithm.

B7-6:	MIN_TONE_PER
00	3.0 * DISEQC_RATIO
01	3.875 * DISEQC_RATIO
10	3.0 * DISEQC_RATIO
11	3.75 * DISEQC_RATIO

bit-5: Send extended pulse to the Status pin 52. This is a test or diagnostics bit. If it is set to 1, then the cleaned up and extended pulse stream is sent to the status pin so that it can be recorded or observed.

bit-4: DISEQC2 reset only the DISEQC2 receive module. Automatically set low again after use.

This is the software (partial) reset for DISEQC2 module. If this is set to 1 in the DISEQC2 listen (or receive) period, any listen operations will be aborted and DISEQC2 will wait until the end of the next transmission to expect a reply.
Note that the host starting the next DISEQC2 transmission will have a similar effect to writing bit 4.

bit-3: Interrupt enable for bit-3 of DISEQC2_INT STAT register 118.

bit-2: Interrupt enable for bit-2 of DISEQC2_INT STAT register 118.

bit-1: Interrupt enable for bit-1 of DISEQC2_INT STAT register 118.

bit-0: Interrupt enable for bit-0 of DISEQC2_INT STAT register 118.

Bits-0 and bit-3 are interrupt enables. These determine whether bits-0 to bit-3 of DISEQC2_INT (register 118, see page 37) have any impact on the pin $\overline{IRQ}$ 57 of the MT312.

Note that buffer overflow interrupt does not have an interrupt enable and hence this cannot be brought out to the $\overline{IRQ}$ pin.

6.2.5 DISEQC2 Control 2 registers 122 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_CTRL2	122	MIN_PULS_PER			TONE_EXT_PER			MAX_TONE_PER		R/W	D4

B[7:5]: MIN_PULS_PER Minimum Pulse Period.

bit-7-5:	MIN_PULS_PER
000	24 * DISEQC_RATIO
001	25 * DISEQC_RATIO
010	26 * DISEQC_RATIO
011	27 * DISEQC_RATIO

100	28 * DISEQC_RATIO
101	29 * DISEQC_RATIO
110	30 * DISEQC_RATIO (default)
111	31 * DISEQC_RATIO

B[4-2]: TONE_EXT_PER Tone Impulse Extended Period.

bit-1-0:	**TONE_EXT_PER**
000	7 * DISEQC_RATIO
001	8 * DISEQC_RATIO
010	9 * DISEQC_RATIO
011	10 * DISEQC_RATIO
100	11 * DISEQC_RATIO.
101	12 * DISEQC_RATIO. (default)
110	13 * DISEQC_RATIO.
111	14 * DISEQC_RATIO.

B[1-0]: MAX_TONE_PER Maximum Tone Period.

bit-1-0:	**TONE_EXT_PER**
00	6.0 * DISEQC_RATIO. (default)
01	6.25 * DISEQC_RATIO.
10	5.75 * DISEQC_RATIO.
11	5.5 * DISEQC_RATIO.

6.3 DiSEqC Control Read Registers

6.3.1 DISEQC2 Interrupt Indicators register 118 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_INT	118	DISEQC2_INT[7:0]								R	00

Note that the most significant four bits are not reset on read. The least significant four bits are interrupt bits which are reset when the register is read. Interrupts indicate events in history. The interrupts may be enabled to drive the IRQ pin 57 by setting required bit(s) in the DISEQC2_CTRL1 register 121, see page 35.

bit-7-4: Bits-7-4 denote the following number of bytes received:

bit-7-4 = (Number of bytes received - Number of bytes read)

Hence this is the number of bytes that would be in the FIFO BUFFER if this buffer had unlimited capacity. Since the size of this buffer is only 8 bytes, if the above difference, given by bits 7-4, exceeds eight, that indicates buffer overflow.

bit-3: Silent period exceeds 176 ms interrupt (reset on read)

The host may enable interrupts bit-1 and bit-3. Then when an interrupt is received, the host may read the DISEQC2_INT register. Then if bit-3 is one and bit-1 is 0, this indicates there has been a continuous period 176ms of silence since the end of the transmission. If the host is expecting a reply, then this silence may be taken to signify a hardware fault in the system.

There is a 5-bit number in the DISEQC2_STATUS BYTE which indicates the length of a continuous period of silence up to the read time, in multiples of 16 ms.

bit-2: Receive error interrupt (reset on read).

Bit-2 indicates an error in the received message. This does not refer to a parity error. It indicates that a bit has been lost due to excessive noise or interference in the return channel. This is identified within MT312 by the occurrence of an excessively long tone or silence period within a byte.

bit-1: End of message interrupt (reset on read).

Bit-1 indicates a new message has been received. The end of a message is identified by a silent period of about 6 ms following a byte. The end-of-message interrupt bit makes it easier for the host processor to read DiSEqC™ data from MT312. Instead of reading a byte at a time, it can read the message as a whole.

It is important to note that MT312 does not stop accepting bytes after setting end-of-message interrupt. It will receive new messages, if any, whilst the current message is being read by the host. Since the 2-wire bus read rate is higher than the byte receive rate, there is no reason for FIFO buffer overflow. After every received message there will be an interrupt.

bit-0: End of byte interrupt (reset on read).

Bit-0 is set when a new byte is received. The host may wish to ignore byte interrupts and opt to read received messages, as described below.

It is important to note that MT312 does not stop accepting bytes after setting end-of-message interrupt. It will receive new messages, if any, whilst the current message is being read by the host. Since 2-wire bus read rate is higher than the byte receive rate, there is no reason for FIFO buffer overflow.

After every received message there will be an interrupt.

6.3.2 DISEQC2 Status Indicators register 119 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_STAT	119	DISEQC2_STATUS[7:0]								R	00

bit-7-5: DISEQC2 Finite State Machine State. This is primarily for debugging the device.

bit-4-0: Silent period since last received bit, in multiples of 16 ms.

Bits 4-0 are reset to zero when a bit is received. When this 5-bit number reaches 11 (176ms), the interrupt bit-3 of DISEQC2_INT register is set. This is saturated at 31. Hence if the total period exceeds 496 ms this counter will continue to indicate 31.

6.3.3 DISEQC2 FIFO register 120 (R)

Odd byte read of register 120:

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_FIFO	120	DISEQC2_FIFO[7:0]								R	00

Even byte read of register 120:

This FIFO contains data bytes and parity bits collected. This can hold a maximum of 8 data bytes, 8 parity bits and 8 parity error bits. The parity error bit is defined as the inverse of the exclusive-OR combination (or modulo-2 addition) of all 9 bits (8 data and 1 parity). This bit will be zero when there is no parity error.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
DISEQC2_FIFO	120	Reserved						Par error	Par bit	R	00

Refer to preceding section for buffer overflow.

The received bytes are read from this location with 2-wire bus auto-increment bit set to zero. The received bytes will be available in the order received, i.e. the buffer is a First In First Out (FIFO) memory.

Note that two read operations are needed for each byte. The first read operation will give the data byte and the second will provide the associated parity bit (bit-0) and the parity-error bit (bit-1), the other 6 bits will be zero. For example, if four bytes are received, then eight read operations (with auto-increment bit set to zero) are needed to get all data bytes as well as the parity bits.

The number of bytes received is given by bits-3-0 of DISEQC2_STATUS BYTES register 119.

7.0 QPSK demodulator

7.1 QPSK Demodulator Read/Write Registers

7.1.1 Symbol rate registers 23 - 24 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
SYM_RATE_H	23	SEARCH	SR_FMT	SYM_RATE[13:8] in MS/s (high byte)						R/W	1B
SYM_RATE_L	24	SYM_RATE[7:0] in MS/s (low byte)								R/W	80

bit-15: SEARCH bit 15 = 0 known symbol rate mode

bit 15 = 1 search mode

bit-14: SR_FMT bit 14 = 0 normal mode, bits 13:0 = symbol rate * 256

bit 14 = 1 reserved mode

Known symbol rate mode:

bits13-0: Required symbol rate in MS/s x 256. Unsigned 14-bit number. e.g. for a symbol rate of 27.5 MS/s: SYM_RATE = 27.5 * 256 = 7040 = 1B80 (hex)

If either of the two DSS bits are set in the CONFIG register, then the SYM_RATE register contents are ignored and the symbol rate is taken as 20 MS/s. Hence it is not necessary to program the SYM_RATE register for DSS applications.

Search Mode:

bits 13-12: don't care

bits 11-0: sub-ranges to be searched (scaled by clock rate).

The total symbol rate range is divided into 12 sub-ranges. A bit in the above register pair is assigned to each sub-range, as defined in Figure 3 below. The symbol rate sub-range or sub-ranges to be searched are defined by setting the appropriate bits high. Small overlaps are automatically provided between successive sub-ranges. Note that the lowest sub-ranges have been provided for 90 MHz operation and the device has not been optimised for operation below 1 MS/s.

Therefore for example, (with a 90MHz system clock) to search for all signals with symbol rates from 15 MS/s to 45 MS/s, bits 15, 11, 10 & 9 are all set to '1' and all other to '0'.

Bit	Symbol Rate Sub Range MS/s
11	SYS_CLK/2 to SYS_CLK/3
10	SYS_CLK/3 to SYS_CLK/4
9	SYS_CLK/4 to SYS_CLK/6
8	SYS_CLK/6 to SYS_CLK/8
7	SYS_CLK/8 to SYS_CLK/12
6	SYS_CLK/12 to SYS_CLK/16
5	SYS_CLK/16 to SYS_CLK/24
4	SYS_CLK/24 to SYS_CLK/32
3	SYS_CLK/32 to SYS_CLK/48
2	SYS_CLK/48 to SYS_CLK/64
1	SYS_CLK/64 to SYS_CLK/96
0	SYS_CLK/96 to SYS_CLK/128

Table 3 - Symbol Sweep Ranges for General Case

Bit	Symbol Rate Sub Range MS/s
11	45 - 30
10	30 - 22.5
9	22.5 - 15
8	15 - 11.25
7	11.25 - 7.5
6	7.5 - 5.625
5	5.625 - 3.75
4	3.75 - 2.8125
3	2.8125 - 1.875
2	1.875 - 1.40625
1	1.40625 - 0.9375
0	0.9375 - 0.703125

Table 4 - Symbol Sweep Ranges for 90MHz System Clock

7.1.2 Viterbi mode register 25 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
VIT_MODE	25	AUT_IQ	V_IQ_SP	CR_ 7/8	CR_ 6/7	CR_ 5/6	CR_ 3/4	CR_ 2/3	CR_ 1/2	R/W	44

bit-7: AUT_IQ Automatic IQ phase

High = Search for correct IQ phase.

Low = Use IQ phase setting in V_IQ_SP.

When this bit is set high, the Viterbi decoder will start with the IQ phase defined in V_IQ_SP and the code rate defined in VIT_MODE[5:0], to establish the correct IQ phase of the incoming signal. When this is established, the V_IQ_SP bit will be set to that phase indication so that it can be read by software for subsequent re-tuning to the same channel.

bit-6: V_IQ_SP Swap I and Q inputs to the Viterbi decoder to overcome spectral inversion caused by the transmitter.

High = I-Q swap

Low = No I-Q swap

If the transmitted signal is known to be spectrally inverted then set this bit to 1. When AUT_IQ is set high, this bit will indicate the IQ phase following successful channel acquisition. In manual mode, when AUT_IQ is set low, software is required to determine the spectrum phase and control this bit externally.

bit-5: CR_7/8 High = Viterbi code rate 7/8.

bit-4: CR_6/7 High = Viterbi code rate 6/7.

bit-3: CR_5/6 High = Viterbi code rate 5/6.

bit-2: CR_3/4 High = Viterbi code rate 3/4.

bit-1: CR_2/3 High = Viterbi code rate 2/3.

bit-0: CR_1/2 High = Viterbi code rate 1/2.

The Viterbi decoder will search for a signal with the code rates selected by this register. If one code rate is selected, the MT312 will search for a signal with only that code rate. If the code rate is unknown then all bits 5-0 may be set, allowing the MT312 to search for all code rates.

It is also possible to choose the starting point for the code rate search by setting a bit in VIT_SETUP[bit-3:1] register (86). After searching for a signal with the initial code rate, if no signal is found the search proceeds to the next higher code rate, see page 72. All selected code rates are searched until a signal is found, irrespective of the start point. Setting the starting code rate for a search to the most likely value, can speed up a search.

In the DSS mode the code rate is not specified using VIT_MODE register. If either of the two DSS bits of the Configuration Register (127) are set, then the code rates selected by the VIT_MODE register are ignored. The DSS code rate selection is carried out as described in section 4.1 “Initialization sequence” on page 20.

The result of the search is reported in the FEC_STAT register (6), see page 51.

7.1.3 QPSK control register 26 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_CTRL	26	Rsvd	Q_IQ_SP	Rsvd	Rsvd	Rsvd	AFC_M	Rsvd	ROLL_20	R/W	00

bit-7: Rsvd — Must be set low.

bit-6: Q_IQ_SP — Swap I and Q inputs before QPSK demodulation to overcome spectral inversion caused by the receiver front-end, for example through the swapping I and Q wires on the board.

High = I-Q swap

Low = No I-Q swap

bit-5: Reserved — Must be set low.

bit-4: Reserved — Must be set low.

bit-3: Reserved — Must be set low.

bit-2: AFC_M — High = Use AFC mode, for low symbol rates only, < 10MSym/s.

bit-1: Reserved — Must be set low.

bit-0: ROLL_20 — High = Roll-off 0.20

Low = Roll-off 0.35

If either of the two DSS control bits of the Configuration Register (127) is active (section 4.2), then bit-0 (ROLL_20) is ignored and the matched filter root-raised-cosine roll-off factor is taken as 0.20. Hence this bit only allows the choice of roll-off in the DVB mode.

If the Q_IQ_SP bit is not set correctly, i.e. according to the hardware in use, the AUT_IQ bit in the VIT_MODE register [see Viterbi mode register 25 (R/W)] will allow the system to lock, but calculated frequency offsets will have the wrong sign, and may confuse the software.

7.1.4 Go command register 27 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
GO	27	Reserved							GO	R/W	00

bit-7-1: Reserved - not used.

bit-0: GO — High = release reset state to start signal capture, automatically reset to zero.

Low = no action.

If this register is read, it will return zero.

7.1.5 QPSK interrupt output enable registers 28 - 30 (R/W)

When the bits of these three registers are set high, they enable an event to generate an interrupt on the $\overline{IRQ}$ pin 57. All interrupts may be enabled together. These registers do not affect the indication of events in the read registers 0 - 3.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
IE_QPSK_H	28	IE_QPSK[23:16] Interrupt enable QPSK (high byte)								R/W	00

bit-7: High = Enable QPSK_CT_LOCK indication on interrupt pin.

bit-6: High = Enable QPSK_CT_UNLOCK indication on interrupt pin.

bit-5: High = Enable QPSK_LOCK indication on interrupt pin.

bit-4: High = Enable QPSK_UNLOCK indication on interrupt pin.

bit-3: High = Enable QPSK_TS_LOCK indication on interrupt pin.

bit-2: High = Enable QPSK_TS_UNLOCK indication on interrupt pin.

bit-1: High = Enable QPSK_CS_LOCK indication on interrupt pin

bit-0: High = Enable QPSK_CS_UNLOCK indication on interrupt pin.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
IE_QPSK_M	29	IE_QPSK[15:8] Interrupt enable QPSK (middle byte)								R/W	00

bit-7: High = Enable QPSK_FE_AGC_LOCK indication on interrupt pin.

bit-6: High = Enable QPSK_TS_AGC_LOCK indication on interrupt pin.

bit-5: High = Enable QPSK_TS_AGC_UNLOCK indication on interrupt pin.

bit-4: High = Enable QPSK_FR_LOCK indication on interrupt pin.

bit-3: High = Enable QPSK_FR_UNLOCK indication on interrupt pin.

bit-2: High = Enable QPSK calculation complete indication on interrupt pin.

bit-1: High = Enable QPSK_TS_MAX indication on interrupt pin.

bit-0: High = Enable QPSK_CS_MAX indication on interrupt pin.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
IE_QPSK_L	30	IE_QPSK[7:0] Interrupt enable QPSK (low byte)								R/W	00

bit-7: High = Enable QPSK_ST_CHA indication on interrupt pin.

bit-6: High = Enable QPSK frequency end indication on interrupt pin.

bit-5: High = Enable QPSK_BAUD end indication on interrupt pin.

bit-4: High = Enable QPSK_AFC success indication on interrupt pin.

bit-3: High = Enable QPSK_AFC fail indication on interrupt pin.

bit-2: High = Enable QPSK next FRS21 indication on interrupt pin.

bit-1: High = Enable QPSK same FRS21 indication on interrupt pin.

bit-0: High = Enable QPSK LTV limit indication on interrupt pin.

7.1.6 QPSK status output enable register 32 (R/W)

These bits enable various QPSK outputs on the STATUS pin. If more than one bit is enabled then the logical-OR combination of the selected status signals will appear on the STATUS pin (52).

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_STAT_EN	32	QPSK_STAT_EN[7:0]								R/W	00

bit-7: High = QPSK_TS sweep on

bit-6: High = QPSK_CS sweep on

bit-5: High = QPSK_FR_LOCK

bit-4: High = QPSK_TS_AGC_LOCK

bit-3: High = QPSK_TS_LOCK

bit-2: High = QPSK_CS_LOCK

bit-1: High = QPSK_CT_LOCK

bit-0: Reserved. Must be set low.

7.2 QPSK Demodulator Read Registers

7.2.1 QPSK Interrupt registers 0 - 2 (R)

The majority of these interrupts are for diagnostic purposes and generally not useful in normal operation, unless otherwise indicated.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_INT_H	00	QPSK_INT[23:16] interrupt QPSK (high byte)								R	00

bit-7: High = QPSK Carrier and Timing LOCK - important indicator.

bit-6: High = QPSK Carrier and Timing UNLOCK

bit-5: High = QPSK_LOCK - important indicator.

bit-4: High = QPSK_UNLOCK

bit-3: High = QPSK Timing LOCK

bit-2: High = QPSK Timing UNLOCK

bit-1: High = QPSK Carrier LOCK

bit-0: High = QPSK Carrier UNLOCK

Reading an interrupt register resets that register.

After the QPSK demodulator achieves Carrier and Timing Lock, from now on referred to as QPSK CT Lock, it waits some time for the FEC to confirm this lock. When the FEC locks, the QPSK enters QPSK Lock state. The time QPSK waits for the FEC to gain lock is programmable via register 81 (see Section 11.2.31 “FEC Lock Time register 81 (R/W)” on page 71). If the FEC does not achieve lock during this period (very unlikely), then MT312 drops its QPSK CT Lock status and resumes search for another QPSK signal.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_INT_M	01	QPSK_INT[15:8] Interrupt QPSK (middle byte)								R	00

bit-7: High = QPSK_FE_AGC_LOCK

bit-6: High = QPSK Digital Internal AGC LOCK

bit-5: High = QPSK Digital Internal AGC UNLOCK

bit-4: High = QPSK_FR_LOCK

bit-3: High = QPSK_FR_UNLOCK

bit-2: High = QPSK calculation complete

bit-1: High = QPSK_TS_MAX

bit-0: High = QPSK_CS_MAX

Reading an Interrupt register resets that register.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_INT_L	02	QPSK_INT[7:0] Interrupt QPSK (low byte)								R	00

The majority of these interrupts are for diagnostic purposes and generally not useful in normal operation, unless otherwise indicated.

bit-7: High = QPSK state change

bit-6: High = QPSK frequency end of search range - important indicator.

bit-5: High = QPSK_BAUD end of range - important indicator.

bit-4: High = QPSK_AFC success

bit-3: High = QPSK_AFC fail

bit-2: High = QPSK next frequency search

bit-1: High = QPSK same frequency search

bit-0: High = QPSK LTV limit

Reading an Interrupt register resets that register.

Frequency and symbol rate search is carried out as follows. If the symbol rate is known then MT312 will search the specified frequency range for this symbol rate. Once the end of this range has been reached, "QPSK end of frequency range search" interrupt will be issued and MT312 will resume the search beginning from frequency zero. A "QPSK end of symbol rate range(s) search" interrupt will not be issued.

If the symbol rate is not known, then MT312 can be made to search several sub-ranges of symbol rates, by setting up to 12-bits of the pair of SYM_RATE registers, as described in “Symbol rate registers 23 - 24 (R/W)” on page 39.

For illustration purposes, assume that the symbol rate sub-ranges SYS_CLK/2 to SYS_CLK/3 and SYS_CLK/4 to SYS_CLK/6 are to be searched. Then MT312 will begin the search from the upper sub-range SYS_CLK/2 to SYS_CLK/3. MT312 will search for a channel with a symbol rate in this range over the specified frequency range, for example ± 10 MHz. If no channel is found then MT312 will issue a "QPSK end of frequency range search" interrupt and will go on to search the sub-range SYS_CLK/4 to SYS_CLK/6 over the specified frequency range. If no channel is found, then MT312 will issue a "QPSK end of frequency range search" interrupt as well as a "QPSK end of symbol rate range(s) search" interrupt. Then MT312 will return to search the specified frequency range for a symbol rate in the range SYS_CLK/2 to SYS_CLK/3. This process continues indefinitely, unless it is interrupted by host processor software.

7.2.2 QPSK Status registers 4 - 5 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK_STAT_H	04	QPSK_STATUS[15:8] (high byte)								R	00

bit-15: High = QPSK_SNR_MSB

bit-14: High = QPSK_SNR_LSB

bit-13: High = QPSK_FR_LOCK

bit-12: High = QPSK timing AGC lock

bit-11: High = QPSK timing lock

bit-10: High = QPSK carrier lock

bit-9: High = QPSK carrier and timing (CT) lock

bit-8: High = QPSK_LOCK

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK STAT L	05	QPSK_STATUS[7:0] (low byte)								R	00

bit-7: High = QPSK Timing sweep on

bit-6: High = QPSK Carrier sweep on

bit-5-0: Reserved

7.2.3 Symbol Rate Output registers 116 - 117 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
SYM_RAT_OP_H	116	SYM_RAT_OP[15:8] Symbol Rate Output (high byte)								R	00
SYM_RAT_OP_L	117	SYM_RAT_OP[7:0] Symbol Rate Output (low byte)								R	00

SYM_RAT_OP[15:0] These two bytes contain a positive number that is inversely proportional to the symbol rate. The decimation ratio index must also be read from the MONITOR register bits B[7:5] and divided by 32 to normalise the result.

$$Rs = \frac{PLL\_CLK \times 8192}{SYM\_RAT\_OP + 8192} \times 2^{-DEC\_RATIO}$$

Where: Rs = symbol rate in MS/s

PLL_CLK = PLL clock frequency in MHz

SYM_RAT_OP = value of registers 116 and 117.

DEC_RATIO = MONITOR_H[7:5] when MON_CTRL[2:0] = 5.

7.2.4 Monitor registers 123 - 124 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
MONITOR_H	123	MONITOR[15:8] Monitor (high byte)								R	00
MONITOR_L	124	MONITOR[7:0] Monitor (low byte)								R	00

For details, see MON_CTRL register (103) on page 63.

MON_CTRL[3:0] = 0: MONITOR_H = CS_SYM_I and MONITOR_L = CS_SYM_Q.

This is a snapshot of two I and Q samples (of the same symbol) after carrier synchroniser. This information can be used to produce a scatter diagram. Keep reading these continuously and mark these as points on a 2-D I-Q plane to get a scatter diagram.

MON_CTRL[3:0] = 1: MONITOR_H = DC_OFFSET_I and MONITOR_L = DC_OFFSET_Q.

This will give the amount of DC offset in the I and Q inputs from the ADC compensated by the QPSK. Each of these is a two's complement number. If the 6-bit ADC range is taken to be in the scale -32 to 31, then it is necessary divide DC_OFFSET_I by 16, to bring it to the same scale as the ADC. For example, if we get the DC_OFFSET_I as "11111101", the corresponding two's complement number is -3. However, the actual offset with respect to the ADC scale of [-32, 31] is actually -3/16. The same applies to DC_OFFSET_Q.

MON_CTRL[3:0] = 3: MONITOR_H = MS/s OP_H and MONITOR_L = MS/s OP_L.

When the QPSK demodulator is in lock following a symbol rate search, the locked symbol rate may be read from the MONITOR register. Then:

Symbol Rate = MONITOR[15:0]/1024.

The accuracy of this reading is within ±0.25% of the actual symbol rate. Note that the channel with this symbol rate can be subsequently re-acquired without a search by programming the 14 MSBs of the above read-out (discarding the two LSBs) as the 14 LSBs of the 16-bit SYM_RATE register (23,24), see page 39.

MON_CTRL[3:0] = 5:

Decimation ratio = MONITOR[15:13]/32.

MON_CTRL[3:0] = 6: MONITOR_H = MONITOR_L = M_FLD[7:0].

M_FLD[7:0]: This byte contains a number calculated in the TS_FLD Timing synchroniser frequency lock detector and is used for frequency lock detection in the manual programming mode.

MON_CTRL[3:0] = 7: MONITOR_H = M_TLD_H and MONITOR_L = M_TLD_L.

M_TLD[15:0]: Measurement of the Timing lock detector value. Reading the bytes does NOT reset the value.

MON_CTRL[3:0] = 8: MONITOR_H = M_PLD_H and MONITOR_L = M_PLD_L

M_PLD[15:0]: Measurement of the Phase lock detector value. Reading the bytes does NOT reset the value.

Other settings of MON_CTRL[3:0] are either reserved for diagnostic purposes or not used.

8.0 Forward Error Correction

8.1 Forward error correction read/write registers

8.1.1 FEC interrupt enable register 31 (R/W)

When the bits of this register are set high, they enable an event to generate an interrupt on the pin 57. All interrupts may be enabled together.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
IE FEC	31	IE FEC[7:0] Interrupt enable FEC								R/W	00

bit-7: High = Enable DiSEqC™ indication on interrupt pin.

bit-6: High = Enable byte align lock lost indication on interrupt pin.

bit-5: High = Enable byte align lock indication on interrupt pin.

bit-4: High = Enable Viterbi lock lost indication on interrupt pin.

bit-3: High = Enable Viterbi lock indication on interrupt pin.

bit-2: High = Enable Viterbi BER monitor period reached indication on interrupt pin.

bit-1: High = Enable de-scrambler lock lost indication on interrupt pin.

bit-0: High = Enable de-scrambler lock indication on interrupt pin.

8.1.2 FEC_STATUS output enable register 33 (R/W)

If more than one bit is enabled then the logical-OR combination of the selected status signals will appear on the STATUS pin 52.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FEC_STAT_EN	33	MOCLK_RATIO[3:0]				DS_lock	BA_lock	VIT_lock	BER_tog	R/W	14

bit-7-4: MOCLK_RATIO[3:0] MPEG clock ratio - 6. i.e. range is from 6 to 21
see section 10.1.3 “MANUAL MOCLK = 1 and DIS_SR = 0” on page 56.

bit-3: DS_lock High = De-scrambler lock

bit-2: BA_lock High = Byte Align lock

bit-1: VIT_lock High = Viterbi lock

bit-0: BER_tog High = BER toggle. This bit enables an audio frequency signal to be output on the STATUS pin to indicate BER during dish alignment, see section 2.4.1.1 “Viterbi error count coarse indication” on page 13. The frequency of the signal is controlled by VIT_MAXERR register (94), see page 73.

8.1.3 FEC setup register 97 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FEC_SETUP	97	DIS_SR	ENCL_KO	DIS_DS	DIS_RS	DIS_VIT	EN_PRS	DS_LK[1:0]		R/W	03

bit-7: When MANUAL_MOCLK (“Output data control register 96 (R/W)” on page 62) is low then:

DIS_SR High = Disable use of symbol rate for MOCLK generation.

Low = Use symbol rate for MOCLK generation.

When MANUAL MOCLK (register 96 bit 7) is high then:

DIS_SR High = Use external MICLK (pin 14) signal for MOCLK.

Low = Manually set MOCLK period from MOCLK_RATIO (“FEC_STATUS output enable register 33 (R/W)” on page 50).

bit-6: ENCL_KO High = Enable clock out for test purposes.

bit-5: DIS_DS High = Disable de-scrambler.

bit-4: DIS_RS High = Disable Reed-Solomon decoder.

bit-3: DIS_VIT High = Disable Viterbi (Viterbi by pass mode)

bit-2: EN_PRS High = Enable programmed synchronisation byte in register 98 (see “Program Synchronising Byte register 98 (R/W)” on page 74).

bits1-0: DS_LK[1:0] + 2 = Number of bytes for de-scrambler to lose lock. The default register value of 3 is equivalent to 5 bad sync words.

8.2 Forward Error Correction Read Registers

8.2.1 FEC interrupt register 3 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FEC_INT	03	FEC_INT[7:0] Interrupt FEC								R	00

bit-7: High = DiSEqC™ event, see “DISEQC instruction register 36 (R/W)” on page 34

bit-6: High = Byte align lock lost

bit-5: High = Byte align lock - important indicator.

bit-4: High = Viterbi lock lost

bit-3: High = Viterbi lock

bit-2: High = Viterbi BER monitor period reached

bit-1: High = De-scrambler lock lost

bit-0: High = De-scrambler lock

Reading an Interrupt register resets that register.

8.2.2 FEC status register 6 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
FEC_STATUS	06	FEC_STATUS[7:0]								R	00

bit-7: Reserved

bit-6-4: Viterbi coding rate

bit 6	bit5	bit 4	bits 6-4	Code rate indication
0	0	0	0	1/2
0	0	1	1	2/3
0	1	0	2	3/4
0	1	1	3	5/6
1	0	0	4	6/7
1	0	1	5	7/8

Table 5 - Viterbi Code Rate Indication

bit-3: High = De-scrambler lock

bit-2: High = Byte align lock

bit-1: High = Viterbi lock

bit-0: Reserved

8.2.3 Measured Signal-to-Noise-Ratio registers 9 - 10 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
M_SNR_H	09	Reserved	M_SNR[14:8] measured SNR (high byte)							R	00
M_SNR_L	10	M_SNR[7:0] measured SNR (low byte)								R	00

bit-15: Reserved

M_SNR[14:0]: These two registers provide a indication of the signal to noise ratio of the channel being received by the MT312. It should not be taken as the absolute value of the SNR.

$$Eb/N0 \sim \frac{13312 - M\_SNR[14:0]}{683} \text{ dB}$$

The equation given only holds for Es/N0 values in the range 3 to 15 dB, i.e. Eb/N0 values in the range 0 to 12 dB.

8.2.4 Viterbi error count at Viterbi input registers 11 - 13 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
VIT_ERRCNT_H	11	VIT_ERRCNT[23:16] - Viterbi error count (high byte)								R	00
VIT_ERRCNT_M	12	VIT_ERRCNT[15:8] - Viterbi error count (middle byte)								R	00
VIT_ERRCNT_L	13	VIT_ERRCNT[7:0] - Viterbi error count (low byte)								R	00

This is effectively the QPSK Bit Error Rate.

VIT_ERRCNT[23:0]: This is the count of bits corrected by the Viterbi decoder. This value is updated when the Viterbi error timer (VIT_ERRPER) expires (indicated by bit-2 in register FEC_INT) and is NOT reset by reading.

$$QPSK\_BER = \frac{VIT\_ERRCNT[23:0]}{VIT\_ERRPER[23:0] * 4}$$

8.2.5 Reed-Solomon bit errors corrected registers 14 - 16 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
RS_BERCNT_H	14	RS_BERCNT[23:16] - Reed-Solomon bit errors corrected (high byte)								R	00
RS_BERCNT_M	15	RS_BERCNT[15:8] - Reed-Solomon bit errors corrected (middle byte)								R	00
RS_BERCNT_L	16	RS_BERCNT[7:0] - Reed-Solomon bit errors corrected (low byte)								R	00

This is effectively the Viterbi Bit Error Rate.

RS_BERCNT[23:0]: These three registers provide a measurement of the number of bit errors corrected by the Reed-Solomon decoder. Reading the high byte stops the count incrementing. Reading the low byte resets all three bytes and restarts the count incrementing again.

$$\text{Viterbi BER} = \frac{\text{RS\_BERCNT[23:0]}}{dt * Rs * 2 * CR}$$

Where: dt = delta time between two readings in sec (recommend 20s for 20 - 30 MS/s signals)
Rs = symbol rate in Baud
CR = Viterbi code rate
In denominator: the factor 2 is for QPSK, change it to 1 for BPSK

e.g. for Rs = 27.5MS/s, CR = 3/4 and dt = 20 sec

$$\text{Viterbi BER} = \frac{\text{RS\_BERCNT[23:0]} \times 4}{20 \times (27.5 \times 10^6) \times 2 \times 3} = \frac{\text{RS\_BERCNT[23:0]}}{8.25 \times 10^8}$$

8.2.6 Reed-Solomon uncorrected block errors registers 17 - 18 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
RS_UBC_H	17	RS_UBC[15:8] - Reed-Solomon uncorrected block errors (high byte)								R	00
RS_UBC_L	18	RS_UBC[7:0] - Reed-Solomon uncorrected block errors (low byte)								R	00

RS_UBC[15:0]: These two registers provide a measurement of the Reed-Solomon uncorrected block errors.

Reading the high byte resets the byte and stops the count incrementing. Reading the low byte resets the byte and restarts the count incrementing again.

$$\text{Block error rate} = \frac{\text{RS\_UBC[15:0]} \times \text{Blk\_size}}{dt \times Rs \times 2 \times CR}$$

where: dt = delta time between two readings in sec

Rs = symbol rate in Baud

CR = Viterbi code rate

Blk_size = 1632 bits for DVB and 1096 bits for DSS

In denominator, the factor 2 is for QPSK, change it to 1 for BPSK

9.0 Automatic Gain Control

9.1 Automatic gain control read/write registers

9.1.1 AGC control register 39 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
AGC_CTRL	39	Reserved	Reserved	AGC_SD[1:0]		AGC_BW[2:0]			AGC_SL	R/W	26

bit-7: Reserved. Must be set low.

bit-6: Reserved. Must be set low.

bit-5-4: AGC_SD[1:0] Sigma-Delta clock decimation ratio related to system clock.

AGC_SD[1:0]	Decimation
00	2
01	4
10	8
11	16

Table 6 - Sigma Delta Clock Decimation Ratio Programming

AGC control output is a pulse density modulated output created by a sigma-delta modulator. To reduce power consumption this is not clocked at the full system clock rate. The frequency at which this is clocked is the system clock divided by the decimation factor in Table 6.

bit-3-1: AGC_BW[2:0] Front End AGC bandwidth (retain default value of 3).

bit-0: AGC_SL Analogue AGC slope

High = positive slope i.e. RF gain proportional to AGC voltage.

Low = negative slope i.e. RF gain inversely proportional to AGC voltage (default).

9.1.2 AGC_REF Reference Value register 41 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
AGC_REF	41	AGC_REF[7:0] AGC reference level								R/W	67

AGC_REF[7:0] Front End AGC reference value.

The AGC loop control in MT312 is designed to bring the mean square value of the I signal (or the Q signal) at the ADC output (prior to any digital filtering) to the value set by the AGC_REF register.

9.2 Automatic gain control read registers

9.2.1 Measured signal level at MT312 input register 19 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
SIG_LEVEL	19	SIG_LEVEL[7:0] - Signal level at MT312 input								R	00

bits 7-0: SIG_LEVEL[7:0]: This register provides a measurement of the MT312 input signal level. When AGC is controlling the signal level, there is a direct relationship between SIG_LEVEL and AGC_REF: SIG_LEVEL * 8 = AGC_REF

Note: the signal level is measured at the output of the ADC before any digital filtering takes place. Hence the reading includes all noise and other signal channels passed by the SAW or baseband filter.

9.2.2 Measured AGC feed back value registers 108 - 110 (R)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
AGC H	108	AGC[13:6] - Front end AGC (high byte)								R	00
AGC M	109	AGC[5:0] - Front end AGC (low byte)						ERR_DB[9:8]		R	00
AGC L	110	ERR_DB[7:0] - Error difference (low byte)								R	00

AGC[13:0]: These two registers provide a measurement of the AGC error feed back value by the MT312 to the front end. Reading the bytes does NOT reset the value.This measurement can be used to provide an indication of the signal level at the input to the tuner.

To avoid having too large a number, the following formula extracts a number less than 1024:

Approximate input level = AGC[13-4].

ERR_DB[9:0]: The ERR_DB is the difference between the expected signal level defined by AGC_REF and received signal level. This is in a non-linear logarithmic scale (hence the notation DB).

The way H/M/L registers work within the QPSK block is as follows. When the H register is read, the 24-bit value is copied into a shadow register. Reading the M and L registers is optional after this. It is NOT an option to read M and L (or just L of a 24 or 16-bit register) without reading H. The safest solution is to read H/M/L in that order.

10.0 MPEG Packet Data Output

10.1 MPEG clock modes

There are four MOCLK modes of operation, controlled by register bits.

MANUAL MOCLK (register 96 bit 7)	DIS_SR (register 97 bit 7)	MOCLK generation mode
0	0	Use symbol rate for MOCLK generation.
0	1	Disable use of symbol rate for MOCLK generation.
1	0	Manually set MOCLK period from MOCLK_RATIO (reg. 33).
1	1	Use external MICLK (pin 14) signal for MOCLK.

Table 7 - MPEG Clock Modes

10.1.1 MANUAL MOCLK = 0 and DIS_SR = 0.

In this mode MOCLK is generated from the symbol clock. MOCLK will be a continuously running clock once symbol lock has been achieved in the QPSK block.

10.1.2 MANUAL MOCLK = 0 and DIS_SR = 1.

In this mode MOCLK is not generated from the symbol clock but instead uses the data in the QPSK decimation ratio. This mode is not normally used but is available for engineering test purposes.

10.1.3 MANUAL MOCLK = 1 and DIS_SR = 0

This is the Programmable Clock Division Ratio mode of operation. MOCLK is generated by dividing the PLL clock frequency by the MOCLK_RATIO + 6 see register 33 on see “FEC_STATUS output enable register 33 (R/W)” on page 50.

$$\text{MOCLK frequency} = \frac{\text{PLL frequency}}{(\text{MCLK\_RATIO} + 6)}$$

PLL Frequency	Moclk Ratio + 6	Moclk Frequency	Comment
60MHz	6	10.0MHz	maximum
60MHz	9	6.667MHz	minimum
90MHz	6	15MHz	maximum
91MHz	9	10.111MHz	minimum

Table 8 - MOCLK Input Minimum And Maximum Frequencies

The range of values of 6 to 9 for (MOCLK_RATIO + 6) will guarantee operation for 2 - 45 MSym/s. However, for a restricted range of symbol rates, higher (MOCLK_RATIO + 6) values may be used with a lower MOCLK frequency. The equation in “Data output timing” on page 61 must be evaluated to ensure successful operation and avoid buffer overflow in the MT312.

10.1.4 MANUAL MOCLK = 1 and DIS_SR = 1.

This is the External MPEG Clock mode of operation. The external MOCLK is input on the MICLK pin 14. The clock supplied must be a continuous clock, otherwise the data buffers in the MT312 would overflow and data would be lost. The maximum permitted MICLK frequency is:

$$\text{MICLK frequency maximum} = \frac{\text{PLL frequency}}{6.3}$$

Where PLL frequency is 60MHz the MICLK frequency maximum = 9.524MHz.

Where PLL frequency is 91MHz the MICLK frequency maximum = 14.444MHz.

As in the Programmable Clock Division Ratio mode, the minimum MICLK frequency must be high enough to clock the complete MPEG packet out before the next one arrives. For this reason, the minimum MICLK frequency recommended is 6.7MHz at 60MHz and 10MHz at 90MHz.

The MCLKINV control bit in the Output Data Control register (96) will change the phase of the MICLK used to clock the data out. With MCLKINV = 0, data are clocked out on the positive edge of MICLK. If MCLKINV = 1, data are clocked out on the negative edge of MICLK.

10.2 Data Output Header Format - DVB

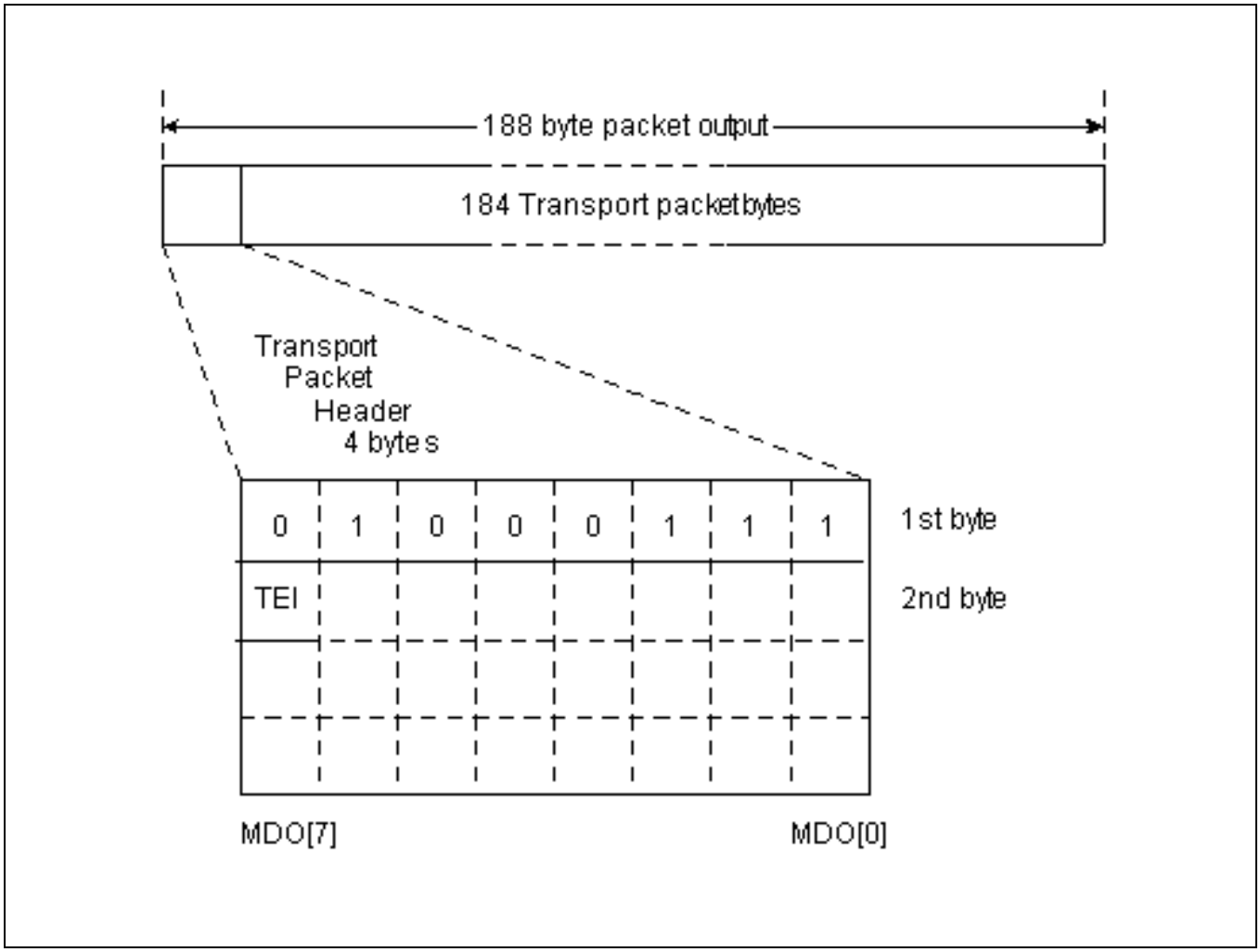

Figure 20 - DVB Transport Packet Header Bytes

After decoding the 188 byte MPEG packet, it is output on the MDO pins in 188 consecutive clock cycles.

Additionally, in DVB mode, when the EN_TEI bit in the OP_CTRL register (96) is set high (default), the TEI bit of any uncorrectable packet will automatically be set to 1, see page 62. If the EN_TEI bit is low, the TEI bit will not be changed (but note that if this bit is already 1, for example, due to a channel error which has not been corrected, it will remain high at output).

10.3 MPEG/DSS Data Output Signals

MOCLK will be a continuously running clock once symbol lock has been achieved in the QPSK block and is derived from either the system clock or MICLK if external clock is selected. MOCLK is the MPEG data byte rate clock, the internal rate is calculated from the formulae in section 10.4. The maximum movement in the packet synchronisation byte position is limited to ± one output clock period.

All output data and signals (MDO[7:0], MOSTRT, MOVAL, $\overline{\text{BKERR}}$) change on the negative edge of MOCLK (MCLKINV = 1) to present stable data and signals on the positive edge of the clock. A complete packet is output on MDO[7:0] on 188 (DVB) or 130 (DSS) consecutive clocks and the MDO[7:0] pins will remain low during the inter packet gaps. MOSTRT goes high for the first byte clock of a packet. MOVAL goes high on the first byte of a packet and remains high until the 188th byte (DVB) or 130th byte (DSS) has been clocked out.

$\overline{\text{BKERR}}$ has two modes of operation, selected by ERR_IND bit 7 of MON_CTRL register 103, see page 63.

10.3.1 ERR_IND = 0

When ERR_IND is Low: $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the 188th byte (DVB) or 130th byte (DSS) has been clocked out. $\overline{\text{BKERR}}$ also goes high when there is no de-scrambler lock, i.e. there are no MPEG packets being output.

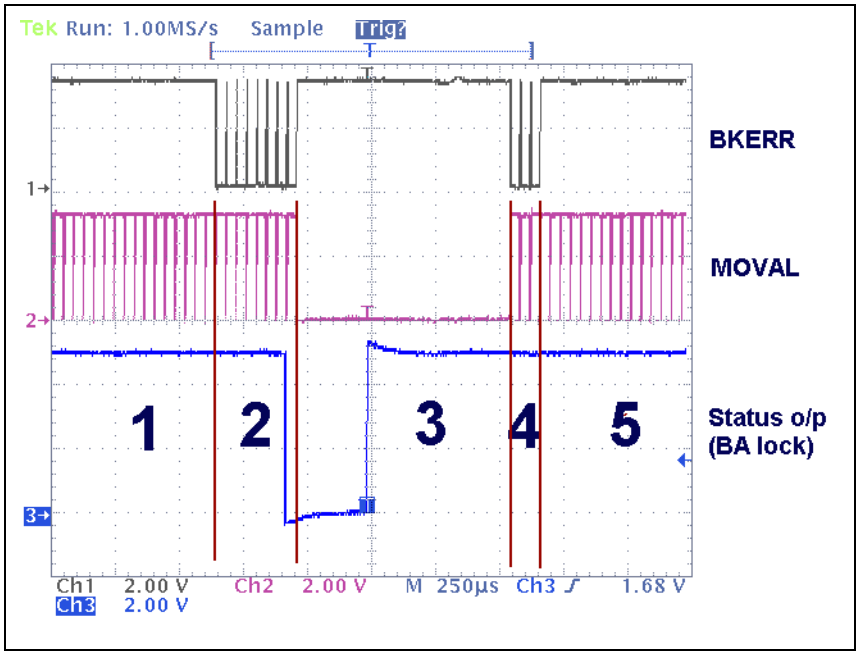

Figure 21 - $\overline{\text{BKERR}}$ example when ERR_IND is low

Figure 21 above shows lock being lost while ERR_IND is low. The event is divided into five significant periods:

1. Packets being received without errors.
2. Packets being received with errors.
3. Signal too poor for any packets to be received (lost lock).
4. Lock regained but packets still have errors.
5. Packets being received again with no errors.

10.3.2 ERR_IND = 1

When ERR_IND is High: BKERR remains high when error free MPEG packets are being output on the MDO[7:0] bus. BKERR goes low when there is no de-scrambler lock or on the first byte of a packet where uncorrectable bytes are detected. BKERR remains low until error free MPEG packets are being output on the MDO[7:0] bus.

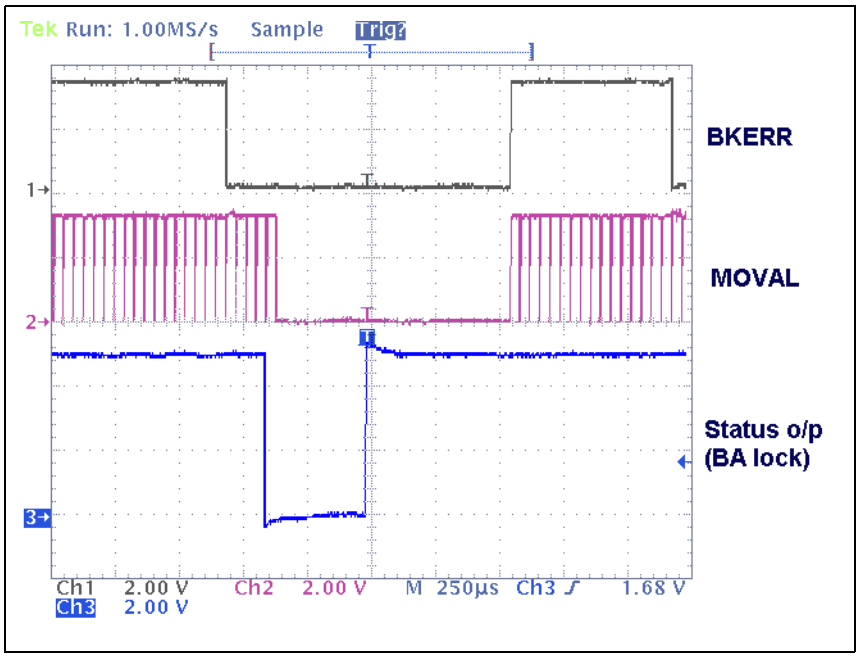

Figure 22 - BKERR example when ERR_IND is high.

Figure 22 above shows lock being lost while ERR_IND is high. The events are similar to the previous figure but BKERR remains low when signal lock is lost.

Note: the signal on pin 75 can be inverted by setting the BKERIV bit 6 of OP_CTRL register 96, see page 62.

10.4 Data output timing

The number of PLL clocks per Byte clock is:

$$N = \frac{Q*R*P}{2*V} * \frac{PLL}{RS}$$ truncated to an integer

Where: Q = 1 for QPSK, 2 for BPSK

R = 204/193 for DVB, 147/135 for DSS

P = 8 for parallel byte output, 1 for serial byte output

V = Viterbi code rate, e.g. 3/4 for typical ASTRA signals

PLL = Sampling frequency MHz

RS = symbol rate in MS/s, e.g. 27.5MS/s for typical ASTRA signals

e.g. For DVB ASTRA	N	= 1 * 204/193 * 8/2 * 4/3 *90E6/27.5E6
	N	= 18
The transport Stream clock rate		= PLL/N
		= 90E6/18
		= 5E6Hz
The time to transmit a packet		= 204 * 8/2 * 4/3 *1/RS
		= 1088/RS
		= 3.9564E-5 sec
Time to output 188 bytes		= 188/5E6
		= 3.76E-5 sec
The gap between packets		= 3.9564E-5 - 3.76E-5
		= 1.936E-6 sec
The gap as number of byte clocks		= 1.936E-6 * 5E6
		= 9.82

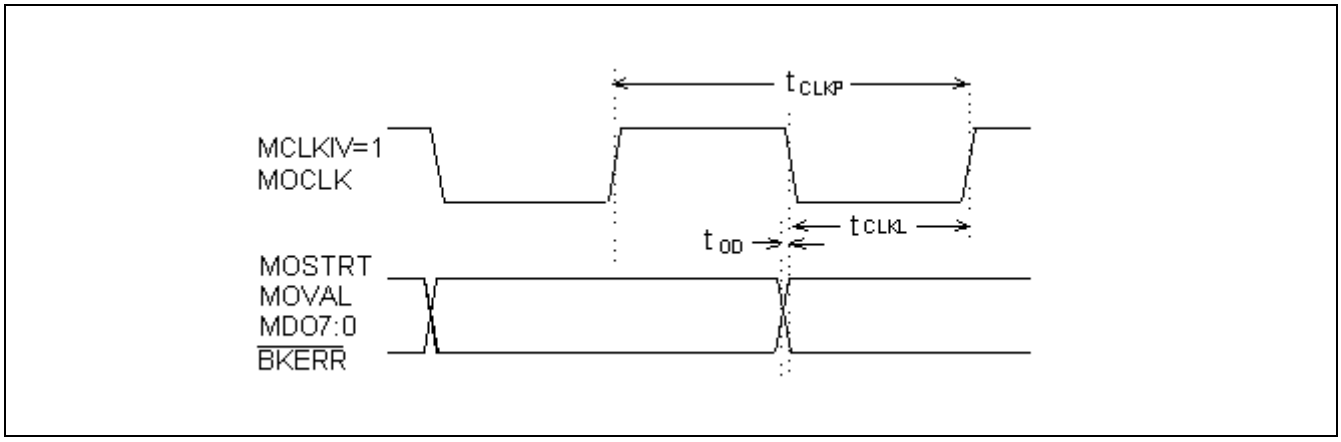

Figure 23 - MT312 Data Output Timing Diagram

Parameter	Symbol	Min	Typ	Max	Units
Data output delay (when MCLKINV = 1)	tOD		±2	±4	ns

10.5 MPEG Packet Data Output Read/Write Registers

10.5.1 Output data control register 96 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
OP_CTRL	96	MANUAL_MOCLK	BKERIV	MCLKINV	EN_TEI	BSO	BA_LK[2:0]			R/W	33

bit-7: MANUAL_MOCLK Manual MOCLK mode selection, see register 97 on page 50.

bit-6: BKERIV High = Inverted signal on $\overline{\text{BKERR}}$ output pin.

Low = Normal signal on $\overline{\text{BKERR}}$ output pin.

bit-5: MCLKINV High = Normal signal on MOCLK output pin.

Low = Inverted signal on MOCLK output pin.

For a description of how to use these features, see section 10.1 “MPEG clock modes” on page 56.

With MCLKINV = 0, data are clocked out on the positive edge of MOCLK. If MCLKINV = 1, data are clocked out on the negative edge of MOCLK.

bit-4: EN_TEI High = Enable automatic setting of transport error indicator (TEI) bit in MPEG packet header byte 2 when the block is flagged as uncorrectable by the Reed-Solomon decoder. See section 10.2 “Data Output Header Format - DVB” on page 58. (Not used in DSS).

bit-3: BSO High = Bit serial output of the MPEG data on MDO0 pin.

Low = Parallel output of the MPEG data on MDO[7:0] pins.

bit-2 -0: BA_LK[2:0] + 2 = Number of bytes for byte aligner to lock.

The default register value of 3 is equivalent to 5 good sync words.

10.5.2 Monitor Control register 103 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
MON_CTRL	103	ERR_IND	Reserved			MON_CTRL[3:0]				R/W	00

bit-7: ERR_IND Error Indicator.

High $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low when there is no De-scrambler lock OR on the first byte of a packet where uncorrectable bytes are detected. $\overline{\text{BKERR}}$ will remain low until error free MPEG packets are being output on the MDO[7:0] bus.

Low $\overline{\text{BKERR}}$ remains high when error free MPEG packets are being output on the MDO[7:0] bus. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the 188th byte (DVB) or 130th byte (DSS) has been clocked out.

Note: the $\overline{\text{BKERR}}$ signal on pin 75 can be inverted by setting the BKERIV bit 6, see page 62.

bit-6-4: Reserved, not used.

bit-3-0: MON_CTRL[3:0] selects which pair of registers will be read from MONITOR_H & L registers 123 and 124, (see section 7.2.4 “Monitor registers 123 - 124 (R)” on page 48).

MON_CTRL[3:0]	MONITOR_H (123)	MONITOR_L (124)
0	CS_SYM_I	CS_SYM_Q
1	DC_OFFSET_I	DC_OFFSET_Q
2	Reserved	Reserved
3	MS/s OP_H	MS/s OP_L
4	Reserved	Reserved
5	DEC_RATIO[15:13] and the rest reserved	Reserved
6	M_FLD[7:0]	M_FLD7:0]
7	M_TLD_H	M_TLD_L
8	M_PLD_H	M_PLD_L
15 - 9	Not used	Not used

I and Q input samples when MON_CTRL[3:0] = 0.

DC offset in the I and Q inputs when MON_CTRL[3:0] = 1.

Symbol Rate when MON_CTRL[3:0] = 3, (see page 48).

Decimation ratio when MON_CTRL[3:0] = 5, (see page 48).

Timing synchroniser frequency lock detector value when MON_CTRL[3:0] = 6, (see page 48).

Timing lock detector value when MON_CTRL[3:0] = 7, (see page 48).

Phase lock detector value when MON_CTRL[3:0] = 8, (see page 48).

The remaining settings of MON_CTRL[3:0] are either reserved for diagnostic purposes or not used.

11.0 Secondary Registers for Test and De-Bugging

11.1 Read/Write Secondary Register Map

Name	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex	Page
AGC_INIT	40	AGC_INIT[7:0] Front end AGC initial value								R/W	3B	66
AGC_MAX	42	AGC_MAX[7:0] Front end AGC maximum value								R/W	FF	66
AGC_MIN	43	AGC_MIN[7:0] Front end AGC minimum value								R/W	00	66
AGC_LK_TH	44	AGC_LK_TH[7:0] Front end AGC lock threshold value								R/W	0A	66
TS_AGC_LK_TH	45	TS_AGC_LK_TH[7:0] Fine AGC lock threshold value								R/W	1E	66
AGC_PWR_SET	46	AGC_PWR_SET[7:0] AGC power initial value								R/W	14	66
QPSK_MISC	47	DAGC_D	A_OPEN	MIX_D	CACC_D	FOC_D	TSLP_D	CSLP_D	ADC_FM	R/W	00	66
SNR_THS_LOW	48	SNR_THS_LOW[7:0] SNR estimator low threshold								R/W	5A	66
SNR_THS_HIGH	49	SNR_THS_HIGH[7:0] SNR estimator high threshold								R/W	46	67
TS_SW_RATE	50	TS_SW_RATE[7:0] TS sweep rate								R/W	1E	67
TS_SW_LIM_L	51	TS_SW_LIM_L[7:0] TS sweep limit low								R/W	40	67
TS_SW_LIM_H	52	TS_SW_LIM_H[7:0] TS sweep limit high								R/W	84	67
CS_SW_RATE_1	53	CS_SW_RATE_1[7:0] CS sweep rate								R/W	20	67
CS_SW_RATE_2	54	CS_SW_RATE_2[7:0] CS sweep rate								R/W	48	67
CS_SW_RATE_3	55	CS_SW_RATE_3[7:0] CS sweep rate								R/W	70	67
CS SW RATE 4	56	CS_SW_RATE_4[7:0] CS sweep rate								R/W	90	67
CS_SW_LIM	57	CS SW LIM[7:0] CS sweep limit								R/W	7C	68
TS_LPK	58	TS_KPROPE[11:4]								R/W	57	68
TS_LPK_M	59_	TS_KPROPE[3:0]				TS_KINTE[11:8]				R/W	85	68
TS_LPK_L	60	TS_KINTE[7:0]								R/W	9B	68
CS_KPROP_H	61	NONSNR	CS_KP2[4:0]					CS_KP1[4:3]		R/W	12	68
CS_KPROP_L	62	CS_KP1[2:0]			CS_KP0[4:0]					R/W	96	68
CS_KINT_H	63	Reserved	CS_KI2[4:0]					CS_KI1[4:3]		R/W	51	69
CS_KINT_L	64	CS_KI1[2:0]			CS_KI0[4:0]					R/W	3B	69
QPSK_SCALE	65	QPSK_SCALE[7:0] QPSK output scale factor for IOUT and QOUT outputs								R/W	27	69
TLD_OUTLK_TH	66	TLD_OUTLK_TH[7:0] TLD threshold when not in lock								R/W	82	69
TLD_INLK_TH	67	TLD_INLK_TH[7:0] TLD threshold when in lock								R/W	0A	69
FLD_TH	68	FLD_TH[7:0] Frequency lock threshold								R/W	20	69
PLD_OUTLK3	69	SW_R_N_MX[1:0]	PLD_OUTLK3[9:4]							R/W	AE	70
PLD_OUTLK2	70	PLD_OUTLK3[3:0]				PLD_OUTLK2[9:6]				R/W	E6	70
PLD_OUTLK1	71	PLD_OUTLK2[5:0]						PLD O LK1 [9:8]		R/W	40	70
PLD_OUTLK0	72	PLD_OUTLK1[7:0]								R/W	7E	70
PLD_INLK3	73	Reserved	PLD_INLK3[9:4]							R/W	01	70
PLD_INLK2	74	PLD_INLK3[3:0]_				PLD_INLK2[9:6]				R/W	A0	70
PLD_INLK1	75	PLD_INLK2[5:0]						PLD INLK1 [9:8]		R/W	68	70
PLD_INLK0	76	PLD_INLK1[7:0]								R/W	1A	70
PLD_ACC_TIME	77	CS_PLD_MPLEN[3:0]				LOSSLOCK_INT_SW[3:0]				R/W	48	70
SWEEP_PAR	78	SW_LIM_SC[1:0]	TS_NR_SWEEP[2:0]				CS_NR_SWEEP[2:0]			R/W	49	71

Table 9 - Read/write Secondary Register Map

Name	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex	Page
STARTUP_TIME	79	STARTUP_INTERVAL[7:0]								R/W	30	71
LOSSLOCK_TH	80	LOSSLOCK_TH_SPUR[3:0]				LOSSLOCK_TH_SW[3:0]				R/W	21	71
FEC_LOCK_TM	81	FEC_LOCK_TIME[7:0]								R/W	20	71
LOSSLOCK_TM	82	LOSSLOCK_TIME[7:0]								R/W	10	72
VIT_ERRPER_H	83	VIT_ERRPER[23:16] Viterbi error period (high byte)								R/W	FF	72
VIT_ERRPER_M	84	VIT_ERRPER[15:8] Viterbi error period (middle byte)								R/W	FF	72
VIT_ERRPER_L	85	VIT_ERRPER[7:0] Viterbi error period (low byte)								R/W	FF	72
VIT_SETUP	86	FR_AL_TM_O[1:0]		SRCH_CYC[1:0]		SEARCH_START[2:0]			EX_F_LK	R/W	34	72
VIT_REF0	87	VIT_REF0[7:0] Viterbi reference byte 0								R/W	80	73
VIT_REF1	88	VIT_REF1[7:0] Viterbi reference byte 1								R/W	14	73
VIT_REF2	89	VIT_REF2[7:0] Viterbi reference byte 2								R/W	0A	73
VIT_REF3	90	VIT_REF3[7:0] Viterbi reference byte 3								R/W	06	73
VIT_REF4_	91	VIT_REF4[7:0] Viterbi reference byte 4								R/W	04	73
VIT_REF5	92	VIT_REF5[7:0] Viterbi reference byte 5								R/W	02	73
VIT_REF6	93	VIT_REF6[7:0] Viterbi reference byte 6								R/W	01	73
VIT_MAXERR	94	VIT_MAXERR[7:0] Viterbi max. error bit count								R/W	FF	73
BA_SETUPT	95	BA_FSM[1:0]		BA_MV_[1:0]		BA_UNLK[3:0]				R/W	D4	74
PROG_SYNC	98	PROG_SYNC_BYTE[7:0] Enabled by FEC_SETUP [2]								R/W	47	74
AFC_SEAR_TH	99	AFC_SEAR_TH[7:0]								R/W	23	74
CSACC_DIF_TH	100	ACC_DIF_TH[7:0]								R/W	20	74
QPSK_LK_CT	101	CS_LLK	TS_LLK	ACC_CK	NUM_PLD_INT[4:0]					R/W	04	74
QPSK_ST_CT	102	HLD_ST	AFC_RS	M_SRS	NXT_FR	FCE_ST	FORCED_ST[2:0]			R/W	00	75
QPSK_RESET	104	Reserved		REL_QP	PR_QP	PR_CS	PR_TS	PR_FE	PR_AGC	R/W	00	75
QPSK_TST_CT	105	QPSK_TEST_CTRL[7:0]								R/W	00	75
QPSK_TST_ST	106	QPSK_TEST_TS[7:0]								R/W	00	75
TEST_MODE	125	Test mode								R/W	00	75

Table 9 - Read/write Secondary Register Map (continued)

11.2 Secondary Registers for Test and De-Bugging Read/Write Registers

11.2.1 AGC Initial Value register 40 (R/W)

AGC INIT (40)	**Default value**	**59 dec.**	**3B hex.**
AGC INIT[7:0]	Front End AGC initial value.		

11.2.2 AGC Maximum Value register 42 (R/W)

AGC MAX (42)	**Default value**	**255 dec.**	**FF hex.**
AGC MAX[7:0]	Front End AGC maximum value.		

11.2.3 AGC Minimum Value register 43 (R/W)

AGC MIN (43)	**Default value**	**0 dec.**	**00 hex.**
AGC MIN[7:0]	Front End AGC minimum value.		

11.2.4 AGC Lock Threshold Value register 44 (R/W)

AGC LK TH (44)	**Default value**	**10 dec.**	**0A hex.**
AGC LK TH[7:0]	Front End AGC lock threshold value.		

11.2.5 AGC Lock Threshold Value register 45 (R/W)

TS AGC LK TH (45)	**Default value**	**30 dec.**	**1E hex.**
TS AGC LK TH[7:0]	Timing synchroniser fine AGC lock threshold value.		

11.2.6 AGC Power Setting Initial Value register 46 (R/W)

AGC PWR SET (46)	**Default value**	**20 dec.**	**14 hex.**
AGC PWR AGC SET[7:0]	power setting initial value.		

11.2.7 QPSK Miscellaneous register 47 (R/W)

QPSK MISC (47)	**Default value**	**0 dec.**	**00 hex.**
QPSK MISC[bit-7-0]	Reserved, must be set low,		

11.2.8 SNR_LOW threshold value register 48 (R/W)

SNR_THS_LOW (48)	**Default value**	**90 dec.**	**5A hex.**
SNR THS LOW[7:0]	SNR low threshold value.		

11.2.9 SNR_HIGH threshold value register 49 (R/W)

SNR_THS_HIGH (49)	**Default value**	**70 dec.**	**46 hex.**

SNR_THS_HIGH[7:0]	SNR high threshold value.	**Change to 50 dec. 32 hex. after a full reset.**

11.2.10 Timing Synchronisation Sweep Rate register 50 (R/W)

TS_SW_RATE (50)	**Default value**	**30 dec.**	**1E hex.**

TS SW RATE[7:0]	Timing Synchronisation sweep rate. For DSS set the value to 20 dec. 14 hex. after a full reset.

11.2.11 Timing Synchronisation Sweep Limit Low register 51 (R/W)

TS SW LIM L (51)	**Default value**	**64 dec.**	**40 hex.**

TS SW LIM L[7:0]	Timing Synchronisation sweep limit low.

11.2.12 Timing Synchronisation Sweep Limit High register 52 (R/W)

TS SW LIM H (52)	**Default value**	**132 dec.**	**84 hex.**

TS SW LIM H[7:0]	Timing Synchronisation sweep limit high.

11.2.13 Carrier Synchronisation Sweep Rate 1 register 53 (R/W)

CS SW RATE 1 (53)	**Default value**	**32 dec.**	**20 hex.**

CS SW RATE 1[7:0]	Carrier Synchronisation sweep rate 1.

11.2.14 Carrier Synchronisation Sweep Rate 2 register 54 (R/W)

CS SW RATE 2 (54)	**Default value**	**72 dec.**	**48 hex.**

CS SW RATE 2[7:0]	Carrier Synchronisation sweep rate 2

11.2.15 Carrier Synchronisation Sweep Rate 3 register 55 (R/W)

CS SW RATE 3 (55)	**Default value**	**112 dec.**	**70 hex.**

CS SW RATE 3[7:0]	Carrier Synchronisation sweep rate 3.

11.2.16 Carrier Synchronisation Sweep Rate 4 register 56 (R/W)

CS SW RATE 4 (56)	**Default value**	**144 dec.**	**90 hex.**

CS SW RATE 4[7:0]	Carrier Synchronisation sweep rate 4.

11.2.17 Carrier Synchronisation Sweep Limit register 57 (R/W)

CS SW LIM (57) **Default value 124 dec. 7C hex.**

CS SW LIM[7:0] Carrier Synchronisation sweep limit.

11.2.18 Timing Synchronisation Coefficients registers 58 - 60 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
TS LPK H	58	TS KPROPE[11:4]								R/W	57
TS LPK M	59	TS KPROPE93:0]				TS KINTE[11:8]				R/W	85
TS LPK L	60	TS KINTE[7:0]								R/W	9B

bit-23-12: TS KPROPE[11:0] Timing Synchronisation Proportional path coefficients.

bit-11-0: TS KINTE [11:0] Timing Synchronisation Integration path coefficients.

11.2.19 Carrier Synchronisation Proportional Part Coefficients registers 61 - 62 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
CS KPROP_H	61	NON SNR	CS KP2[4:0]					CS KP1[4:3]		R/W	12
CS KROP_L	62	CS KP1 [2:-0]			CS KP0[p4:0]					R/W	3B

bit-15: NONSNR High = Non SNR sweep.

bit-14-10: CS KP2[4:0] Carrier proportional tracking coefficients.

bit-9-5: CS KP14:0] Carrier proportional transition coefficients.

bit-4-0: CS KP04:0] Carrier proportional acquire coefficients.

11.2.20 Carrier Synchronisation Integral Coefficients registers 63 - 64 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
CS KINT H	63	Reserved	CS KI2[4:0]					CS KI1[4:3]		R/W	51
CS KINT L	64	CS KI1[2:0]			CS KI0[4:0]					R/W	3B

bit-15: Reserved

bit-14-10: CS KI2 [4:0] Carrier integer tracking coefficients.

bit-9-5: CS KI1 [4:0] Carrier integer transition coefficients.

bit-4-0: CS KI0[4:0] Carrier integer acquire coefficients.

11.2.21 QPSK Output Scale Factor register 65 (R/W)

QPSK SCALE (65) **Default value 39 dec. 27 hex.**

QPSK SCALE [7:0] QPSK output scale factor for IOUT and QOUT outputs.

11.2.22 Timing Lock Detect Threshold out of lock register 66 (R/W)

TLD OUTLK TH (66) **Default value 130 dec. 82 hex.**

TLD OUTLK TH [7:0]Timing Lock Detect threshold when not in lock.

11.2.23 Timing Lock Detect Threshold in lock register 67 (R/W)

TLD INLK TH (67) **Default value 10 dec. 0A hex.**

TLD INLK TH[7:0] Timing Lock Detect threshold when in lock.

11.2.24 Frequency Lock Detect Threshold register 68

FLD TH (68) **Default value 32 dec. 2 0 hex.**

FLD TH[7:0] Frequency lock detect threshold.

11.2.25 Phase Lock Detect Threshold out of lock registers 69 - 72 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
PLD OUTLK3	69	SW R N MX[1:0]				PLD OUTLK3[9:4]				R/W	AE
PLD OUTLK2	70	PLD OUTLK3[3:0]				PLD OUTLK2[9:6]				R/W	E6
PLD OUTLK1	71	PLD OUTLK2[5:0]						PLD O LK1[9:8]		R/W	40
PLD OUTLK0	72	PLD OUTLK1[7:0]								R/W	7E

bit-31-30: SW R N MX[1:0] CS Sweep rate number max.

bit-29-20: PLD OUTLK TH3[9:0]

bit-19-10: PLD OUTLK TH2[9:0]

bit-9-0: PLD OUTLK TH1[9:0]

11.2.26 Phase Lock Detect Threshold in lock registers 73 - 76 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
PLD INLK3	73	Reserved								R/W	01
PLD INLK2	74	PLD INLK3[3:0]				PLD INLK2[9:6]				R/W	A0
PLD INLK1	75	PLD INLK2[5:0]							PLD INLK1 [9:8]		68
PLD INLK0	76	PLD INLK1[7:0]								R/W	1A

bit-31-30: Reserved

bit-29-20: PLD INLK TH3[9:0]

bit-19-10: PLD INLK TH2[9:0]

bit-9-0: PLD INLK TH1[9:0]

11.2.27 Phase Lock Detect Accumulator Time register 77 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
PLD ACC TIME	77	CS PLD MPLEN[3:0]				LOSSLOCK INT SW[3:0]				R/W	48

bit-7-4: CS PLDMPLEN[3:0] Maximum value allowed is 8.

bit-3-0: LOSSLOCK INT SW[3:0]

11.2.28 Sweep PAR register 78 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
SWEEP PAR	78	SW LIM SC [1:0]		TS NR SWEEP[2:0]			CS NR SWEE{[2:0]			R/W	49

bit-7-6: SW LIM SC[1:0] Frequency sweep limit scale.

bit-5-3: TS NR SWEEP[2:0]

bit-2-0: CS NR SWEEP[2:0]

11.2.29 Start up Time register 79 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
STARTUP TIME	79	STARTUP INTERVAL[7:0]								R/W	30

STARTUP INTERVAL[7:0]

11.2.30 Loss Lock Threshold register 80 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
LOSSLOCK TH	80	LOSSLOCK TH SPUR[3:0]				LOSSLOCK TH SW[3:0]				R/W	21

bit-7-4: LOSSLOCK TH SPUR[3:0]

bit-3-0: LOSSLOCK TH SW[3:0]

11.2.31 FEC Lock Time register 81 (R/W)

FEC LOCK TM (81). Default value 32 dec. 20 hex.

FEC LOCK TM[7:0]

The number of symbol periods which the QPSK allows for the FEC to lock after achieving carrier and timing synchronisation is given by:

FEC LOCK TM * Search factor * 65536

The parameter Search Factor is 1 if there is no code rate search and is 8 if there is a code rate search, i.e. the QPSK allows more time for the FEC to lock in the presence of a code rate search.

If the FEC does not lock within the allotted number of symbol periods, then the QPSK resets the timing and carrier loops and resumes the search for a QPSK signal.

11.2.32 Loss Lock Time register 82 (R/W)

LOSSLOCK TM (82) Default value 16 dec. 10 hex.

LOSSLOCK TM[7:0]

After the FEC locks it can unlock due to a signal fade or a cycle slip. Then the QPSK allows the following number of symbol periods for the FEC to regain lock:

LOSSLOCK TM * 262144

If the FEC does not regain lock during this number of symbol periods, then QPSK will re-acquire lock.

11.2.33 Viterbi Error Period registers 83 - 85 (R/W)

VIT ERRPER (83, 84 & 85) Default value 16,777,215 dec.FF FF FF hex.

VIT ERRPER [23:0] Viterbi error period. This is the period over which the Viterbi error count is measured. See Section 8.2.4 “Viterbi error count at Viterbi input registers 11 - 13 (R)” on page 52.

11.2.34 Viterbi Set up register 86 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
VIT_SETUP	86	FR AL TM O[1:0]		SRCH CYC [1:0]		SEARCH START [2:0]			EX F LK	R/W	34

bit-7-6: FR AL TM O [1:0] Frame (or byte) align time out.

bit-5-4: SRCH CYC[2:0] Viterbi BER based search cycles.

bit-3-1: SEARCH START[2:0] Code rate search start, only one code rate may be selected.

bit-6-4	Code rate search start at:
0	1/2
1	2/3
2	3/4
3	5/6
4	6/7
5	7/8

Table 10 - Viterbi Code Rate Search Start

bit-0: EX F LK Exit false lock.

11.2.35 Viterbi Reference Byte 0 register 87 (R/W)

VIT REF0 (87) **Default value 128 dec. 80 hex.**

VIT REF0[7:0] Viterbi reference byte 0.

11.2.36 Viterbi Reference Byte 1 register 88 (R/W)

VIT REF1 (88) **Default value 20 dec. 14 hex.**

VIT REF1[7:0] Viterbi reference byte 1.

11.2.37 Viterbi Reference Byte 2 register 89 (R/W)

VIT REF2 (89) **Default value 10 dec. 0A hex.**

VIT REF2[7:0] Viterbi reference byte 2.

11.2.38 Viterbi Reference Byte 3 register 90 (R/W)

VIT REF3 (90) **Default value 6 dec. 06 hex.**

VIT REF3[7:0] Viterbi reference byte 3.

11.2.39 Viterbi Reference Byte 4 register 91 (R/W)

VIT REF4 (91) **Default value 4 dec. 04 hex.**

VIT REF4[7:0] Viterbi reference byte 4.

11.2.40 Viterbi Reference Byte 5 register 92 (R/W)

VIT REF5 (92) **Default value 2 dec. 02 hex.**

VIT REF5[7:0] Viterbi reference byte 5.

11.2.41 Viterbi Reference Byte 6 register 93 (R/W)

VIT REF6 (93) **Default value 1 dec. 01 hex.**

VIT REF6[7:0] Viterbi reference byte 6.

11.2.42 Viterbi Maximum Error register 94 (R/W)

VIT_MAXERR (94) **Default value 148 dec. 94 hex.**

VIT_MAXERR[7:0] Viterbi maximum error.

This register controls the frequency of the BER indication audio signal, output on the status pin when the FEC_STAT_EN register bit-0 is set high, see pages 13 and 50.

11.2.43 Byte Align Set up register 95 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
BA SETUP	95	BA FSM[1:0]		BA MV[1:0]		BA UNLK[3:0]				R/W	D4

bit-7-6: BA FSM[1:0] Byte Align FSM mode.

bit-5-4: MA MV[2:0] + 5 = Byte Align majority voting.

bit-3-0: BA UNLK[3:0] +3 = Number of bad sync words to unlock the Byte Align. The default register value of 4 is equivalent to 7 bad sync words.

11.2.44 Program Synchronising Byte register 98 (R/W)

PROG SYNC (98) **Default value 71 dec. 47 hex.**

PROG SYNC[7:0] If FEC_SETUP[2] is high, use the PROG SYNC value to synchronise MPEG data packets.

11.2.45 AFC Frequency Search Threshold register 99 (R/W)

AFC SEAR TH (99) **Default value 35 dec. 23 hex.**

AFC SEAR TH[7:0]

11.2.46 Accumulator Differential Threshold register 100 (R/W)

CSACC DIFF TH (100) **Default value 32 dec. 20 hex.**

CSACC DIFF TH[7:0]

11.2.47 QPSK Lock Control register 101 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK LK CT	101	CS L LK	TS L LK	ACC CK	NUM_PLD INT[4:0]					R/W	04

bit-7: CS L LK High = Use CS long lock.

bit-6: TS L LK High = Use TS long lock.

bit-5: ACC CK High = Disable Accumulator check option.

bit-4-0: NUM_PLD INT[4:0] Maximum value allowed is 29.

11.2.48 QPSK State Control register 102 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK ST CT	102	HLD ST	AFC RS	M S RS	NXT FR	FCE ST	FORCED ST[2:0]			R/W	00

bit-7: HLD ST — High = Hold state.

bit-6: AFC RS — High = AFC reset.

bit-5: M S RS — High = Mixer scan reset.

bit-4: NXT FR — High = Get next frequency.

bit-3: FCE ST — High = Force state.

bit-2-0: FORCED ST[2:0] — Forced state.

11.2.49 QPSK Reset register 104 (R/W)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
QPSK $\overline{\text{RESET}}$	104	Reserved		REL QP	PR_QP	PR CS	PR TS	PR FE	PR AGC	R/W	00

bit-7-6: Reserved Must be set low.

bit-5: REL QP — High = Release QPSK FSM.

bit-4: PR_QP — High = Partial reset FSM (applies to QPSK control).

bit-3: PR CS — High = Partial reset carrier synchroniser

bit-2: PR TS — High = Partial reset timing synchroniser (includes fine AGC).

bit-1: PR FE — High = Partial reset front-end logic.

bit-0: PR AGC — High = Partial reset analogue AGC.

11.2.50 QPSK Test Control register 105 (R/W)

QPSK_TST CT (105) **Default value 0 dec. 00 hex.**

QPSK TEST CTRL[7:0] For factory test purposes only.

11.2.51 QPSK Test State register 106 (R/W)

QPSK TEST ST (106) **Default value 0 dec. 00 hex.**

QPSK TEST ST[7:0] For factory test purposes only.

11.2.52 Test Mode register 125 (R/W)

TEST MODE (125) **Default value 0 dec. 00 hex.**

TEST MODE[7:0]: This register is for testing purposes only.

11.3 Read only Secondary Register Map

Writing to these registers will have no effect.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
TEST R	107	TEST R[7:0] Test Read, for test purposes only.								R	00

11.4 Secondary Registers for Test and De-Bugging Read Register

11.4.1 Test Read register 107 (R)

TEST R (107) **Default value 0 dec. 00 hex.**

TEST R[7:0] For test purposes only.

12.0 Microprocessor Control

12.1 Primary 2-wire Bus Address

The 2-wire bus Address is determined by applying VDD or VSS to the ADDR[7:1] pins. See Primary 2-wire Bus Interface.

12.2 RADD: 2-wire Register Address (W)

RADD is the 2-wire register address. It is the first byte written after the MT312 2-wire chip address when in write mode.

To write to the chip, the microprocessor should send a START condition and the chip address with the write bit set, followed by the register address where subsequent data bytes are to be written. Finally, when the 'message' has been sent, a STOP condition is sent to free the bus.

To read from the chip from register address zero, the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of CLK1 clocks to read the bytes out. Finally a STOP condition is sent to free the bus. RADD is not sent in this case.

To read from the chip from an address other than zero, the microprocessor should send the chip address with the write bit set, followed by the register address where subsequent data bytes are to be read. Then the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of CLK1 clocks to read the bytes out. Finally a STOP condition is sent to free the bus. A STOP condition resets the RADD value to 00. For examples of use, see “Examples of 2-wire Bus Messages” on page 78.

RADD (virtual register, address none)

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
RADD	N/A	IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W	-

bit-7: IAI High = Inhibit auto increment.

Low = Increment addresses.

bit-6-0: AD[6:0] 2-wire register address, numbers in the range 0 to 127 are allowed.

When the register address is incremented to 127 it stops and the bus will continue to write to or read from register 127 until a STOP condition is sent.

12.3 Primary 2-wire Bus Interface

The primary 2-wire bus serial interface uses pins:

DATA1 (pin 54) Serial data, the most significant bit is sent first.

CLK1 (pin 53) Serial clock.

The 2-wire bus Address is determined by applying VDD or VSS to the ADDR[7:1] pins.

For compatibility with earlier devices, the 2-wire bus address should be 0001 110 R/$\overline{W}$ and the pins connected as follows:

ADDR[7]	ADDR[6]	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]
VSS	VSS	VSS	VDD	VDD	VDD	VSS

When the MT312 is powered up, the $\overline{\text{RESET}}$ pin 49 should be maintained low for typically 250ms (minimum 100ms) after VDD has reached normal operation levels. This is to ensure that the crystal oscillator and internal PLL have become fully established and that the internal reset signal is fully clocked into all parts of the circuit. As the reset pin is pulled high, the logic levels on ADDR[7:1] are latched to become the 2-wire bus address AD[6:0].

IIN[5:1] are only used for test purposes and should be wired to VSS.

The circuit works as a slave transmitter with the eighth bit set high or as a slave receiver with the eighth bit set low. In receive mode, the first data byte is written to the RADD virtual register, which forms the register sub-address.

Bit 7 of the RADD register, IAI is an Inhibit Auto Increment function. When the IAI bit is set high, the automatic incrementing of register addresses is inhibited. IAI set low is the normal situation so that data bytes sent on the 2-wire bus after the RADD register data are loaded into successive registers. This automatic incrementing feature avoids the need to individually address each register.

Following a valid chip address, the 2-wire bus STOP command resets the RADD register to 00. If the chip address is not recognised, the MT312 will ignore all activity until a valid chip address is received. The 2-wire bus START command does NOT reset the RADD register to 00. This allows a combined 2-wire bus message to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. Finally a STOP command should be sent to free the bus.

When the 2-wire bus is addressed (after a recognised STOP command) with the read bit set, the first byte read out will be the content of register 00.

12.4 Secondary 2-wire bus for tuner control

The MT312 has a General Purpose Port that can be configured to provide a secondary 2-wire bus with full bi-directional operation. When pass-through is enabled, a transparent connection is made to the tuner. This innovative design simplifies the software required to program the tuner to only five data bytes.

Pass-through mode is selected by setting register (20) GPP_CTRL[bit-6] = 1.

The allocation of the pins is: GPP[0] pin 44 = CLK2, GPP[1] pin 45 = DATA2.

12.5 Examples of 2-wire Bus Messages

KEY:	S	Start condition	W	Write (= 0)
	P	Stop condition	R	Read (= 1)
	A	Acknowledge	NA	NOT Acknowledge
	RADD	Register Address	***ITALICS***	***MT312 output***

Write operation - as a slave receiver:

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	DATA (reg n)	***A***	DATA (reg n+1)	***A***	P

Read operation - MT312 as a slave transmitter:

S	DEVICE ADDRESS	R	***A***	***DATA (reg 0)***	A	***DATA (reg 1)***	A	***DATA (reg 2)***	NA	P

Write/read operation with repeated start - MT312 as a slave transmitter:

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	S	DEVICE ADDRESS	R	***A***	***DATA (reg n)***	A	***DATA reg n+1)***	NA	P

Write/read/write operation with repeated start and auto increment off with IAI set high - MT312 as a slave transmitter. This example uses the GPP_CTRL register where the register address is 20 + 128 (IAI). Data are first read from the GPP_CTRL register, then following a restart, data are written to the GPP_CTRL register.

S	DEVICE ADDRESS	W	***A***	RADD (148)	***A***	S	DEVICE ADDRESS	R	***A***	***DATA (reg 20)***	NA	S	DEVICE ADDRESS	W	***A***	DATA (reg 20)	***A***	P

To program the Tuner, use the following sequence of three messages:

Open secondary 2-wire port:

S	MT312 ADDRESS	W	***A***	GPP_CTRL (20)	***A***	DATA (64)	***A***	P

Program Tuner:

S	TUNER ADDRESS	W	***A***	DATA (BYTE 2)	***A***	DATA (BYTE 3)	***A***	DATA (BYTE 4)	***A***	DATA (BYTE 5)	***A***	P

Close secondary 2-wire port:

S	MT312 ADDRESS	W	***A***	GPP_CTRL (20)	***A***	DATA (0)	***A***	P

Always close the secondary 2-wire port after programming the Tuner, to avoid 2-wire bus clock interference in the Tuner.

12.6 Primary 2-wire Bus Timing

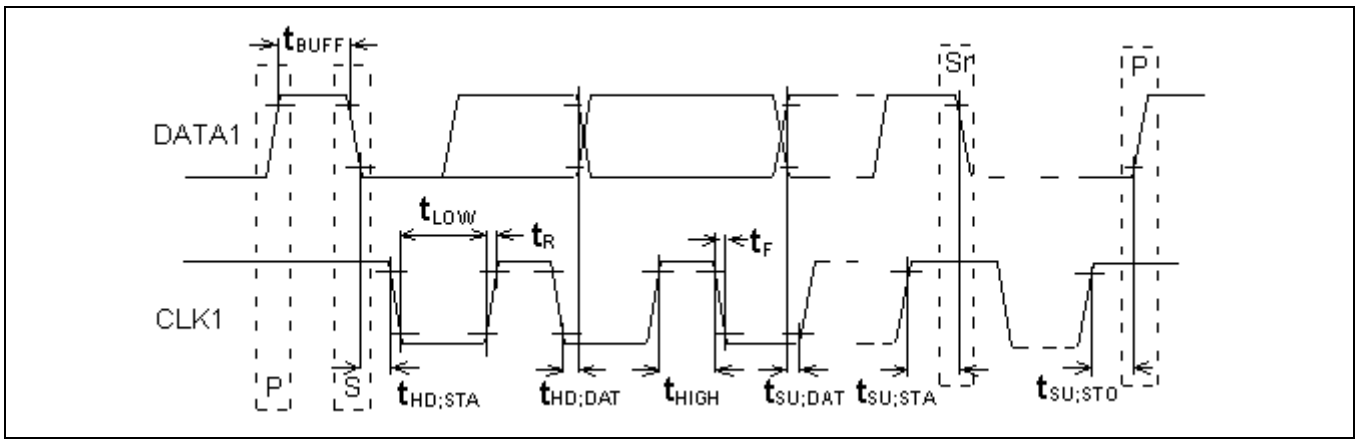

Figure 24 - Primary 2-wire Bus Timing

Where: S = Start
Sr = Restart, i.e. Start without stopping first.
P = Stop.

Parameter: Primary 2-wire bus only	Symbol	Value		Unit
		Min	Max	
CLK1 clock frequency	fCLK	0	450	kHz
Bus free time between a STOP and START condition.	tBUFF	200		ns
Hold time (repeated) START condition.	tHD;STA	200		ns
LOW period of CLK1 clock.	tLOW	450		ns
HIGH period of CLK1 clock.	tHIGH	600		ns
Set-up time for a repeated START condition.	tSU;STA	200		ns
Data hold time (when input).	tHD;DAT	100		ns
Data set-up time	tSU;DAT	100		ns
Rise time of both CLK1 and DATA1 signals.	tR		note 1	ns
Rise time of both CLK1 and DATA1 signals, (100pF to ground)	tF	20		ns
Set-up time for a STOP condition.	tSU;STO	200		ns

Table 11 - Primary 2-wire bus timing

Note 1: The rise time depends on the external bus pull-up resistor.

13.0 Electrical Characteristics

13.1 Recommended Operating Conditions

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Core power supply voltage	CVDD	1.62	1.8	1.98	V
Core power supply current	CIDD		130	150	mA
Power supply voltage	VDD	3.0	3.3	3.6	V
Power supply current	IDD		170	220	mA
Input clock frequency 1	$\overline{XTI}$	9.99		16.00	MHz
CLK1 clock frequency	FCLK1			450	kHz
Ambient operating temperature		0		70	°C

Note 1: When not using a crystal, $\overline{XTI}$ may be driven from an external source over the frequency range shown.

13.2 Absolute Maximum Ratings

Maximum Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power supply	VDD	-0.3	+3.6	V
Voltage on input pins (5 v rated)	VI	-0.3	5.5	V
Voltage on input pins (3.3v rated)	VI	-0.3	VDD+ 0.3	V
Voltage on input pins (1.8v rated)	VI	-0.3	CVDD + 0.3	V
Voltage on output pins (5v rated)	VO	-0.3	5.5	V
Voltage on output pins (3.3v rated)	VO	-0.3	VDD + 0.3	V
Voltage on output pins (1.8v rated)	VO	-0.3	CVDD + 0.3	V
Storage temperature	TSTG	-55	150	°C
Operating ambient temperature	TOP	0	70	°C
Junction temperature	TJ		125	°C

Note 1: Stresses exceeding these listed under 'Absolute Ratings' may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

13.3 Crystal Specification

Parallel resonant fundamental frequency (preferred)	9.99 to 16.00MHz.
Tolerance over operating temperature range	±25ppm.
Tolerance overall	±50ppm.
Nominal load capacitance	30pF.
Equivalent series resistance	<35Ω

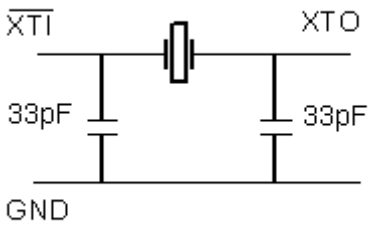

Figure 25 - Crystal Oscillator Circuit

Note: The crystal frequency should be chosen to ensure that the system clock would marginally exceed the maximum symbol rate required.

13.4 Electrical Characteristics

DC Electrical Characteristics

Parameter	Conditions/Pin	Symbol	Min.	Typ.	Max.	Unit
Core operating voltage		CVDD	1.62	1.8	1.98	V
Peripheral operating voltage		VDD	3.0	3.3	3.6	V
Average core power supply current		CIDD		130	150	mA
Average peripheral power supply current		IDD		170	220	mA
Average supply current Stand-by Mode				1	2	mA
Output levels VOH Tri-state push pull	1 mA drive current. IIN, QIN, TESTCLK, MDO, MOVAL, MOSTRT, MOCLK, BKERR, DISECQ, STATUS	VOH	0.80 VDD	0.92 VDD		V
Output levels VOL Tri-state push pull	1 mA drive current, Pins as VOH.			0.2	0.4	V

DC Electrical Characteristics (continued)

Parameter	Conditions/Pin	Symbol	Min.	Typ.	Max.	Unit
Output level open drain	4 mA drive current. 6 mA drive current. AGC, DATA1, $\overline{IRQ}$, GPP<2:0>				0.4 0.6	V V
Input levels VIH CMOS	3.3V input	VIH	0.7 VDD			V
Input levels VIH	CMOS 5.0V input	VIH	0.7 VDD			V
Input levels VIL CMOS		VIL			VIL 0.3VDD	V
Input leakage Current	VIN = 0 and VDD				10	µA

13.5 MT312 Pinout Description

Pin Description Table

Pin	Name	Description	I/O	Note	V	mA
4,5,6,7, 8,11,12	ADDR[7:1]	Primary 2-wire bus address defining pins	I/O	CMOS	3.3	1
14	MICLK	MPEG clock input used to generate MOCLK. Enabled when both register 96 bit 7 and register 97 bit 7 are set high. In this mode, MICLK must be continuous.	I	CMOS	5[1]	
16	TESTCLK	External ADC mode clock.	O	PECL	Tri-state	3.3
18	$\overline{XTI}$	Crystal clock input or external reference clock input.	I	CMOS	3.3	
19	XTO	Crystal output. An internal feedback resistor to $\overline{XTI}$ is included	O	CMOS	3.3	
23	PLL1	Phase Locked Loop test output	23			
26	VRT	ADC Voltage top reference level	26			
27	IREF	I channel de-coupling input	I			
28	ISINGP	I channel input	I			
29	NC	No connection	I			
32	VRM	ADC Voltage middle reference level				
33	QSINGP	Q channel input	I			
34	QREF	Q channel de-coupling input	I			
35	VRB	ADC Voltage bottom reference level				
38	RREF	Bias level				
39	TEST1	For factory test only. This pin must be connected to VSS in normal operation	I	CMOS	3.3	
40	TEST2	For factory test only. This pin must be connected to VSS in normal operation	I	CMOS	3.3	

Pin Description Table (continued)

Pin	Name	Description	I/O	Note	V	mA
43	AGC	AGC sigma-delta output	O	Open drain	5[1]	6
46,45,44	GPP[2:0] (DISEQC2)	General Purpose Port for tuner control, register defined. GPP0 = secondary CLK2, GPP1 = secondary DATA2, GPP2 = DiSEqC™ v2.2 input signal.	I/O	Open drain	5[1]	6
47	DISEQC1	DiSEqC^{TM} Horizontal/Vertical control	O	CMOS	3.3	1
48	DISEQC0	DiSEqCTM 22kHz output	O	CMOS	3.3	1
49	$\overline{\text{RESET}}$	Active low reset input	I	CMOS	5	1
52	STATUS	Audio BER or Status output, register defined	O	CMOS	3.3	1
53	CLK1	2-wire serial bus clock	I	CMOS		
54	DATA1	2-wire serial bus data	I/O	Open drain	5[1]	6
57	$\overline{\text{IRQ}}$	Active low interrupt output. A low output on this pin indicates an event has occurred and the microprocessor should read the interrupt registers. Reading all interrupt registers resets this pin.	O	Open drain	5[1]	6
58	MOCLK	MPEG clock output at the data byte rate.	O	CMOS Tri-state	3.3	1
69,68,66,65, 64,63,61,59	MDO[7:0]	MPEG transport packet data output bus.	O	CMOS Tri-state	3.3	1
71	$\overline{\text{MDOEN}}$	Logic 1 = MPEG data and clock outputs disable - Tri-state. Logic 0 = MPEG data and clock outputs enable	I	CMOS	5[1]	
72	MOVAL	MPEG data output valid. This pin is high during the MOCLK clock cycles when valid data bytes are being output.	O	CMOS Tri-state	3.3	1
75	$\overline{\text{BKERR}}$	Active low uncorrectable block indicator OR no signal indicator selected by ERR_IND bit 7 of MON_CTRL register.	O	CMOS Tri-state	3.3	1
76	MOSTRT	MPEG output start signal, high on the first byte of a packet.	O	CMOS Tri-state	3.3	1
2,9,17,42,50, 55,62,67	CVDD	Core Digital CVDD. All pins must be connected.			1.8	
13,73	VDD	Peripheral VDD. All pins must be connected.			3.3	
37	ADCAVDD	ADC core analogue VDD. All pins must be connected.			1.8	
30	ADCDVDD	ADC core digital VDD. All pins must be connected.			3.3	
25	ADCFVDD	ADC core front end VDD. All pins must be connected.			3.3	
21	PLLVDD	PLL VDD. All pins must be connected.			1.8	

Pin Description Table (continued)

Pin	Name	Description	I/O	Note	V	mA
1,10,20, 41, 51, 60,70	CVSS	Digital VSS. All pins must be connected.				
15,56,74	VSS	Peripheral VSS. All pins must be connected.			0	
36	ADCAGND	ADC core analogue VSS. Must be connected to analogue GND.			0	
31	ADCDGND	ADC core digital VSS. Must be connected to analogue GND.			0	
53	CLK1	2-wire serial bus clock	I	CMOS	5[1]	
24	ADCFGND	ADC core front end VSS. Must be connected to analogue GND.			0	
22	PLLGND	PLL VSS. Must be connected to analogue GND.			0	
77,78,79, 80,3	IIN[5:1]	Test bus, all inputs must be connected to VSS.	I/O	CMOS	3.3	1

Note 1: 5V tolerant pins with thresholds related to 3.3V.

13.6 Alphabetical Listing of Pin-Out

Alphabetical Listing of Pin-Out

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
ADCAGND	36	CVDD	17	IIN[4]	78	PLLVDD	21
ADCAVDD	37	CVDD	42	IIN[5]	77	QREF	34
ADCDVDD	30	CVDD	50	IREF	27	QSINGP	33
ADCDGND	31	CVDD	62	$\overline{\text{IRQ}}$	57	$\overline{\text{RESET}}$	49
ADCFGND	24	CVDD	67	ISINGP	28	RREF	38
ADCFVDD	25	CVSS	1	MDO[0]	59	STATUS	52
ADDR[1]	12	CVSS	10	MDO[1]	61	TEST1	39
ADDR[2]	11	CVSS	20	MDO[2]	63	TEST2	40
ADDR[3]	8	CVSS	41	MDO[3]	64	TESTCLK	16
ADDR[4]	7	CVSS	51	MDO[4]	65	VRB	35
ADDR[5]	6	CVSS	60	MDO[5]	66	VRM	32
ADDR[6]	5	CVSS	70	MDO[6]	68	VRT	26
ADDR[7]	4	DATA1	54	MDO[7]	69	VDD	13
AGC	43	DATA2 /GPP1	45	$\overline{\text{MDOEN}}$	71	CVDD	55
$\overline{\text{BKERR}}$	75	DISEQC0 22kHz	48	MICLK	14	VDD	73
CLK1	53	DISEQC1	HV	47	MOCLK	58	VSS
CLK2/GPP0	44	DISEQC2 /GPP2	46	MOSTRT	76	VSS	56
NC	29	IIN[1]	3	MOVAL	72	VSS	74
CVDD	2	IIN[2]	80	PLL1	23	$\overline{\text{XTI}}$	18
CVDD	9	IIN[3]	79	PLLGND	22	XTO	19

14.0 MT312 Register Map

RADD is a virtual register with no address containing the address of the register to be accessed. It is written immediately after the 2-wire write address.

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex
RADD	N/A	IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W	-

14.1 Read/Write Register Map

Read/Write Register Map

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex	Page
GPP_CTRL	20	Reserved	2W_PAS	GPP_DIR[2:0]			GPP_PIN[2:0]			R/W	20	29
RESET	21	FR_312	PR_312	FR_QP	PR_QP	FR_VIT	PR_VIT	PR_BA	PR_DS	R/W	00	24
DISEQC_MODE	22	Reserved	HV	DISEQC INSTRuction length			22kHz mode			R/W	00	33
SYM_RATE_H	23	SEARCH	SR_FMT	SYM_RATE[13:8] in MS/s (high byte)						R/W	1B	39
SYM_RATE_L	24	SYM_RATE[7:0] in MS/s (low byte)								R/W	80	39
VIT_MODE	25	AUT_IQ	V_IQ_SP	CR_7/8	CR_6/7	CR_5/6	CR_3/4	CR_2/3	CR_1/2	R/W	44	41
QPSK_CTRL	26	Reserved	Q_IQ_SP	Reserved	Reserved	Reserved	AFC_M	Reserved	ROLL_20	R/W	00	42
GO	27	Reserved							GO	R/W	00	42
IE_QPSK_H	28	IE_QPSK[23:16] Interrupt enable QPSK (high byte)								R/W	00	43
IE_QPSK_M	29	IE_QPSK[15:8] Interrupt enable QPSK (middle byte)								R/W	00	43
IE_QPSK_L	30	IE_QPSK[7:0] Interrupt enable QPSK (low byte)								R/W	00	43
IE_FEC	31	IE_FEC[7:0] Interrupt enable FEC								R/W	00	49
QPSK_STAT_EN	32	QPSK_STAT_EN[7:0] Enable various QPSK outputs on STATUS pin								R/W	00	44
FEC_STAT_EN	33	MOCLK_RATIO[3:0]				DS_Lock	BA_lock	VIT_lock	BER_tog	R/W	14	50
SYS_CLK	34	SYS_CLK[7:0] - System clock frequency x2 in MHz								R/W	00	25
DISEQC_RATIO	35	DISEQC_RATIO[7:0]								R/W	00	34
DISEQC_INSTR	36	DISEQC_INSTRuction[7:0]								R/W	00	34
FR_LIM	37	Reserved	FR_LIM[6:0] - Freq. Limit in MHz							R/W	00	30
FR_OFF	38	FR_OFF[7:0] - Freq. Offset in MHz								R/W	00	30
AGC_CTRL	39	Reserved	Reserved	AGC_SD[1:0]		AGC_BW[2:0]			AGC_SL	R/W	26	54
AGC_REF	41	AGC_REF[7:0] AGC reference level								R/W	67	54
OP_CTRL	96	MANUAL MOCLK	BKERIV	MCLKINV	EN_TEI	BSO	BA_LK[2:0]			R/W	03	62
FEC_SETUP	97	DIS_SR	ENCL_KO	DIS_DS	DIS_RS	DIS_VIT	EN_PRS	DS_LK[1:0]		R/W	00	50
MON_CTRL	103	ERR_IND	Reserved			MON_CTRL[3:0] Monitor control				R/W	00	63
DISEQC2_CTRL1	121	DISEQC2_CTRL1 [7:8]								R/W	00	35
DISEQC2_CTRL2	122	MIN_PULS_PER			TONE_EXT_PER			MAX_TONE_PER		R/W	D4	35
CONFIG	127	312_EN	DSS_B	DSS_A	BPSK	PLL_FACTOR[1:0]		CRYS15	ADC EXT	R/W	08	21

14.2 Read Only Register Map

NAME	ADR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0		Def hex	Page
QPSK_INT_H	00	QPSK_INT[23:16] Interrupt QPSK (high byte)								R	00	45
QPSK_INT_M	01	QPSK_INT[15:8] Interrupt QPSK (middle byte)								R	00	45
QPSK_INT_L	02	QPSK_INT[7:0] Interrupt QPSK (low byte)								R	00	45
FEC_INT	03	FEC_INT[7:0] Interrupt FEC								R	00	51
QPSK_STAT_H	04	QPSK_STATUS[15:8] (high byte)								R	00	47
QPSK STAT L	05	QPSK_STATUS[7:0] (low byte)								R	00	47
FEC_STATUS	06	FEC_STATUS[7:0]								R	00	50
LNB_FREQ H	07	LNB_FREQ[15:8] Measured LNB frequency error (high byte)								R	00	31
LNB_FREQ L	08	Reserved	LNB_FREQ[7:0] Measured LNB frequency error (low byte)							R	00	31
M_SNR_H	09	M_SNR[14:8] Measured SNR (high byte)								R	00	52
M_SNR_L	10	M_SNR[7:0] Measured SNR (low byte)								R	00	52
VIT_ERRCNT_H	11	VIT_ERRCNT[23:16] - Viterbi error count (high byte)								R	00	52
VIT_ERRCNT_M	12	VIT_ERRCNT[15:8] - Viterbi error count (middle byte)								R	00	52
VIT_ERRCNT_L	13	VIT_ERRCNT[7:0] - Viterbi error count (low byte)								R	00	52
RS_BERCNT_H	14	RS_BERCNT[23:16] - Reed-Solomon bit errors corrected (high byte)								R	00	53
RS_BERCNT_M	15	RS_BERCNT[15:8] - Reed-Solomon bit errors corrected (middle byte)								R	00	53
RS_BERCNT_L	16	RS_BERCNT[7:0] - Reed-Solomon bit errors corrected (low byte)								R	00	53
RS_UBC_H	17	RS_UBC[15:8] - Reed-Solomon uncorrected block errors (high byte)								R	00	53
RS_UBC_L	18	RS_UBC[7:0] - Reed-Solomon uncorrected block errors (low byte)								R	00	53
SIG_LEVEL	19	SIG_LEVEL[7:0] - Signal level at MT312 input								R	00	55
AGC H	108	AGC[23:16] - Front end AGC (high byte)								R	00	55
AGC M	109	AGC[15:8] - Front end AGC (middle byte)								R	00	55
AGC L	110	AGC[7:0] - Front end AGC (low byte)								R	00	55
FREQ_ERR1 H	111	FREQ_ERR1[23:16] Input frequency error course (high byte)								R	00	31
FREQ_ERR1 M	112	FREQ_ERR1[15:8] Input frequency error course (middle byte)								R	00	31
FREQ_ERR1 L	113	FREQ_ERR1[7:0] Input frequency error course (low byte)								R	00	31
FREQ_ERR2 H	114	FREQ_ERR2[15:8] Input frequency error fine (high byte)								R	00	31
FREQ_ERR2 L	115	FREQ_ERR2[7:0] Input frequency error fine (low byte)								R	00	31
SYM_RAT_OP_H	116	SYM_RAT_OP[15:8] Symbol Rate Output (high byte)								R	00	48
SYM_RAT_OP_L	117	SYM_RAT_OP[7:0] Symbol Rate Output (low byte)								R	00	48
DISEQC2_INT	118	DISEQC2_INT[7:0]								R	00	37
DISEQC2_STAT	119	DISEQC2_STATUS[7:0]								R	00	38
DISEQC2_FIFO	120	DISEQC2_FIFO[7:0]								R	00	38
MONITOR_H	123	MONITOR[15:8] Monitor (high byte)								R	00	48
MONITOR_L	124	MONITOR[7:0] Monitor (low byte)								R	00	48
ID	126	ID[7:0] Chip identification.								R	03	25

15.0 References

1. European Digital Video Broadcast Standard, ETS 300 421 December 1994.
   ETS Secretariat
   06921 Sophia Antipolis Cedex
   France.
2. Digital Satellite Equipment Control (DiSEqC™)
   EUTELSAT
   European Telecommunications Satellite Organisation
   70, rue Balard - 75502 PARIS Cedex 15
   France.

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