

MT3256/S

N-Channel 60V/50A Power MOSFET

Features

- Max $R_{DS(on)} = 10m\Omega$ at $V_{GS} = 10V, I_D = 25A$
- Low gate charge (typical 43 nC)
- Low cr_{ss} (typical 85pF)
- 100% avalanche tested
- Improved dv/dt capability

General Description

These N-Channel enhancement mode power field effect transistors are produced using Mos-tech's proprietary, planar stripe, DMOS technology.

Applications

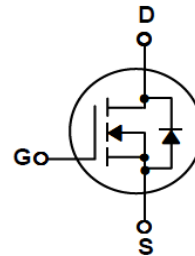
- DC-DC Buck Converters
- Notebook battery power management
- Load Switch in Notebook



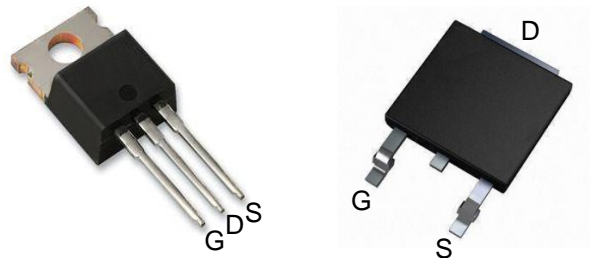
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



		Package Code MT3256: TO-220FB-3L MT3256S: TO-252-2L	
Date Code PYWWM		Lot NO XX	

MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	- Continuous (Silicon Limited) $T_C = 25^\circ C$	50	A
		- Continuous (Package Limited) $T_C = 25^\circ C$	28	
		- Continuous $T_C = 25^\circ C$ (Note 1a)	45	
		- Pulsed	180	A
E_{AS}	Single Pulsed Avalanche Energy (Note 3)		10	mJ
P_D	Power Dissipation	- $T_C = 25^\circ C$ (Note 1a)	TO-220=100/TO-252=50	W
		- $T_A = 25^\circ C$ (Note 1b)	0.9	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	1.64	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT3256/S	MT3256/S	TO-220/TO-252	-	-	50/2500

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	2.7	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$	--	10	--	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 25\text{ A}$ (Note 4)	--	20	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1380	1600	pF
C_{oss}	Output Capacitance		--	490	590	pF
C_{rss}	Reverse Transfer Capacitance		--	85	90	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 25\text{ A},$ $R_G = 25\text{ }\Omega$	--	18	45	ns
t_r	Turn-On Rise Time		--	135	270	ns
$t_{d(off)}$	Turn-Off Delay Time		--	60	130	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	65	140	ns
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 10\text{ V}$	--	31	41	nC
Q_{gs}	Gate-Source Charge		--	8	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	50	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	170	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 50 A	--	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 50 A, dI _F / dt = 100 A/μs (Note 4)	--	57	--	ns
Q _{rr}	Reverse Recovery Charge		--	79	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 230\text{ }\mu\text{H}, I_{AS} = 50\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 50\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

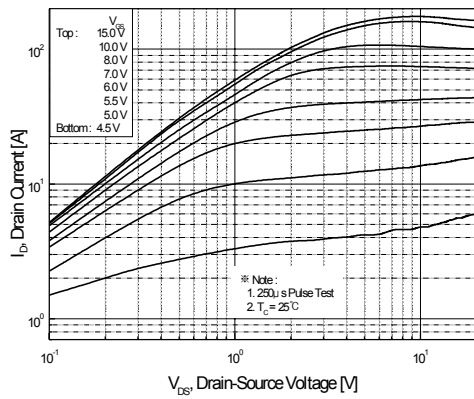


Figure 1. On-Region Characteristics

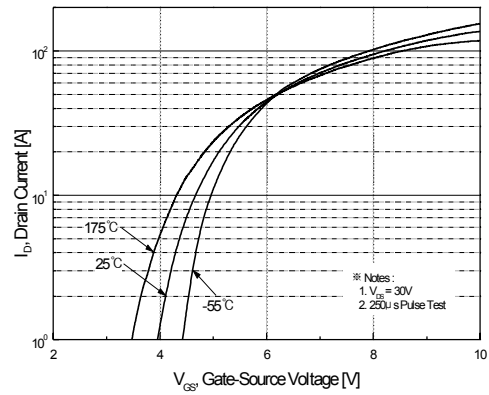


Figure 2. Transfer Characteristics

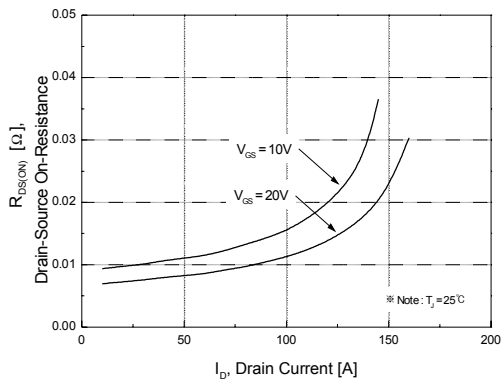


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

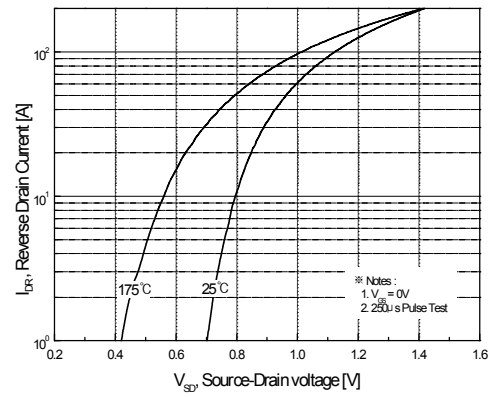


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

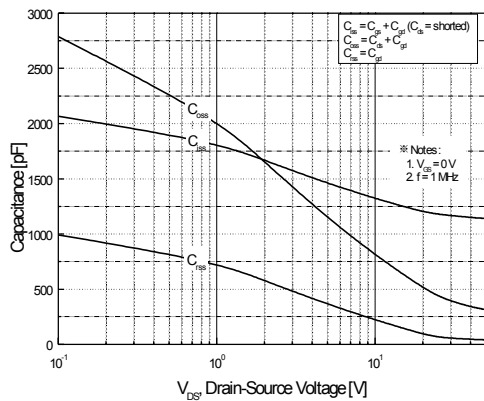


Figure 5. Capacitance Characteristics

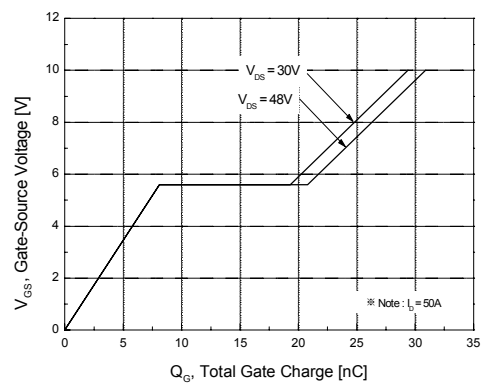


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

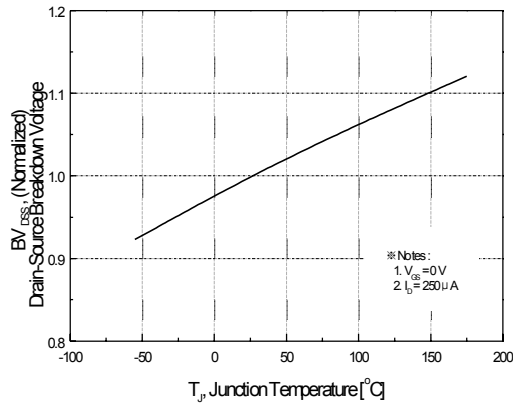


Figure 7. Breakdown Voltage Variation vs. Temperature

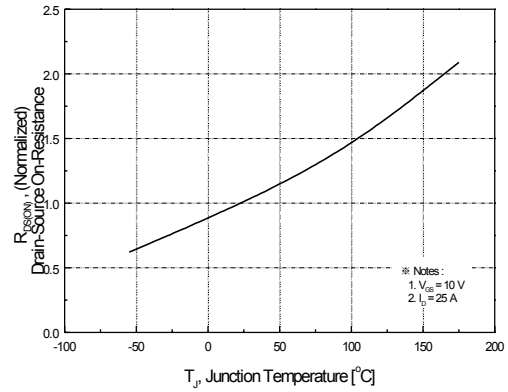


Figure 8. On-Resistance Variation vs. Temperature

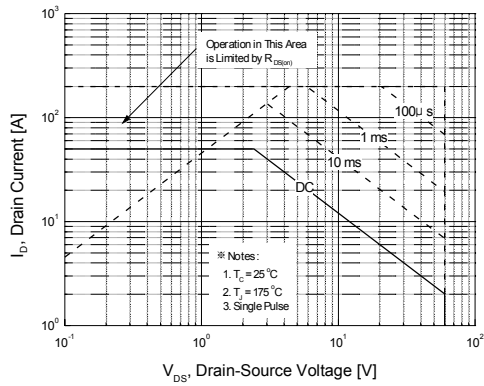


Figure 9. Maximum Safe Operating Area

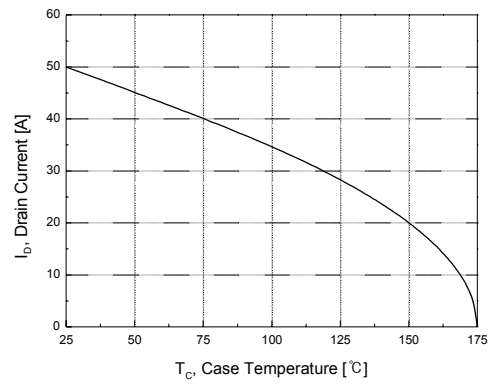


Figure 10. Maximum Drain Current vs. Case Temperature

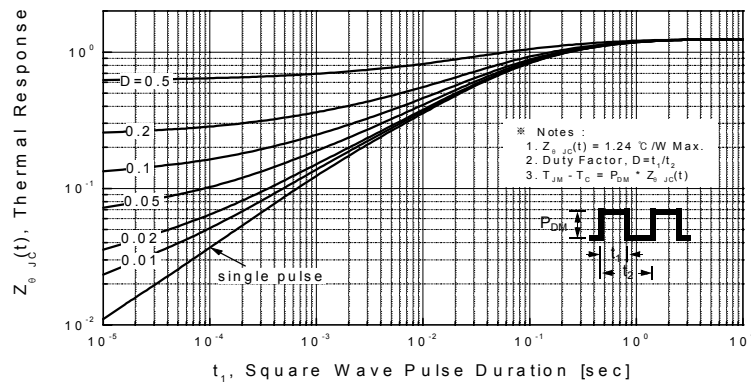
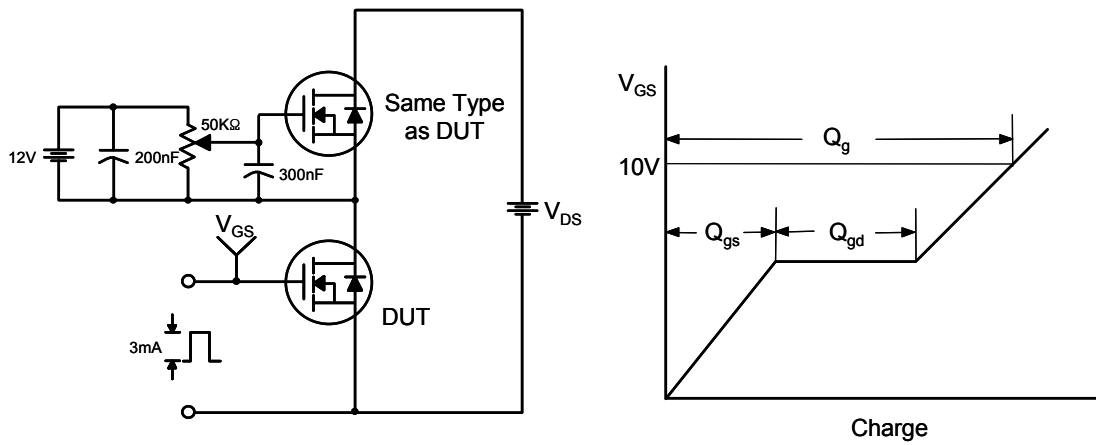
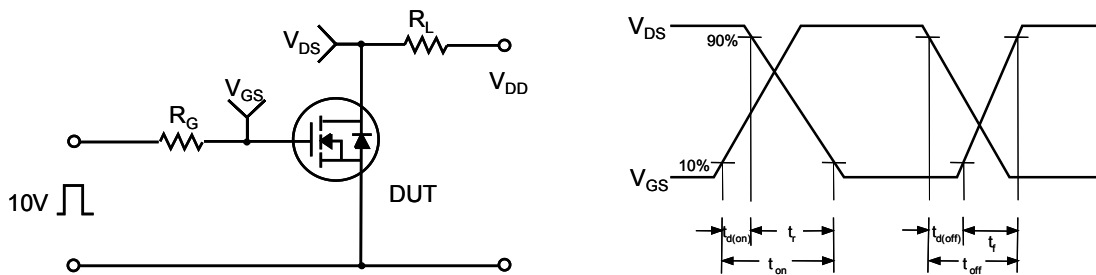


Figure 11. Transient Thermal Response Curve

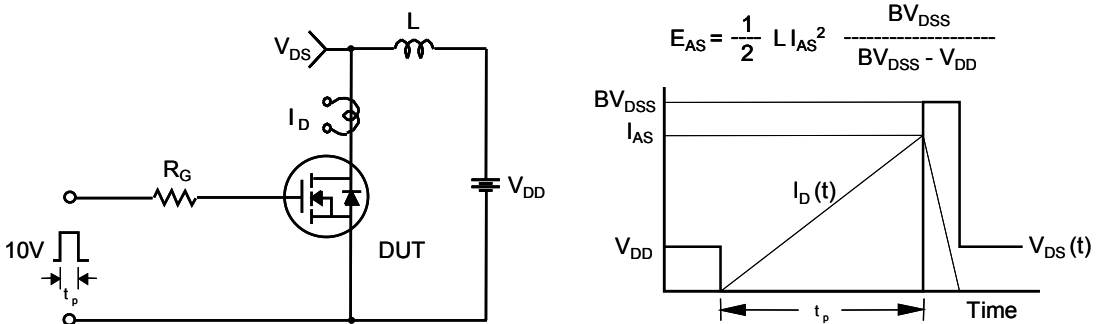
Gate Charge Test Circuit & Waveform



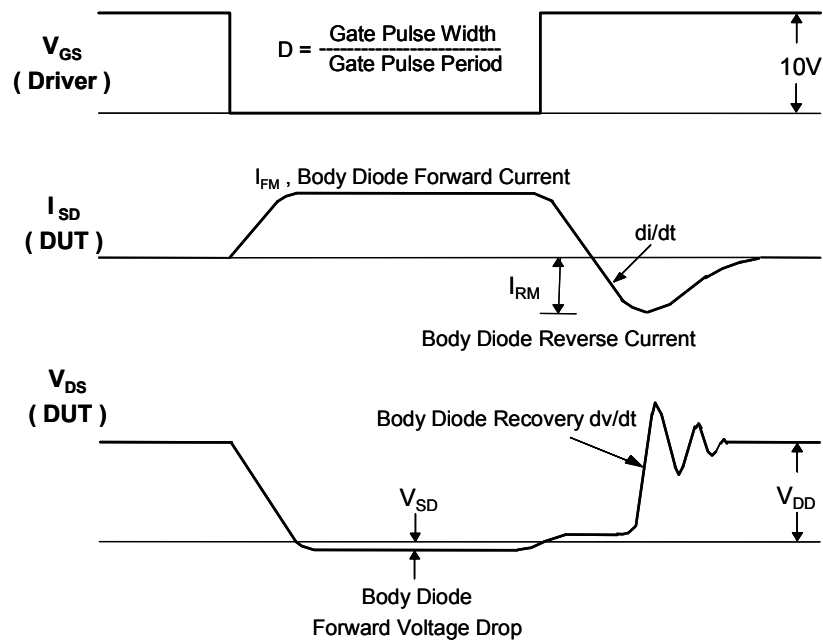
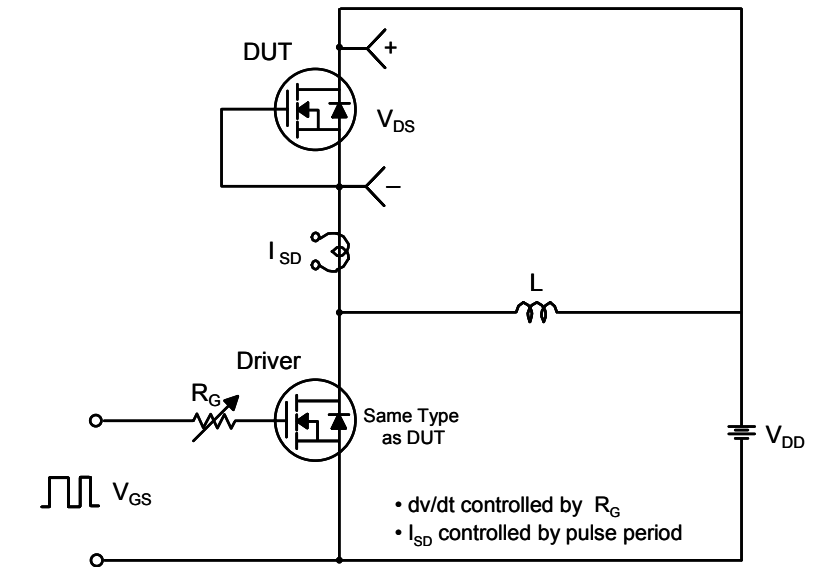
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

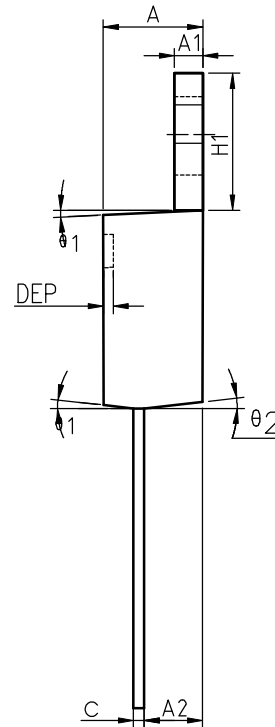
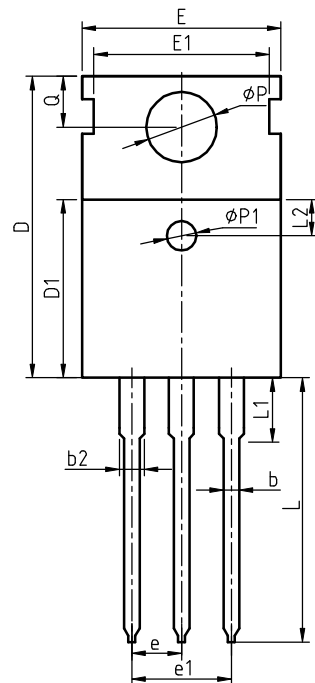


Peak Diode Recovery dv/dt Test Circuit & Waveforms



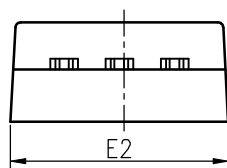
Package Information

TO-220FB-3L



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e	-	2.54	BSC	-	0.100	BSC
e1	-	5.08	BSC	-	0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2	-	2.50	REF	-	0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ_1	5°	7°	9°	5°	7°	9°
θ_2	1°	3°	5°	1°	3°	5°
θ_3	1°	3°	5°	1°	3°	5°



Technical drawing of a 2-pin connector with dimensions in millimeters. The drawing includes a front view, a side view, and a detail view of the pin.

Front View Dimensions:

- Overall width: 6.60 ± 0.20
- Pin width: 2.30 ± 0.20 (2.30TYP)
- Pin height: 0.76 ± 0.10
- Pin spacing: 5.34 ± 0.30
- Pin diameter: 0.70 ± 0.20
- Pin length: 0.60 ± 0.20
- Pin thickness: 0.80 ± 0.20
- Pin width (bottom): 0.89 ± 0.10
- Pin width (top): 0.91 ± 0.10
- Pin width (middle): 0.50 ± 0.10
- Pin width (bottom): 1.02 ± 0.20
- Pin width (top): 2.30 ± 0.20

Side View Dimensions:

- Overall height: 9.50 ± 0.30
- Pin height: 6.10 ± 0.20
- Pin width: 2.70 ± 0.20
- Pin length: 0.70 ± 0.20
- Pin width (bottom): 0.76 ± 0.10
- Pin width (top): 0.89 ± 0.10
- Pin width (middle): 0.91 ± 0.10
- Pin width (bottom): 0.50 ± 0.10
- Pin width (top): 1.02 ± 0.20
- Pin width (bottom): 2.30 ± 0.20

Detail View Dimensions:

- Overall width: 6.60 ± 0.20
- Pin width: 2.30 ± 0.20
- Pin height: 0.76 ± 0.10
- Pin spacing: 5.34 ± 0.30
- Pin diameter: 0.70 ± 0.20
- Pin length: 0.60 ± 0.20
- Pin thickness: 0.80 ± 0.20
- Pin width (bottom): 0.89 ± 0.10
- Pin width (top): 0.91 ± 0.10
- Pin width (middle): 0.50 ± 0.10
- Pin width (bottom): 1.02 ± 0.20
- Pin width (top): 2.30 ± 0.20

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1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.