MEDIATEK

MT3329

GPS all in one solution

Version 0.5

Specifications are subject to change without notice

Data Sheet

MT3329 Data Sheet

Revision History

Revision	Date	Comments
0.1	2007/08/06	First release
0.2	2007/08/23	Add package part, USB description and RF block diagram
0.3	2007/11/05	Added RF part description
0.4	2007/12/26	Update RTC figure and IC logo
0.5	2008/02/01	Update pad type to 5V-tolerance

Table of Contents

1. General Description

MT3329, a high performance single chip GPS navigation solution, which includes on chip CMOS RF, digital baseband, and an optional embedded flash. It achieves the industry's highest levels of sensitivity, accuracy, and Time-to-First-Fix (TTFF) with lowest power consumption in a small-footprint lead-free package. Its small footprint and minimal accessary provide significant reductions in the design, manufacturing and testing resource required to navigation device and handsets.

With an on-chip integrated LNA, MT3329 delivers a total receiver noise figure of 4 dB (before ADC). With its on-chip image-rejection mixer, the spec of external SAW filter is alleviated. With an on chip automatic center frequency calibration band pass filter, external filter is not required. The integrated PLL with Voltage Controlled Oscillator (VCO) provides excellent phase noise performance and fast locking time.

MT3329 supports up to 210 PRN channels. With 66 search channels and 22 simutaneous tracking channels, MT3329 acquires and tracks satellites in the shortest time even at indoor signal levels. MT3329 supports various location and navigation applications, including autonomous GPS, SBAS (WAAS, EGNOS, GAGAN, MSAS), DGPS (RTCM), and AGPS.

MT3329 contains ARM7EJ-S CPU providing powerful calculating capability, while extremely low MIPs is required to calculate the navigation information. A battery backed-up memory and a real time clock is also provided to accelerate acquistion at system restart up. On chip power management design makes MT3329 easily integrated into your system without extra voltage regulator. With both linear and an high effcient switching type regulator embedded, MT3329 give user plenty of choices for their application circuit.

Through MT3329's excellent low power consumption characteristic(acquisition 50mW, tracking 38mW), power sensitive devices, especially embedded systems, need not worry about operating time anymore and user can get more fun. Besides, MT3329 has an USB device port and is compliant with Universal Serial Bus(USB) 2.0 Full-speed specification. With this feature, GPS devices, such as Logger, Gmouse, PDA, Notebook..., need not additional chipset to convert signal and save BOM cost.

2. Features

Specification
- 22 tracking/ 66 acquisition-channel GPS Receiver
- WAAS/EGNOS/MSAS/GAGAN supported
- Support up to 210 PRN channels
- RTCM ready
- Jammer detection and reduction
- Indoor and outdoor multi-path detection and compensation
- FCC E911 compliance and A-GPS supported
- Low MIPS navigation software on ARM7 CPU
- Maximum fix update rate up to 10Hz

RF Configuration
- 4-bit IF signal.
- SoC, integrated in single chip with CMOS process.

ARM7EJ-S CPU
- Up to 56MHz processor clock
- Dynamic Clock rate control
- Support ARM/thumb (32/16-bit) instruction set
- Instruction cache embedded

Reference Oscillator
- TCXO
- Frequency : 12.6MHz to 40.0MHz
- Frequency Max Error : +/- 2.5 ppm

Built-in PLL series
- Built-in small jitter clock synthesizer to provide better acquisition and tracking quality.

1 pulse-per-second (1PPS) GPS time reference
- Duty cycle adjustable
- Accuracy < 100ns

Power down mode
- Intelligent power management

Power Scheme
- A 2.0V SMPS build-in SOC
- Self build 1.2V RTC, 1.2V core power and 1.5V LDO
- Bypass mode for external 1.2V and 1.5V suppliers

Build-in reset controller
- Needless of external reset control IC

Internal Real Time Clock (RTC)
- 8K byte battery backed-up memory
- 32.768KHz +/- 20ppm crystal
- Timer pin for external device on/off control
- 1.2V RTC clock output

Serial interface
- Three UARTs
- SPI
- I2C
- GPIO interface (up to 19 pins)

USB interface
- Logo certified USB 2.0 full-speed compatible

Internal memory - 4M-bit Flash

NMEA
- NMEA 0183 standard V3.01 and backward compliance
- Support 219 different Datum

Outline
- 81-pin TFBGA lead-free package 6.2mmx6.2mm.
- No external TTL component

3. Pin Assignment and Description / Functional Diagram

3.1. Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9
A	RF_IN	VCC_LNA	GND	LNA_OUT	MIX_IN	VCC_IF	VCC_ADC	GIO12	GIO13
B	GND	GND	GND	GND	GND	GND	TEST1	HRST#	INT0#
C	NC	OSC2	VCC_SX	VCC_BAT	VS_LNA	VS_AA	VDD_GND	JDI	STANDBY
D	NC	OSC1	VCCREG	GND	VCCF	DVIO28	VDD_GND	JRCK	JRST#
E	VS_15	VS_TCXO	GND	GND	GND	VDD_GND	JCK	SIN0	SO0
F	ACDUP	ATEST	LDO1.2V_INPUT	GND	DVDD12	VDD_GND	JDO	SCS0#	SCK0
G	LDO2.8V_INPUT	LDO2.8V_OUT	LDO1.2V_OUT	GND	RGND	TIMER	JMS	RX0	TX0
H	SMPS-GND	SMPS-S	32K_OUT	RTCCLK_O	RTCCLK	VDDU	RX2	RX1	TX1
J	SMPS-F	SMPS-VDD	RTC_VDD	R1V2	D_PLUS	D_MINUS	TX2	SCS1#	SCK1

3.2. Pin Identification (81 Pin)

Pin Name	BGA	Pin Name	BGA	Pin Name	BGA	Pin Name	BGA
JCK /GIO0 / DSP_I2CC /SP_CK	E7	RX2 /GIO8 /GPSIF[1] / SIN1/SYNC /SP_DAT	H7	VDD_GND	C7	VCCREG	D3
JDI /GIO1 /DSP_I2CD / SP_DAT	C8	TX2 /GIO7 /GPSIF[0] / SO1 /DUTY /SP_CK	J7	VDD_GND	D7	GND	B3
JMS /GIO2 /ECLK/S4W_CS/ RF_ASHORT	G7	SCK1 /ANA_DBG[0] / MA[20]/CLK MON	J9	VDD_GND	E6	GND	E4
JRST# /GIO3 /RF_AOK	D9	SCK0 /GO14 I2C_MST_CK	F9	VDD_GND	F6	OSC1	D2
JDO /GO18 /RF_LOCK_DET	F7	SIN0 /GIO6 /I2C_SLV_CK	E8	VS_LNA	C5		
JRCK /GO20 /RF_CLKO	D8	SO0 /GIO5 /I2C_DAT	E9	VS_TCXO	E2	GND	E5
GIO13 /GPSIF[3]/ I2C_DAT /SP_CK	A9	SCS0# /GIO4	F8	RF IN	A1	GND	A5
GIO12 /GPSIF[2]/ I2C_CK /SP_DAT	A8	SCS1#/ GO15 / ANA_DBG[1] /MA[21]	J8	GND	B1	GND	G4
R1V2	J4	D_minus	J6	GND	B4	GND	F4
RGND	G5	D_plus	J5	GND	A3	GND	E3
RTCCLK	H5	VDDU	H6	GND	B2		
RTCCLK_O	H4	ACDUP	F1	VS_AA	C6	SMPS_GND	H1
32K_OUT	H3	ATEST	F2	VS_15	E1	SMPS_S	H2
TIMER	G6	VCC_LNA	A2	VCC_SX	C3	SMPS_F	J1
HRST#	B8	VCC_ADC	A7	GND	D4	SMPS_VDD	J2
STANDBY /GIO11	C9	GND	B6	VCC_BAT	C4	VCC_IF	A6
INT0# /GIO10	B9	DVDD12	F5	VCCF	D5	GND	B5
RX0	G8	LDO2.8V_Out	G2	DVIO28	D6	LNA_OUT	A4
TX0	G9	LDO2.8V_input	G1	VS_SDM	D1	VS_VCO	C1
RX1 /GIO9 /BT_Reset/ ECLK /Ext_SYNC	H8	LDO1.2V_Out	G3	LDO1.2V_input	F3	RTC_VDD	J3
TX1 /GO16 /TMARK	H9						

3.3. Pin Description

Pin Numbers	Symbol	Type	Description
GIO Interface			
	GIO13/ GPSIF[3]/ I2C_DAT/ SP_CK	2.8V LVTTL I/O Output, 75K pull up, PSR, SMT 2mA, 4mA, 6mA, 8mA, PDR	Default : 8mA driving, 75K pull down, slow slew rate.
	GIO12/ GPSIF[2]/ I2C_CK/ SP_DAT	2.8V LVTTL I/O Output, 75K pull up, PSR, SMT 2mA, 4mA, 6mA, 8mA	
RTC Interface (5 pins)			
J4	R1V2	Analog power	RTC Circuit Power
G5	RGND	Analog power	RTC Circuit Ground
H5	RTCCLK	Analog input	RTC 32k Hz clock input
H4	RTCCLK_O	Analog output	RTC 32k Hz clock output
H3	32K_OUT	1.2V LVTTL output, no slew rate 2mA, 4mA, 6mA, 8mA PDR	RTC 32k Hz clock output
G6	TIMER	1.2V LVTTL output, no slew rate 2mA, 4mA, 6mA, 8mA PDR	Wake up other device from RTC
System Interface (3 pins)			
B8	HRST#	2.8V LVTTL input 75K pull up, SMT	System reset. Active low
C9	STANDBY	2.8V LVTTL input PPU, PPD, slow slew rate, SMT	Standby mode Default 75K pull up Share with GIO11
B9	INT0#	2.8V, LVTTL Input PPU, PPD, SMT,	External interrupt 0 Default 75K pull up Share with GIO10
Peripheral Interface (12 pins)			
G8	RX0	2.8V LVTTL input 75K pull up, SMT	Serial input for UART 0
G9	TX0	2.8V LVTTL Output, 75K pull up 2mA, 4mA, 6mA, 8mA PDR	Serial output for UART 0 Default 4ma driving
H8	RX1/ BT_Reset/ ECLK/ Ext_SYNC	2.8V LVTTL input 75K pull up, SMT	Serial input for UART 1 Share with GIO9

H9	TX1/ TMARK/	2.8V LVTTL pure Output, SMT 2mA, 4mA, 6mA, 8mA, PDR	Serial output for UART 1 / 1PPS time mark output Default 4ma driving Share with GO16
H7	RX2/ GPSIF[1]/ SIN1/ SYNC/ SP_DAT	2.8V LVTTL I/O slow slew rate 75K pull up, SMT, 2mA, 4mA, 6mA, 8mA, PDR	Serial input for UART 2 Default input Share with GIO8
J7	TX2/ GPSIF[0]/ SO1/ DUTY/ SP_CK	2.8V LVTTL I/O, slow slew rate no pull, SMT, 2mA, 4mA, 6mA, 8mA, PDR	Serial output for UART 2 Default output 4ma driving. Share with GIO7
J9	SCK1/ ANA_DBG[0]/ MA[20]/ CLK MON	2.8V LVTTL I/O, 75K pull down, PSR, SMT 4mA, 8mA, 12mA, 16mA PDR	Default: input, slow slew rate while switching to output Share with GO14
F9	SCK0/ I2C_MST_CK	2.8V LVTTL pure Output, SMT 4mA, 8mA, 12mA, 16mA PDR	Synchronous serial interface (SPI) Default: output 4ma driving
E8	SIN0/ I2C_SLV_CK	2.8V LVTTL I/O, 75K pull down, SMT 4mA, 8mA, 12mA, 16mA PDR	Synchronous serial interface (SPI) Default: input Share with GIO6
E9	SO0/ I2C_DAT	2.8V LVTTL I/O, no pull, SMT 4mA, 8mA, 12mA, 16mA PDR	Synchronous serial interface (SPI) Default: output 4ma driving Share with GIO5
F8	SCS0#	2.8V LVTTL I/O, 75K pull up, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave select 0. Active low Default output 4mA driving Share with GIO4
J8	SCS1#/ ANA_DBG[1]/ MA[21]	2.8V LVTTL pure Output, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave select 1. Active low Default: output 4mA driving Share with GO15
Debug Interface (6 pins)			
E7	JCK/ DSP_I2CC/ Ext RF_CLK/ SP_CK	2.8V LVTTL I/O 75K Pull Down, slow slew rate, 4mA driving SMT	JTAG Interface clock. Default input Share with GIO0
C8	JDI/ DSP_I2CD/ SP_DAT	2.8V LVTTL I/O 75K Pull Down, slow slew rate, 4mA driving SMT	JTAG Interface data input. Default input Share with GIO1
G7	JMS/ ECLK/ S4W_CS/ RF_ASHORT	2.8V LVTTL I/O 75K Pull Down, slow slew rate, 4mA driving SMT	JTAG Interface mode select. Default input Share with GIO2

D9	JRST#/ RF_AOK	2.8V LVTTL input 75K Pull up, SMT	JTAG Interface reset. Active low Default: input Share with GIO3
F7	JDO/ RF_LOCK_DET	2.8V LVTTL I/O 75K Pull Down, slow slew rate, 4mA driving SMT	JTAG Interface data output. Default output Share with GO18
D8	JRCK/ RF_CLKO	2.8V LVTTL I/O 75K Pull Down, slow slew rate, 4mA driving SMT	JTAG Interface return clock. Default output Share with GO20
USB (3 pins)			
J6	D_minus	3.3V I/O	
J5	D_plus	3.3V I/O	
H6	VDDU	Digital supply	5V for USB power
	GIO20~GIO0		GIO0 share with JCK GIO1 share with JDI GIO2 share with JMS GIO3 share with JRST# GIO4 share with SCS0# GIO5 share with SO0# GIO6 share with SIN0 GIO7 share with TX2 GIO8 share with RX2 GIO9 share with RX1 GIO10 share with INT0# GIO11 share with STANDBY# GIO12 share with I2C_clk1 GIO13 share with I2C_dat1 GO14 share with SCK1 GO15 share with SCS1_ GO16 share with TX1 GO18 share with JDO GO20 share with JRCK
RF & Power Supply			
F1	ACDUP	Analog input	Voltage reference Cap
F2	ATEST	Analog output	Analog test signal
A2	VCC_LNA	Analog power	LNA VCC supply
A7	VCC_ADC	RF Supply	ADC VCC supply
B6	GND	RF GND	ADC Ground

F5	DVDD12	Digital Supply	Core Power at 1.2V
G2	LDO2.8V_Out	Digital Supply	2.8V LDO output
G1	LDO2.8V_input	Digital Supply	2.8V LDO input
G3	LDO1.2V_Out	Digital Supply	1.2V LDO output
F3	LDO1.2V_input	Digital Supply	1.2V LDO input
C7,D7,E6,F6	VDD_GND	Digital Supply	Ground (decrease pin number)
C5	VS_LNA	Analog output	Supply Voltage to external LNA
E2	VS_TCXO	RF Supply	Supply Voltage to external TCXO
A1	RF IN	RF	LNA RF Input pin
B1	GND	Analog	Battery Ground
B4	GND	RF GND	LNA Ground
A3	GND	RF GND	LNA Ground
B2	GND	RF GND	LNA Ground
C6	VS_AA	Analog input	Monitor pin for active antenna
E1	VS_15	RF Supply	RF VCC Supply
C3	VCC_SX	RF Supply	RF supply
D4	GND	RF Ground	
C4	VCC_BAT	RF Supply	Supply Voltage for external LNA or active antenna circuit
D5	VCCF	Digital Supply	Flash VCC Supply
D6	DVIO28	Digital Supply	Digital IO VCC Supply
D1	NC		
D3	VCCREG	Analog	1.5V LDO input
B3	GND	RF GND	VCO Ground
E4	GND	RF GND	VCO Ground
D2	OSC1	Analog	Input for crystal oscillator or TCXO
E5	GND	RF GND	Mixer Ground
A5	MIX_IN	Mixer Input	Mixer Input
G4	GND	Analog GND	Analog Ground
F4	GND	Analog GND	Analog Ground
E3	GND	Analog GND	Analog Ground
H1	SMPS_GND	SMPS	
H2	SMPS_S	SMPS	
J1	SMPS_F	SMPS	
J2	SMPS_VDD	SMPS	
A6	VCC_IF	RF Supply	IF Supply
B5	GND	RF GND	IF Ground
C1	NC		
J3	RTC_VDD	Analog Supply	Supply Voltage to RTC LDO
A4	LNA_OUT	RF	LNA RF Output

Parallel Flash Interface

N/A	MD7-MD 0	2.8V LVTTL I/O, PPU, PPD, PSMT, PSR, 2mA, 4mA, 6mA, 8mA PDR	Lower 8 bits Memory Data Bus. These pins are the bi-directional upper Buffer RAM data bus to the external buffer memory. Default : 8mA, no pull, no SMT, slow slew rate.[2]
N/A	MD15~MD8	2.8V LVTTL I/O, PPU, PPD, PSMT, PSR, 2mA, 4mA, 6mA, 8mA PDR	Upper 8 bits Memory Data Bus. These pins are the bi-directional upper Buffer RAM data bus to the external buffer memory. Default : 8mA, no pull, no SMT, slow slew rate.
N/A	MA19~MA0	2.8V LVTTL I/O, 75K pull down, PSR, SMT 2mA, 4mA, 6mA, 8mA PDR	Memory Address Bus [19:0]. Default : 8mA driving, 75K pull down,, slow slew rate.
N/A	CS0#	2.8V LVTTL Output, PSR, 2mA, 4mA, 6mA, 8mA PDR	Read on Memory Chip Select. Active low Default : 8mA driving, slow slew rate.
N/A	WE#, OE#	2.8V LVTTL Output, PSR, 2mA, 4mA, 6mA, 8mA PDR	Memory write enable and output

Note:

PPU: Programmable pull up

PPD: Programmable pull down

PSR: Programmable slew rate

PDR: Programmable driving

4. Block Diagrams

4.1. Single Chip Receiver Architecture

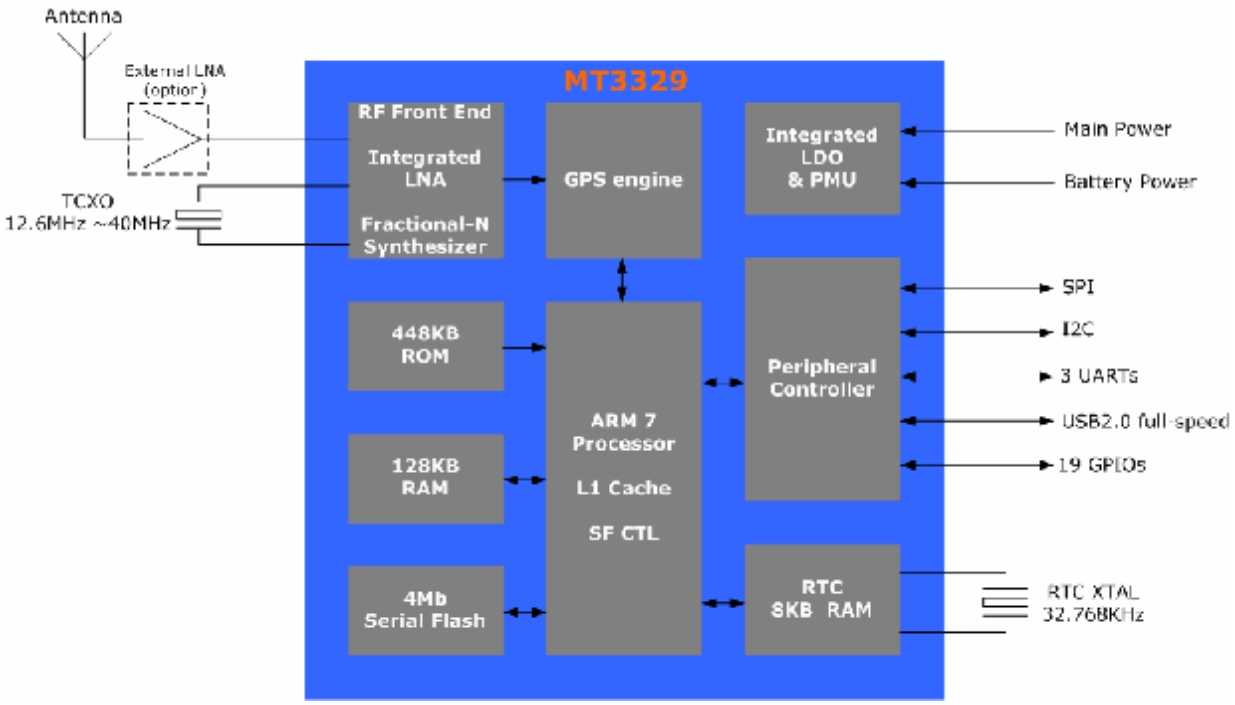


Fig. 1 MT3329 system block diagram

4.2. Functional Block Diagram (RF PART)

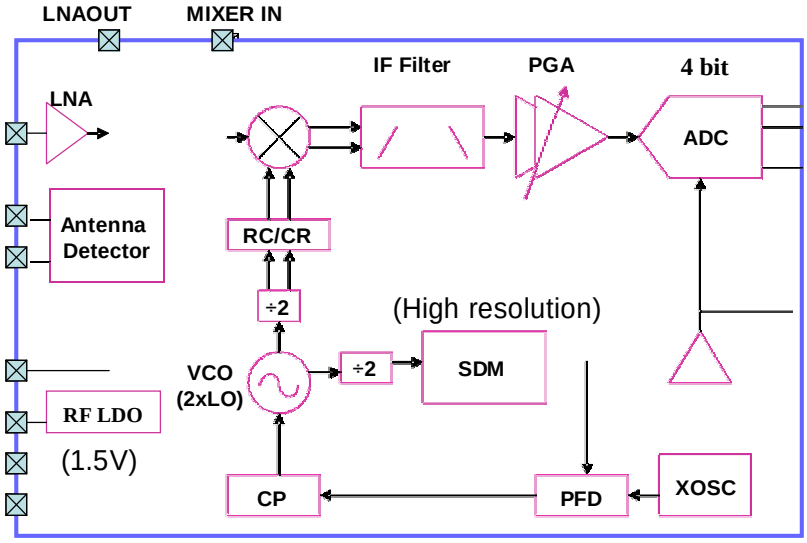


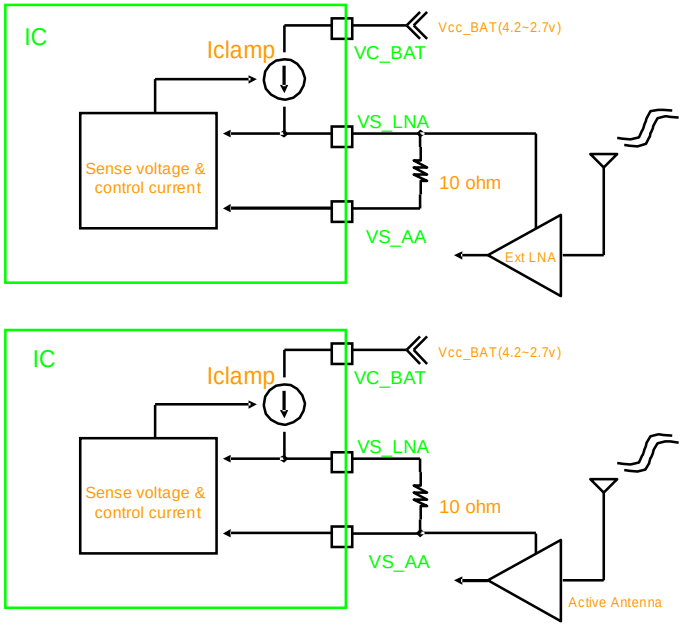
Fig. 2 MT3329 functional block diagram (RF part)

5. MT3329 RF Part Description

5.1. Antenna Detection

Antenna detection capability in the MT3329 enables IC to recognize the presence of an external antenna. In the event that there is a short circuit occurring at the active antenna portion, the IC is able to limit the drawn current to a safe level. By using baseband control, active antenna current will be limited around 30mA or 40mA, which is set by baseband. And when active antenna sink a current higher than 3mA, the IC will send a signal to baseband to indicate that active antenna is functional.

On board external LNA can also make use of VS_LNA pin as a power supply to draw current. This allows external LNA to be powered-down through IC's baseband control.



5.2. LNA/Mixer

Upon receiving RF input signal in through either GPS antenna to internal LNA or external antenna and LNA, the mixer down converts the amplified signal (1575.42MHz) to a differential IF signal of 4.092MHz. The current chip configuration also allows external LNA to be connected directly to the MIXER_IN pin. The internal LNA has a power-down option. Upon detection of an external active antenna connected to VS_AA, this internal LNA will automatically enter into power-down mode. This feature can also be disabled through baseband control to allow active antenna to be directly connected to RF_IN.

5.3. VCO/Synthesizer

The entire frequency synthesizer including crystal oscillator, VCO, divider, phase frequency detector (PFD), charge pump

(CP), and loop filter are all integrated on MT3329 chip. Upon power-on, VCO is auto-calibrated to its required sub-band.
The synthesizer has two topologies (integer-N or fractional-N) selectable through the basnband control

Integer-N synthesizer is meant for supporting 16.368MHz and 26MHz reference frequency. Other clock modes from
12.6MHz up to 40MHz are supported by fractional-N synthesizer, together with a sigma-delta modulator (SDM) and multi-modulus divider (MMD).

5.4. IF CSF

The down converted IF signal from the mixer output passes through a bandpass CSF. Centered at 4.08/4.092MHz (freq. 26MHz / 16.368MHz), the filter rejects out-of-band (10MHz) interferences by more than 20dB, and has a pass band ripple of <0.2dB. The filter also provides a 17dB pass band gain to improve noise figure.

It supports both 2MHz (GPS) and 4MHz (Galileo).

5.5. PGA

The PGA has approximately 48dB of gain control range with approximately 1.6dB per step. The maximum gain is around 48dB.

5.6. ADC

The differential IF signal is being quantized by a 2 or 4-bit ADC, depending on the option set through baseband control.

6. MT3329 Digital Part Description

6.1. ARM7EJ-S

The ARM7EJ-S processor provides the flexibility necessary to build Java-enabled, real-time embedded devices requiring small size, low power and high performance. It builds on the features and benefits of the established ARM7TDMI core and is delivered in synthesizable form. The ARM7EJ-S is supported by a wide variety of development tools and can run at speeds up to 56MHz.

The ARM7EJ-S includes a JTAG interface which provides a standard development and debugging interface. The interface can connect to a variety of off-the-shelf emulators. The emulators provide single-step, trap and access to all the internal registers of the digital portion of MT3329.

6.2. Cache

MT3329 provides cache to speed-up program execution and reduce external flash access times. It supports up to 64Kbits cache buffer and can be used as internal memory when it is not fully used.

6.3. Boot ROM

The embedded Boot ROM provides a function of loading a set of user code through UART or USB into the SRAM. It can be used to execute Flash update and no external strap pin is needed.

6.4. Battery Backed-up Memory

MT3329 provides very low leakage (about 4uA) battery backed-up memory, which contains all the necessary GPS information for quick start up and a small amount of user configuration variables. There is a build-in 1.26V LDO for RTC domain, and it could be bypassed while an external LDO applied. This RTC LDO is a voltage regulator which has very low quiescent current, typical quiescent current <1.2uA, Small ceramic capacitor can be used as the ouput capacitor, the stable operation region ranges from very light load (~=0) to about 5mA.

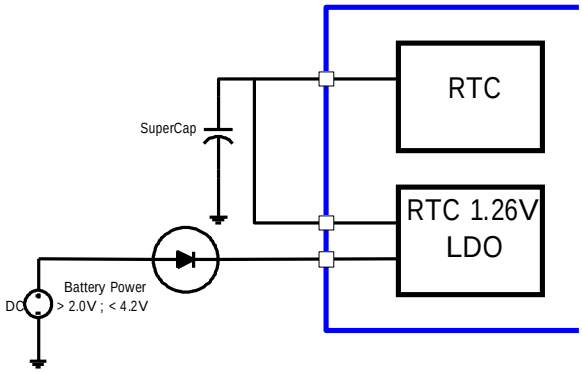


Fig. 3.1 RTC with internal RTC LDO application circuit

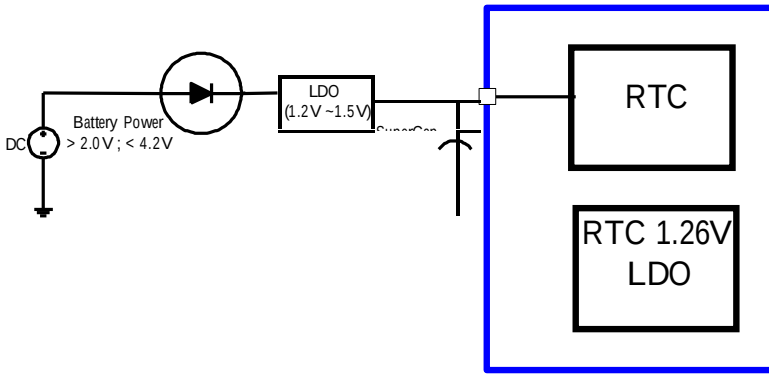


Fig. 3.2 RTC with external RTC LDO application circuit

6.5. Timer function

The timer function supports a resolution of 32.25ms resolution time tick generation. With 16 bits counter, the period of timer can be from 0~2047s. One pin named "PAD_TIMER" outputs signal 1'b0 during the timer period and becomes an input pin after time out. Power-control-function for the system can be implemented by connecting this pin to an external LDO controller and add external pull high circuit.

6.6. Clock output

One pin named "PAD_32K_OUT) outputs 32.768KHz clock which can be used to support low clock rate operation mode for some applications or peripherals that need an external clock source.

6.7. Low power detection

A low power detection circuit is implemented and whenever the independent power source (PAD_R1V2, which may be supplied by a backup battery) becomes low voltage, the low power detection circuit can detect this condition and use a indicator signal (output high in normal condition and low in low power condition) to reflect this condition

6.8. Clock Module

This module generates all internal clocks required by processor, correlator, internal memory, bus interface and so on. The referenced input clock is generated from RF block. For system flexibility and the maximum power savings, various power management modes are supported.

6.9. Reset Controller

A build-in reset controller generate reset signal for all digital blocks. It includes power on reset feature and hardware trapping function. Software reset function for different circuit blocks are also included for usage flexibility.

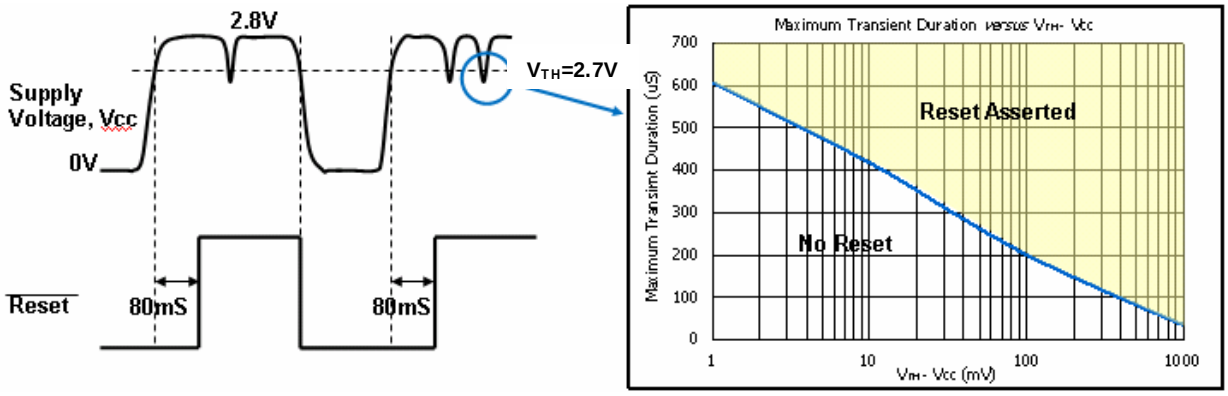


Fig. 4 power on reset diagram

6.10. UART

UART is an abbreviation of "Universal Asynchronous Receiver/Transmitter". MT3329 contains three full duplex serial ports. It is used in serial data communication, and a UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses.

In MT3329, there are several functions related to UART communication, such as UART data output and NMEA sentences receive/output. In generally, UART0 is as NMEA output and PMTK command input, UART1 as RTCM input. Customers can adjust UART2 port as they want. The receiver (RX) and transmitter (TX) side of every port contains a 16-byte FIFO. The bit rates are selectable and ranging from 4.8 to 921.6 kbps. UART can provide the developers signal or message outputs.

6.11. Interrupt Control Unit

The interrupt control unit manages all internal and external sources of interrupts. These include Timer, Watch dog, all peripheral interfaces such as UART, USB, I2C, SPI, and external user interrupt pins. These interrupt sources could act as wake up event during power saving mode also.

6.12. Flash

External SPI serial flash up to 64Mbits is supported. Specific MTK Flash Tool is supported to download firmware into flash.

6.13. GPIO Unit

GPIO is the abbreviation of General Purpose Input/Output. MT3329 supports a variety of peripherals through at most 19 GPIO ports that are programmable to users. The unit that manages all GPIO lines supports a simple control interface. GPIO can provide the developers signal or message outputs.

6.14. Serial Peripheral Interface (SPI)

The serial peripheral interface port manages communication between digital BB and external devices

6.15. USB Interface

The USB (Universal-Serial-Bus) Interface makes GPS receiver capable of significantly improved data

transmission and receiving rate. It is USB 2.0 Full-Speed compatible and certified by USB IF program. This interface is automatically converted to COM port to HOST operating systems (Windows 98, 2000, XP, and Vista). Users can update firmware through this interface and about 50 percent time is saved. (compared with 921600 bps firmware update through UART interface.)

Plug-and-play feature provides easier way for users' data communication with most navigation software. Moreover, flexibility of applications for difference USB classes is available. For portable product, battery can be charged through this interface as well.

6.16. SRAM

768 Kbits on-chip SRAM is supported to be used for instructions or data. It can support single cycle reads and is designed for low power. No external data memory is needed for many applications.

6.17. Factory testing

MT3329 provides full coverage of all the memory during chip testing and qualification. A memory built-in self-test (MEMBIST) function is used. The SCAN test logic using automatic test pattern generation (ATPG) is usually combined with MEMBIST to provide functional test coverage at the wafer level.

7. Electrical Characteristics

7.1. DC Characteristics

7.1.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
LDO2.8V_INPUT	2.8V LDO Power Supply	-0.3 to 3.6	V
LDO1.5V_INPUT	1.5V LDO Power Supply	-0.3 to 3.6	V
LDO1.2V_INPUT	1.2V LDO Power Supply	-0.3 to 3.6	V
VDDF	Embedded Flash Power Supply	-0.3 to 3.6	V
VDDU	USB Power Supply	-0.3 to 3.6	V
DVIO28	IO 2.8V Power Supply	-0.3 to 3.6	V
DVDD12	Baseband 1.2V Power Supply	-0.3 to 3.6	V
R1V2	RTC Power Supply	-0.3 to 1.8	V
VCC_IF, VCC_ADC, VCC_SX, VCCREG, VCC_LNA	1.5V RF Power Supply	-0.3 to 3.6	V
VCC_BAT, RTC_VDD	Power Supply for External Active Antenna	-0.3 to 4.2	V
T_{STG}	Storage Temperature	-45 to +85	℃
T_A	Operating Temperature	-45 to +85	℃

7.1.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VDDBB28	2.8V Baseband Power Supply	2.7	2.8	3.6	V
FVDD	Embedded Flash Power Supply	2.7	2.8	3.6	V
R1V2	RTC Power Supply	0.9	1.2	1.8	V
VCC_IF, VCC_ADC, VCC_LNA, VCC_SX	1.5V RF Power Supply	1.4	1.5	1.6	V
VCC_BAT	Power Supply for External Active Antenna	2.7	3.3	4.2	V
T_A	Operating Temperature	-40	25	85	℃
T_j	Commercial Junction Operating Temperature	0	25	115	℃
	Industry Junction Operating Temperature	-40	25	125	℃

7.1.3. General DC Characteristic

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
IIL	Input low current	No pull-up or down	-1	1	uA
IIH	Input high current	No pull-up or down	-1	1	uA
IOZ	Tri-state leakage current		-10	10	uA

7.1.4. DC Electrical Characteristics for 2.8 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Lower Voltage	LVTTL	-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	3.6	V

V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.8	1.6	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.6	2.0	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD28 + 0.3	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

7.1.5. 1.26V RTC LDO DC Characteristic

SYNBOL	PARAMETER	MIN	TYP	MAX	UNIT
RTC_VDD	RTC LDO input supply voltage	2	3	4.3	V
R1V2	RTC LDO output	1.15	1.25	1.35	V
Iq	Quiescent current	0.6u	1.04	1.5u	uA

7.1.6. DC Electrical Characteristics for 2.8 volts INT0# operation

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Lower Voltage	LVTTL	-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	5.3	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.8	1.6	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.6	2.0	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

7.1.7. DC Electrical Characteristics for RF Part

VCC = 1.5V, Ta = 25 ℃ unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Icc	Total Supply Current		16.5		mA
Icc (STAND-BY)	Only the PLL, Oscillator and Regulator are kept powered up.		7.9		mA
Icc(DOZE)	Only the Oscillator and Regulator are kept powered up.		0.37		mA
Icc(Off)	Power-down state current			2	μA

7.1.8. LNA AC Electrical Characteristics for RF Part

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc	Supply Voltage	1.4	1.5	1.6	V
Icc	Supply current			2.5	mA
NF	Noise Figure 50 ohm Rs		2.1	2.5	dB
|S21|	Forward Voltage Gain		19		dB
|S12|	Reverse Isolation		30		dB
|S11|	Input Return Loss 50 Ohm RS	-10			dB
|S22|	Output Return Loss 50 Ohm RL	-10			dB
IIP3	Input referred IP3 50 ohm RS		-17		dBm
P1dB	1dB Input Compression point		-27		dBm
Tstart	Circuit Start-up time			5	µs

7.1.9. RX chain from LNA to PGA, before ADC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc	Supply Voltage	1.4	1.5	1.6	V
NF	Noise Figure 50 ohm Rs		2.7	3.2	dB
Gain	Forward Voltage Gain		100		dB
P1dB	1dB Input Compression point		-65		dBm
Tstart	Circuit Start-up time			5	µs

7.1.10. RX chain from Mixer to PGA, before ADC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc	Supply Voltage	1.4	1.5	1.6	V
NF	Noise Figure 50 ohm Rs		7	8	dB
Gain	Forward Voltage Gain	50	80	100	dB
P1dB	1dB Input Compression point		-45		dBm
Tstart	Circuit Start-up time			5	µs

7.1.11. Image-Reject Down-conversion Mixer

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
|S11|	Input Return Loss 50 Ohm RS	-10			dB
IRR2M	2MHz Image Rejection Ratio		>30		dB
IRR4M	4MHz Image Rejection Ratio		>30		dB
Tstart	Circuit Start-up time			5	µs

7.1.12. Channel Select Filter (CSF)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fc	Centre Frequency		4.092		MHz
BW3dB	3dB Bandwidth		2.49		MHz
Ripple	Passband Ripple		<0.1	0.1	dB
IRR2M	2MHz Image Rejection Ratio				dB
IRR4M	4MHz Image Rejection Ratio				dB
Tstart	Circuit Start-up time			5	µs

7.1.13. Programmable Gain Amplifier (PGA)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Gv	Voltage Gain	0		48.8	dB
Tstart	Circuit Start-up time			5	µs

7.1.14. 2-Bit & 4-Bit Quantizer (ADC)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fo	Operating Frequency		16.368	26	MHz
Tstart	Circuit Start-up time			5	µs

7.1.15. Integrated Synthesizer

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fosc	VCO Oscillation Frequency		3142.656		MHz
V	Tuning Voltage Range	0.2		Vcc-0.2	V
DIV	Programmable Divider Ratio	32		127	
Tstart	Circuit Start-up time			100	µs

7.1.16. Crystal Oscillator (XO)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Ftcxo	TCXO Oscillation Frequency	12.6	16.368	40	MHz
Vtcxo	TCXO output swing	0.2	0.8		Vpp

7.2. AC Characteristics

7.2.1. JTAG Interface Timing

Description	Symbol	Min	Max	Unit	Notes
TDI input setup to rising TCK	T1	0.35T	-	ns	1
TDI input hold from rising TCK	T2	0.15T	-	ns	1
TMS input setup to rising TCK	T1	0.35T	-	ns	1
TMS input hold from rising TCK	T2	0.15T	-	ns	1
Rising TCK to TDO valid	T3	-	0.5T	ns	1
TDO hold from rising TCK	T4	0	-	ns	1

Note:

1. The maximal condition of JTAG clock cycle (TCK) is 50Mhz.

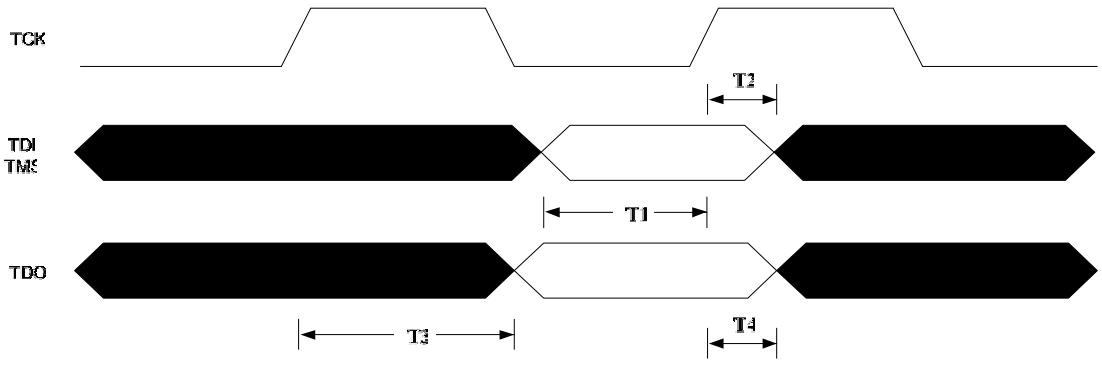


Fig. 2 JTAG interface timing diagram

7.2.2. RS232 Interface Timing

Baud Rate Required (bps)	Programmed Baud Rate (bps)	Baud Rate Error (%)
4800	4800.000	0.000
9600	9600.000	0.000
14400	14395.778	-0.0293
19200	19188.746	-0.0586
38400	38422.535	0.0587
57600	57633.803	0.0587
115200	115267.606	0.0587

1. UART baud-rate settings with UART_CLK frequency = 16.368MHz (UART_CLK uses the reference clock of the system).

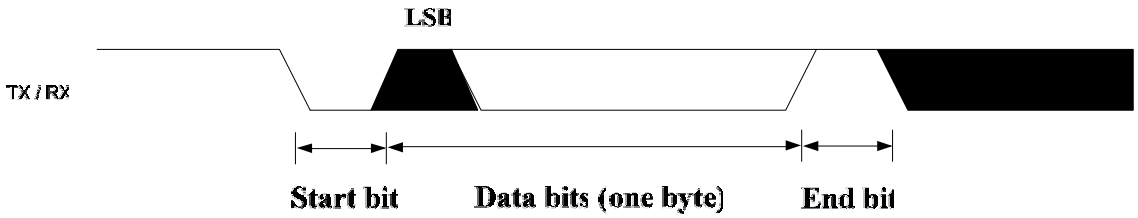


Fig. 3 RS232 interface timing diagram

7.2.3. SPI Interface Timing

Description	Symbol	Min	Max	Unit	Notes
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T - 10	0.5T + 10	ns	1
SO hold time	T4	0.5T - 10	0.5T + 10	ns	1
SIN setup time	T5	10	-	ns	1
SIN hold time	T6	10	-	ns	1

Note:

1. The condition of SPI clock cycle (SCK) is (rf_clk / 16)Mhz ~ (rf_clk / 1036)Mhz.

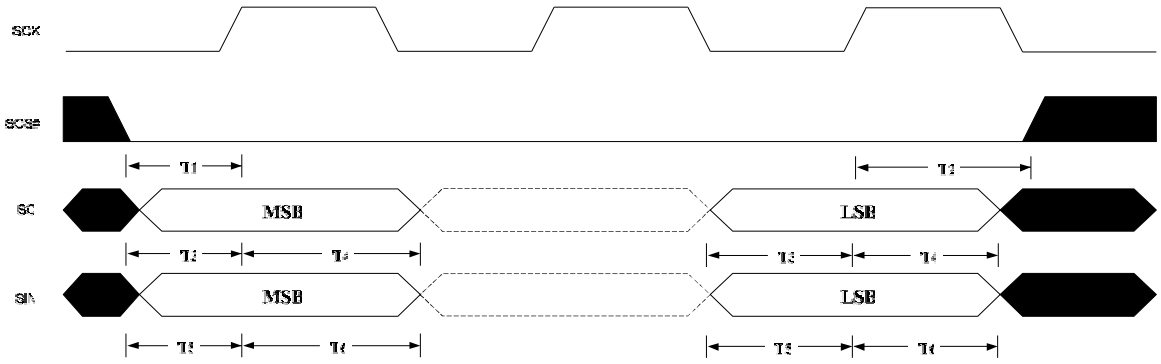


Fig. 4 SPI interface timing diagram

7.2.4. I2C Interface Timing

Description	Symbol	Min	Max	Unit	Notes
I2C_DATA setup time	T1	0.4T - 10	0.4T + 10	ns	1
I2C_DATA hold time	T2	0.6T - 10	0.6T + 10	ns	1

Note:

1. The condition of I2C clock cycle (I2C_CLK) is (rf_clk) Mhz ~ (rf_clk / 253) Mhz.

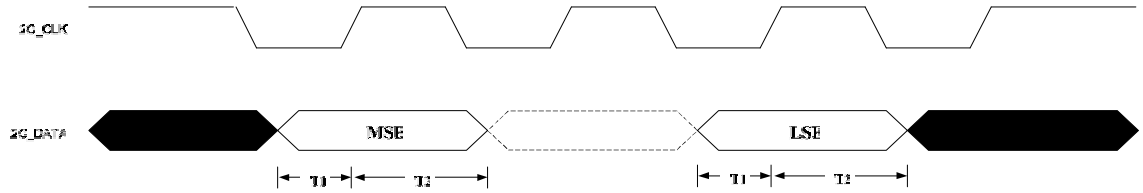


Fig. 5 I2C interface timing diagram

7.2.5. USB Interface

Low-/full-speed signaling levels

Bus State	Signaling Levels		
	At originating source connector (at end of bit time)	At final target connector	
		Required	Acceptable
Differential "1"	D+ > VOH (min) and D- < VOL (max)	(D+) - (D-) > 200 mV and D+ > VIH (min)	(D+) - (D-) > 200 mV
Differential "0"	D- > VOH (min) and D+ < VOL (max)	(D-) - (D+) > 200 mV and D- > VIH (min)	(D-) - (D+) > 200 mV
Single-ended 0 (SE0)	D+ and D- < VOL (max)	D+ and D- < VIL (max)	D+ and D- < VIH (min)
Single-ended 1 (SE1)	D+ and D- > VOSE1(min)	D+ and D- > VIL (max)	
Data J state: Low-speed Full-speed	 Differential "0" Differential "1"	 Differential "0" Differential "1"	
Data K state: Low-speed Full-speed	 Differential "1" Differential "0"	 Differential "1" Differential "0"	
Idle state: Low-speed Full-speed	NA	 D- > VIHZ (min) and D+ < VIL (max) D+ > VIHZ (min) and D- < VIL (max)	 D- > VIHZ (min) and D+ < VIH (min) D+ > VIHZ (min) and D- < VIH (min)
Resume state	Data K state	Data K state	
Start-of-Packet (SOP)	Data lines switch from Idle to K state		
End-of-Packet (EOP)[4]	SE0 for approximately 2 bit times[1] followed by a J for 1 bit time[3]	SE0 for ≥ 1 bit time[2] followed by a J state for 1 bit time	SE0 for ≥ 1 bit time[2] followed by a J state
Disconnect (at downstream port)	NA	SE0 for ≥2.5 µs	
Connect (at downstream port)	NA	Idle for ≥2 ms	Idle for ≥2.5 µs
Reset	D+ and D- < VOL (max) for ≥10ms	D+ and D- < VIL (max) for ≥10 ms	D+ and D- < VIL (max) for ≥2.5 µs

Note 1: The width of EOP is defined in bit times relative to the speed of transmission. (Specification EOP widths are given in Table 7-7 and Table 7-8.)

Note 2: The width of EOP is defined in bit times relative to the device type receiving the EOP. The bit time is approximate.

Note 3: The width of the J state following the EOP is defined in bit times relative to the buffer edge rate. The J state from a low-speed buffer must be a low-speed bit time wide and, from a full-speed buffer, a full-speed bit time wide.

Note 4: The keep-alive is a low-speed EOP.

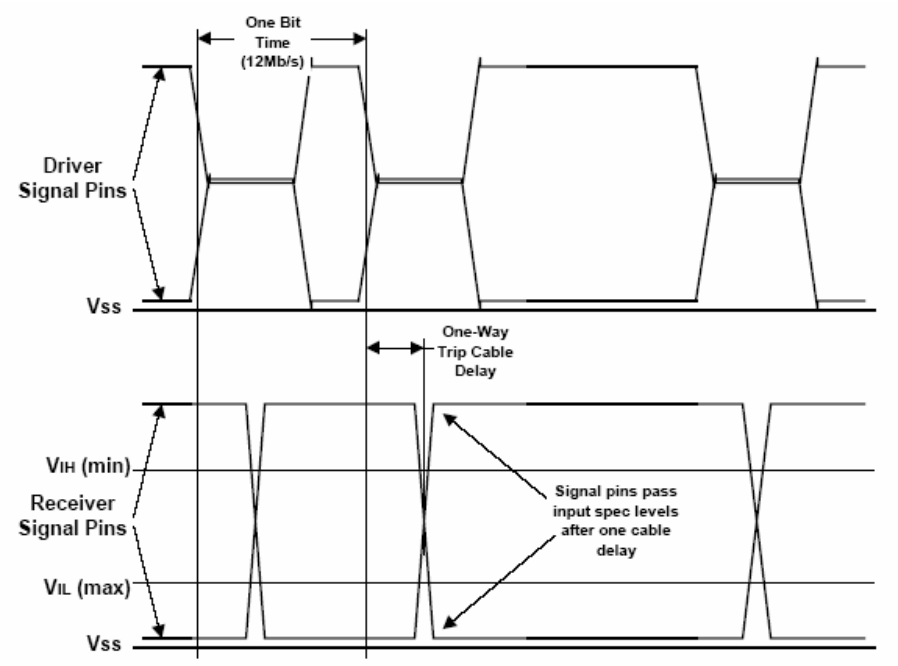


Fig. 10 USB Full-Speed signal waveform.

Detail USB timing diagram and usage could refer to USB specification.

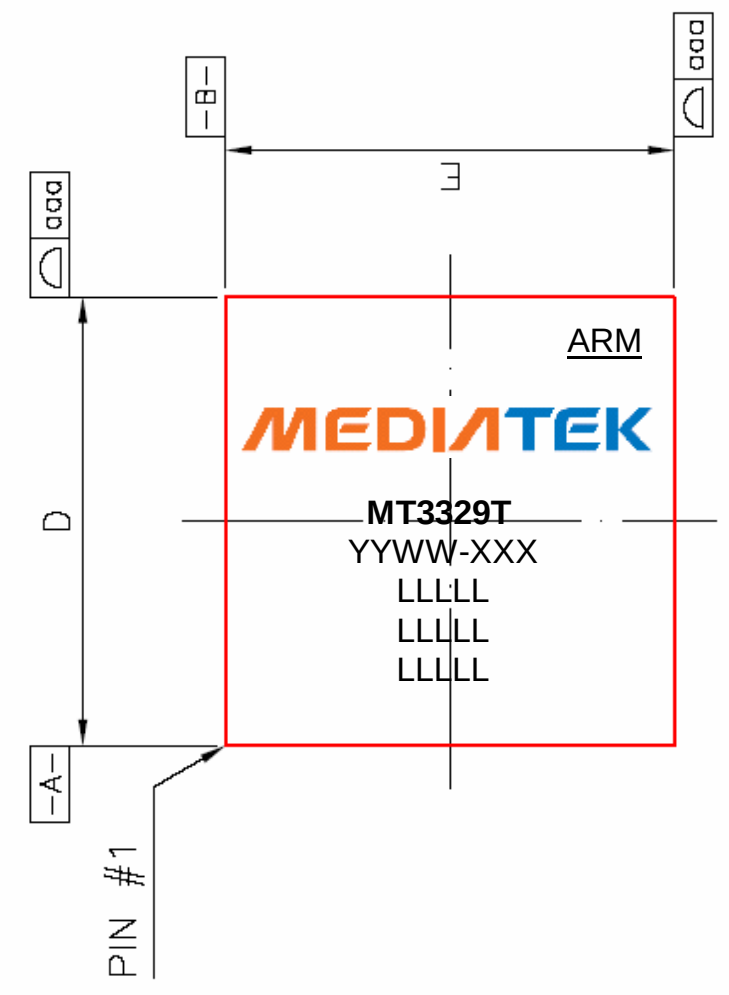
8. Package Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	6.10	6.20	6.30	0.240	0.244	0.248
E	6.10	6.20	6.30	0.240	0.244	0.248
D1	---	5.20	---	---	0.205	---
E1	---	5.20	---	---	0.205	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	9/9			9/9		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

STFBGA 81 (6.2X6.2mm) Outline Dimensions

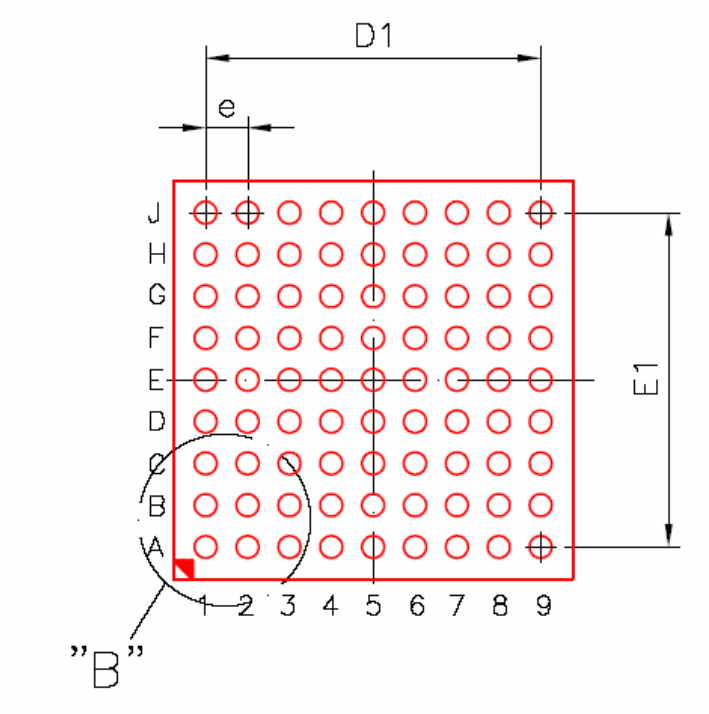


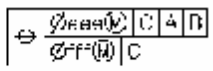
Y = Date Code Year

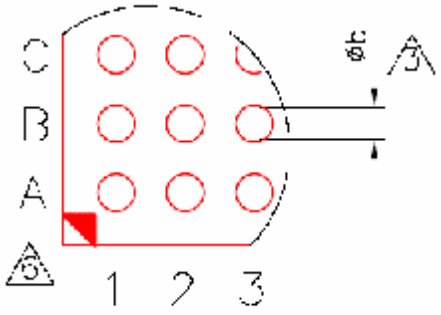
W = Date Code Week

X = MTK Production Code

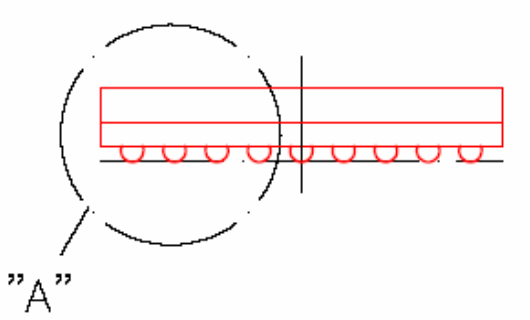
L = Lot No.

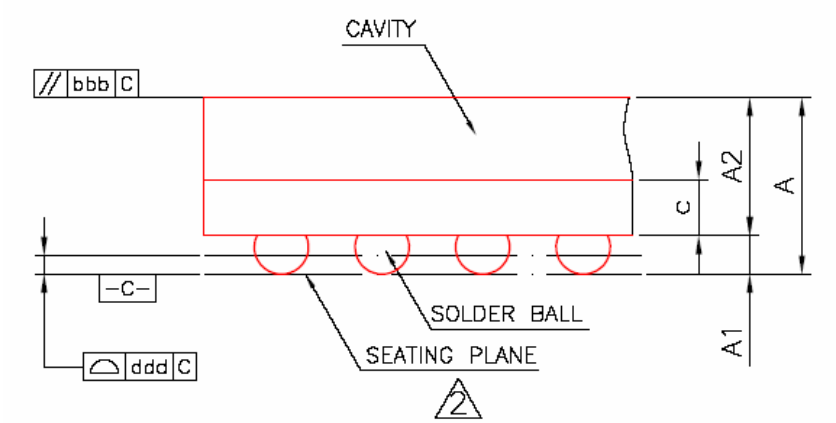






DETA _ : "3"





DETAIL : "A"

ESD CAUTION

MT3329 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although
MT3329 is with built-in ESD protection circuitry, please handle with care to avoid permanent malfunction or performance degradation.

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