

# AH'(\$\$

## **N-Channel Power MOSFET**

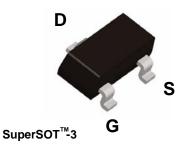
## **General Description**

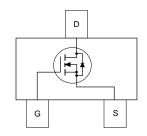
This N-Channel Logic Level MOSFET is produced using T [  $\bullet$   $\mbox{\ensuremath{\mbox{\ensuremath{\mbox{\sc N}}}} \& \mbox{\ensuremath{\mbox{\sc Semiconductor's}} advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.$ 

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

#### **Features**

- $\not$   $\dot{\mathbb{R}}$  A, 30 V.  $R_{DS(ON)} = 0.0 \dot{1}$   $\Omega$  @  $V_{GS} = 10$  V  $R_{DS(ON)} = 0.06 \dot{1}$   $\Omega$  @  $V_{GS} = 4.5$  V
- Very fast switching speed.
- Low gate charge (5nC typical)
- High performance version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Maximum Drain Current – Continuous	(Note 1a)	Ι.€	А
	– Pulsed		1€	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	F.G5	W
		(Note 1b)	0.Ï 6	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		−55 to +150	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a) A					
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W			

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity	
ŒÝÝB€I ÝÝ	###¥	7"	Ásmm	3000 units	

Symbol	Parameter	Test (	Condit	ions	Min	Тур	Max	Units	
Off Char	acteristics						•		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 V$ ,	I <sub>D</sub> = 2	50 μΑ	30			V	
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu A, R$	eference	d to 25°C		21		mV/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V},$	$V_{GS} = 0$	) V			1	μА	
				$T_J = -55^{\circ}C$			10	μА	
I <sub>GSS</sub>	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V},$	$V_{DS} = 0$	V			±100	nA	
On Char	acteristics (Note 2)								
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I <sub>D</sub> = 2	50 μΑ <i>Ά</i>	₩¥ÈÈ	Ë	ÆÈ	Á	
<u>ΔVgs(th)</u> ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu A, R$	eference	d to 25°C		-4		mV/°(	
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V},$ $V_{GS} = 4.5 \text{ V},$ $V_{GS} = 10 \text{ V}, I_D$		0.01 Ì 0.0Í H 0.0Í 3	0.0Í Ì 0.06Í 0.075	Ω			
I <sub>D(on)</sub>	On-State Drain Current						<i>/XXX</i>		
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5V$ ,	I <sub>D</sub> = 2.7 A			∕‱‱ È		AXXXXXXX	
Dvnamio	Characteristics						•		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V,	V 69 =	: 0 V.		ÁHÍ€	Á	pF	
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz	- 65	,		ÁÍ	Á	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance					ΙF	ÁWÁ	pF	
R <sub>G</sub>	Gate Resistance	f = 1.0 MHz				1.8		Ω	
Switchin	ng Characteristics (Note 2)	1					ı		
t <sub>d(on)</sub>		<b>∮∕∕∮∕∕√∕</b>	XXXXX <b>(</b> )XXXXXX(	<u>()A(()()()()()()()()()()()()()()()()()(</u>	((((((((((((((((((((((((((((((((((((((	XXXX	<del>(((((((((((((((((((((((((((((((((((((</del>	ns	
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V},$	R <sub>GEN</sub> :	= 6 Ω	ÁÓÓÓ	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	άά	ÁÁns	
t <sub>d(off)</sub>	Turn-Off Delay Time	1				20	Á	ns	
t <sub>f</sub>	Turn-Off Fall Time	1				ı	Á	Áns	
$\overline{Q_g}$	Total Gate Charge	V <sub>DS</sub> = 15 V,	I <sub>D</sub> = 2	.7 A,	ÁÓÓÓ	‱ ÈG	,	₩₩⁄nC	
$\overline{Q_{qs}}$	Gate-Source Charge	\$			XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	‱́€.Î	ÁÁ	Z)WWW	
Q <sub>gd</sub>	Gate-Drain Charge	1				1.ĺ		nC	

## **Electrical Characteristics**

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source	e Diode Forward Current			0.42	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 0.42 \text{ A}  \text{(Note 2)}$		0.7	1.2	V
trr	Diode Reverse Recovery Time	$IF = 2.7A$ , $diF/dt = 100 A/\mu s$		12	20	ns
Qrr	Diode Reverse Recovery Charge			3	5	nC

#### otes

 R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

## **Typical Characteristics**

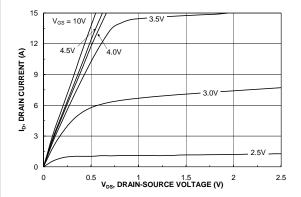
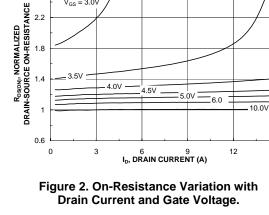


Figure 1. On-Region Characteristics.



2.6

 $V_{GS} = 3.0V$ 

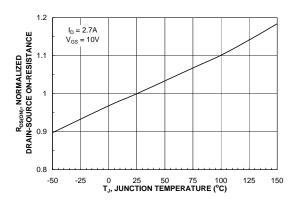


Figure 3. On-Resistance Variation with Temperature.

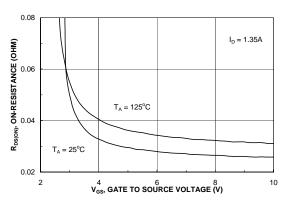


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

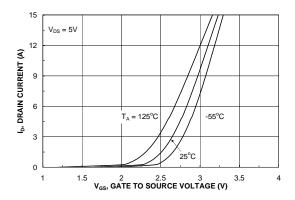


Figure 5. Transfer Characteristics.

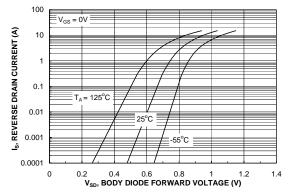
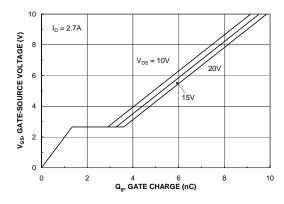


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



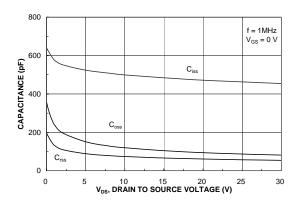
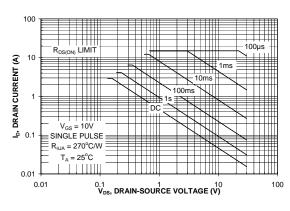


Figure 7. Gate Charge Characteristics.





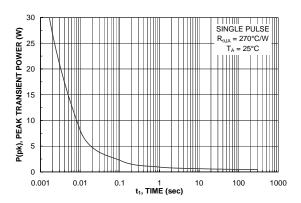


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

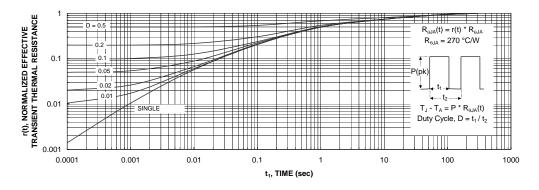
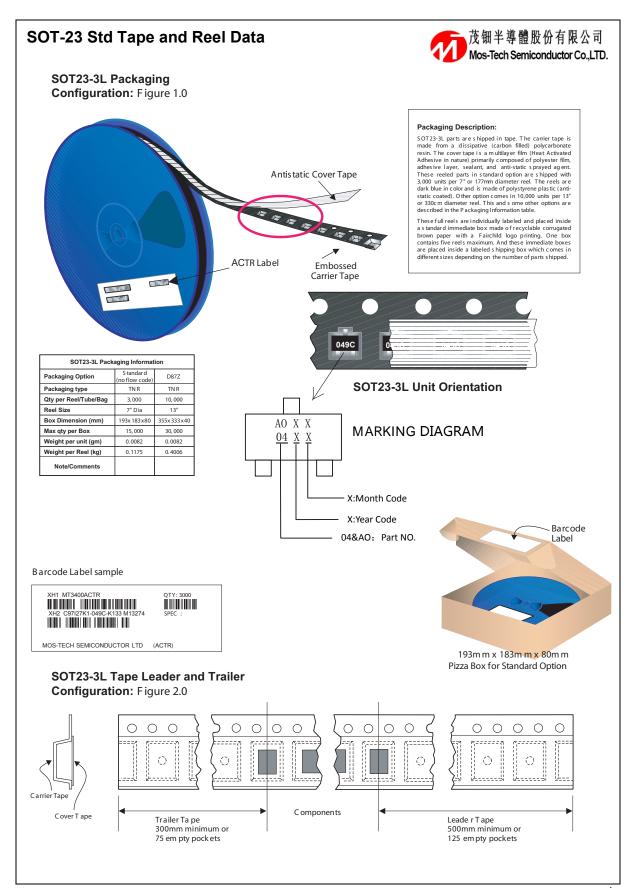


Figure 11. Transient Thermal Response Curve.

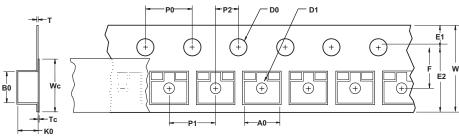
Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



## SOT-23 Std Tape and Reel Data, continued



**SOT23-3L Embossed Carrier Tape Configuration:** Figure 3.0





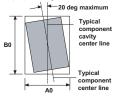
	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
<b>SOT-23</b> (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

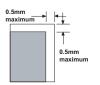


Sketch A (Side or Front Sectional View)

Component Rotation



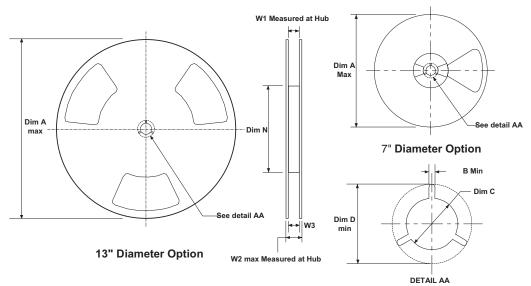
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

#### SOT23-3L Reel Configuration: Figure 4.0



	Dimensions are in inches and millimeters										
Tape Size         Reel Option         Dim A         Dim B         Dim C         Dim D         Dim N         Dim W1         Dim W2						Dim W3 (LSL-USL)					
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10. 9		
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10. 9		

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