

P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- Vps= -30V
- ID= -4.2A (VGS= -10V)
- $RDS(ON) \le 60m \Omega @VGS = -10V$
- $RDS(ON) \le 75m \Omega @VGS = -4.5V$
- $RDS(ON) \leq 120m \Omega @VGS = -2.5V$

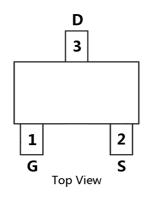
Applications:

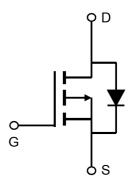
- Power Management in Notebook Computer
- Portable Equipment and Battery Powered Systems

Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.
- SOT-23-3L Package.







Absolute Maximum Ratings (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Steady State	Units
V _{DS}	Drain-Source Voltage	-30	V
V _G S	Gate-Source Voltage	±12	V
I _D	Continuous Drain Current ¹	-4.2	Α
I _{DM}	Pulsed Drain Current ²	-30	Α
Is	Continuous Source Current (Diode Conduction) ¹	-2	Α
PD	Maximum Power Dissipation ¹	1.25	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^{\circ}$ C

Notes:

- 1. Surface Mounted on 1" x 1" FR4 Board, t ≤ 10 Sec.
- 2. Pulse width limited by maximum junction temperature.

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Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
R _{thJA}	Maximum Junction-to-Ambient	t≦10 Sec	65	90	
		Steady State	85	125	°C/W
R _{thJF}	Maximum Junction-to-Foot (Drain)	Steady State	43	60	

Electrical Characteristics (TA=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
Statio	c Characteristics		,		,	
BVDSS	Drain-Source Breakdown Voltage	V _G S= 0V, I _D = -250μA	-30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.7	-1	-1.5	V
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μА
		V _{DS} = -24V, V _{GS} = 0V, T _J = 85℃	-	-	-30	
	Drain Source On State Resistance ^a	V _{GS} = -10V, I _D = -4.2A	-	55	60	mΩ
$R_{DS(on)}$		V _{GS} = -4.5V, I _D = -4A	-	65	75	
		V _{GS} = -2.5V, I _D = -1A	-	-	120	
g _{fs}	Forward Transconductance ^a	V _{DS} = -5V, I _D = -5A	7	11	-	S
V _{SD}	Diode Forward Voltage ^a	I _S = -1A, V _{GS} = 0V	-	-0.77	-1	V
Dyna	mic Characteristics ^b					
C _{iss}	Input Capacitance		-	720	-	pF
Coss	Output Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1MHz	-	90	-	
C _{rss}	Reverse Transfer Capacitance		-	65	-	
Qg	Total Gate Charge		-	11.5	14	
Qgs	Gate-Source Charge	V_{DS} = -15V, V_{GS} = -4.5V, I_{D} = -2.5A	-	1.56	-	nC
Q _{gd}	Gate-Drain Charge		-	2.2	-	
t _{d(on)}	Turn-On Delay Time		-	8.3	12	
tr	Rise Time	$V_{DD} = -15V, R_L = 15\Omega$	-	7.6	15	nSec
T _{d(off)}	Turn-Off Delay Time	I_{D} = -1.0A, V_{GEN} = -10V, R_{G} = 6 Ω	-	26	46	
t _f	Fall Time		-	5.6	10	
Rg	Gate Resistance	V _{GS} =0, V _{DS} =0, f=1MHz	-	8	-	Ω
t _{rr}	Body Diode Reverse Recovery Time	1 10 17 11 10001	-	11	-	nSec
Qrr	Body Diode Reverse Recovery Charge	- I _F = -4A, di/dt = 100A/μs	-	6	-	nC

Note:

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a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.



Characteristics Curve

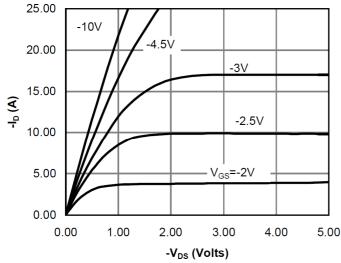


Fig 1: On-Region Characteristics

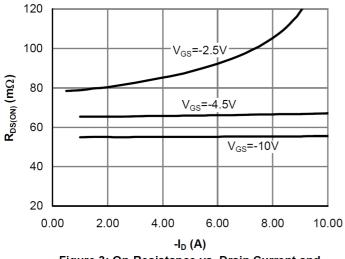


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

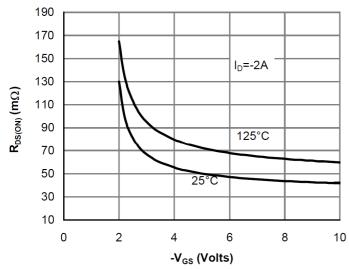


Figure 5: On-Resistance vs. Gate-Source Voltage

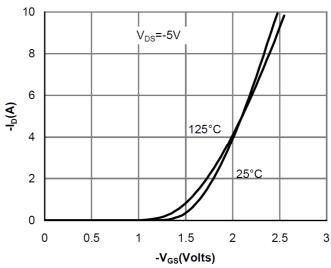


Figure 2: Transfer Characteristics

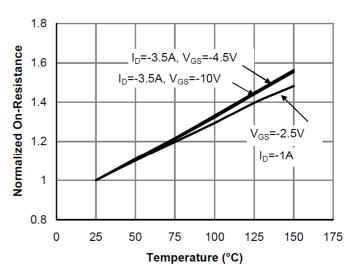


Figure 4: On-Resistance vs. Junction Temperature

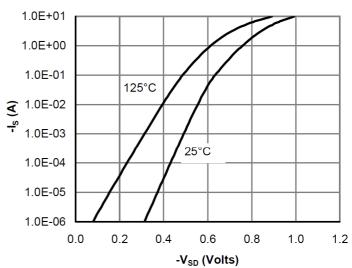


Figure 6: Body-Diode Characteristics

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Characteristics Curve

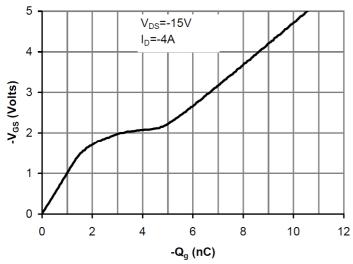


Figure 7: Gate-Charge Characteristics

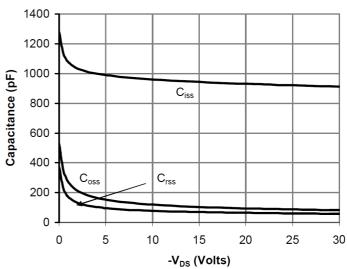


Figure 8: Capacitance Characteristics

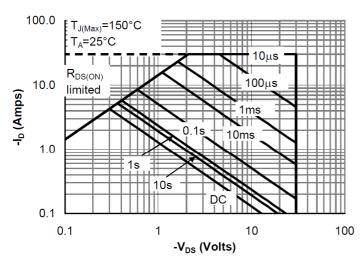


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

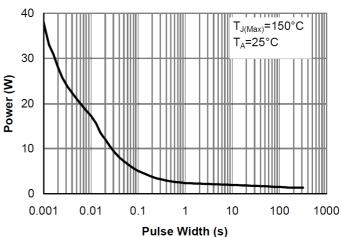


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

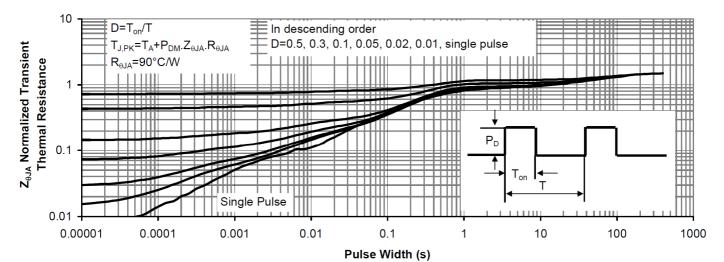


Figure 11: Normalized Maximum Transient Thermal Impedance

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