



## P-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS} = -30V$
- $I_D = -4.1A$  ( $V_{GS} = -10V$ )
- $R_{DS(ON)} \leq 60m\Omega$  @  $V_{GS} = -10V$
- $R_{DS(ON)} \leq 95m\Omega$  @  $V_{GS} = -4.5V$

### Features

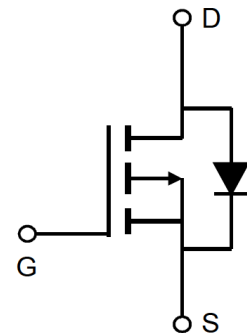
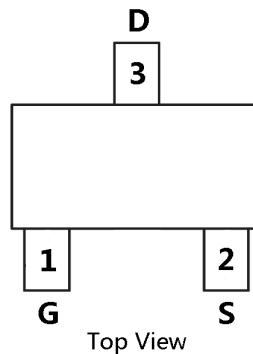
- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

### Applications:

- Power Management in Notebook Computer
- Portable Equipment and Battery Powered Systems.



SOT-23-3L



### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Steady State	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>1</sup>	-4.1	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-20	A
$I_S$	Continuous Source Current (Diode Conduction) <sup>1</sup>	-2	A
$P_D$	Maximum Power Dissipation <sup>1</sup>	1.25	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55~150	$^\circ C$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board,  $t \leq 10$  Sec.
2. Pulse width limited by maximum junction temperature.



## Thermal Resistance Ratings

Symbol	Parameter	Typical	Maximum	Unit	
R <sub>thJA</sub>	Maximum Junction-to-Ambient	t ≤ 10 Sec	65	90	°C/W
		Steady State	85	125	
R <sub>thJF</sub>	Maximum Junction-to-Foot (Drain)	Steady State	43	60	

## Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>● Static Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1	-1.5	-2	V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	-	-	-1	μA
		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 85°C	-	-	-30	
R <sub>DSON</sub>	Drain Source On State Resistance <sup>a</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.1A	-	53	60	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3A	-	80	95	
g <sub>fs</sub>	Forward Transconductance <sup>a</sup>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -4A	5.5	8.2	-	S
V <sub>SD</sub>	Diode Forward Voltage <sup>a</sup>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A	-	-0.8	-1.3	V
<b>● Dynamic Characteristics <sup>b</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> =0V, f=1MHz	-	625	-	pF
C <sub>oss</sub>	Output Capacitance		-	100	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	60	-	
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.5A	-	11.6	16	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.3	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	2.5	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -15V, R <sub>L</sub> = 15Ω I <sub>D</sub> = -1.0A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 6Ω	-	6	12	nSec
t <sub>r</sub>	Rise Time		-	12	23	
T <sub>d(off)</sub>	Turn-Off Delay Time		-	25	46	
t <sub>f</sub>	Fall Time		-	6	12	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0, V <sub>DS</sub> =0, f=1MHz	-	8	-	Ω
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> = -4A, di/dt = 100A/μs	-	14	-	nSec
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	5	-	nC

Note:

a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.



## Characteristics Curve

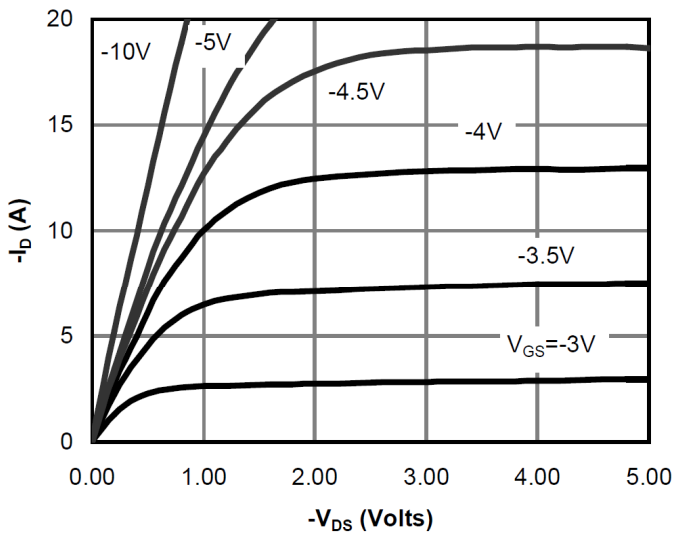


Figure 1: On-Region Characteristics

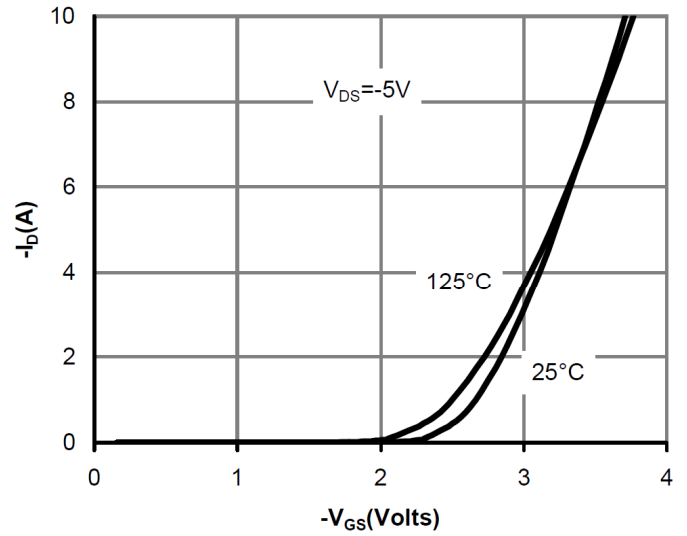


Figure 2: Transfer Characteristics

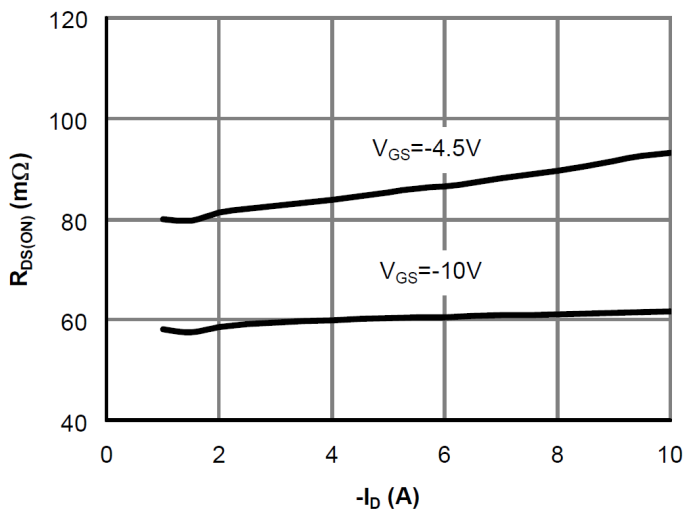


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

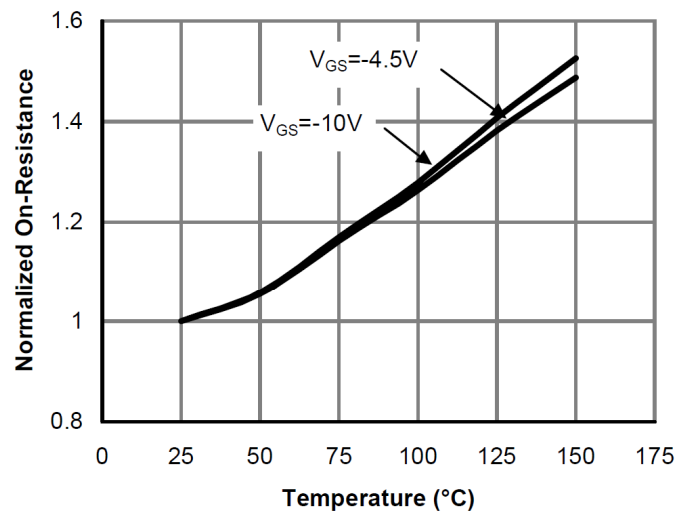


Figure 4: On-Resistance vs. Junction Temperature

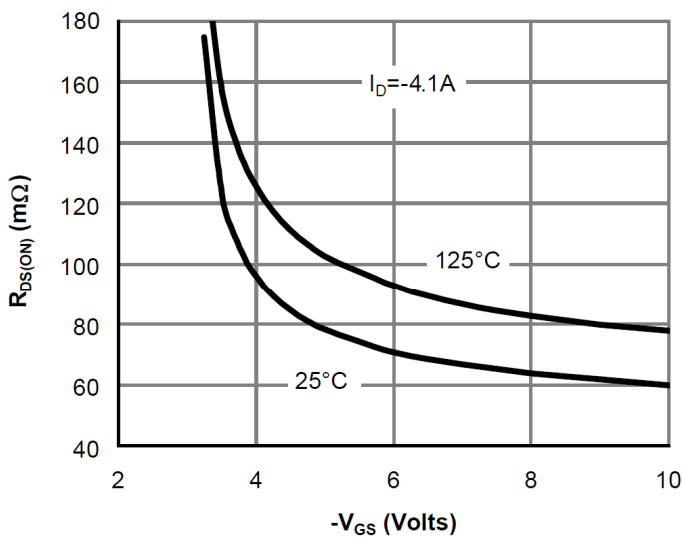


Figure 5: On-Resistance vs. Gate-Source Voltage

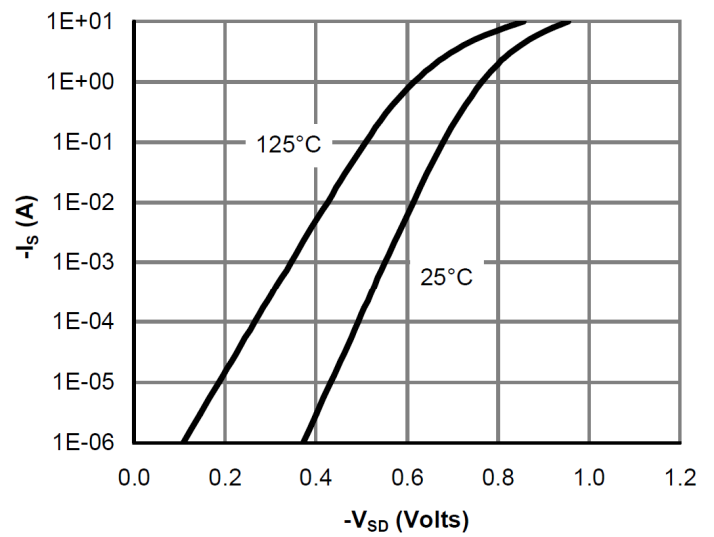


Figure 6: Body-Diode Characteristics



### Characteristics Curve

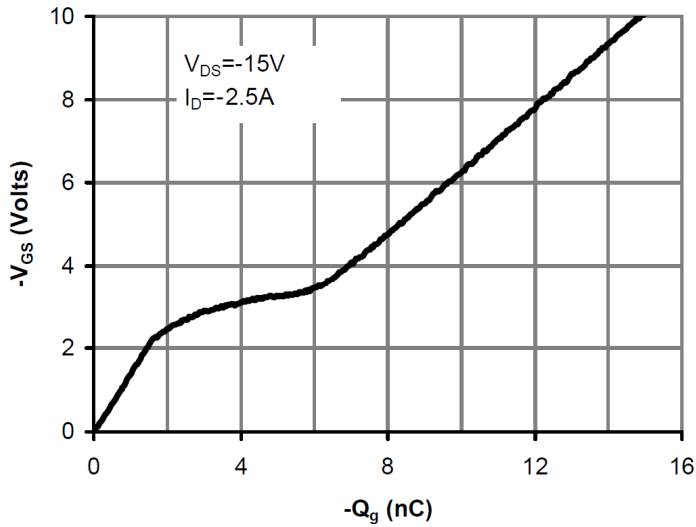


Figure 7: Gate-Charge Characteristics

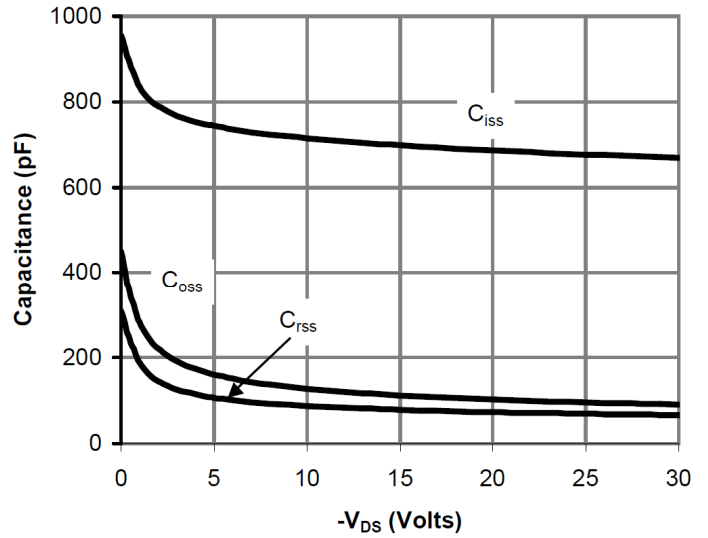


Figure 8: Capacitance Characteristics

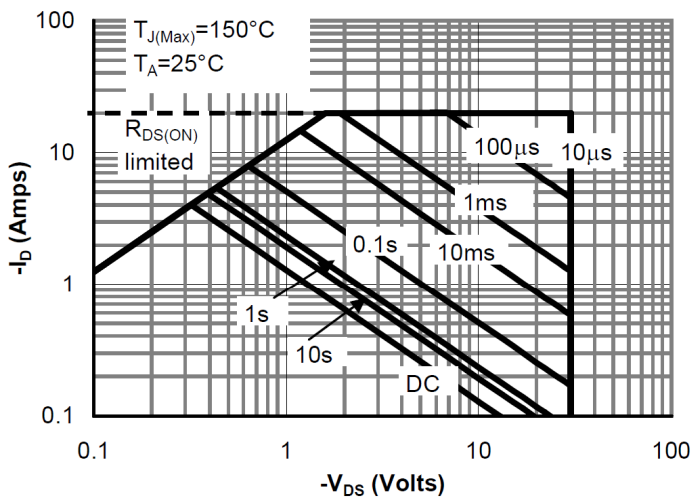


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

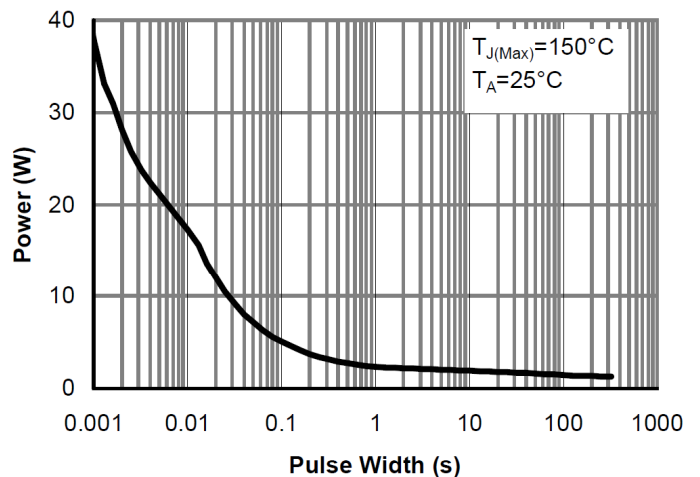


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

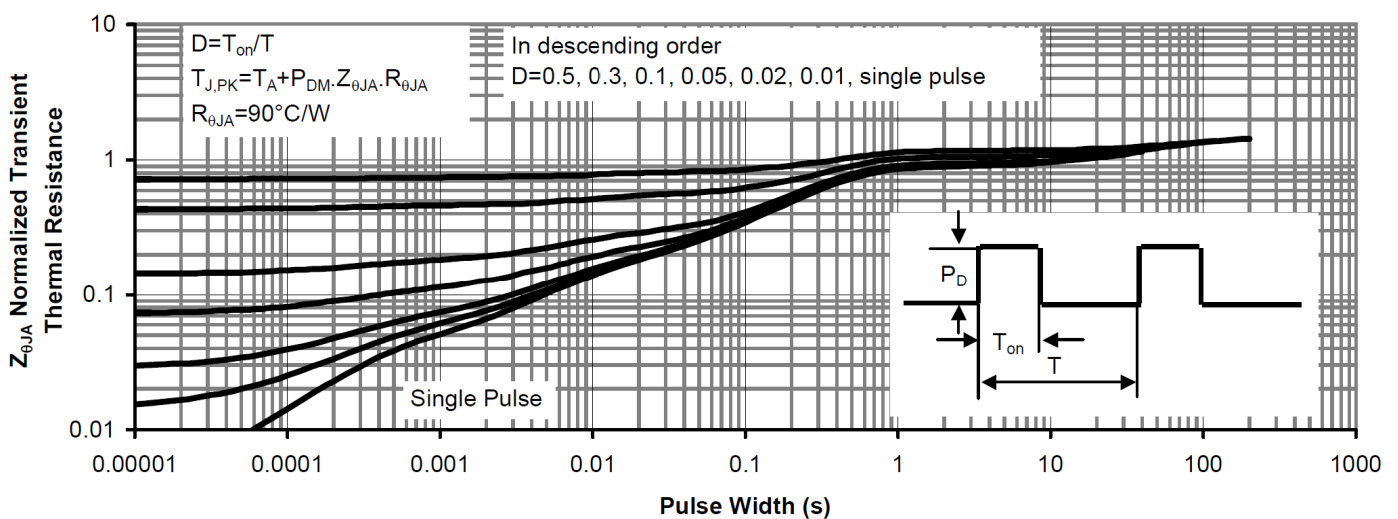


Figure 11: Normalized Maximum Transient Thermal Impedance



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