Dual High-Efficiency PWM Step-Down DC/DC Converter

GENERAL DESCRIPTION

The MT3820 is a dual high-efficiency Pulse-Width-Modulated (PWM) step-down DC/DC converter. It is capable of delivering 1.2A output current over a wide input voltage range from 2.4V to 5.5V, the MT3820 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and other handheld devices. Two operational modes are available. PWM/Low-Dropout auto-switch and shutdown modes. Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application.

The MT3820 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper PMOS. The MT3820 enter shutdown Mode And consumes less than 0.1μA when EN pin is pulled low.

FEATURES

- High Efficiency: Up to 96%
- 1.5MHz Constant Frequency Operation
- 1.2A Output Current
- No Schottky Diode Required
- 2.4V to 5.5V Input Voltage Range
- Output Voltage as Low as 0.6V
- Low Quiescent Current: 30μA
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- <1μA Shutdown Current
- Small 12-Lead WDFN package

APPLICATIONS

- Cellular and Smart Phones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Digital Still and Video Cameras

Typical Application

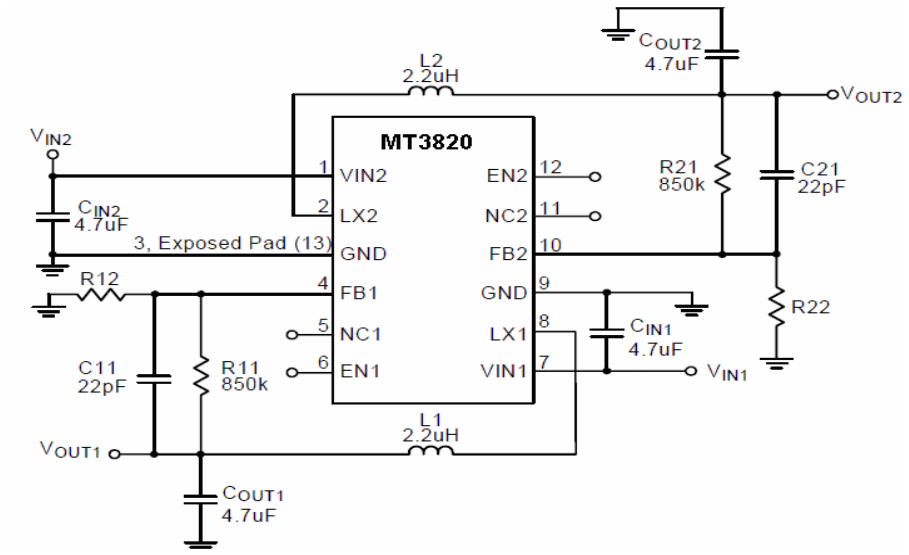
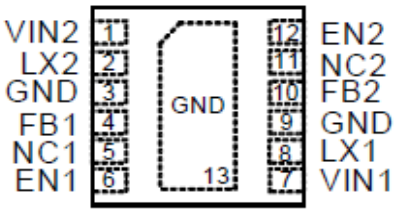


Figure 1. Basic Application Circuit

Package/Order Information

(TOP VIEW)



WDFN-12L 3x3

Part Number	SWICHING FREQUENCY	Temp Range	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)
MT3820-ADJ	1.5MHz	-40°C to +85°C	ADJ	1.2

Pin Description

PIN	NAME	FUNCTION
1	VIN2	Power Input of Channel2
2	LX2	Pin for Switching of Channel2
3,9,EP	GND	Ground,The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	FB1	Feedback of Channel1
5,11	NC1,NC2	No connection
6	EN1	Chip Enable of Channel1
7	VIN1	Power Input of Channel1
8	LX1	Pin for Switching of Channel1
10	FB2	Feedback of Channel2
12	EN2	Chip Enable of Channel2

Absolute Maximum Ratings

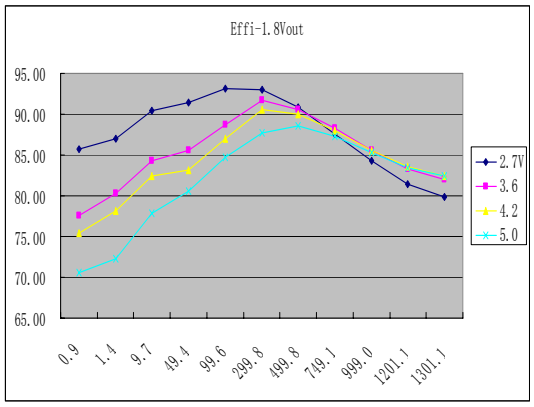
VINx Voltage …… -0.3V to 6V
ENx,FBx Voltages……-0.3 to (Vin+0.3V)
LXx Voltage ……-0.3V to (Vin+0.3V)
Operating Temperature Range … -40°C to +85°C
Lead Temperature(Soldering,10s)……....+260°C
Storage Temperature Range .….-65°C to 150°C

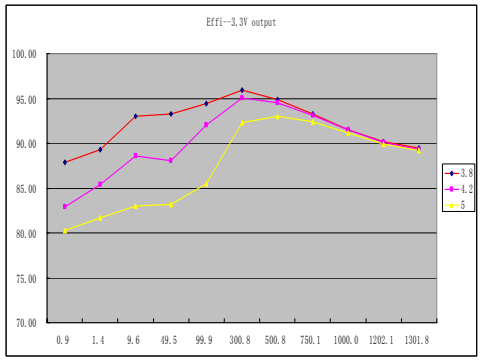
Electrical Characteristics

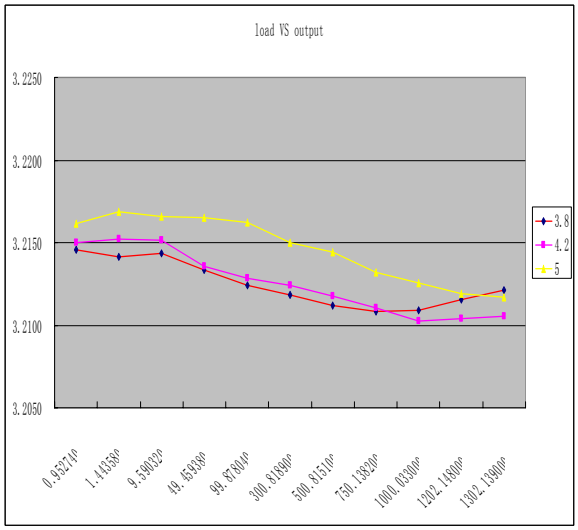
(Vin=3.6V,Vout=1.8V,L=2.2uH, Cin=4.7uF, Cout=10uF, Ta=25oC)

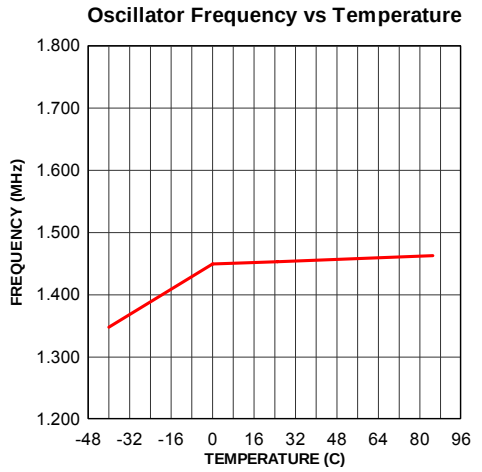
Parameter	Conditions	MIN	TYP	MAX	unit
Channel1 and Channel2					
Input Voltage Range		2.4		5.5	
UVLO Threshold		1.7	1.8	1.9	V
Input DC Supply Current	(Note 4)				μA
PWM Mode	Vout = 90%, Iload=0mA		140	200	μA
PFM Mode	Vout = 105%, Iload=0mA		30	60	μA
Shutdown Mode	V_{RUN} = 0V, V_{IN}=4.2V		0.1	1.0	μA
Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
	T_A = 0°C ≤ T_A ≤ 85°C	0.586	0.600	0.613	V
	T_A = -40°C ≤ T_A ≤ 85°C	0.585	0.600	0.615	V
Reference Voltage Line Regulation	Vin=2.4V to 5.5V		0.04	0.40	%/V
Output Voltage Line Regulation	V_{IN} = 2.4V to 5.5V		0.04	0.4	%
Output Voltage Load Regulation			0.5		%
Oscillation Frequency	Vout=100%		1.5		MHz
	Vout=0V		300		KHz
On Resistance of PMOS	I_{SW}=100mA		0.15	0.22	Ω
ON Resistance of NMOS	I_{SW}=-100mA		0.12	0.2	Ω
Peak Current Limit	V_{IN}= 3V, Vout=90%		2		A
EN Threshold		0.40	1.0	1.50	V
EN Leakage Current			±0.01	±0.1	μA
LX Leakage Current	V_{RUN}=0V,V_{IN}=Vsw=3.6V		±0.01	±1.0	μA

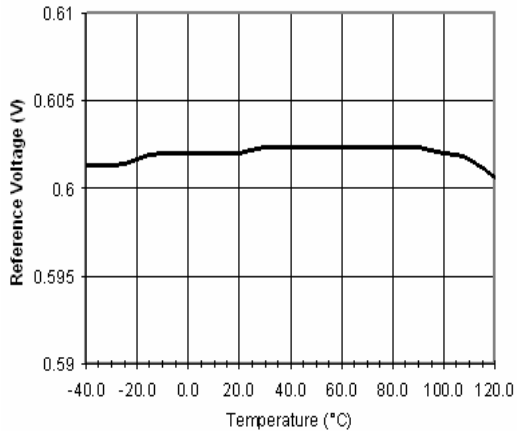
Typical Performance Characteristics

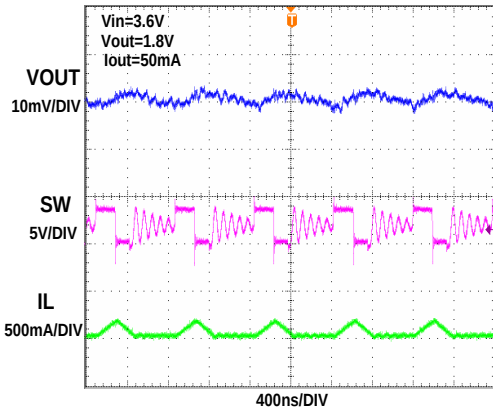




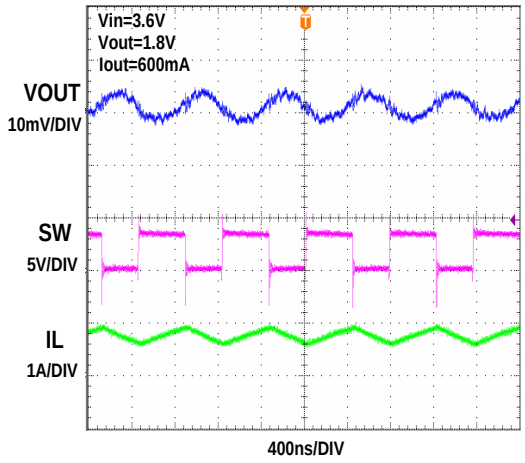




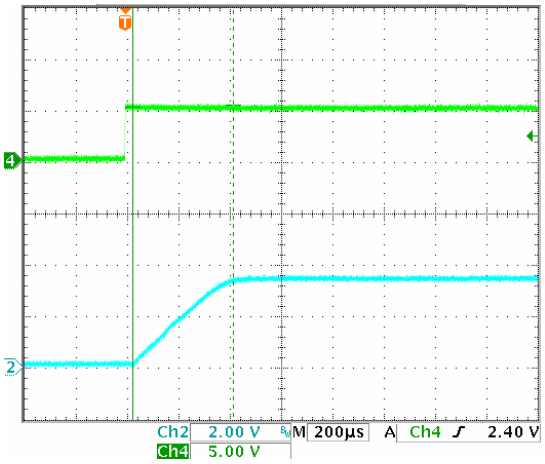




PFM MODE

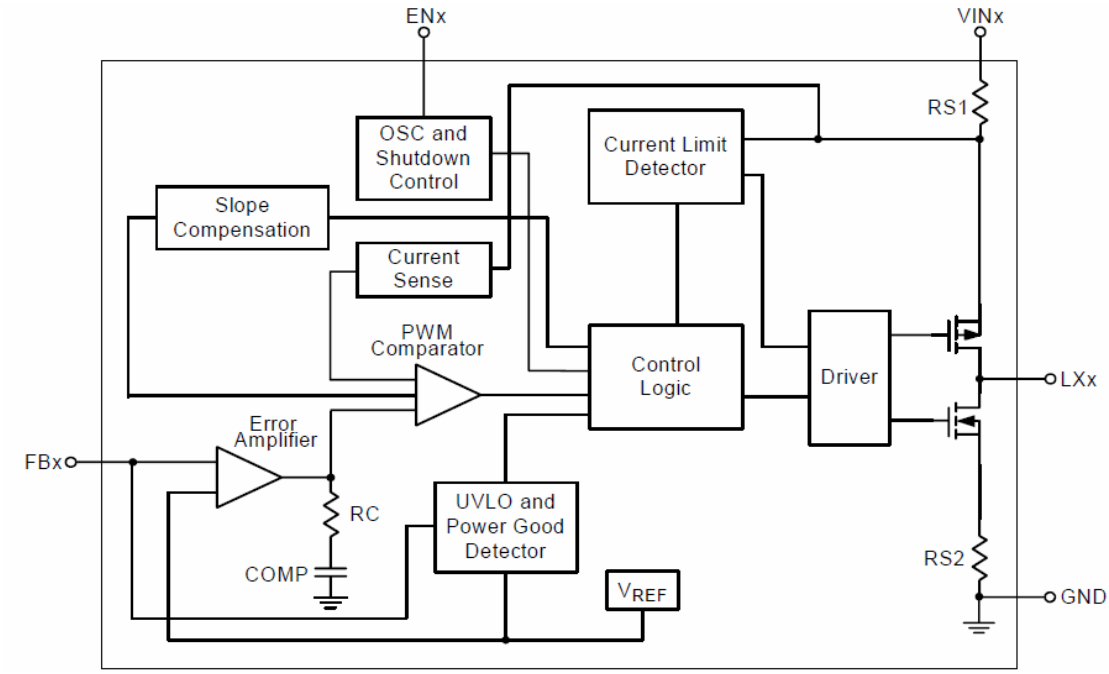


PWM MODE



Start up

Functional Block Diagram



Functional Description

The MT3820 is a high output current monolithic switch mode step-down DC-DC converter. The device operates at a fixed 1.5MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 1.2A output current at VIN = 3V and has an input voltage range from 2.4V to 5.5V. It minimizes external component size and optimizes efficiency at the heavy load range. The slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1μH to 4.7μH) with lower DCR can be used to achieve higher efficiency. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. The fixed output version requires only three external power components (CIN, COUT, and L). The adjustable version can be programmed with external feedback to any voltage, ranging from 0.6V to near the input voltage. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6V. At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the low RDS(ON) drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation. Internal soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

APPLICATIONS INFORMATION

Inductor Selection

For most designs, the MT3820 operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor Ripple Current.

Large value inductors result in lower ripple current and small value inductors result in high ripple current. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{osc} \times C3} \right)$$

A 10μF ceramic can satisfy most applications.

PC Board Layout Checklist

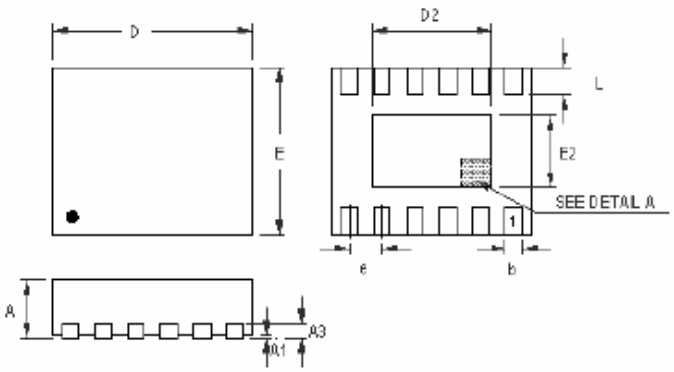
When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the MT3820:

1. The exposed pad (EP) must be reliably soldered to the GND plane. A PGND pad below EP is strongly recommended.
2. The power traces, including the GND trace, the LX trace and the IN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several VIA pads when routing between layers.
3. The input capacitor (C1) should connect as closely as possible to IN and AGND to get good power filtering.
4. Keep the switching node, LX away from the sensitive FB node.
5. The feedback trace or OUT pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin to minimize the length of the high impedance feedback trace.
6. The output capacitor C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as

short as possible and there should not be any signal lines under the inductor.

7. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.400	1.750	0.055	0.069
e	0.450		0.018	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package