# VRAM

# 64K x 4 DRAM WITH 256 x 4 SAM



## FEATURES

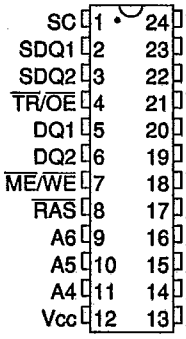
- Industry standard pinout, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, and HIDDEN
- 256-cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port
  256 x 4 SAM port
- Bit MASKED WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 15mW standby; 250mW active, typical
- Fast access times – 100ns parallel, 33ns serial

## OPTIONS

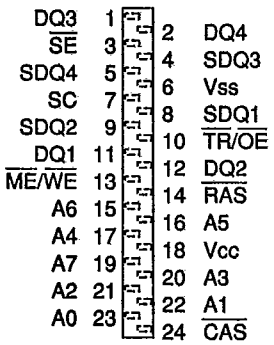
| | MARKING |
|---|---|
| • Timing (DRAM, SAM) | |
| 100ns, 33ns | -10 |
| 120ns, 40ns | -12 |
| 150ns, 60ns | -15 |
| • Packages | |
| Plastic DIP (400 mil) | None |
| Ceramic DIP (400 mil) | C |
| Plastic ZIP | Z |

## PIN ASSIGNMENT (Top View)

**24-Pin DIP (A-8, B-8)**




**24-Pin ZIP (C-4)**




## GENERAL DESCRIPTION

The MT42C4064 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 262,144 bits. They may be accessed by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4067 (64K x 4) bit DRAM. Four 256-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address-decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 256 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

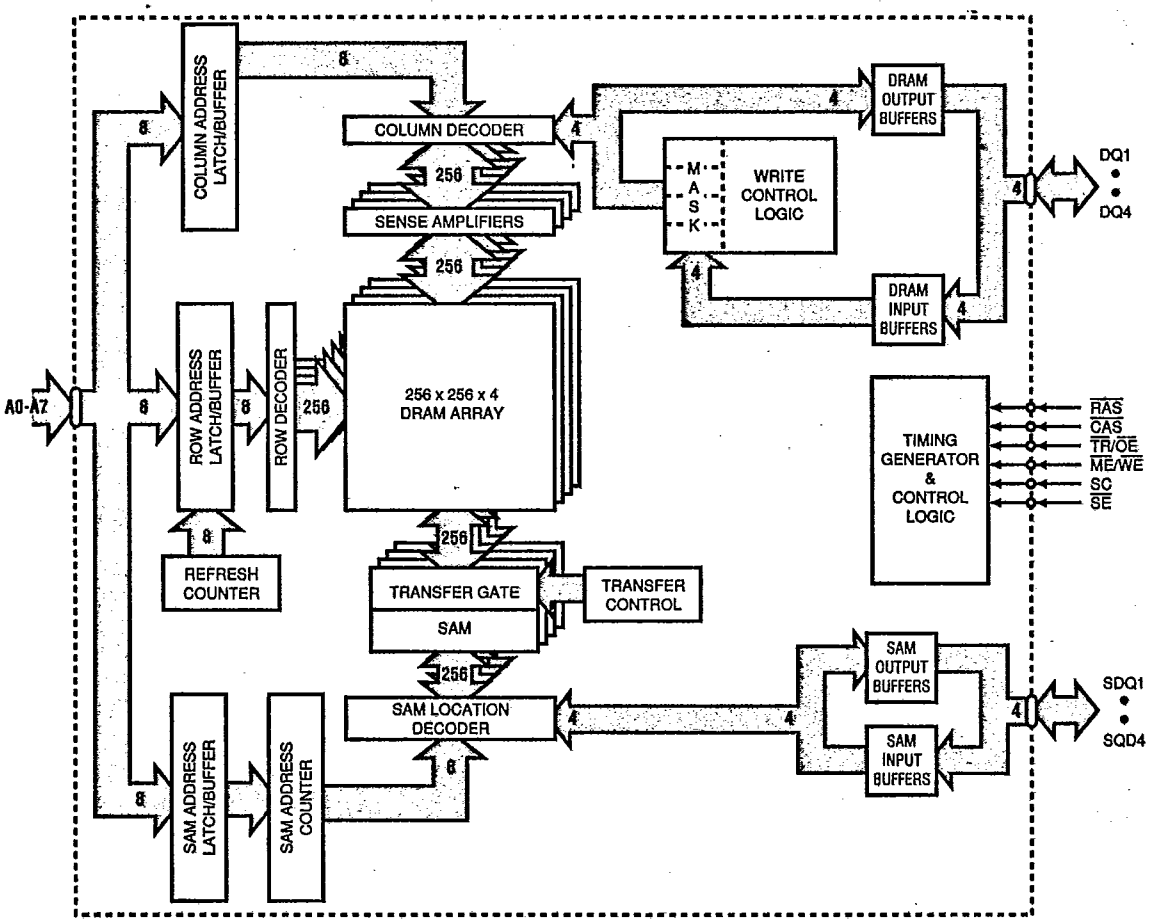



**Figure 1**
**MT42C4064 BLOCK DIAGRAM**

## PIN DESCRIPTIONS

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| DIP PIN NUMBER(S) | ZIP PIN NUMBER(S) | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | 7 | SC | Input | Serial Clock: Clock input to the serial address counter for the SAM registers. |
| 4 | 8, 9, 4, 5 | $\overline{TR/OE}$ | Input | Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or<br>Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW); otherwise, the output buffers are in a High-Z. |
| 7 | 13 | $\overline{ME/WE}$ | Input | Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or<br>Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = H) or WRITE ($\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ($\overline{WE}$ = H) or SAM- TO-DRAM TRANSFER ($\overline{WE}$ = L). |
| 8 | 14 | $\overline{RAS}$ | Input | Row Address Strobe: $\overline{RAS}$ is used to clock in the 8 row-address bits and as a strobe for the MASK ENABLE and TRANSFER functions. |
| 9, 10, 11, 13, 14, 15, 16, 17 | 23, 22, 21, 20 17, 16, 15, 19 | A0 to A7 | Input | Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 64K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW). |
| 18 | 24 | $\overline{CAS}$ | Input | Column Address Strobe: $\overline{CAS}$ is used to clock in the 8 column-address bits and enable the DRAM output buffers ($\overline{TR/OE}$ must also be LOW). |
| 21 | 3 | $\overline{SE}$ | Input | Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state.$\overline{SE}$ is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL-INPUT-MODE ENABLE cycle is performed. |
| 5, 6, 19, 20 | 11,12,1,2 | DQ1 - DQ4 | Input/ Output | DRAM Data I/O: Inputs, Outputs, or High-Z, and/or Mask Data Inputs: For MASKED WRITE cycle only. |
| 2, 3, 22, 23 | 8,9,4,5 | SDQ1 - SDQ4 | Input/ Output | Serial Data I/O: Input, Output, or High-Z. |
| 12 | 18 | Vcc | Supply | Power Supply: +5V ±10% |
| 24 | 6 | Vss | Supply | Ground |

## FUNCTIONAL DESCRIPTION

The VRAM can be divided into three functional blocks (see Figure 1); the DRAM, the transfer control circuitry, and the serial access memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet, and are summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

## DRAM OPERATION

The DRAM portion of the VRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion.

### READ/WRITE Cycles

The 16 address bits that are used to select a 4-bit word from the 65,536 available are latched into the chip using the A0 -A7, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 8 row-address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column-address bits are set up on the address inputs and clocked-in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between an internal transfer operation and a DRAM operation. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for a DRAM port READ or WRITE operation.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The $(\overline{TR})/\overline{OE}$ input must be LOW to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the VRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For a normal DRAM WRITE operation, $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. $(\overline{ME})/\overline{WE}$ is a "don't care" at the $\overline{RAS}$ HIGH to LOW transition for a DRAM READ cycle.

If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If $\overline{ME}/(\overline{WE})$ is LOW when $\overline{RAS}$ goes LOW, the input data will be "masked" before being stored in the DRAM.

The VRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

### REFRESH

The MT42C4064 supports $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN types of refresh cycles. All 256 row-address combinations must be accessed within 4ms. For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode, the row addresses are generated internally and the user need not supply them as he must in $\overline{RAS}$ ONLY refresh. $\overline{TR}/(\overline{OE})$ must be HIGH when $\overline{RAS}$ goes LOW for the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

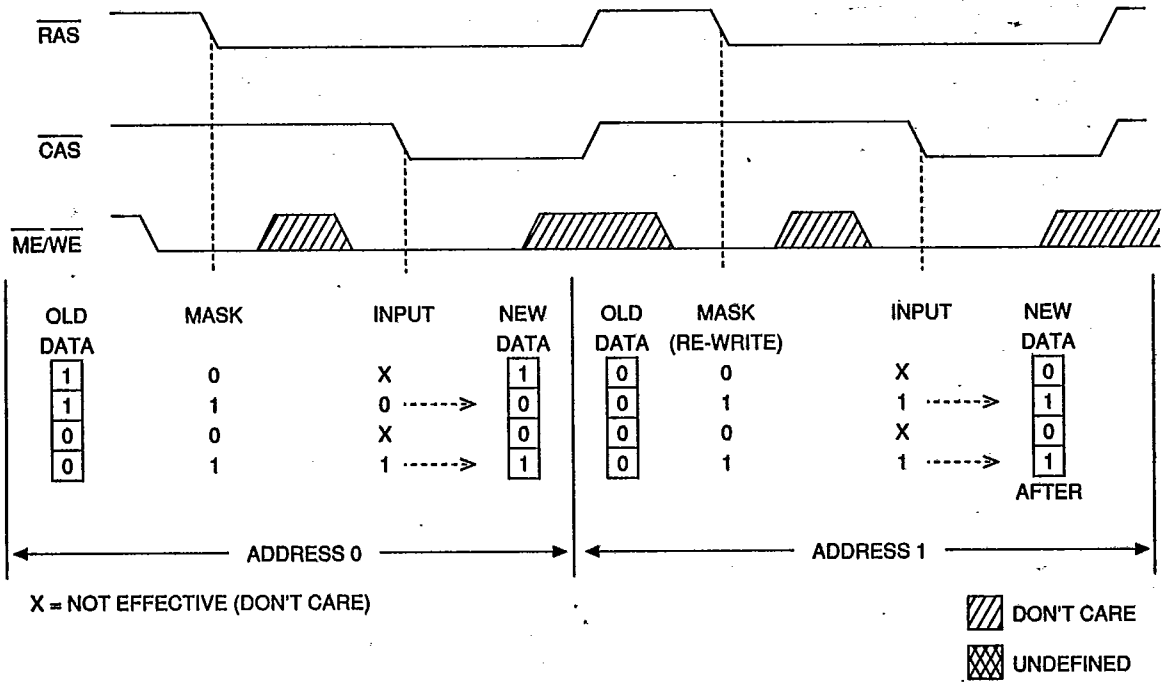


**Figure 2**
**MT42C4064 MASKED WRITE**

### MASKED WRITE

If $\overline{ME}$/($\overline{WE}$) is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1 - DQ4 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASKED WRITE cycle, new mask data must be supplied at the beginning of each MASKED WRITE cycle. An example of a typical MASKED WRITE cycle is shown in Figure 2.

## TRANSFER OPERATION

### DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when $\overline{TR}/(\overline{OE})$ is LOW at $\overline{RAS}$ (HIGH to LOW) time. $(\overline{ME})/\overline{WE}$ indicates the direction of the transfer and must be HIGH as $\overline{RAS}$ goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256-bit DRAM rows that are to be transferred to the four SAM data registers, and the column address bits indicate the start address, or Tap, of the next SERIAL OUTPUT cycle from the SAM data registers. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the address bits into the part. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. There must be no rising edges on the serial clock (SC) input while a normal READ TRANSFER is taking place (refer to the AC timing diagrams for READ TRANSFER). A REAL-TIME READ-TRANSFER cycle is the only time when SC must be synchronized with the DRAM $\overline{RAS}$ and $\overline{CAS}$ timing (by using $\overline{TR}/(\overline{OE})$ is to fire the TRANSFER, LOW to HIGH transition). See the REAL-TIME READ-TRANSFER AC timing waveforms. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation.

### SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the Tap address of the next SERIAL INPUT cycle for the SAM data registers. If $\overline{SE}$ is HIGH when $\overline{RAS}$ goes LOW, a SERIAL-INPUT-MODE ENABLE cycle is performed.

## SAM OPERATION

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### SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER, the SAM port will be in the serial input mode.

### SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL-INPUT-MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

### SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the tap start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the serial address register contents, which was loaded when the serial input mode were enabled, will determine the serial address to which the first bit will be written. $\overline{SE}$ acts as an enable for serial data input and must be LOW for normal serial input. If $\overline{SE}$ is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every L → H transition of SC, regardless of the logic level on the $\overline{SE}$ input.

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## TRUTH TABLE

**DRAM Operations (SC, $\overline{SE}$, and SDQ1 — SDQ4 are "don't care")**

| Function | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{ME}/\overline{WE}$ | | $\overline{TR}/\overline{OE}$ | | Addresses | | DQ1 to DQ4 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | tR* | tC* | tR* | tC* | tR* | tC* | | |
| Standby | H | H | X | X | X | X | X | X | High-Z | |
| READ | L | L | X | H | H | H→L | ROW | COL | Data Out | |
| WRITE (EARLY-WRITE) | L | L | H | L | H | X | ROW | COL | Data In | 1 |
| MASKED WRITE | H→L | L | L | L | H | X | ROW | COL | Mask Data In, Valid Data In | |
| READ-WRITE | L | L | H | H→L | H | L→H | ROW | COL | Valid Data Out | 1 |
| PAGE-MODE READ | L | H→L→H, H→L→H | H | H | H | H→L | ROW | COL | Valid Data Out | |
| PAGE-MODE WRITE | L | H→L→H, H→L→H | H | L | H | X | ROW | COL | Valid Data In | |
| PAGE-MODE READ-WRITE | L | H→L→H, H→L→H | H | H→L | H | L→H | ROW | COL | Valid Data Out, Valid Data In | 1 |
| $\overline{RAS}$-ONLY REFRESH | L | H | X | n/a | H | n/a | ROW | n/a | High-Z | |
| HIDDEN REFRESH | L→H→L | L | X | H | X | L | ROW | COL | Valid Data Out | |
| $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH | H→L | L | X | X | X | X | X | X | High-Z | * |

**TRANSFER Operations (DQ1 — DQ4 are "don't care")**

| Function | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{ME}/\overline{WE}$ | | $\overline{TR}/\overline{OE}$ | | Addresses | | SC | $\overline{SE}$ | SDQ1 to SDQ4 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | tR* | tC* | tR* | tC* | tR* | tC* | | | | |
| DRAM-TO-SAM TRANSFER | L | L | H | X | L | L | ROW | TAP** | X | X | X | 2 |
| SAM-TO-DRAM TRANSFER | L | L | L | X | L | X | ROW | TAP** | X | L | X | 3 |
| SERIAL-INPUT-MODE ENABLE | L | L | L | X | L | X | ROW | TAP** | X | H | X | 4 |

* tR = when $\overline{RAS}$ goes from HIGH to LOW
tC = when $\overline{CAS}$ goes from HIGH to LOW
** TAP = Tap Address, the serial address to which the next serial input or output cycle will start.

**Notes:**
1. Any type of WRITE cycle may also be a MASKED WRITE cycle.
2. The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO- SAM TRANSFER.
3. The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
4. The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

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## TRUTH TABLE

**Serial I/O Operations ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$, and DQ1 - DQ4 are "don't care")**

| Function | SC | $\overline{SE}$ | SDQ1 — SDQ4 | Notes |
|---|---|---|---|---|
| SERIAL OUTPUT | L→H | L | Valid Data Out | 5 |
| SERIAL INPUT | L→H | L | Valid Data In | 6 |

**Notes:** 5. The SAM must be in the SERIAL OUTPUT mode.
6. The SAM must be in the SERIAL INPUT mode.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 W
Short Circuit Output Current .....50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V | 1 |
| Input High (Logic 1) Voltage, All Inputs | $V_{IH}$ | 2.4 | Vcc+1 | V | 1 |
| Input Low (Logic 0) Voltage, All Inputs | $V_{IL}$ | -1.0 | 0.8 | V | 1 |

## DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| INPUT LEAKAGE CURRENT<br>(any input (0V≤VIN≤Vcc), all other pins not under test = 0V). | $I_L$ | -10 | 10 | µA | |
| OUTPUT LEAKAGE CURRENT<br>(DQ, SDQ disabled, 0V≤VOUT≤Vcc). | $I_{OZ}$ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -5mA) | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 5mA) | $V_{OL}$ | | 0.4 | V | 1 |

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## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A7 | $C_{I1}$ | | 5 | pF | 18 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, SC, $\overline{SE}$ | $C_{I2}$ | | 7 | pF | 18 |
| Output Capacitance: DQ, SDQ | $C_O$ | | 7 | pF | 18 |

## CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER/CONDITION OF DRAM | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; $^tRC = {}^tRC$ (MIN)). | $I_{CC1}$ | | 40 | mA | |
| OPERATING CURRENT: PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling; $^tPC = {}^tPC$ (MIN)). | $I_{CC2}$ | | 40 | mA | |
| STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles MIN). | $I_{CC3}$ | | 10 | mA | |
| STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS}$ = Vcc-0.2V after 8 $\overline{RAS}$ cycles MIN. All other inputs at Vcc-0.2V or Vss + 0.2V). | $I_{CC4}$ | | 4 | mA | |
| REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$). | $I_{CC5}$ | | 30 | mA | |
| REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling). | $I_{CC6}$ | | 30 | mA | 22 |
| SAM/DRAM DATA TRANSFER | $I_{CC7}$ | | 60 | mA | |

## CURRENT DRAIN, SAM ACTIVE ($^tSC$ = MIN)

(Notes 2, 3) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

| PARAMETER/CONDITION OF DRAM | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; $^tRC = {}^tRC$ (MIN)). | $I_{CC8}$ | | 60 | mA | |
| OPERATING CURRENT: PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling; $^tPC = {}^tPC$ (MIN)). | $I_{CC9}$ | | 60 | mA | |
| STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles MIN). | $I_{CC10}$ | | 30 | mA | |
| STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS}$ = Vcc-0.2V after 8 $\overline{RAS}$ cycles MIN. All other inputs at Vcc-0.2V or Vss + 0.2V). | $I_{CC11}$ | | 25 | mA | |
| REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS} = V_{IH}$). | $I_{CC12}$ | | 50 | mA | |
| REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling). | $I_{CC13}$ | | 50 | mA | 22 |
| SAM/DRAM DATA TRANSFER | $I_{CC14}$ | | 90 | mA | |

## DRAM TIMING PARAMETERS

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 10, 11, 17) (0°C ≤ $T_A$ ≤ + 70°C; Vcc = 5.0V ± 10%)

| A.C. CHARACTERISTICS | | -10 | | -12 | | -15 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Random READ or WRITE cycle time | $^tRC$ | 190 | | 220 | | 260 | | ns | |
| READ-MODIFY-WRITE cycle time | $^tRWC$ | 250 | | 295 | | 345 | | ns | 20, 21 |
| PAGE-MODE READ or WRITE cycle time | $^tPC$ | 75 | | 90 | | 110 | | ns | 6 |
| PAGE-MODE READ-MODIFY-WRITE cycle time | $^tPRWC$ | 125 | | 150 | | 175 | | ns | 20, 21 |
| Access time from $\overline{RAS}$ | $^tRAC$ | | 100 | | 120 | | 150 | ns | 7, 8 |
| Access time from $\overline{CAS}$ | $^tCAC$ | | 50 | | 60 | | 75 | ns | 7, 9 |
| $\overline{RAS}$ pulse width | $^tRAS$ | 100 | 10,000 | 120 | 10,000 | 150 | 10,000 | ns | |
| $\overline{RAS}$ pulse width (PAGE MODE) | $^tRASP$ | 100 | 100,000 | 120 | 100,000 | 150 | 100,000 | ns | |
| $\overline{RAS}$ hold time | $^tRSH$ | 50 | | 60 | | 75 | | ns | |
| $\overline{RAS}$ precharge time | $^tRP$ | 80 | | 90 | | 100 | | ns | |
| $\overline{CAS}$ pulse width | $^tCAS$ | 50 | 10,000 | 60 | 10,000 | 75 | 10,000 | ns | |
| $\overline{CAS}$ hold time | $^tCSH$ | 100 | | 120 | | 150 | | ns | |
| $\overline{CAS}$ precharge time | $^tCPN$ | 15 | | 20 | | 25 | | ns | |
| $\overline{CAS}$ precharge time (PAGE MODE) | $^tCP$ | 15 | | 20 | | 25 | | ns | 19 |
| $\overline{RAS}$ to $\overline{CAS}$ delay | $^tRCD$ | 15 | 50 | 15 | 60 | 15 | 75 | ns | 13 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $^tCRP$ | 10 | | 10 | | 10 | | ns | |
| Row address setup time | $^tASR$ | 0 | | 0 | | 0 | | ns | |
| Row address hold time | $^tRAH$ | 15 | | 15 | | 15 | | ns | |
| Column address setup time | $^tASC$ | 0 | | 0 | | 0 | | ns | |
| Column address hold time | $^tCAH$ | 20 | | 20 | | 25 | | ns | |
| Column address hold time (referenced to $\overline{RAS}$) | $^tAR$ | 45 | | 70 | | 80 | | ns | |
| READ command setup time | $^tRCS$ | 0 | | 0 | | 0 | | ns | |
| READ command hold time (referenced to $\overline{CAS}$) | $^tRCH$ | 0 | | 0 | | 0 | | ns | 14 |
| READ command hold time (referenced to $\overline{RAS}$) | $^tRRH$ | 0 | | 0 | | 0 | | ns | |
| $\overline{WE}$ command setup time | $^tWCS$ | 0 | | 0 | | 0 | | ns | 16 |
| WRITE command hold time | $^tWCH$ | 20 | | 25 | | 30 | | ns | |
| WRITE command hold time (referenced to $\overline{RAS}$) | $^tWCR$ | 70 | | 80 | | 90 | | ns | |
| WRITE command pulse width | $^tWP$ | 20 | | 25 | | 30 | | ns | |
| WRITE command to $\overline{RAS}$ lead time | $^tRWL$ | 25 | | 30 | | 35 | | ns | |
| WRITE command to $\overline{CAS}$ lead time | $^tCWL$ | 25 | | 30 | | 35 | | ns | |
| Data-in setup time | $^tDS$ | 0 | | 0 | | 0 | | ns | 15 |
| Data-in hold time | $^tDH$ | 15 | | 20 | | 25 | | ns | 15 |
| Data-in hold time (referenced to $\overline{RAS}$) | $^tDHR$ | 70 | | 80 | | 90 | | ns | |
| $\overline{CAS}$ to $\overline{WE}$ delay | $^tCWD$ | 65 | | 80 | | 95 | | ns | 16, 20 |
| $\overline{RAS}$ to $\overline{WE}$ delay | $^tRWD$ | 120 | | 150 | | 185 | | ns | 16, 20 |
| $\overline{ME/WE}$ to $\overline{RAS}$ setup time | $^tWSR$ | 0 | | 0 | | 0 | | ns | |

## DRAM TIMING PARAMETERS (Continued)

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 10, 11, 17) (0°C ≤ $T_A$ ≤ + 70°C; Vcc = 5.0V ± 10%)

| A.C. CHARACTERISTICS | | -10 | | -12 | | -15 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| ME/WE to RAS Hold Time | $t_{RWH}$ | 10 | | 10 | | 15 | ns | | |
| Mask Data (DQ ) to RAS setup time | $t_{MS}$ | 0 | | 0 | | 0 | | ns | |
| Mask Data (DQ ) to RAS hold time | $t_{MH}$ | 20 | | 20 | | 25 | | ns | |
| Transition time (rise or fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| Refresh period (256 cycles) | $t_{REF}$ | | 4 | | 4 | | 4 | ms | |
| RAS to CAS precharge time | $t_{RPC}$ | | 0 | | 0 | | 0 | ns | |
| CAS setup time (CAS-BEFORE-RAS REFRESH) | $t_{CSR}$ | 10 | | 10 | | 10 | | ns | |
| CAS hold time (CAS-BEFORE-RAS REFRESH) | $t_{CHR}$ | 20 | | 25 | | 30 | | ns | 22 |
| CAS to output in Low-Z | $t_{CLZ}$ | 5 | | 5 | | 5 | | ns | |
| Output buffer turn-off delay | $t_{OFF}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns | 7, 12 |
| Access time from (TR)/OE | $t_{OE}$ | | 25 | | 25 | | 30 | ns | |
| Output Disable | $t_{OD}$ | 0 | 25 | 0 | 25 | 0 | 30 | ns | |
| Output Disable hold time from start of WRITE | $t_{OEH}$ | | 25 | | 25 | | 30 | ns | |
| Output Enable to RAS delay | $t_{ORD}$ | | 0 | | 0 | | 0 | ns | |

## TRANSFER AND MODE CONTROL TIMING PARAMETERS

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 6, 17) (0° C ≤ $T_A$ ≤ + 70°C; Vcc = 5.0V ± 10%)

| A.C. CHARACTERISTICS | | -10 | | -12 | | -15 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| TRANSFER command to $\overline{RAS}$ setup time | $^tTS$ | 0 | | 0 | | 0 | | ns | 23 |
| TRANSFER command to $\overline{RAS}$ hold time | $^tRTH$ | 80 | | 90 | | 100 | | ns | 23 |
| TRANSFER command to $\overline{CAS}$ hold time | $^tCTH$ | 30 | | 30 | | 35 | | ns | 23 |
| TRANSFER command to SC lead time | $^tTSL$ | 5 | | 5 | | 10 | | ns | 23 |
| TRANSFER command to $\overline{RAS}$ lead time | $^tTRL$ | 10 | | 10 | | 10 | | ns | 23 |
| TRANSFER command to $\overline{RAS}$ delay time | $^tTRD$ | 15 | | 15 | | 20 | | ns | 23 |
| TRANSFER command to $\overline{CAS}$ time | $^tTCL$ | 10 | | 10 | | 10 | | ns | 23 |
| TRANSFER command to $\overline{CAS}$ delay time | $^tTCD$ | 15 | | 15 | | 20 | | ns | 23 |
| First SC edge to TRANSFER command delay time | $^tTSD$ | 10 | | 10 | | 20 | | ns | 23 |
| $\overline{CAS}$ to first SC delay | $^tRSD$ | | 95 | | 105 | | 115 | ns | |
| RAS to first SC delay | $^tCSD$ | | 25 | | 35 | | 45 | ns | |
| SAM-TO-DRAM (WRITE) transfer command to $\overline{RAS}$ hold time | $^tRTHW$ | 15 | | 15 | | 15 | | ns | |
| Serial output buffer turn-off delay from $\overline{RAS}$ | $^tSDZ$ | 10 | 40 | 10 | 50 | 10 | 60 | ns | |
| SC to $\overline{RAS}$ setup time | $^tSRS$ | 35 | | 40 | | 45 | | ns | |
| $\overline{RAS}$ to SC delay time | $^tSRD$ | 25 | | 30 | | 35 | | ns | |
| Serial data input to SE delay time | $^tSZE$ | 0 | | 0 | | 0 | | ns | |
| $\overline{RAS}$ to SD buffer turn-on time | $^tSRO$ | 0 | | 0 | | 0 | | ns | |
| Serial data input delay from $\overline{RAS}$ | $^tSDD$ | 50 | | 55 | | 60 | | ns | |
| Serial data input to $\overline{RAS}$ delay time | $^tSZS$ | 0 | | 0 | | 0 | | ns | |
| SERIAL INPUT MODE ENABLE ($\overline{SE}$) to $\overline{RAS}$ setup time | $^tESR$ | 0 | | 0 | | 0 | | ns | |
| SERIAL INPUT MODE ENABLE ($\overline{SE}$) to $\overline{RAS}$ hold time | $^tREH$ | 15 | | 15 | | 15 | | ns | |
| NONTRANSFER command to $\overline{RAS}$ setup time | $^tYS$ | 0 | | 0 | | 0 | | ns | 24 |
| NONTRANSFER command to $\overline{RAS}$ hold time | $^tYH$ | 15 | | 15 | | 20 | | ns | 24 |

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## SAM TIMING PARAMETERS

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

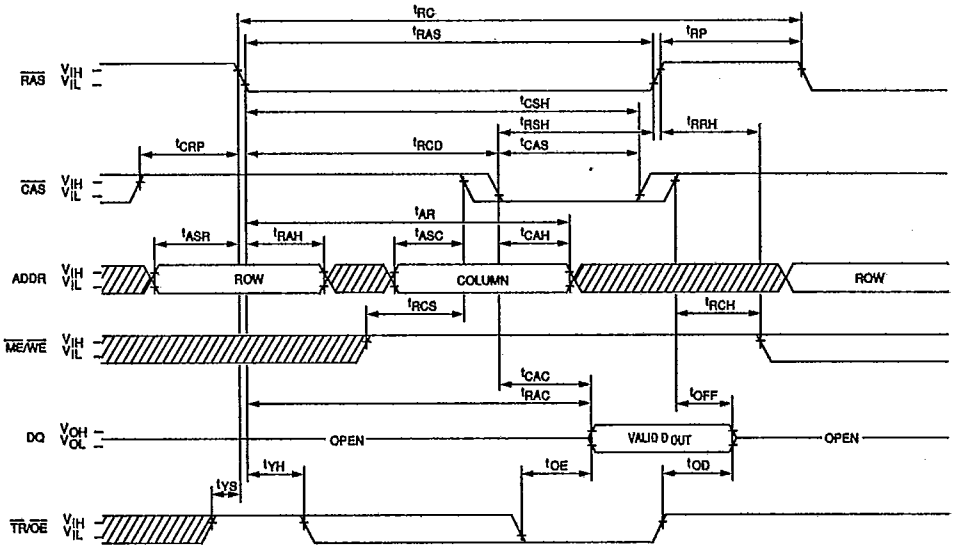
(Notes 3, 4, 5, 17, 25) (0° C ≤ $T_A$ ≤ + 70°C, Vcc = 5.0V ± 10%)

| A.C. CHARACTERISTICS | | -10 | | -12 | | -15 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Serial clock cycle time | $t_{SC}$ | 33 | 50000 | 40 | 50000 | 60 | 50000 | ns | |
| Access time from SC | $t_{SAC}$ | | 33 | | 40 | | 60 | ns | 25 |
| SC precharge time | $t_{SP}$ | 10 | | 10 | | 20 | | ns | |
| SC pulse width | $t_{SAS}$ | 10 | | 10 | | 20 | | ns | |
| Access time from $\overline{SE}$ | $t_{SEA}$ | | 25 | | 30 | | 40 | ns | 25 |
| $\overline{SE}$ precharge time | $t_{SEP}$ | 10 | | 15 | | 20 | | ns | |
| $\overline{SE}$ pulse width | $t_{SE}$ | 15 | | 15 | | 20 | | ns | |
| Serial data out hold time after SC high | $t_{SOH}$ | 10 | | 10 | | 10 | | ns | 25 |
| Serial output buffer turn off delay from $\overline{SE}$ | $t_{SEZ}$ | 0 | 15 | 0 | 25 | 0 | 30 | ns | 25 |
| Serial data in setup time | $t_{SDS}$ | 0 | | 0 | | 0 | | ns | |
| Serial data in hold time | $t_{SDH}$ | 15 | | 20 | | 25 | | | |
| SERIAL INPUT (Write) Enable setup time | $t_{SWS}$ | 0 | | 0 | | 0 | | ns | |
| SERIAL INPUT (Write) Enable hold time | $t_{SWH}$ | 20 | | 35 | | 45 | | ns | |
| SERIAL INPUT (Write) Disable setup time | $t_{SWIS}$ | 0 | | 0 | | 0 | | ns | |
| SERIAL INPUT (Write) Disable hold time | $t_{SWIH}$ | 20 | | 35 | | 45 | | ns | |

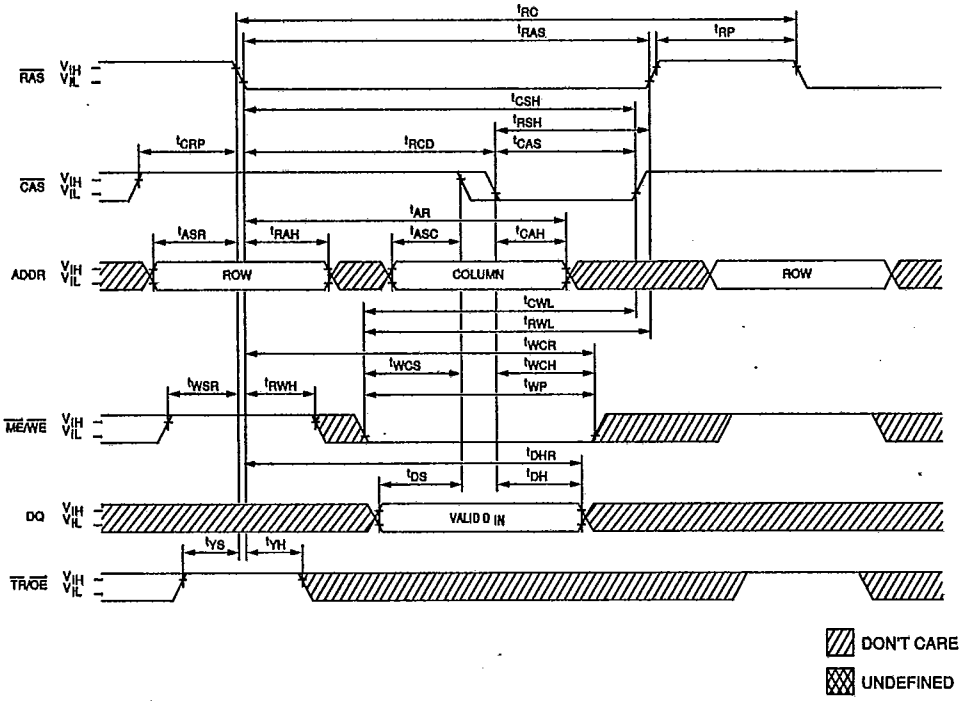
## NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles and 1 SC cycle, before proper device operation is assured. The $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms static refresh require-ment is exceeded.
4. AC characteristics assume $^tT$ = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If $^tRCD$ is greater than the maximum recommended value shown in this table, $^tRAC$ will increase by the amount that $^tRCD$ exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = VIH, DRAM data output is high impedance.
11. If $\overline{CAS}$ = VIL, DRAM data output may contain data from the last valid READ cycle.
12. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, then access time is controlled exclusively by $^tCAC$.
14. $^tRCH$ is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and to $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. $^tWCS$, $^tCWD$ and $^tRWD$ are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (MIN) and $^tRWD \geq ^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate. If $^tWCS \leq ^tWCS$, the cycle is a LATE WRITE [($\overline{ME}$)/$\overline{WE}$ falls after CAS] $^tWCS$, $^tCWD$ and $^tRWD$ do not apply.
17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and Vcc = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for $^tCP$. Note 8 applies to determine valid data out.
20. Includes the $\overline{OE}$ delay time (30ns for the -10, 40ns for the -12, and 50ns for the -15).
21. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH (VIH) DQ goes open. If $\overline{OE}$ is tied permanently LOW a READ-MODIFY-WRITE operation is not possible.
22. Enables on-chip refresh and address counters.
23. TRANSFER command means that $\overline{TR}$/($\overline{OE}$) is LOW when $\overline{RAS}$ goes LOW.
24. NONTRANSFER command means that $\overline{TR}$/($\overline{OE}$) is HIGH when $\overline{RAS}$ goes LOW.
25. Measured with a load equivalent to 2 TTL gates and 50pF.

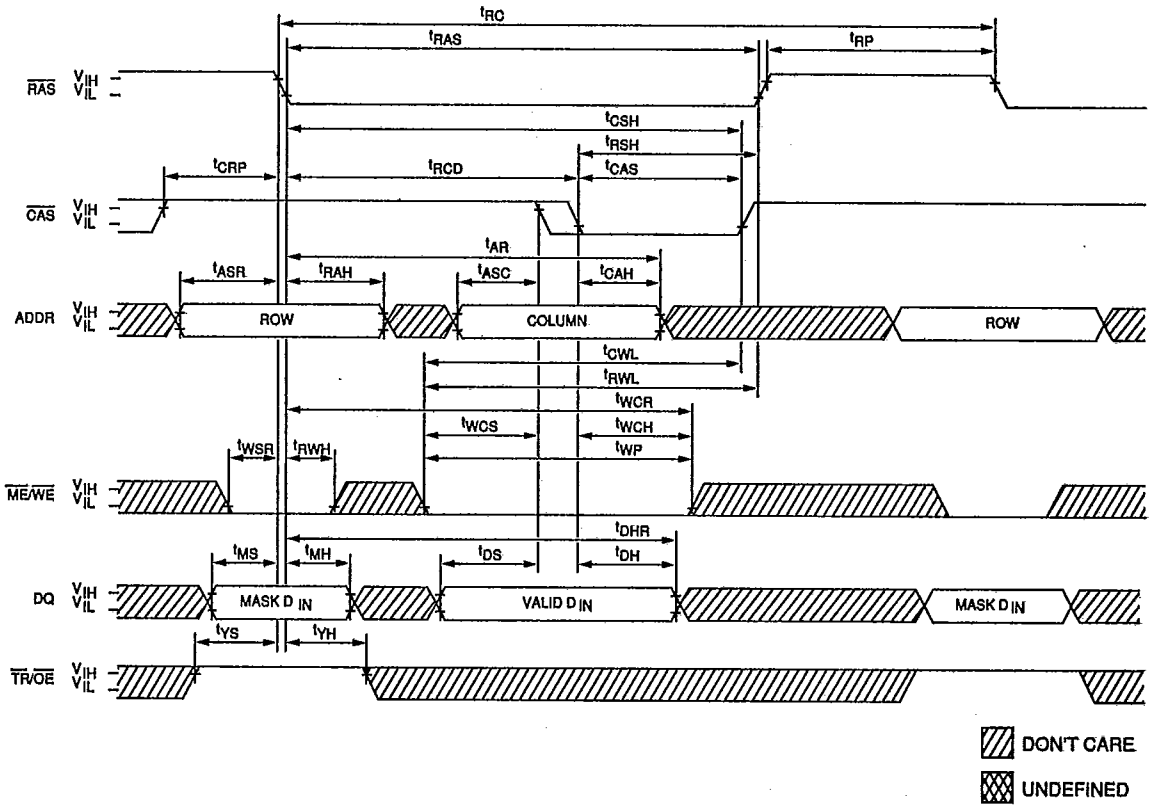
## DRAM READ CYCLE




## DRAM EARLY-WRITE CYCLE



## DRAM MASKED WRITE CYCLE



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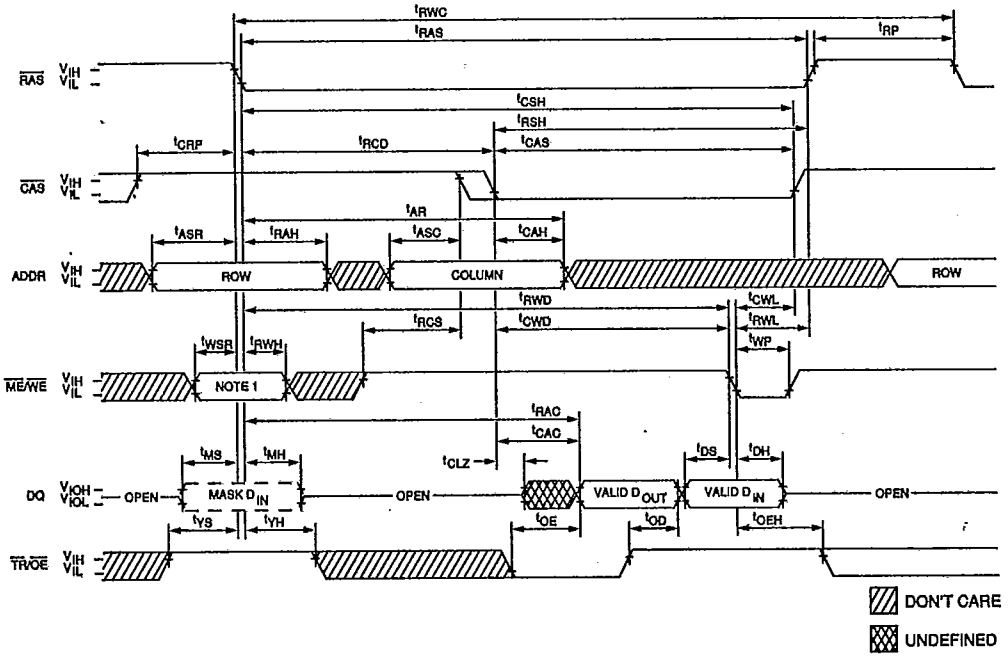
## DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE and LATE-WRITE CYCLE)




**NOTE:** If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

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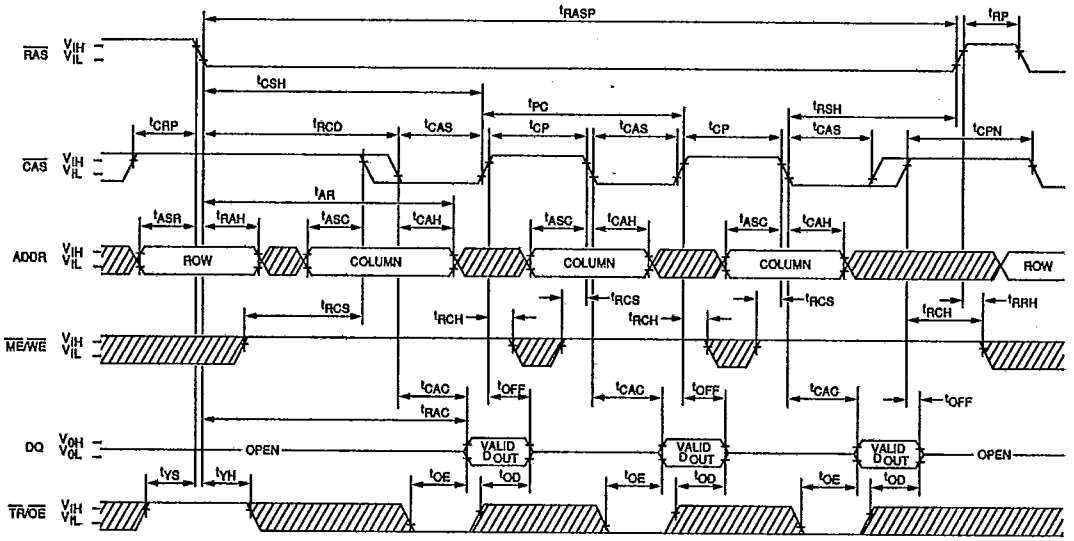
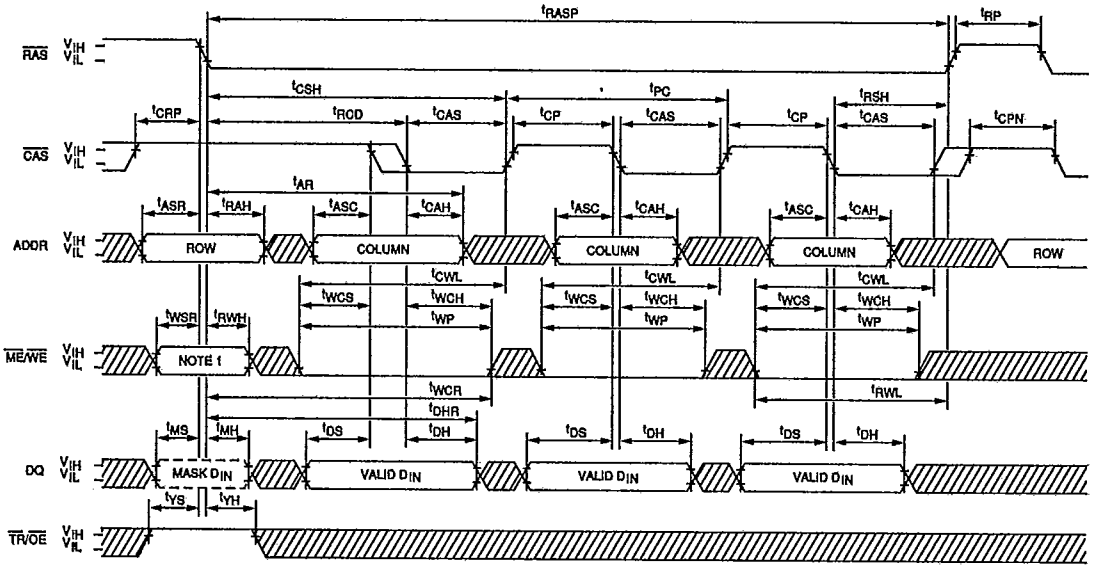
## DRAM PAGE-MODE READ CYCLE




## DRAM PAGE-MODE EARLY-WRITE CYCLE

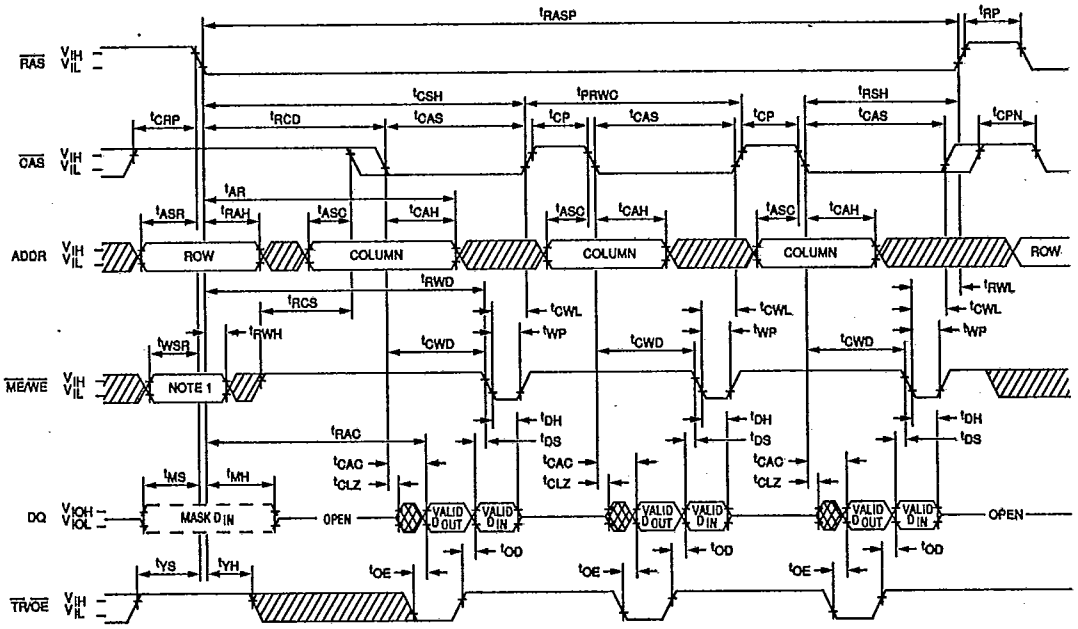



DON'T CARE

UNDEFINED

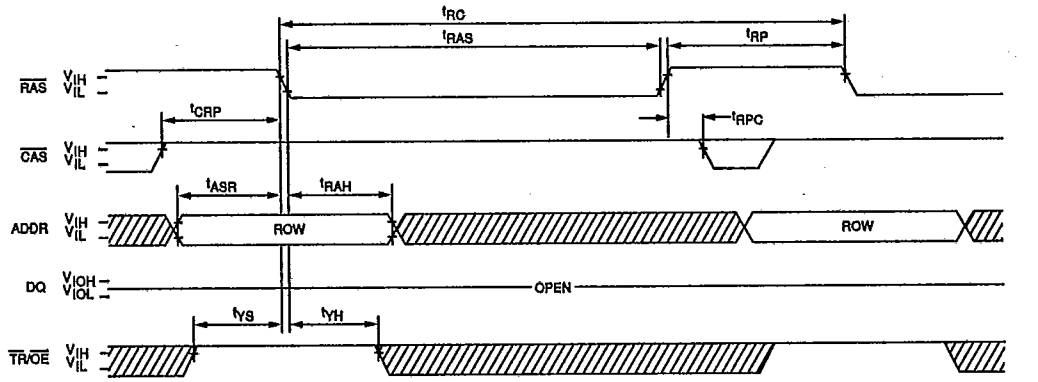
**NOTE:** If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

## DRAM PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)




**NOTE:** 1. If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

## $\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{ME}/\overline{WE}$ = Don't Care)



MULTIPORT DRAM

## CAS-BEFORE-RAS REFRESH CYCLE

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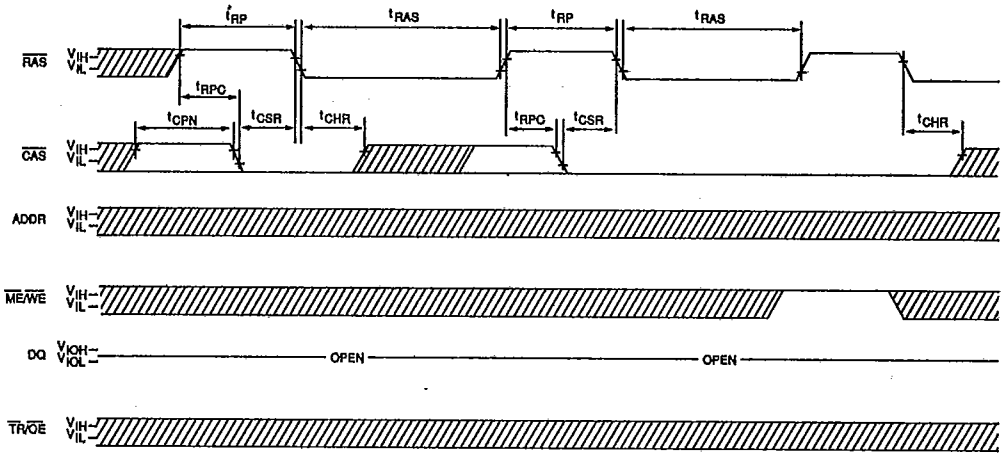
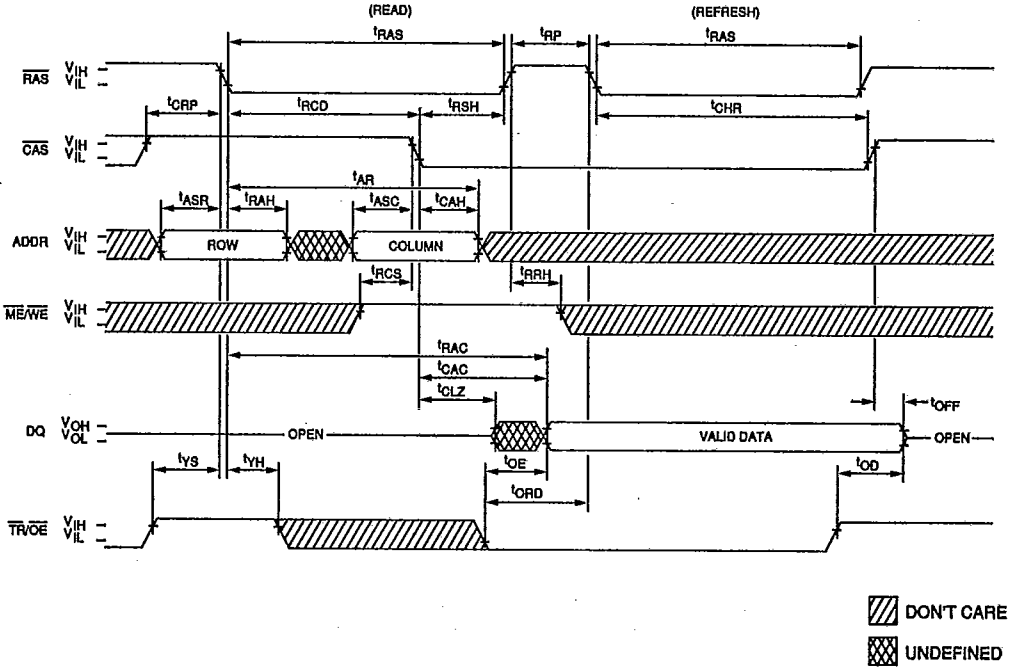
($A_0$ - $A_7$ and ME/WE are Don't Care.)

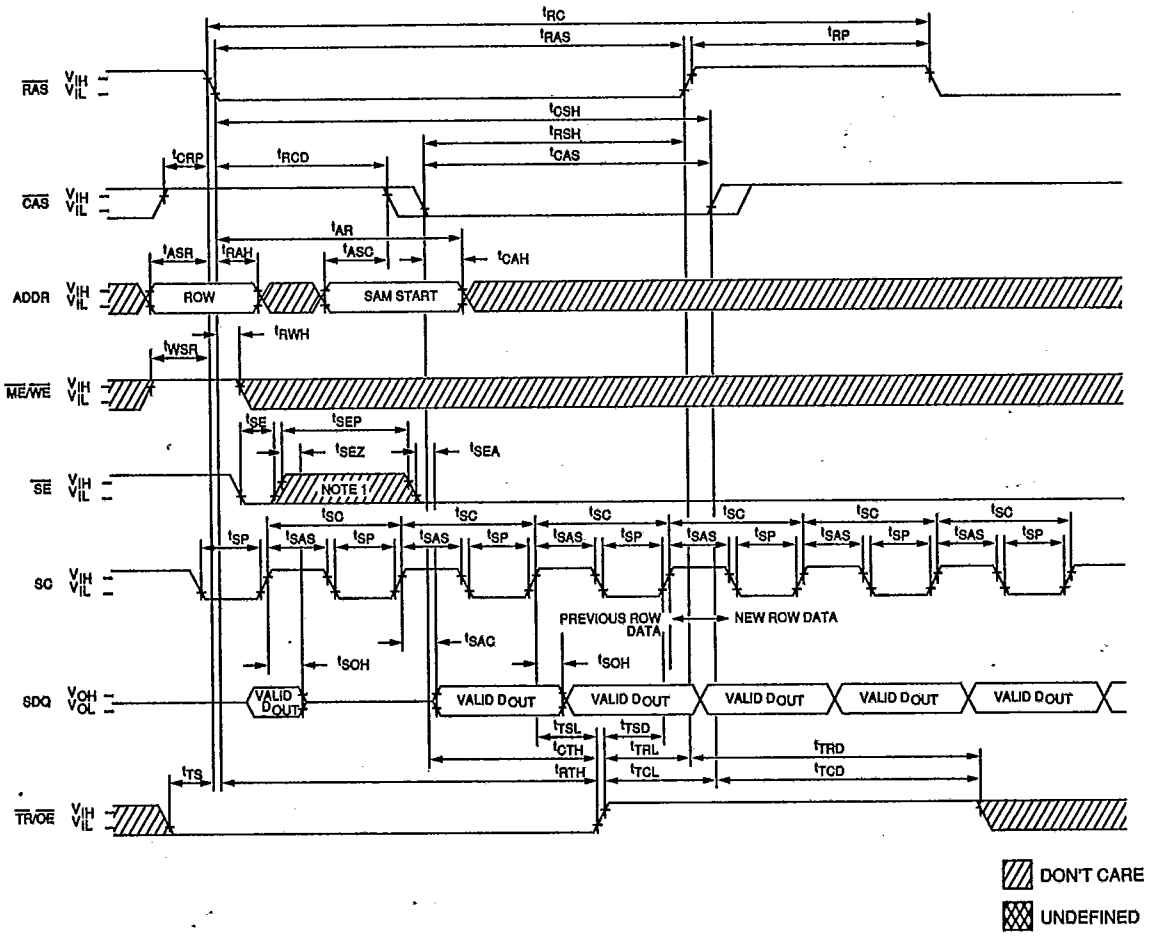



## HIDDEN REFRESH CYCLE




**NOTE:** A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH.

## DRAM-TO-SAM TRANSFER
## (READ TRANSFER)
(When part was previously in the SERIAL OUTPUT mode.)




**NOTE:** This $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

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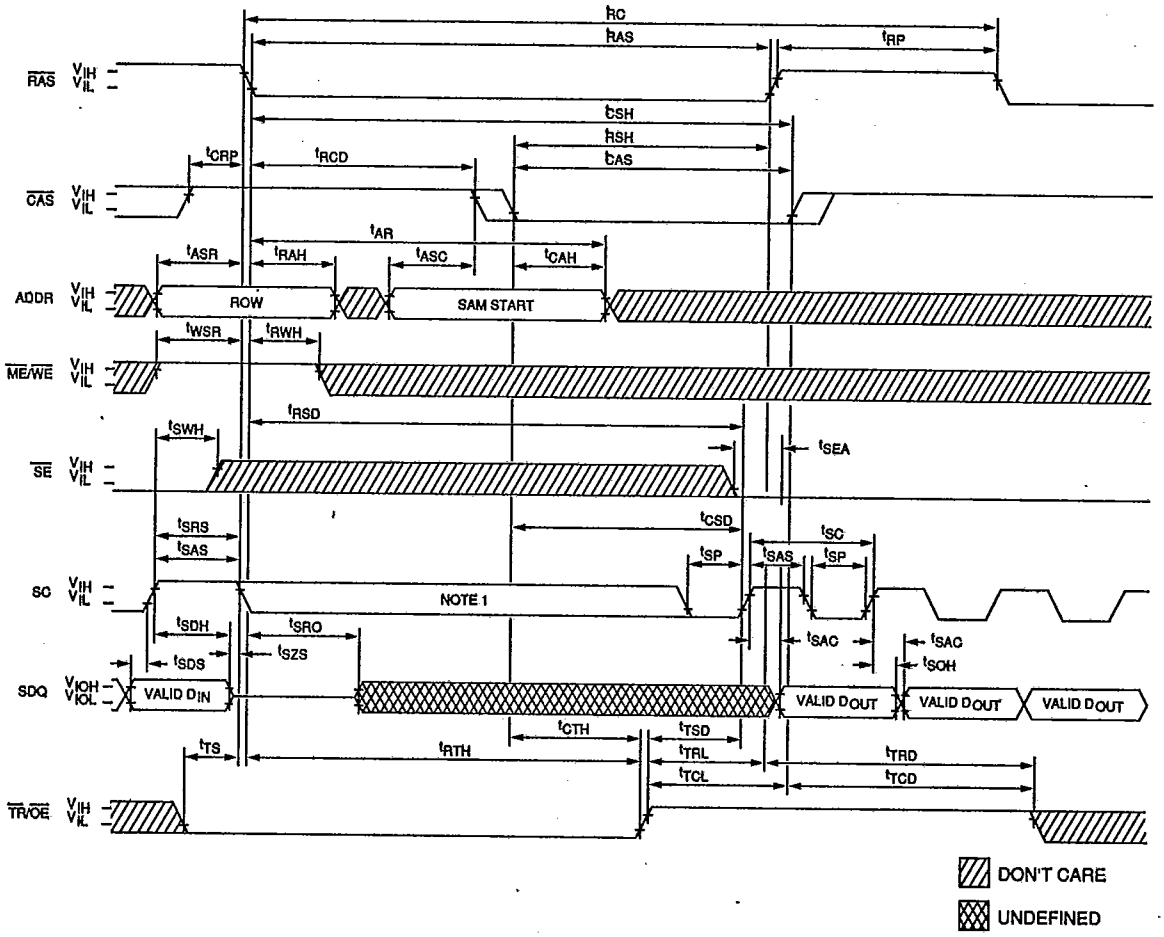
## DRAM-TO-SAM TRANSFER (READ TRANSFER)

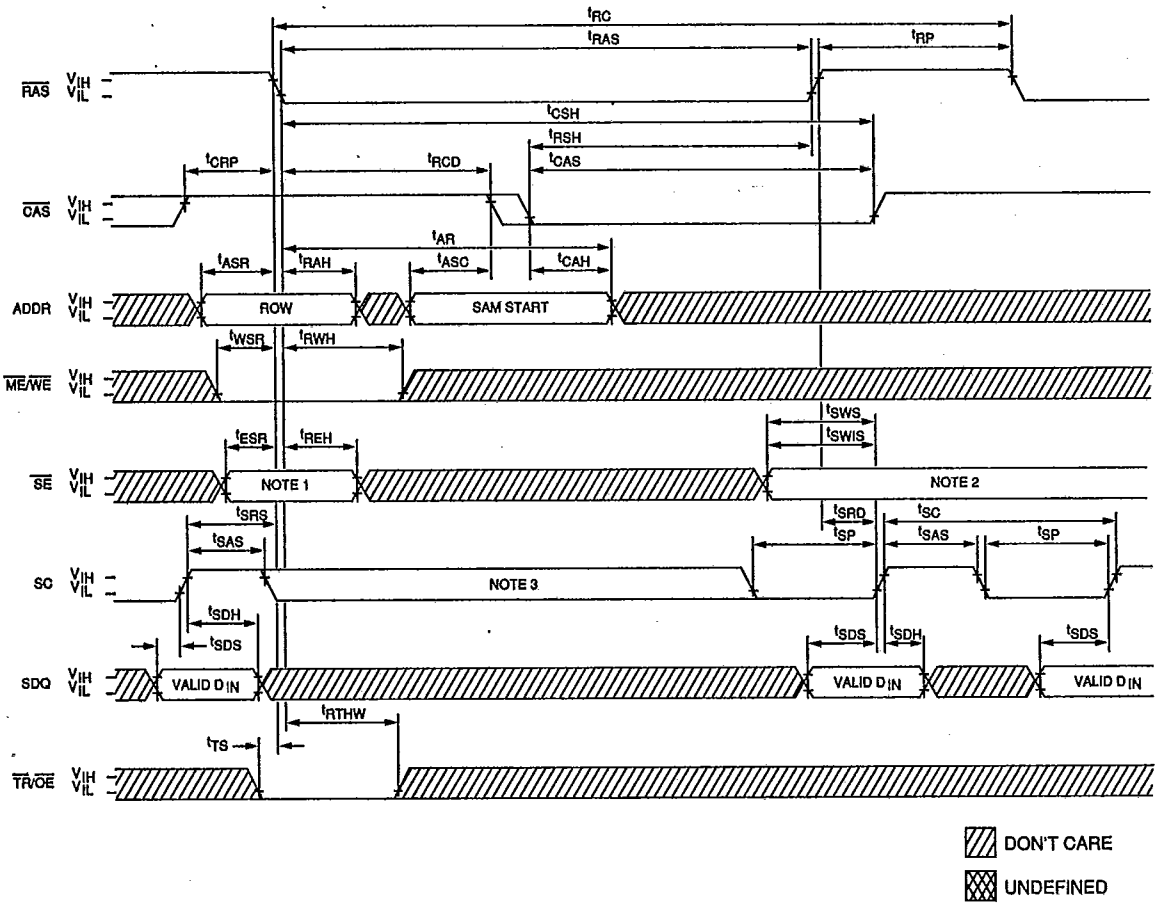
(When part was previously in the SERIAL INPUT mode.)




**NOTE:** There must be no rising edges on the SC input during this time.

## SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)




**NOTE:** 1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

3. There must be no rising edges on the SC input during this time.

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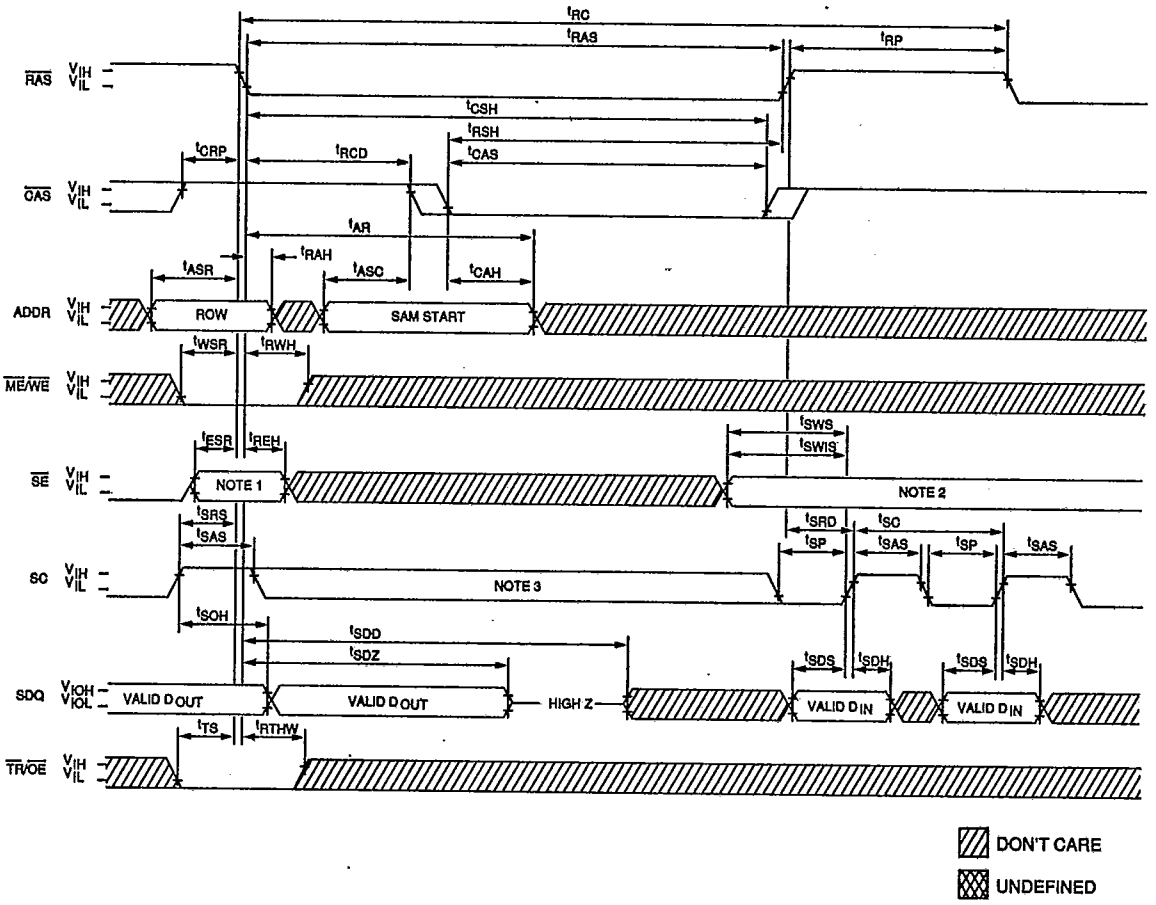
## SAM-TO-DRAM TRANSFER
## (WRITE TRANSFER or PSEUDO WRITE TRANSFER)
(When part was previously in the SERIAL OUTPUT mode.)




**NOTE:** 1. If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).
2. $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.
3. There must be no rising edges on the SC input during this time.

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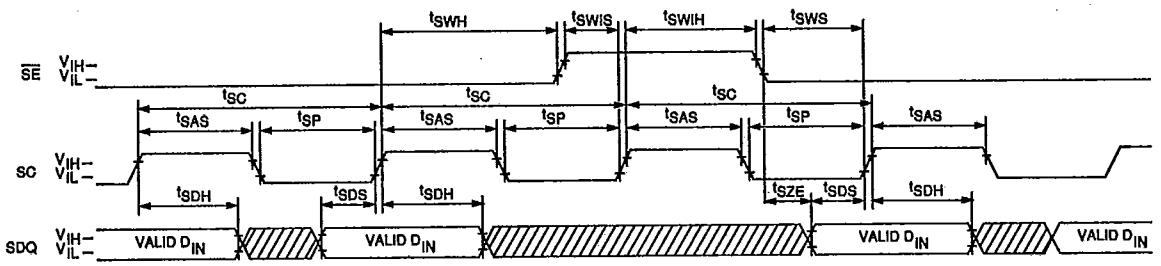
## SAM SERIAL INPUT




## SAM SERIAL OUTPUT