

## P-Channel Enhancement Mode Field Effect Transistor

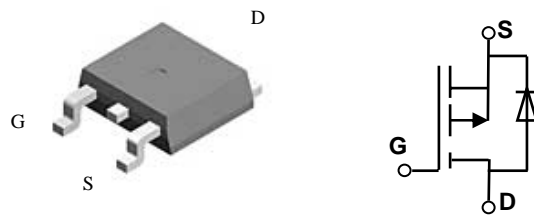
### FEATURES

- Super high dense cell design for low  $R_{DS(ON)}$
- Rugged and reliable
- Simple drive requirement
- TO-252 package

PRODUCT SUMMARY		
$V_{DSS}$	$I_D$	$R_{DS(ON)}$ (m $\Omega$ ) Typ
-30V	-7A	98 @ $V_{GS}=-10V$
		130 @ $V_{GS}=-4.5V$



NOTE: The MT4435L2 is available in a lead-free package



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_j=125^\circ C$ - Pulse $d^b$	$I_D$	-7	A
	$I_{DM}$	-24	A
Drain-source Diode Forward Current <sup>a</sup>	$I_S$	-1.8	A
Maximum Power Dissipation <sup>a</sup>	$P_D$	50	W
Operating Junction and Storage Temperature Range	$T_j, T_{STG}$	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to Ambient <sup>a</sup>	$R_{th JA}$	50	$^\circ C/W$
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**ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)**

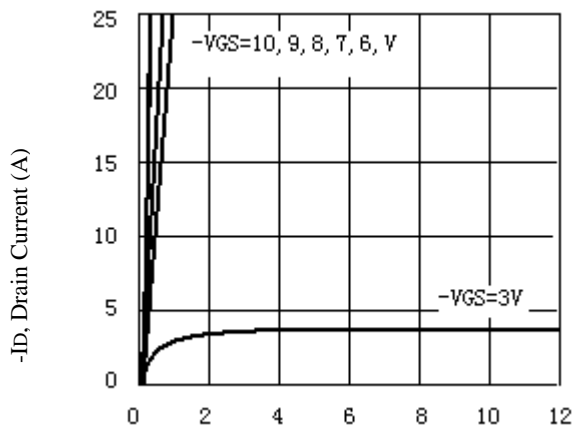
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A		84	98	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5.6A		110	135	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> =-5V, I <sub>D</sub> =-12A		5		S
<b>DAYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V f=1.0MHz		582		pF
Output Capacitance	C <sub>OSS</sub>			125		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			86		pF
<b>SWITCHING CHARACTERISISTICS</b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-15V I <sub>D</sub> =-10A, V <sub>GEN</sub> =-4.5V R <sub>L</sub> =10ohm R <sub>GEN</sub> =6ohm		9		ns
Rise Time	t <sub>r</sub>			10		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			38		ns
Fall Time	t <sub>f</sub>			23		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-1A V <sub>GS</sub> =-10V		11.7		nC
Gate-Source Charge	Q <sub>gS</sub>			2.1		nC
Gate-Drain Charge	Q <sub>gD</sub>			2.9		nC

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

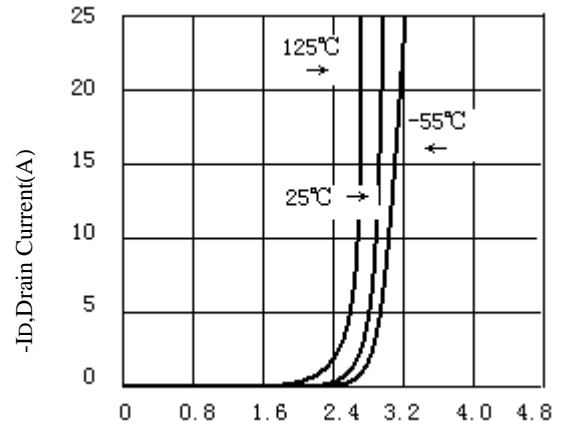
Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage	VSD	VGS=0V, IS=-1.7A		-0.84	-1.2	V

Notes

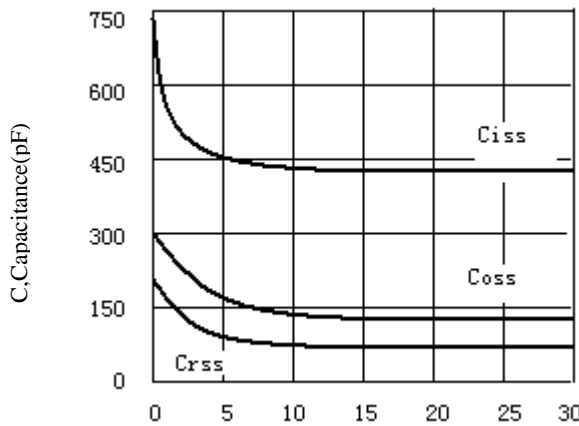
- Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- Guaranteed by design, not subject to production testing.



- V<sub>DS</sub>, Drain-to-Source Voltage (V)  
Figure 1. Output Characteristics



-V<sub>GS</sub>, Gate-to-source Voltage (V)  
Figure 2. Transfer Characteristics



- V<sub>GS</sub>, Drain-to Source Voltage  
Figure 3. Capacitance

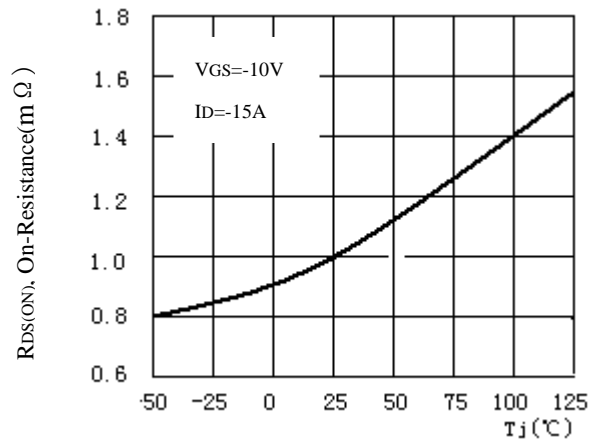
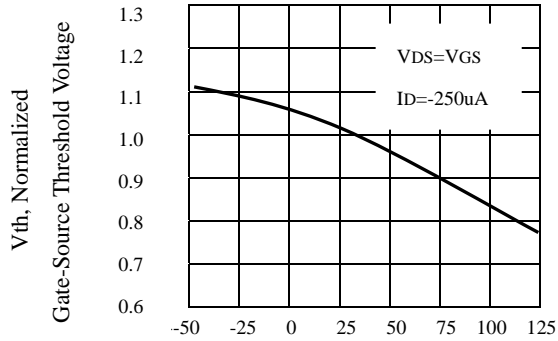
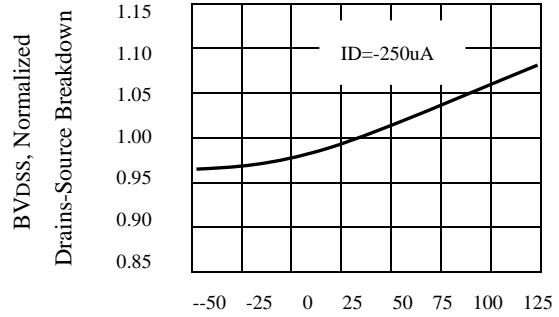


Figure 4. On-Resistance Variation with Temperature



Tj, Junction Temperature(°C)  
Figure5. Gate Threshold Variation  
With Temperature



Tj, Junction Temperature (°C)  
Figure6. Breakdown Voltage Variation  
With Temperature

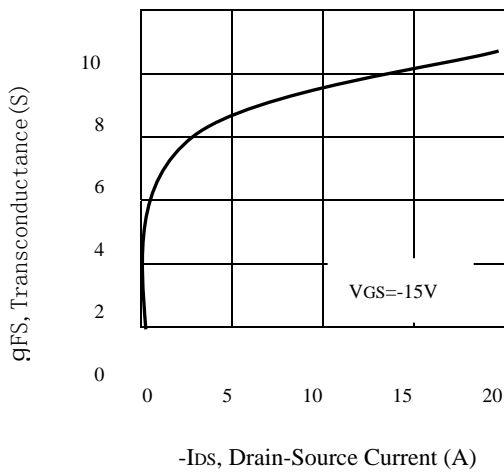


Figure7. Transconductance Variation  
With Drain Current

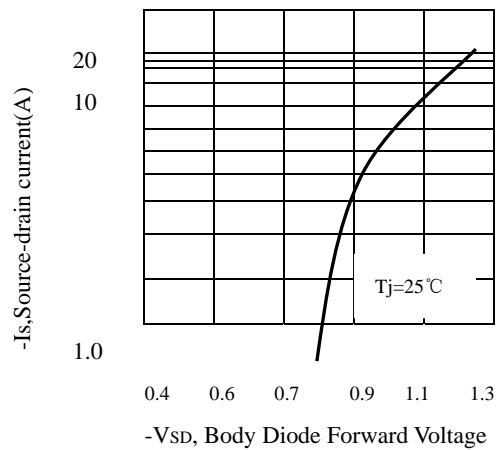


Figure8. Body Diode Forward Voltage  
Variation with Source Current

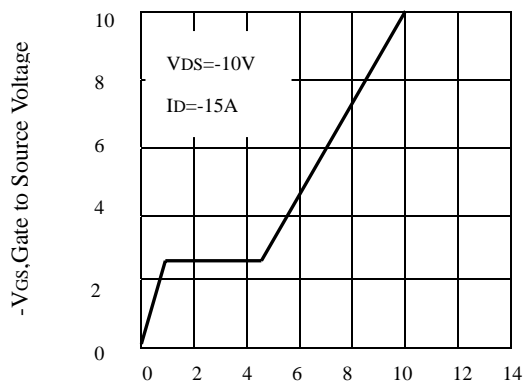


Figure9. Gate Charge

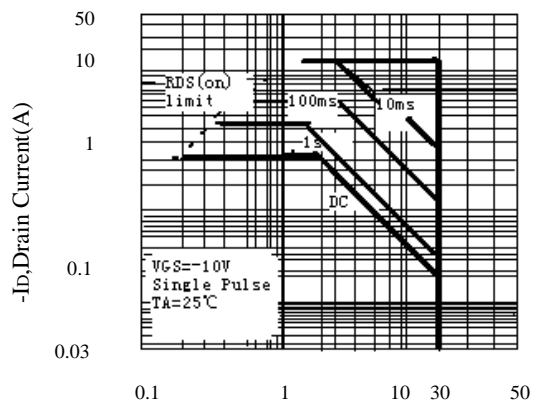


Figure10. Maximum Safe Operating Area



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