September 2008

MT4435

30V P-Channel PowerTrench MOSFET

General Description

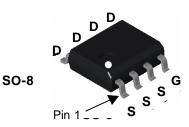
This PChannel MOSFET is a rugged gate version of MOS-TECH Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V-25V).

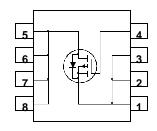
Applications

- · Power management
- Load switch
- Battery protection

Features

- -8.8 A, -30 V $R_{DS(ON)} = 20 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 35 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- Low gate charge (17nC typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{\text{DS(ON)}}$
- · High power and current handling capability





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V _{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±25	V
l _D	Drain Current - Continuous	(Note 1a)	-8.8	Α
	- Pulsed		– 50	
P _D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J , T_{STG}	Operating and Storage Junction Temperat	ture Range	-55 to +175	°C

Thermal Characteristics

R _{0JA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	125	°C/W
R ₀ JC	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

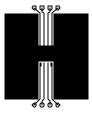
Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT4435		13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			I.	I.	I.
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-30			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-21		mV/°C
l _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 25 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
GSSR	Gate-Body Leakage, Reverse	$V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.7	-3	V
ΔV _{GS(th)} ΔT _J	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C		5		mV/°C
R _{DS(on)}	Static Drain-Source	$V_{GS} = -10 \text{ V}, I_{D} = -8.8 \text{ A}$		15	20	mΩ
	On–Resistance	$V_{GS} = -4.5 \text{ V}, I_{D} = -6.7 \text{ A}$		22	35	
		$V_{GS} = -10 \text{ V}, I_D = -8.8 \text{A}, T_J = 125 ^{\circ}\text{C}$		19	32	
I _{D(on)}	On–State Drain Current	$V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	-50			Α
g FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -8.8 \text{ A}$		24		S
Dynamic	: Characteristics					
Ciss	Input Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$		1604		pF
Coss	Output Capacitance	f = 1.0 MHz		408		pF
C _{rss}	Reverse Transfer Capacitance			202		pF
Switchin	g Characteristics (Note 2)			I	I	I
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, \qquad I_D = -1 \text{ A},$		13	23	ns
t _r	Turn-On Rise Time	$V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		13.5	24	ns
t _{d(off)}	Turn-Off Delay Time			42	68	ns
t _f	Turn-Off Fall Time			25	40	ns
Qg	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -8.8 \text{ A},$		17	24	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -5 \text{ V}$		5		nC
Q _{gd}	Gate-Drain Charge			6		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain–Source				-2.1	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -2.1 \text{ A} \text{(Note 2)}$		-0.73	-1.2	V

Notes

R_{8UA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{8UC} is guaranteed by design while R_{8CA} is determined by the user's board design.



a) 50°C/W when mounted on a 1ir² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu s,$ Duty Cycle < 2.0%

Typical Characteristics

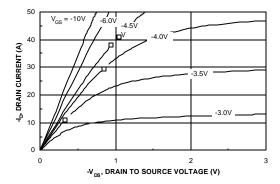


Figure 1. On-Region Characteristics.

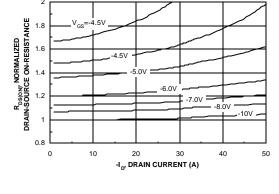


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

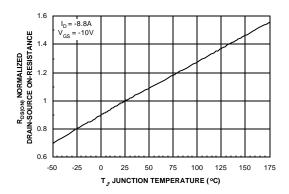


Figure 3. On-Resistance Variation with Temperature.

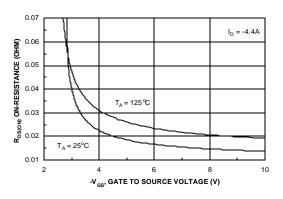


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

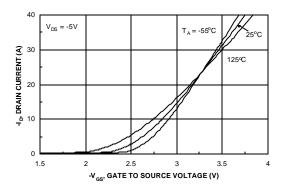


Figure 5. Transfer Characteristics.

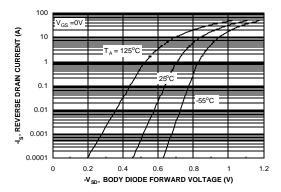
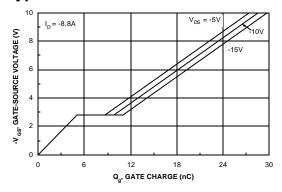


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



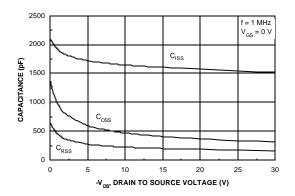
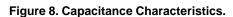
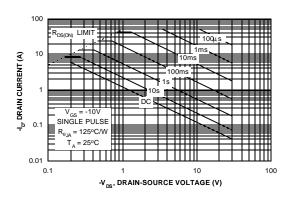


Figure 7. Gate Charge Characteristics.





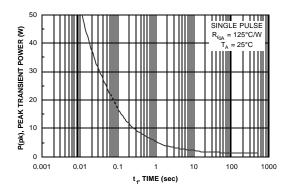


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

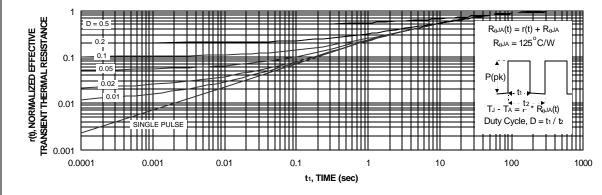
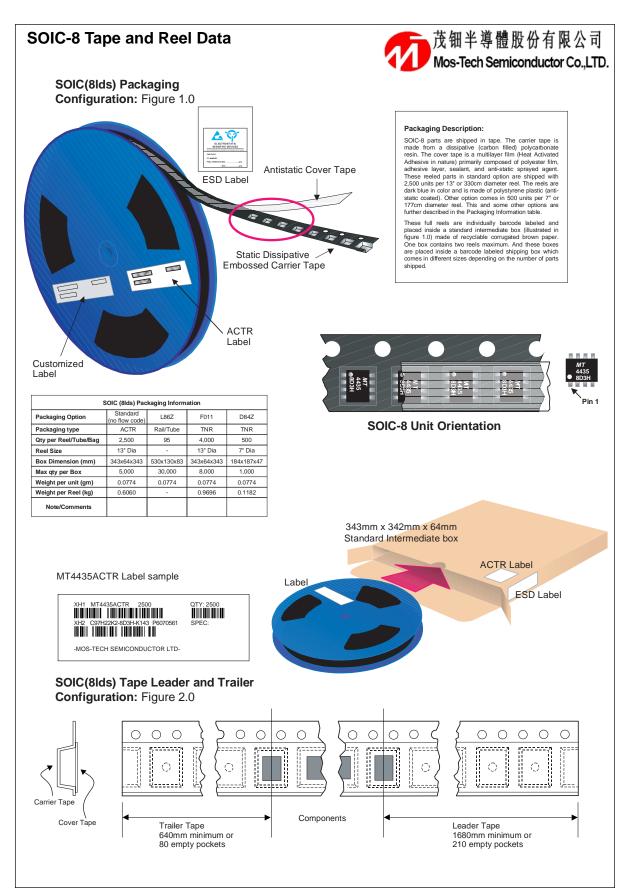


Figure 11. Transient Thermal Response Curve.

- Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

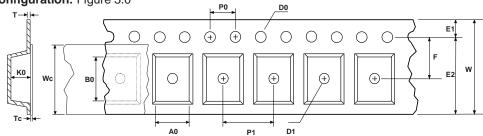


SEP 2008, Rev. B

SOIC-8 Tape and Reel Data, continued



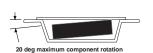




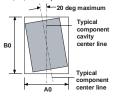


Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

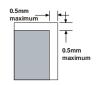


Sketch A (Side or Front Sectional View)
Component Rotation



Sketch B (Top View)

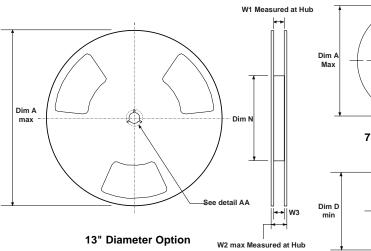
Component Rotation



Sketch C (Top View)
Component lateral movement

See detail AA

SOIC(8lds) Reel Configuration: Figure 4.0



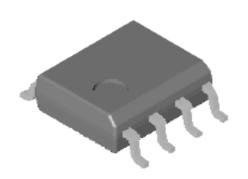
		7" Diameter Option
		→ B Min
,	Dim D min	Dim C
		DETAIL AA

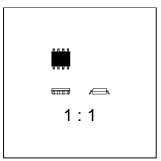
Dimensions are in inches and millimeters										
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)	
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	

SOIC-8 Package Dimensions



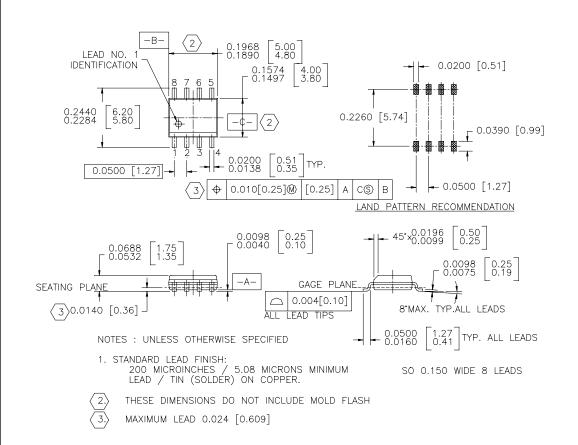
SOIC-8 (PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774





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