ASYNCHRONOUS CellularRAM™

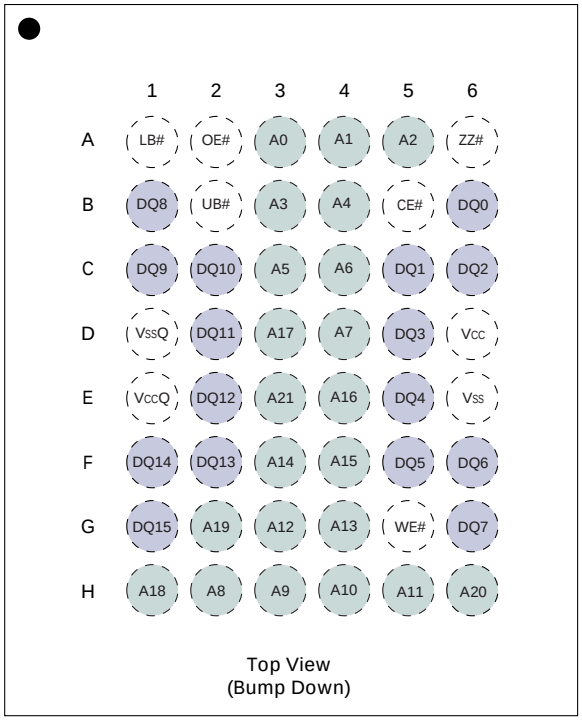
MT45W4MW16PFA **MT45W2MW16PFA**
MT45W4MV16PFA **MT45W2MV16PFA**
MT45W4ML16PFA **MT45W2ML16PFA**

For the latest data sheet, please refer to Micron's Web site:
www.micron.com/datasheets

Features

- Asynchronous and Page Mode interface
- Random Access Time: 70ns, 85ns
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns, 85ns
  Intrapage read access: 20ns, 25ns
- VCC, VCCQ Voltages
  1.70V–1.95V VCC
  1.70V–2.25V VCCQ (Option W)
  2.30V–2.70V VCCQ (Option V)
  2.70V–3.30V VCCQ (Option L)
- Low Power Consumption
  Asynchronous READ < 25mA
  Intrapage READ < 15mA
  Standby: 90µA (32Mb), 100µA (64Mb)
  Deep Power-Down < 10µA
- Low-Power Features
  Temperature Compensated Refresh (TCR)
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

Figure 1: 48-Ball FBGA



Top View
(Bump Down)

NOTE: See Table 1 on page 3 for Ball Descriptions. See Figure 18 on page 22 for the 48-ball mechanical drawing.

Options

Options	Marking
• VCC Core Voltage Supply	
1.8V – MT45WxMx16PFA	W
• VCCQ I/O Voltage	
3.0V – MT45WxML16PFA	L
2.5V – MT45WxMV16PFA	V
1.8V – MT45WxMW16PFA	W
• Access Time	
60ns	(contact factory)
70ns	-70
85ns	-85
• Configuration	
4 Meg x 16	MT45W4Mx16PFA
2 Meg x 16	MT45W2Mx16PFA
• Package	
48-ball FBGA	FA
• Operating Temperature Range	
Wireless (-25°C to +85°C)	WT
Industrial (-40°C to +85°C)	IT (contact factory)

NOTE: A part marking guide for the FBGA devices can be found on Micron's Web site: www.micron.com/numberguide.

Part Number Example:
MT45W2ML16PFA-70WT

General Description

Micron® CellularRAM™ products are high-speed, CMOS dynamic random access memories that have been developed for low-power portable applications. The MT45W4Mx16PFA is a 64Mb device organized as 4 Meg x 16 bits, and the MT45W2Mx16PFA is a 32Mb device organized as 2 Meg x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings.

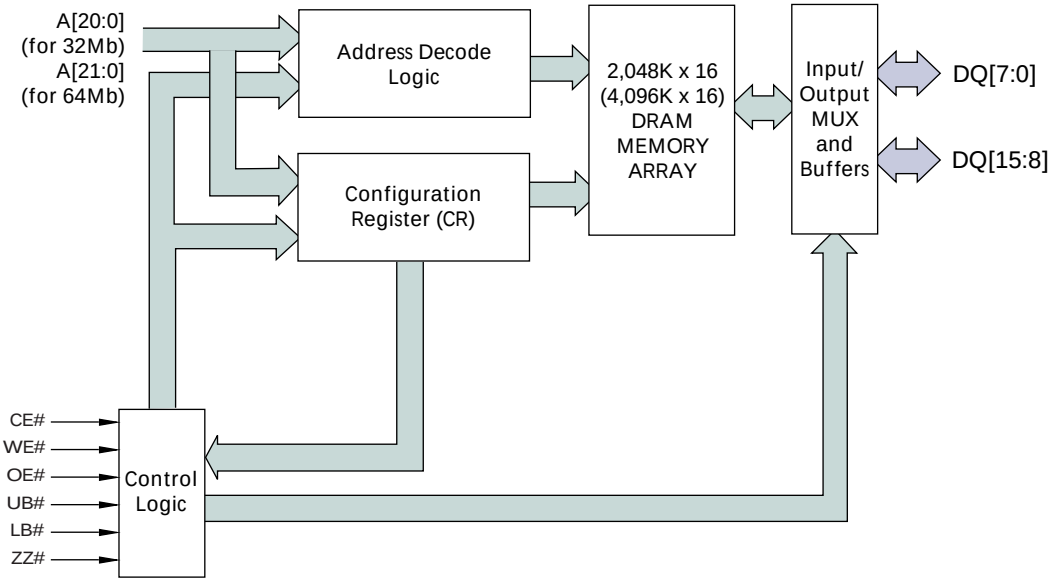
Operating voltages have been reduced in an effort to minimize power consumption. The core voltage has been reduced to a 1.80V operating level. To maintain compatibility with different memory bus interfaces, CellularRAM devices are available with I/O voltages of 3.00V, 2.50V or 1.80V.

A user-accessible configuration register (CR) has been included to define device operation. The CR defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

To operate seamlessly on an asynchronous memory bus, CellularRAM products have incorporated a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. CellularRAM products include three system-accessible mechanisms used to minimize refresh current. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the case temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Setting the sleep enable pin ZZ# to LOW enables one of two low-power modes: partial array refresh (PAR); or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

Figure 2: Functional Block Diagram
4 Meg x 16 and 2 Meg x 16



NOTE:

Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.

Table 1: FBGA Ball Descriptions

FBGA BALL ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6, E3	A[21:0]	Input	Address Inputs: Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the configuration register. On the 32Mb device, A21 (ball E3) is not internally connected.
A6	ZZ#	Input	Sleep Enable: When ZZ# is LOW, the configuration register can be loaded or the device can enter one of two low-power modes (DPD or PAR).
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Enables WRITE operations when LOW.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
D6	V_{CC}	Supply	Device Power Supply: (1.7V–1.95V) Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O Power Supply: (1.8V, 2.5V, 3.0V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

Table 2: Bus Operations

MODE	POWER	CE#	WE#	OE#	LB#/UB#	ZZ#	DQ[15:0][1]	NOTES
Standby	Standby	H	X	X	X	H	High-Z	2, 5
Read	Active > Standby	L	H	L	L	H	Data-Out	1, 4
Write	Active > Standby	L	L	X	L	H	Data-In	1, 3, 4
Active	Standby	L	H	H	L	H	High-Z	4, 5
PAR	Partial Array Refresh	H	X	X	X	L	High-Z	6
DPD	Deep Power-Down	H	X	X	X	L	High-Z	6
Load Configuration Register	Active	L	L	X	X	L	High-Z	

NOTE:

1. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# only is in select mode, only DQ[7:0] are affected. When UB# only is in the select mode, DQ[15:8] are affected.
2. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When WE# is invoked, the OE# input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. V_{IN} = V_{CC} or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
6. DPD is enabled when configuration register bit CR[4] is “0”; otherwise, PAR is enabled.

Table 3: Abbreviated Component Marks— CellularRAM FBGA-Packaged Components

PART NUMBER	ENGINEERING SAMPLE	QUALIFIED SAMPLE
MT45W4MW16PFA-85 WT	PX300	PW300
MT45W4MW16PFA-70 WT	PX306	PW306
MT45W4ML16PFA-85 WT	PX303	PW303
MT45W4ML16PFA-70 WT	PX304	PW304
MT45W2MW16PFA-85 WT	PX200	PW200
MT45W2MW16PFA-70 WT	PX206	PW206
MT45W2ML16PFA-85 WT	PX203	PW203
MT45W2ML16PFA-70 WT	PX204	PW204
MT45W4MW16PFA-85 IT	PX348[1]	PW348[1]
MT45W4MW16PFA-70 IT	PX349[1]	PW349[1]
MT45W4ML16PFA-85 IT	PX350[1]	PW350[1]
MT45W4ML16PFA-70 IT	PX351[1]	PW351[1]
MT45W2MW16PFA-85 IT	PX207[1]	PW207[1]
MT45W2MW16PFA-70 IT	PX208[1]	PW208[1]
MT45W2ML16PFA-85 IT	PX209[1]	PW209[1]
MT45W2ML16PFA-70 IT	PX210[1]	PW210[1]

NOTE:

1. Contact factory for availability.

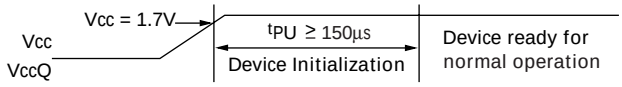
Functional Description

In general, the MT45W4Mx16PFA device and the MT45W2Mx16PFA device are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The MT45W4Mx16PFA contains 67,108,864 bits organized as 4,194,304 addresses by 16 bits. The MT45W2Mx16PFA contains 33,554,432 bits organized as 2,097,152 addresses by 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default settings. VCC and VCCQ must be applied simultaneously, and when they reach a stable level above 1.70V, the device will require 150µs to complete its self-initialization process (see Figure 3 below). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation. At power-up, the CR is set to 0070h.

Figure 3: Power-Up Initialization Timing



Bus Operating Modes

The MT45W4Mx16PFA and the MT45W2Mx16PFA CellularRAM products incorporate the industry-standard, asynchronous interface found on other low-power SRAM or Pseudo SRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 4) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 5) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a "Don't Care"; WE# will override OE#. The data to be written will be latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first).

Figure 4: READ Operation

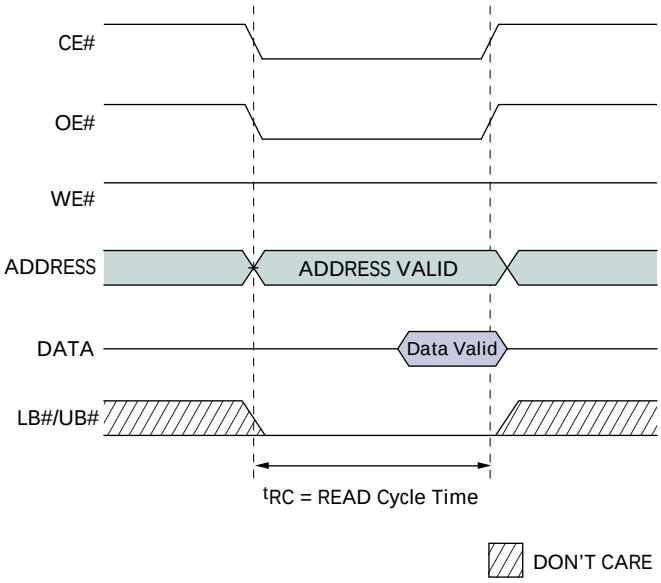
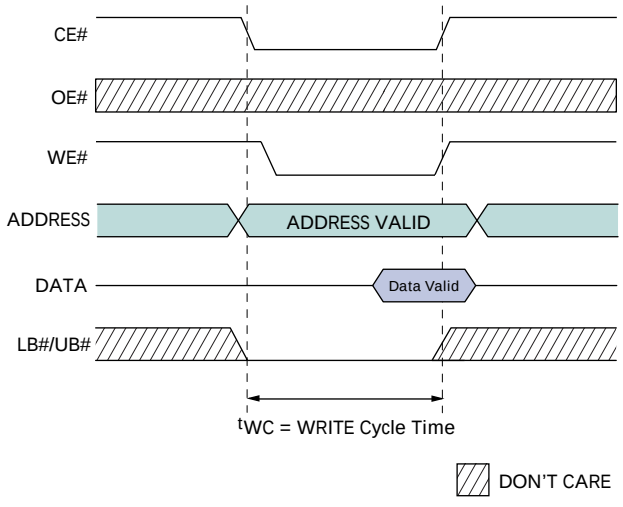


Figure 5: WRITE Operation

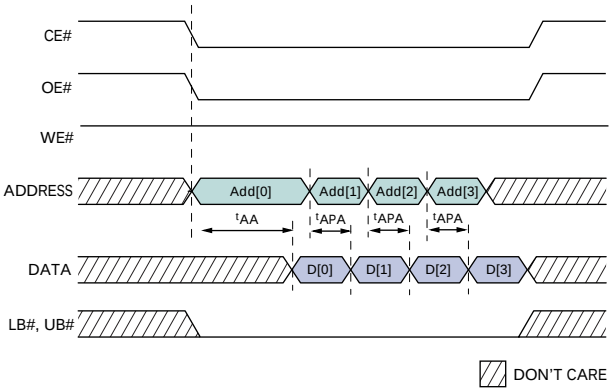


Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 6 shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

Figure 6: Page READ Operation



LB#/UB# Operation

The lower byte (LB#) enable and upper byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, the device remains in an active mode as long as CE# remains LOW.

Low Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. Standby operation occurs when CE# and ZZ# are HIGH and there are no transactions in progress.

The device will enter standby operation during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This “active” standby mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires more frequent refresh operations to maintain data integrity as temperatures increase. More frequent refresh is required due to the increased leakage of the DRAM's capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (Tables 5 and 6). READ and WRITE operations are ignored during PAR operation.

The device can only enter PAR mode if the SLEEP bit in the configuration register has been set HIGH (CR[4] = 1). PAR is initiated by bring the ZZ# pin to the LOW state for longer than 10µs. Returning ZZ# to HIGH will

cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing the ZZ# pin to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

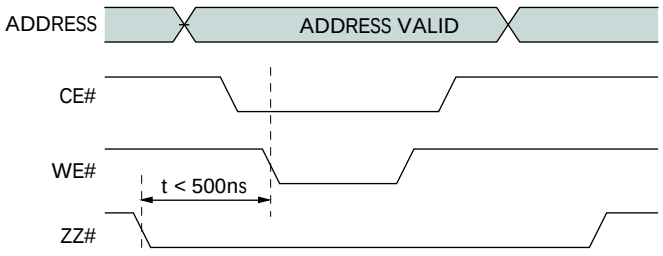
Driving the ZZ# pin LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

Configuration Register Operation

The configuration register (CR) defines how the CellularRAM device performs its transparent self refresh. This register is automatically loaded with default settings during power-up and can be updated anytime while the device is operating in a standby state.

The CR is loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 7). The values placed on addresses A[21:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the configuration register. Table 4 on page 9 describes the control bits used in the CR. At power up, the CR is set to 0070h.

Figure 7: Load Configuration Register Operation



Partial Array Refresh (CR[2:0])
Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Tables 5 and 6 on page 9).

Sleep Mode (CR[4])
Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled.

DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operation can resume.

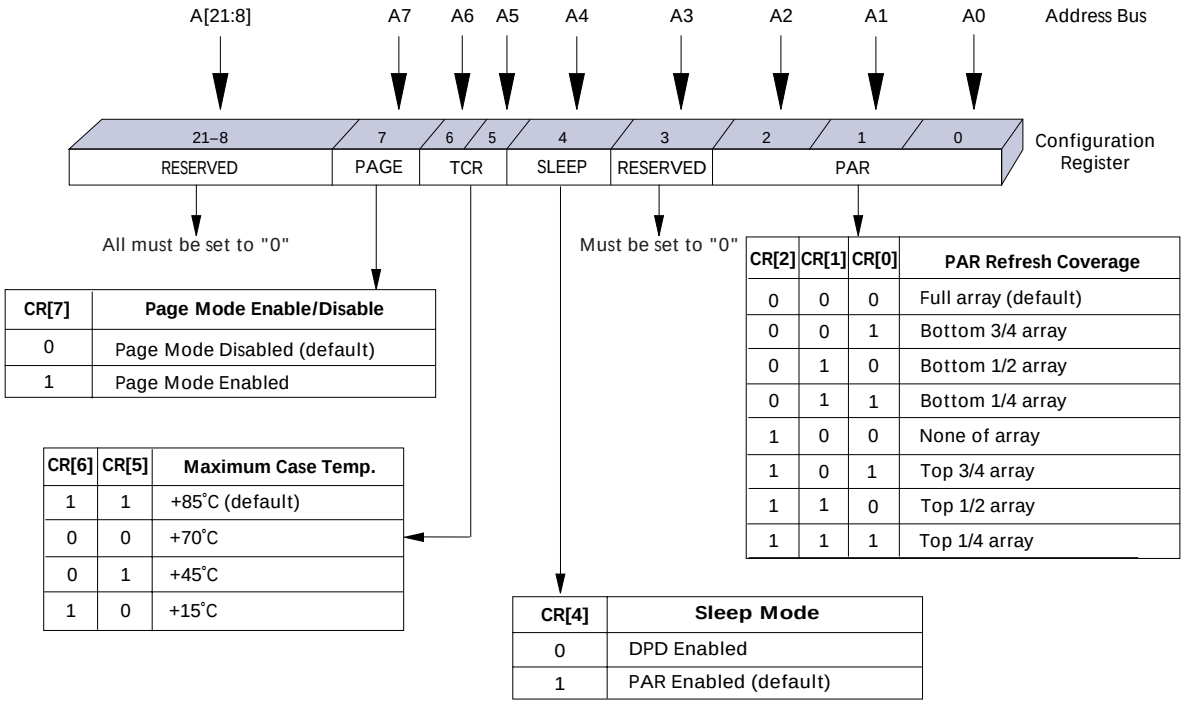
Temperature Compensated Refresh (CR[6:5])
Default = +85°C Operation

The TCR bits allow for adequate refresh at four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Page Mode READ Operation (CR[7])
Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

Table 4: Configuration Register Bit Mapping



CR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enabled

CR[6]	CR[5]	Maximum Case Temp.
1	1	+85°C (default)
0	0	+70°C
0	1	+45°C
1	0	+15°C

CR[2]	CR[1]	CR[0]	PAR Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 3/4 array
0	1	0	Bottom 1/2 array
0	1	1	Bottom 1/4 array
1	0	0	None of array
1	0	1	Top 3/4 array
1	1	0	Top 1/2 array
1	1	1	Top 1/4 array

CR[4]	Sleep Mode
0	DPD Enabled
1	PAR Enabled (default)

Table 5: 32Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	Three-quarters of die	000000h–17FFFFh	1.5 Meg x 16	24Mb
0	1	0	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	080000h–1FFFFFh	1.5 Meg x 16	24Mb
1	1	0	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	1	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb

Table 6: 64Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h-3FFFFFh	4 Meg x 16	64Mb
0	0	1	Three-quarters of die	000000h-2FFFFFh	3 Meg x 16	48Mb
0	1	0	One-half of die	000000h-1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-quarter of die	000000h-0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	100000h-3FFFFFh	3 Meg x 16	48Mb
1	1	0	One-half of die	200000h-3FFFFFh	2 Meg x 16	32Mb
1	1	1	One-quarter of die	300000h-3FFFFFh	1 Meg x 16	16Mb

Absolute Maximum Ratings*

Voltage to Any Ball Except V_{CC}, V_{CCQ}
Relative to V_{SS} . . . . . .
-0.50V to (4.0V or VccQ + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS}. . -0.20V to 2.45V
Voltage on V_{CCQ} Supply Relative to V_{SS} . -0.20V to 4.0V
Storage Temperature . . . . . -55°C to 150°C
Operating Temperature (Case)
Wireless. . . . . -25°C to 85°C
Industrial . . . . . -40°C to 85°C
Soldering Temperature and Time
10s (lead only) . . . . . 260°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Electrical Characteristics and Operating Conditions

Wireless Temperature (-25ºC ≤ T_C ≤ +85 ºC)
Industrial Temperature (-40ºC < T_C < +85ºC)

DESCRIPTION	CONDITIONS		SYMBOL		MIN	MAX	UNITS	NOTES
Supply Voltage			V_{CC}		1.70	1.95	V	
I/O Supply Voltage		L: 3.00V	V_{CCQ}		2.70	3.30	V	
		V: 2.50V	V_{CCQ}		2.30	2.70	V	
		W:1.80V	V_{CCQ}		1.70	2.25	V	
Input High Voltage			V_{IH}		1.4	V_{CCQ} + 0.2	V	
Input Low Voltage			V_{IL}		-0.2	+0.4	V	
Output High Voltage	I_{OH} = -0.2mA		V_{OH}		0.80 V_{CCQ}		V	
Output Low Voltage	I_{OL} = 0.2mA		V_{OL}			0.20 V_{CCQ}	V	
Input Leakage Current	V_{IN} = 0 to V_{CCQ}		I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled		I_{LO}			1	µA	2
Read Operating Current	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0		I_{CC1}	-70		25	mA	1, 2
				-85		20	mA	1, 2
Write Operating Current	V_{IN} = V_{CCQ} or 0V Chip Enabled		I_{CC2}	-70		25	mA	1, 2
				-85		20	mA	1, 2
MAX Standby Current	V_{IN} = V_{CCQ} or 0V Chip Disabled		I_{SB}	32Mb		90	µA	2, 3
				64Mb		100	µA	2, 3

NOTE:

1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled (CE# HIGH). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling), regardless of the state of CE#, LB#, and UB#. In order to achieve low standby current, all inputs must be either V_{CCQ} or V_{SS}.
3. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C.

Table 8: Temperature Compensated Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	DENSITY	MAX CASE TEMPERATURES	TYP	MAX	UNITS
Temperature Compensated Refresh Standby Current	V_{IN} = $V_{CC}Q$ or 0V, Chip Disabled	I_{TCR}	64Mb	+85°C		100	µA
				+70°C		TBD	µA
				+45°C		TBD	µA
				+15°C		50	µA
			32Mb	+85°C		90	µA
				+70°C		TBD	µA
				+45°C		TBD	µA
				+15°C		50	µA

NOTE:

1. I_{TCR} (MAX) values measured with FULL ARRAY refresh.
2. This device assumes a standby mode if the chip is disabled (CE# HIGH). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling), regardless of the state of CE#, LB#, and UB#. In order to achieve low standby current, all inputs must be either $V_{CC}Q$ or V_{SS}.

Table 9: Partial Array Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	DENSITY	ARRAY PARTITION	TYP	MAX	UNITS
Partial Array Refresh Current	V_{IN} = $V_{CC}Q$ or 0V ZZ# = LOW CR[4] = 1	I_{PAR}	64Mb	Full		100	µA
				3/4		TBD	µA
				1/2		TBD	µA
				1/4		TBD	µA
				0		50	µA
			32Mb	Full		90	µA
				3/4		TBD	µA
				1/2		TBD	µA
				1/4		TBD	µA
				0		50	µA

NOTE:

I_{PAR} (MAX) values measured with TCR set to 85°C.

Table 10: Deep Power-Down Specifications and Conditions

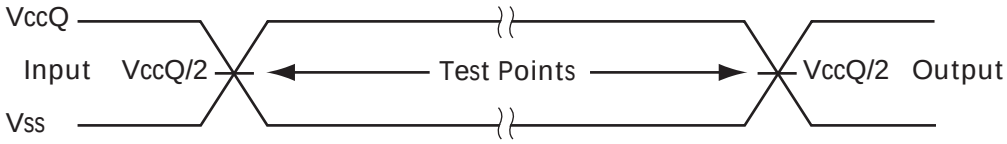
DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Deep Power-Down	V_{IN} = $V_{CC}Q$ or 0V; +25°C ZZ# = LOW CR[4] = 0	I_{ZZ}		10	µA

Table 11: Capacitance Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_C = +25ºC; f = 1 MHz;	CIN	–	6	pF	1
Input/Output Capacitance (DQ)	VIN = 0V	CIO	–	6	pF	1

NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

Figure 8: AC Input/Output Reference Waveform



NOTE:
AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input timing begins at VccQ/2, and output timing ends at VccQ/2. Input rise and fall times (10% to 90%) < 1.6ns.

Figure 9: Output Load Circuit

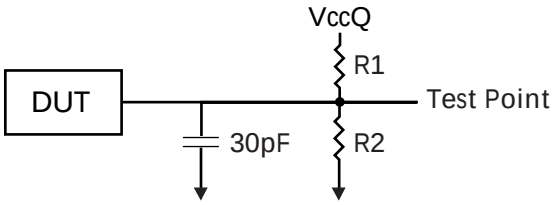


Table 12: Output Load Circuit

VccQ	R1/R2
1.8V	2.7KΩ
2.5V	3.7KΩ
3.0V	4.5KΩ

Table 13: READ Cycle Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Access Time	^tAA		70		85	ns	
Page Access Time	^tAPA		20		25	ns	
LB#/UB# Access Time	^tBA		70		85	ns	
LB#/UB# Disable to High-Z Output	^tBHZ	0	8	0	8	ns	2
LB#/UB# Enable to Low-Z Output	^tBLZ	10		10		ns	1
Chip Select Access Time	^tCO		70		85	ns	
Chip Disable to High-Z Output	^tHZ	0	8	0	8	ns	2
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
Output Enable to Valid Output	^tOE		20		20	ns	
Output Hold from Address Change	^tOH	5		5		ns	
Output Disable to High-Z Output	^tOHZ	0	8	0	8	ns	2
Output Enable to Low-Z Output	^tOLZ	5		5		ns	1
Page Cycle Time	^tPC	20		25		ns	
Read Cycle Time	^tRC	70		85		ns	

Table 14: WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	^tAS	0		0		ns	
Address Valid to End of Write	^tAW	70		85		ns	
Byte Select to End of Write	^tBW	70		85		ns	
CE# HIGH Time During Write	^tCEH	5		5		ns	
Maximum CE# Pulse Width	^tCEM		10		10	µs	
Chip Enable to End of Write	^tCW	70		85		ns	
Data Hold from Write Time	^tDH	0		0		ns	
Data Write Setup Time	^tDW	23		25		ns	
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
End Write to Low-Z Output	^tOW	5		5		ns	
Write Cycle Time	^tWC	70		85		ns	
Write to High-Z Output	^tWHZ	0	8	0	8	ns	2
Write Pulse Width	^tWP	46		50		ns	
Write Recovery Time	^tWR	0		0		ns	

NOTE:

1. High-Z to Low-Z timings are tested with the circuit shown in Figure 9 on page 12. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 9 on page 12. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.

Table 15: Load Configuration Register Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Setup Time	^tAS	0		0		ns	
Address Valid to End of Write	^tAW	70		85		ns	
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns	
Chip Enable to End of Write	^tCW	70		85		ns	
Write Cycle Time	^tWC	70		85		ns	
Write Pulse Width	^tWP	40		40		ns	
Write Recovery Time	^tWR	0		0		ns	
ZZ# LOW to WE# LOW	^tZZWE	10	500	10	500	ns	

Table 16: Deep Power-Down Timing Requirements

DESCRIPTION	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns	
Deep Power-Down Recovery	^tR	150		150		µs	
Minimum ZZ# Pulse Width	^tZZMIN	10		10		µs	

Table 17: Power-Up Initialization Timing Requirements

PARAMETER	SYMBOL	-70		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Power-Up Initialization Period	^tPU	150		150		µs	

Figure 10: Power-Up Initialization Period

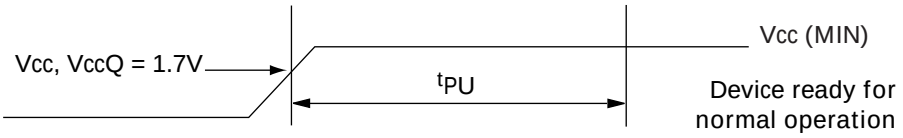


Table 18: Initialization Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{PU}	150		150		µs

Figure 11: Load Configuration Register

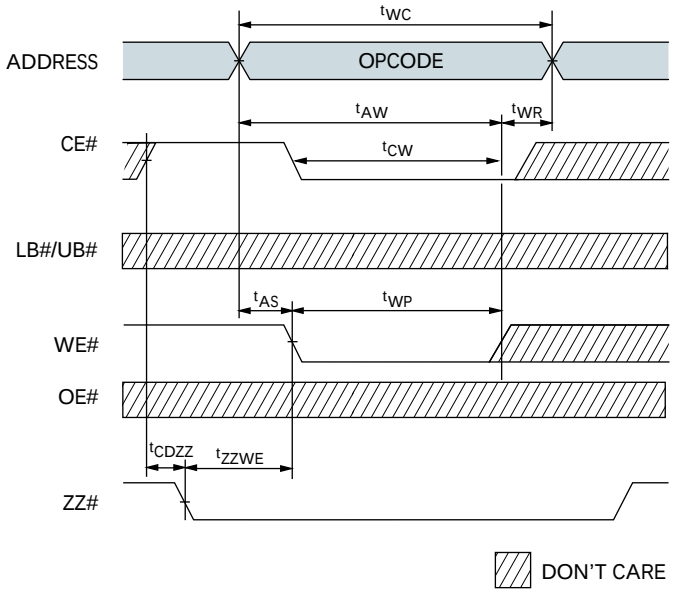


Table 19: Load Configuration Register Timing Requirements

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{CDZZ}	5		5		ns
t_{CW}	70		85		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{WC}	70		85		ns
t_{WP}	40		40		ns
t_{WR}	0		0		ns
t_{ZZWE}	10	500	10	500	ns

Figure 12: Deep Power-Down — Entry/Exit

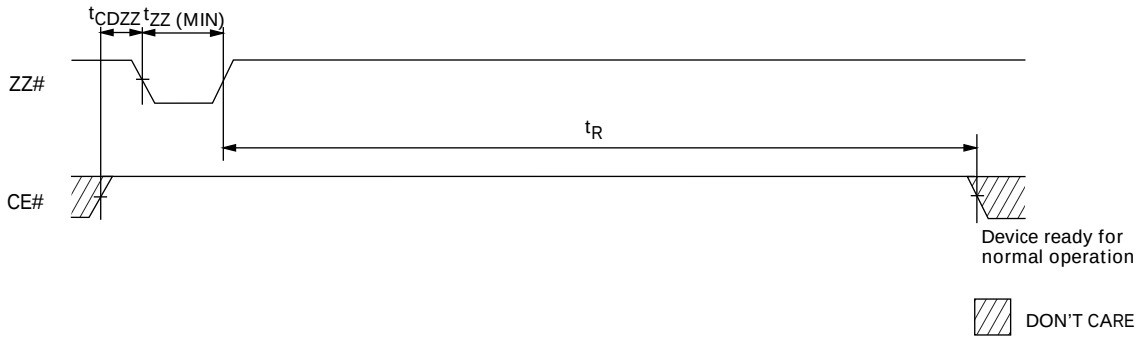


Table 20: Deep Power-Down Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
$^{t}CDZZ$	5		5		ns
^{t}R	150		150		µs
^{t}ZZ (MIN)	10		10		µs

Figure 13: Single READ Operation (WE# = VIH)

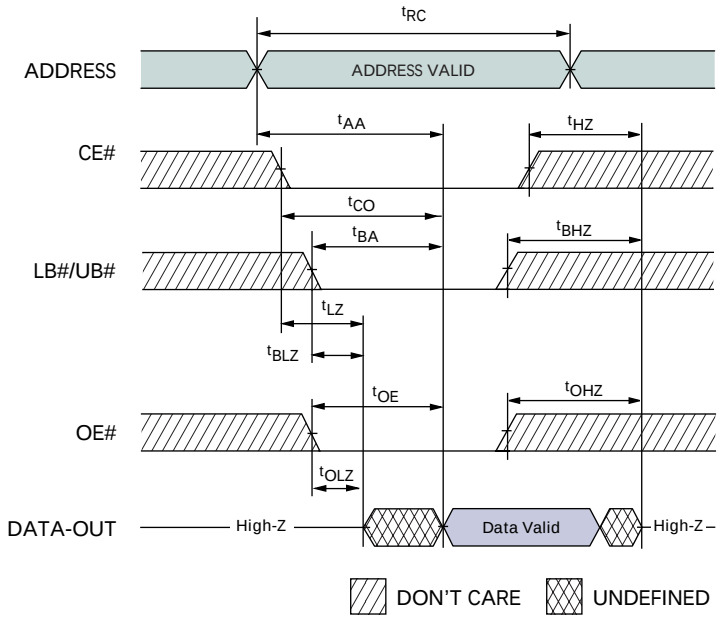


Table 21: READ Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
tAA		70		85	ns
tBA		70		85	ns
tBHZ	0	8	0	8	ns
tBLZ	10		10		ns
tCO		70		85	ns
tHZ	0	8	0	8	ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
tLZ	10		10		ns
tOE		20		20	ns
tOHZ	0	8	0	8	ns
tOLZ	5		5		ns
tRC	70		85		ns

Figure 14: Page Mode READ Operation (WE# = VIH)

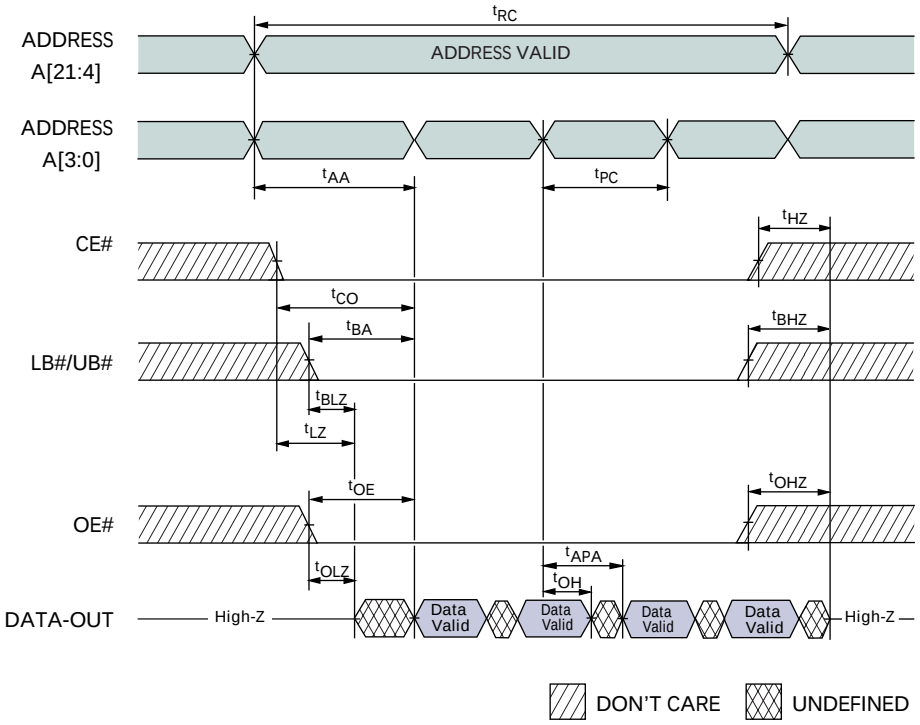


Table 22: Page Mode READ Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{AA}		70		85	ns
t_{APA}		20		25	ns
t_{BA}		70		85	ns
t_{BHZ}	0	8	0	8	ns
t_{BLZ}	10		10		ns
t_{CO}		70		85	ns
t_{HZ}	0	8	0	8	ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OH}	5		5		ns
t_{OHZ}	0	8	0	8	ns
t_{OLZ}	5		5		ns
t_{PC}	20		25		ns
t_{RC}	70		85		ns

Figure 15: WRITE Cycle (WE# Control)

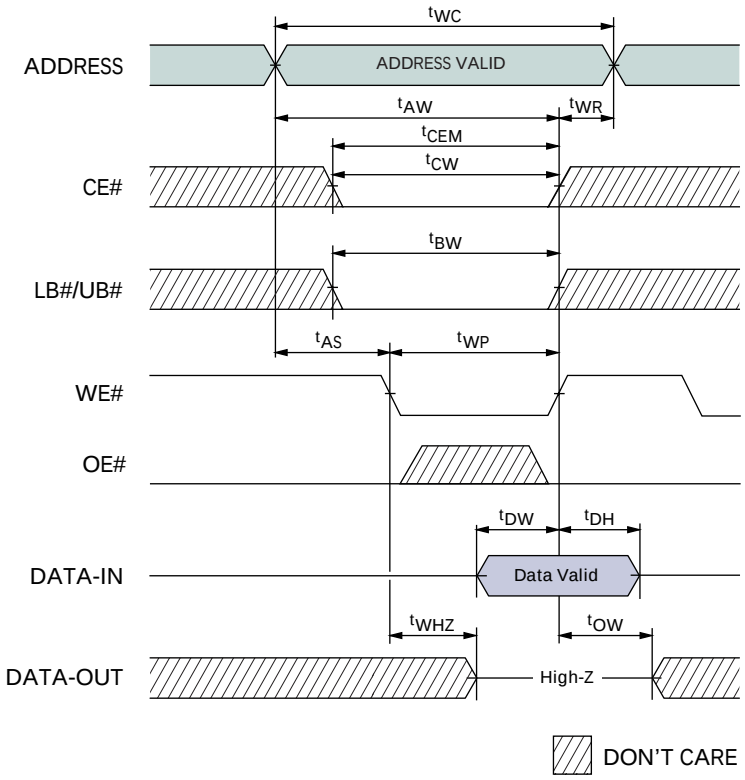


Table 23: WRITE Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}AS	0		0		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CEM		10		10	µs
^{t}CW	70		85		ns
^{t}DH	0		0		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
^{t}DW	23		25		ns
^{t}OW	5		5		ns
^{t}WC	70		85		ns
^{t}WHZ	0	8	0	8	ns
^{t}WP	46		50		ns
^{t}WR	0		0		ns

Figure 16: WRITE Cycle (CE# Control)

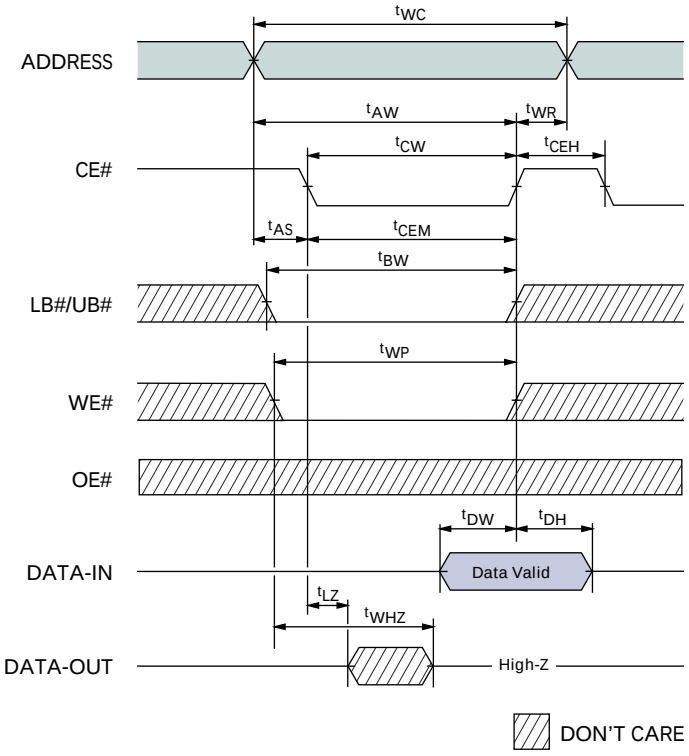


Table 24: WRITE Timing Parameters

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEH}	5		5		ns
t_{CEM}		10		10	µs
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-70 MIN	-70 MAX	-85 MIN	-85 MAX	UNITS
t_{DW}	23		25		ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0		ns
t_{WP}	46		50		ns
t_{WR}	0		0		ns

Figure 17: WRITE Cycle (LB#/UB# Control)

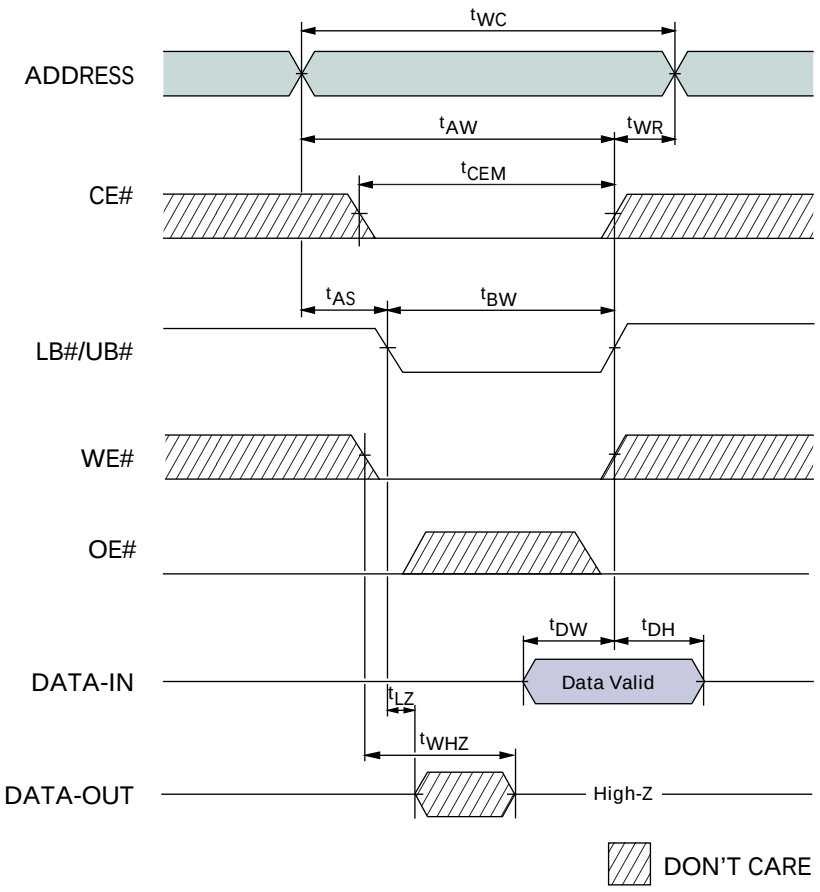
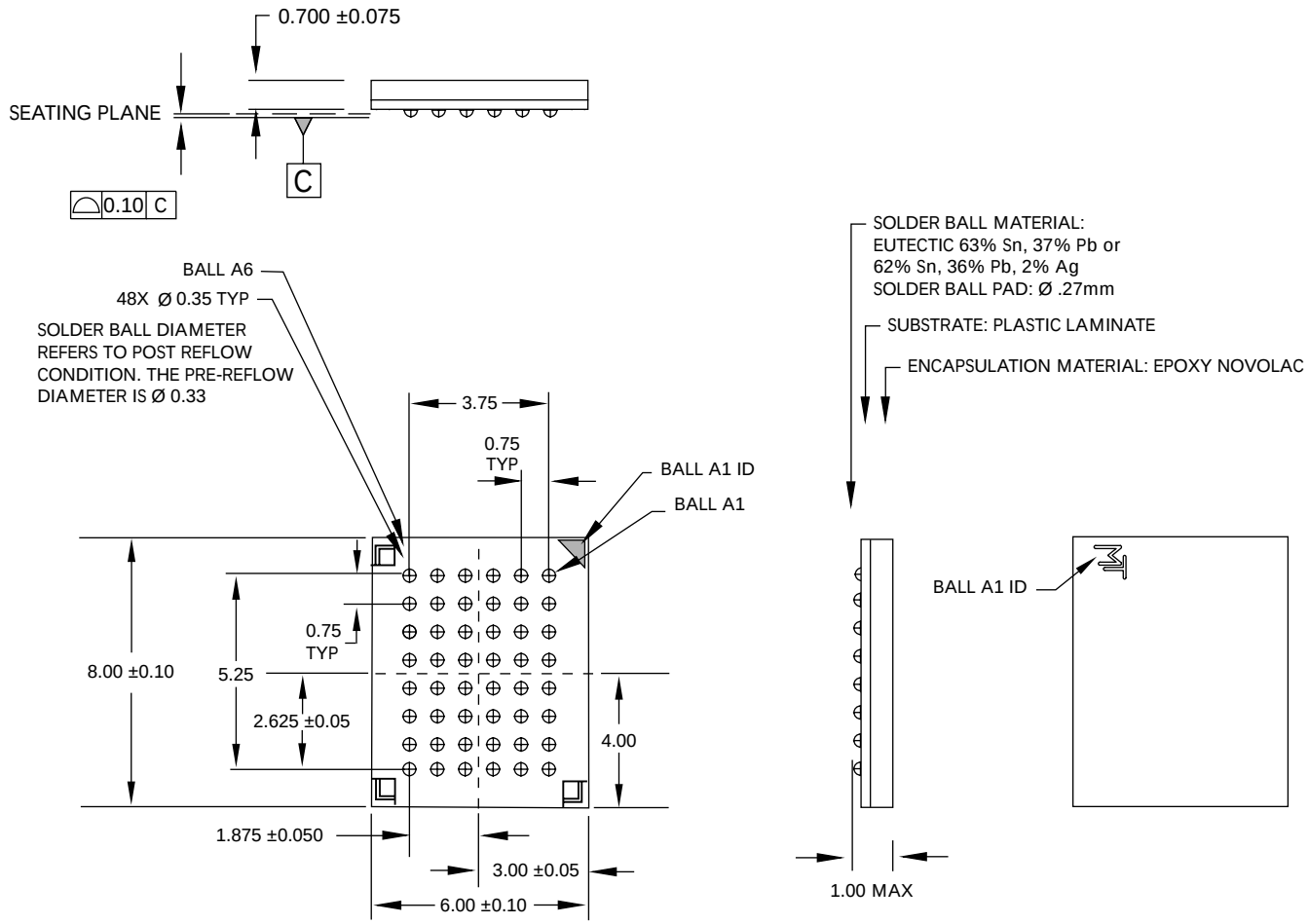


Table 25: WRITE Timing Parameters

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{DH}	0		0		ns

SYMBOL	-70		-85		UNITS
	MIN	MAX	MIN	MAX	
t_{DW}	23		25		ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WR}	0		0		ns

Figure 18: 48-Ball FBGA



NOTE:

1. All dimensions in millimeters, MAX/MIN or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Data Sheet Designation: PRELIMINARY

This data sheet contains initial characterization limits, subject to change upon full characterization of production devices.

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APPENDIX A

How Extended Timings Impact CellularRAM™ Operation

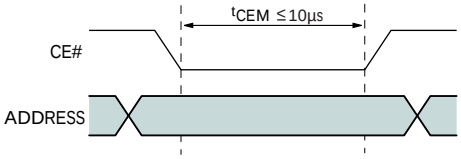
Introduction

CellularRAM™ products use a DRAM technology that periodically requires refresh to ensure against data corruption. CellularRAM devices include on-chip circuitry that performs the required refresh in a manner that is completely transparent in systems with normal bus timings. The refresh circuitry does impose constraints on timings in systems that take longer than 10µs to complete WRITE operations. This appendix describes CellularRAM timing requirements in systems that perform extended operations.

Operation When Page Mode is Disabled

CellularRAM products require that all WRITE operations must be completed within 10µs. After completing an operation, the device must either enter standby (by transitioning CE# HIGH), or else perform a second operation using a new address. Figures 19 and 20 demonstrate these constraints as they apply during an asynchronous (page-mode-disabled) operation. Either the CE# active period (^{t}CEM in Figure 19) or the address valid period (^{t}TM in Figure 20) must be less than 10µs during any operation to accommodate orderly scheduling of refresh.

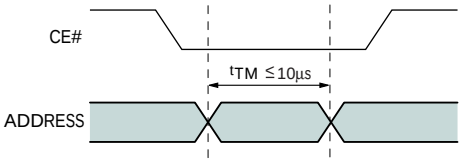
Figure 19: Extended Timing for ^{t}CEM



NOTE:

Timing constraints when page mode is disabled.

Figure 20: Extended Timing for ^{t}TM



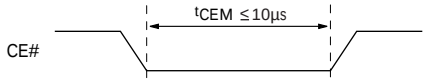
NOTE:

Timing constraints when page mode is disabled.

Operation When Page Mode is Enabled

When a CellularRAM device is configured for page mode operation, the address inputs are used to accelerate read accesses and cannot be used by the on-chip circuitry to schedule refresh. CE# must return HIGH upon completion of all WRITE operations when page mode is enabled (Figure 21). The total time taken for a WRITE operation should not exceed 10µs to accommodate orderly scheduling of refresh.

Figure 21: Extended Timing for ^{t}CEM



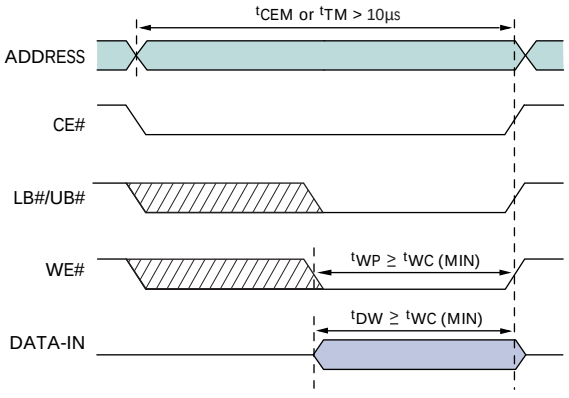
NOTE:

Timing constraints when page mode is enabled.

Impact on Extended WRITE Operations

Modified timings are only required during extended WRITE operations (see Figure 22 below). An extended WRITE operation requires that both the write pulse width (^{t}WP) and the data valid period (^{t}DW) will need to be lengthened to at least the minimum WRITE cycle time (^{t}WC [MIN]). These increased timings ensure that time is available for both a refresh operation and successful completion of the WRITE operation.

Figure 22: Extended WRITE Operation



Summary

CellularRAM products are designed to ensure that any possible bus timings do not cause corruption of array data due to lack of refresh. The on-chip refresh circuitry will only affect the required timings for WRITE operations (READs are unaffected) performed in a system with a slow memory interface. The impact for WRITE operations is that some of the timing parameters (^{t}WP, ^{t}DW) are lengthened. The modified timings are likely to have little or no impact when interfacing a CellularRAM device with a low-speed memory bus.

Table 26: Revision History

CHANGE	DATE	CHANGED BY	DESCRIPTION
7	07/10/03	ddb	Input/Output leakage to 1µA.
6	6/23/03	ddb	Incorporated Industrial Temperature data where applicable.
5	6/20/03	ddb	Added condition ZZ# LOW to PAR and DPD tables.
4	6/19/03	ddb	Changed standby power to 90µA and 100µA respectively; changed specified values to “TBD.” Moved LB#/UB# rising edge back in WRITE Operation diagram.
3	06/09/03	ddb	Absolute Maximum Signal Input value changed.
2	06/06/03	ddb	Edits suggested 6/6: Electrical Characteristics and Operating Conditions (Table 7 on page 10), changed Input High Voltage MAX to VccQ + 0.2, Output HIGH Voltage and Output LOW Voltage presentation changed for consistency.
1	06/05/03	ddb	Initial release.