MODEL: MT4761B01-1

Ver. 1.1

Date: 4.Sep.2012

Customer's Approval	CSOT
Signature Date	Approved By Product Director Date Name: Signature:
	Reviewed By PM Manager Date Name: Signature:
	Reviewed By Project Leader Date Name: Signature:
	Reviewed By PM Date Name: Signature:

Contents

Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver. 0.1	7.Jun.2012	36	9	Tentative Specification was First Issued.	Qiaoling Wu
Ver. 1.1	4.Sep.2012	37	9	Optical characteristics were updated.	Yingnan Zou

1. General Description

1.1 Product Features

- **FHD Resolution (1920 x 1080)**
- **High Brightness: 400 cd/m²**
- **Very High Contrast Ratio: 4000:1**
- **Fast Response Time**
- **High Color Saturation: 72% NTSC**
- **Ultra Wide Viewing Angle: 178° (H)/178° (V) (CR ≥ 10)**
- **Low Power Consumption: Typ. 68.5 W**
- **DE (Data Enable) Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

1.2 Overview

MT4761B01-1 is a diagonal 47.6" color active matrix LCD module with edge LED backlight and 2ch-LVDS interface. This module is a transmissive type display operating in the normally black mode. It supports 1920 x 1080 FHD resolution and can display up to 16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe. The converter of backlight is built-in.

This module dedicates for LCD TV products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth.

1.3 General Information

Item	Specification	Unit	Note
Active Area	1054.08 (H) x 592.92 (V)	mm	
Bezel Opening Area	1062.08 (H) x 601.28(V)	mm	
Outline Dimension	1078.6 (H) x 626.0(V) x 15.1 (D)	mm	D: From Bezel to Rear
Weight	9.5	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.183 (H) x 0.549 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Transmissive Mode, Normally Black	-	
Surface Treatment	Anti-glare, Haze 2%,Hard Coating (3H)	-	
Luminance of White	400	cd/m²	Center Point, Typ.

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings (Ta = 25 ± 2 °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Power Supply Voltage	V_{CC}	- 0.3	13.8	V
Logic Input Signal Voltage	V_{IN}	- 0.3	3.6	V
Light Bar Voltage	$V_{W(2D)}$	45.8	53.4	V_{RMS}
	$V_{W(3D)}$	51	60	
Converter Input Voltage	V_{BL}	0	30	V
Control Signal Level	-	-0.3	4.0	V

2.2 Environment Requirement

(1) Temperature and relative humidity range are shown as below.

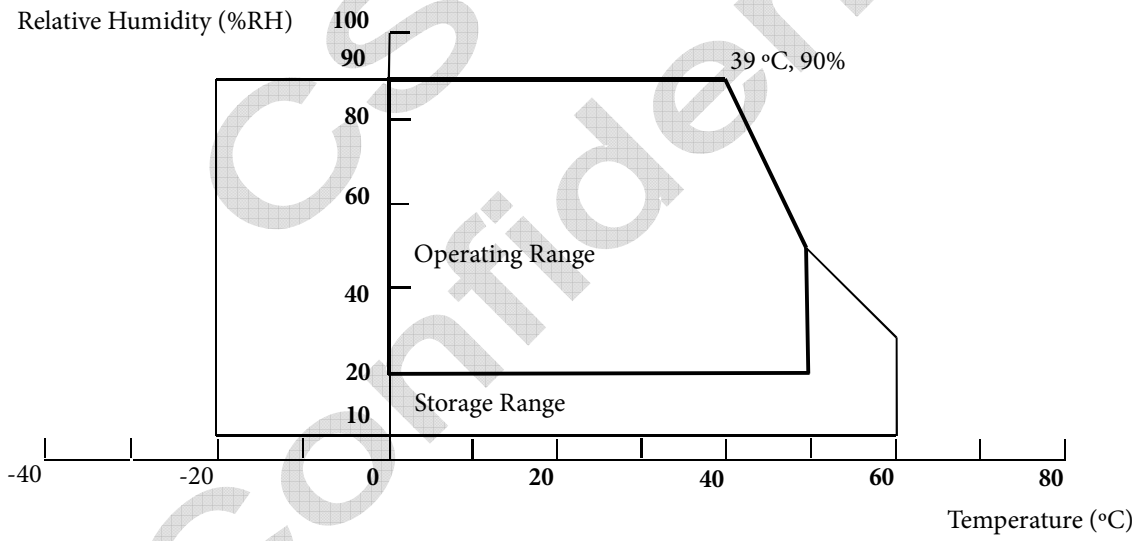


Fig. **2.1** Operating and storage environment

(a) 90%RH maximum (Ta ≤ 39 °C).

(b) Wet-bulb temperature should be 39 °C maximum (Ta > 39 °C).

(c) No condensation.

(2) The storage temperature is between - 20 °C to 60 °C, and the operating ambient temperature is between 0 °C to 50 °C. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The TFT module including glass should be avoided any shock or vibration.

While testing shock and vibration, the fixture holding the module should be assured to be hard and rigid enough to prevent the module twisted or bent by the fixture. The test conditions should be less than:

Shock (Non-operating): 35 G, 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Vibration (Non-operating): Random 1.0 Grms, 10 ~ 200 Hz, 10 min, 1 time for each X, Y, Z.

2.3 Package Storage

When storing modules as spares for a long time, please follow the precaution instructions:

(1) Do not store the module in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 0 °C to 35 °C in normal humidity.

(2) The module shall be stored in a dark area and avoided to be exposed in direct sunlight or fluorescent light.

3. Electrical Specification

3.1 Electrical Characteristics

3.1.1 Power Consumption (Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	2.0	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.38	0.49	A	(3)
	Horizontal Stripe	I_{CC}	-	0.78	1.01	A	
	Black Pattern	I_{CC}	-	0.34	0.44	A	

Note:

(1) The ripple voltage should be controlled less than 10% of V_{CC}.

(2) Measurement condition: $V_{CC=12V}$ rising time = 470 μs.

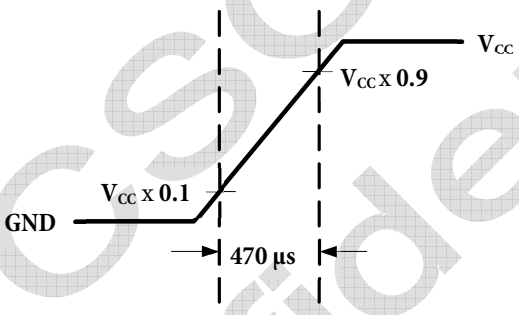
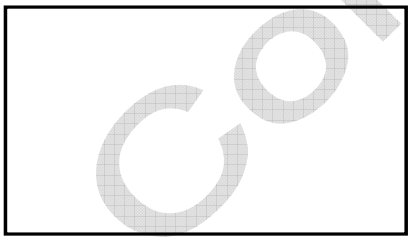


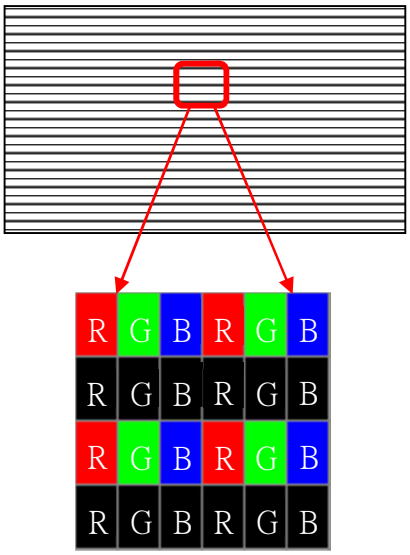
Fig. 3.1 V_{CC} rising time condition

(3) Measurement condition: V_{CC} = 12 V, Ta = 25 ± 2 °C, F = 120 Hz. The test patterns are shown as below.

A. White Pattern



B. Horizontal Pattern



C. Black Pattern

Fig. 3.2 Test patterns

3.1.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+ 100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	- 100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$\|V_{ID}\|$	200	400	600	mV	
	Terminating Resistor	R_T	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note:

(1) The LVDS input signal has been defined as follows:

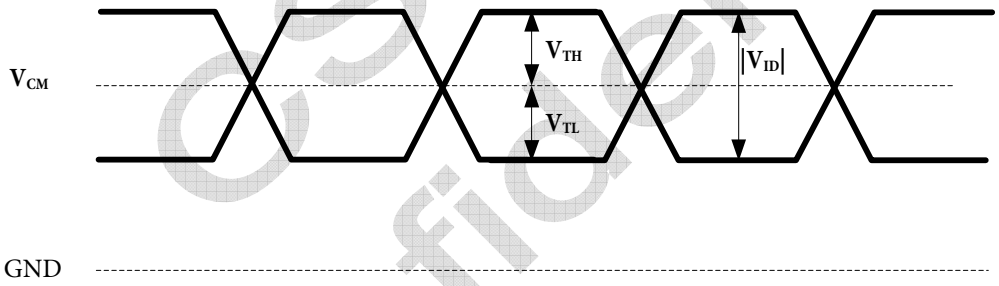


Fig. 3.3 LVDS input signal

3.2 Backlight Converter Unit

3.2.1 LED Converter Electrical Characteristics (Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Consumption		$P_{BL(2D)}$	-	62.13	67.96	W_{att}	No dimming
		$P_{BL(3D)}$	-	33.65	35.34	W_{att}	
Input Voltage		V_{BL}	21.6	24.0	26.4	V	
Input Current		$I_{BL(2D)}$	-	2.59	3.15	A	No dimming
		$I_{BL(3D)}$	-	1.40	1.64	A	
Input Inrush Current		I_{RS-VIN}	-	-	4.10	A	(1)
		I_{RS-EN}	-	-	5.67	A	(2)
On/Off Control Voltage	On	V_{BLON}	2.5	3.3	3.6	V	
	Off		0.0	-	0.8	V	
On/Off Control Current	-	I_{BLON}	-	-	1.5	mA	
PWM Dimming Control Voltage	Max.	V_{PDIM}	2.5	3.3	3.6	V	
	Min.		0.0	-	0.8	V	
External PWM Control Current		I_{P-DIM}	-	-	2	mA	
PWM Dimming Frequency		F_{PWM}	140	180	240	Hz	
Dimming Duty Ratio		D_{DIM}	10	-	100	%	(3)
DET Status Signal		DET HI	Open Collector				
		DET Low	0.0		0.8	V	
Input Impedance		R_{IN}	300			Kohm	

Note:

(1) The measurement condition: V_{BL} rising time is 20 ms. (V_{BL} from 10% ~ 90%)

(2) The measurement condition: the V_{BL} = 24V, and then on the V_{BLON} = 3.3V.

(3) Less than 10% dimming control is functional well and no backlight happens to shut down.

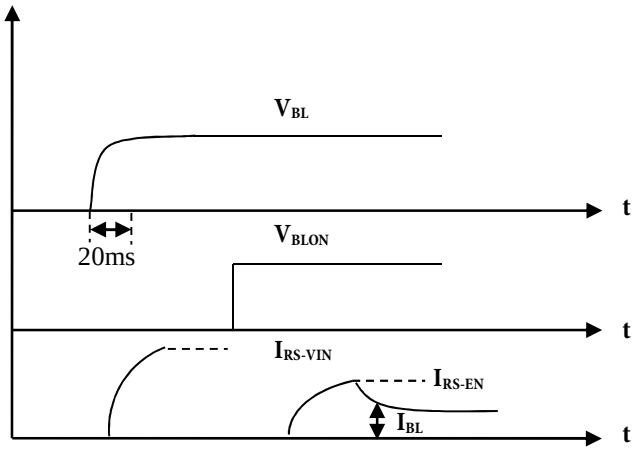


Fig. 3.4 The timing sequence diagram of inrush current measurement

3.2.2 LED Converter Power Sequence

No	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
1	VBL Rising Time	Tr	20	—	—	ms	See Fig.3.5
2	VBL Falling Time Time	Tf	20	—	—	ms	
3	VBLON Rising Time	Tr1	—	—	100	ms	
4	VBLON Falling Time	Tf1	—	—	100	ms	
5	VBL to VP_DIM Delay Time	T1	500	—	—	ms	
6	BLON Delay Time	T2	250	—	—	ms	
7	BLON Off Time	T3	0	—	—	ms	
8	VP_DIM Off Time	T4	250	—	—	ms	

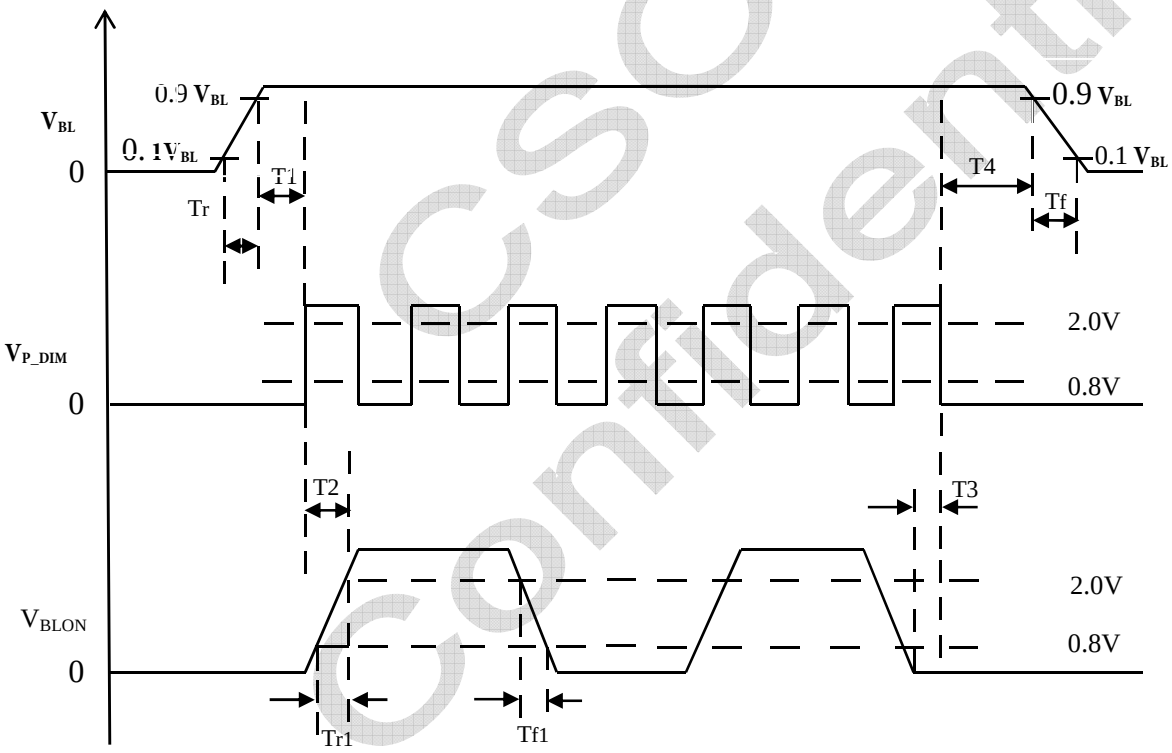


Fig. 3.5 The power sequence of V_{BL} and V_{BLON}

Note :The power sequence.

Power On : VBL > VP_DIM >VBLON

Power Off: V_{BLON} >= V_{P_DIM}> V_{BL}

4. Input Terminal Pin Assignment

4.1 TFT LCD Module

CN1: CT000041-513C (FCN)or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	N.C	No Connection	(1)
2	SCL	I2C Serial Clock (for 3D format selection function)	
3	SDA	I2C Serial Data (for 3D format selection function)	
4	N.C	No Connection	(1)
5	L/R_O	Output Signal for Left Right Glasses Control (High :Left Glass turn on Low: Right glass turn on)	
6	N.C.	No Connection	
7	SELLVDS	Input signal for LVDS Data Format Selection (Hi:VESA Format,Low or Open JEIDA Format)	(2)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd Pixel Negative LVDS Differential Data Input. Channel 0	
13	ORX0+	Odd Pixel Negative LVDS Differential Data Input. Channel 0	
14	ORX1-	Odd Pixel Negative LVDS Differential Data Input. Channel 1	
15	ORX1+	Odd Pixel Negative LVDS Differential Data Input. Channel 1	
16	ORX2-	Odd Pixel Negative LVDS Differential Data Input. Channel 2	
17	ORX2+	Odd Pixel Negative LVDS Differential Data Input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd Pixel Negative LVDS Differential Clock Input	
20	OCLK+	Odd Pixel Positive LVDS Differential Clock Input	
21	GND	Ground	
22	ORX3-	Odd Pixel Negative LVDS Differential Data Input. Channel 3	
23	ORX3+	Odd Pixel Positive LVDS Differential Data Input. Channel 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	2D/3D	Input Signal for 2D/3D Mode Selection (High:3D Enable,LOW:3D Disable)	
27	N.C.	No Connection	
28	ERX0-	Even Pixel Negative LVDS Differential Data input. Channel 0	
29	ERX0+	Even Pixel Negative LVDS Differential Data input. Channel 0	
30	ERX1-	Even Pixel Negative LVDS Differential Data input. Channel 1	
31	ERX1+	Even Pixel Negative LVDS Differential Data input. Channel 1	

32	ERX2-	Even Pixel Negative LVDS Differential Data input. Channel 2	
33	ERX2+	Even Pixel Negative LVDS Differential Data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even Pixel Negative LVDS Differential Clock Input.	
36	ECLK+	Even Pixel Positive LVDS Differential Clock Input.	
37	GND	Ground	
38	ERX3-	Even Pixel Negative LVDS Differential Data Input. Channel 3	
39	ERX3+	Even Pixel Positive LVDS Differential Data Input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

Note:

(1) For CSOT internal only, please let it open.

(2) High: connect to + 3.3 V →VESA Format; Low: connect to GND or Open → JEIDA format.

(3) The first LVDS data is ODD LVDS data

(4)The direction of pin assignment is shown as below:

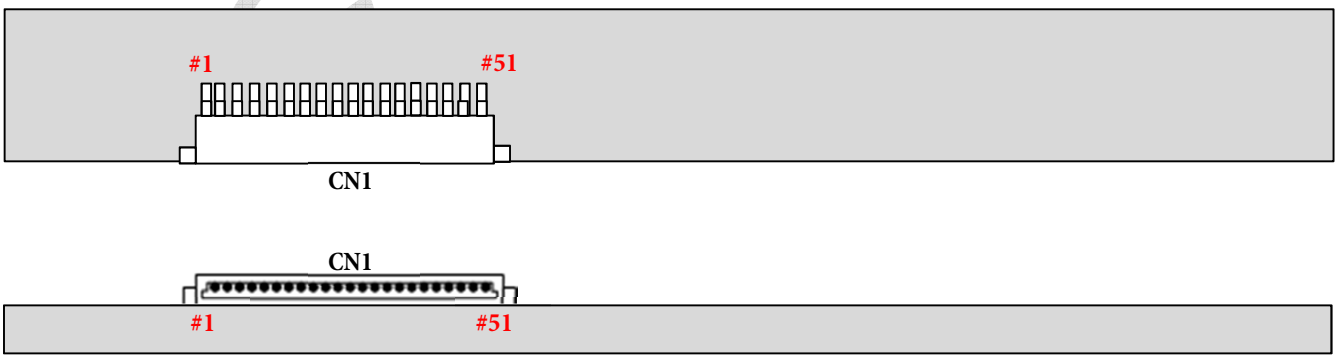


Fig. 4.1 LVDS connector direction sketch map

4.2 Converter Unit

Converter Input Connector Pin Definition

CN1: 50308-0140N-002 (Aces) (see Note (1))

Pin No.	Symbol	Feature
1	V_{BL}	Power Supply, + 24 V DC Regulated
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	DET	Normal (0 ~ 0.8 V), Abnormal (Open Collector)
12	BLON	BLON/OFF, BLON Floating: BLU ON
13	NC	NC
14	P_DIM	PWM Dimming Control (Open for 100%)

Note (1):

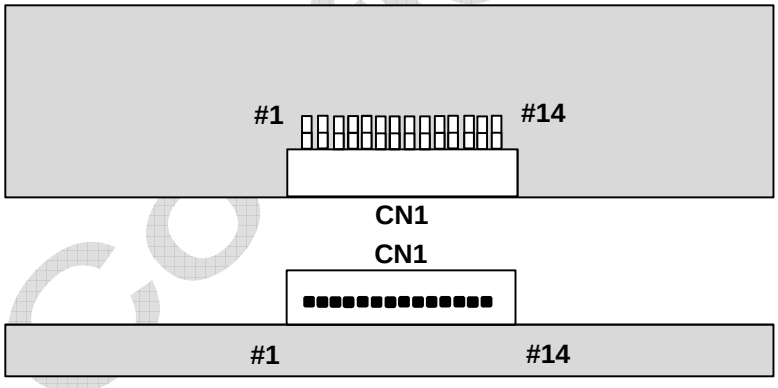


Fig. 4.2 Power input connector direction sketch map

Attention:

If the external PWM function includes 10% dimming ratio, the judge conditions are as below:

(1) Backlight module must be lighted on normally.

(2) All protection functions must work normally.

(3) Uniformity and flicker could not be guaranteed.

4.3 Block Diagram of Interface

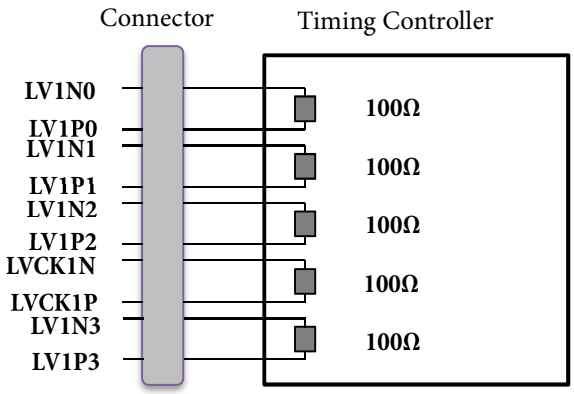


Fig. 4.3 Block diagram of interface

Attention:

(1) LCD module uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.4 LVDS Interface

4.4.1 VESA Format (SELLVDS = H)

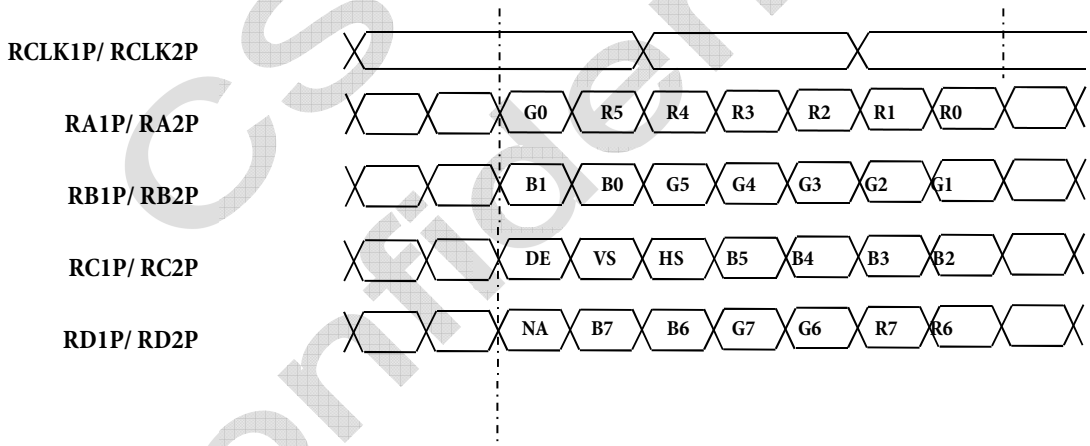


Fig. 4.4 VESA format

4.4.2 JEIDA Format (SELLVDS = L or Open)

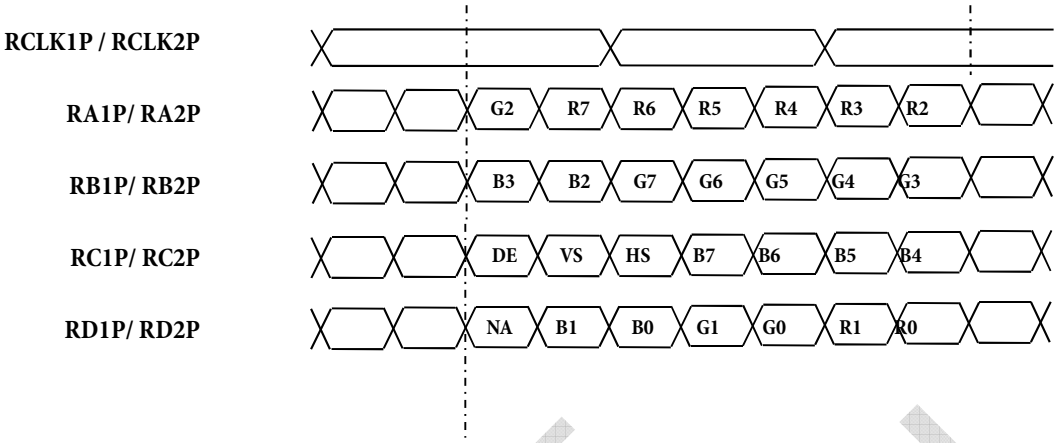


Fig. 4.5 JEIDA format

4.5 Color Data Input Assignment

The brightness of each primary color is based on the 8-bit gray scale data input for each color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus.

Data Input Color		Data Signal																							
		Red								Green								Blue							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Red (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1022)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1022)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Blue (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Attention:

0: Low level voltage; 1: High level voltage.

5. Interface Timing

5.1 Timing Table (DE Only Mode)

Signal		Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock		Frequency	FCLK (= 1 / TCLK)	60	74.25	77	MHz	(2)
		Input cycle to cycle jitter	Trcl	-	-	200	ps	(3)
		Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	-	Fclkin+2%	MHz	(4)
		Spread spectrum modulation frequency	FSSM			200	KHz	
LVDS Receiver Data		Receiver Skew Margin	TRSM	-400	-	400	ps	(5)
Frame Rate		2D Mode	F	57	60	62	Hz	
		3D Mode	F	60	60	60	Hz	(7)
Vertical Term	2D	Total	TV	1115	1125	1380	TH	TV = TVD + TVB
		Display	TVD		1080		TH	
		Blank	TVB	35	45	300	TH	
	3D	Total	TV		1125		TH	(6) , (8)
		Display	TVD		1080		TH	
		Blank	TVB		45		TH	
Horizontal Term	2D	Total	TH	1050	1100	1150	TCLK	TH = THD + THB
		Display	THD		960		TCLK	
		Blank	THB	90	140	190	TCLK	
	3D	Total	TH	1050	1100	1150	TCLK	TH = THD + THB
		Display	THD		960		TCLK	
		Blank	THB	90	140	190	TCLK	

Notes:

(1)The module is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

(2) Please make sure the range of pixel clock follows the following equations:

Fclkin(max) ≥ Fmax×Tv×Th

Fmin×Tv×Th≥Fclkin(min)

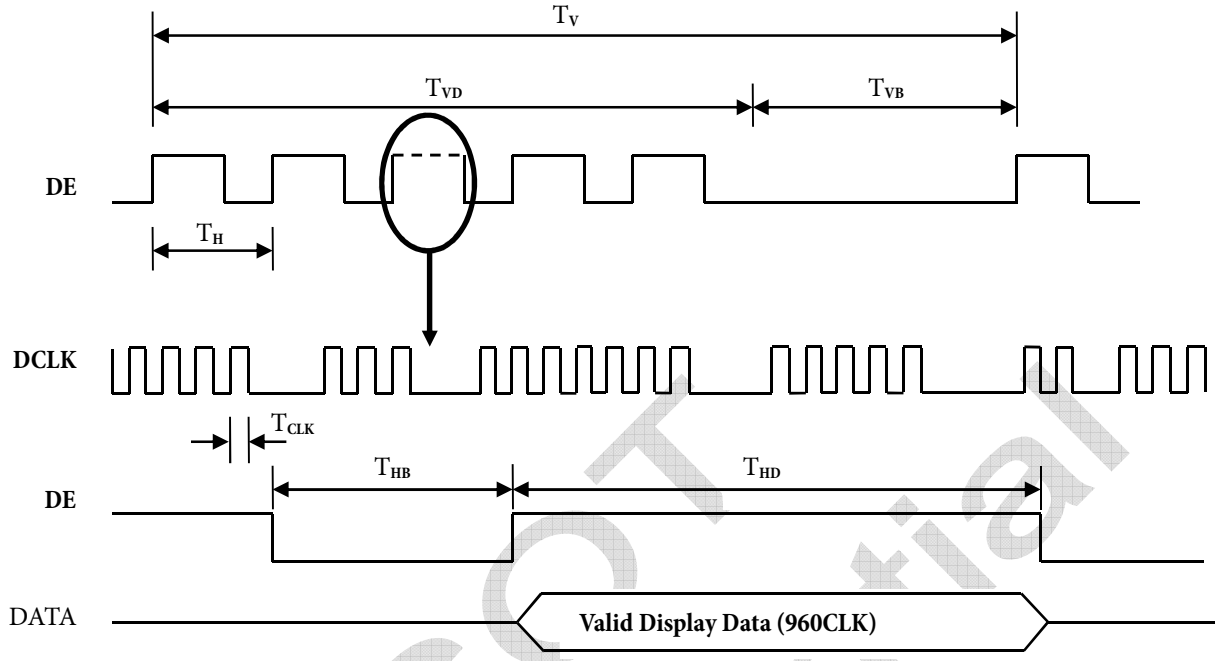


Fig. 5.1 Interface signal timing diagram

(3) The input clock cycle-to-cycle jitter is defined as the following figure. Trcl = I T1– TI

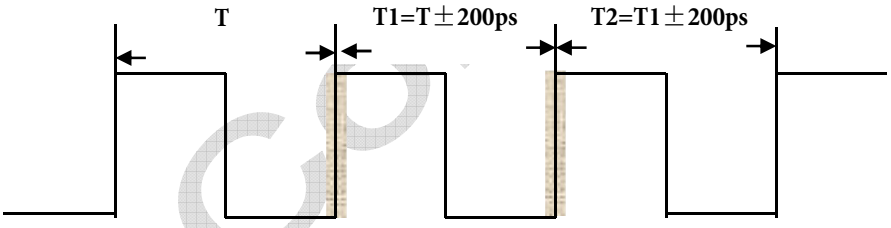
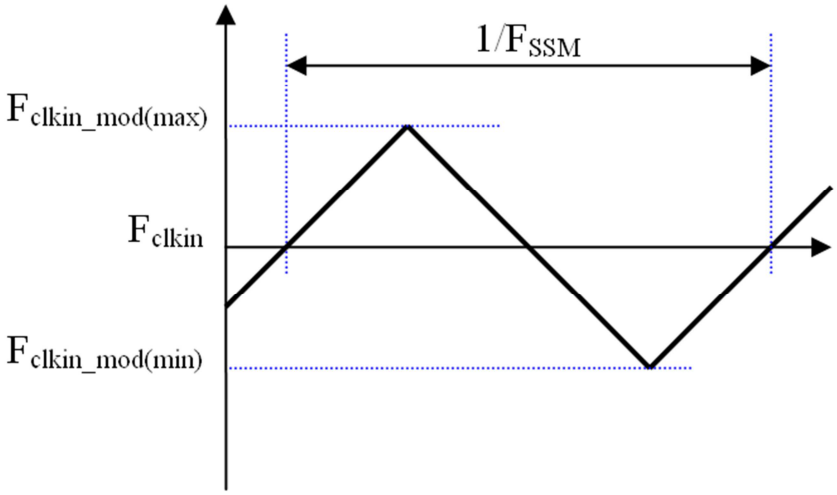


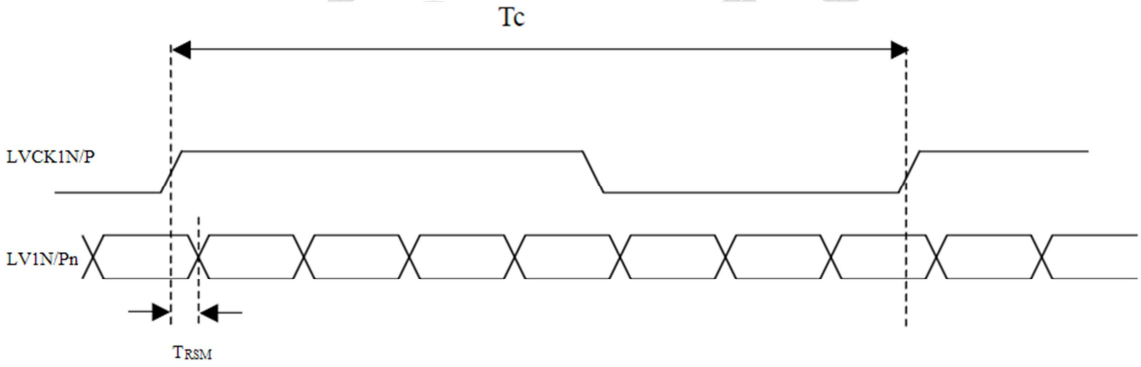
Fig. 5.2 jitter

(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.



(5) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

LVDS RECEIVERINTERFACE TIMING DIAGRAM



(6) Please fix the vertical timing in 3D mode.(Vertical Total =1125/Display=1080/Blank=45)

(7) In 3D mode, the setup F should be in Typ. In order to ensure that the eclectic function performance to avoid no display symptom.(Except picture quality symptom)

(8) In 3D mode, the setup Tv and Tvb should be in Typ. In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom)

5.2 Power On/Off Sequence

5.2.1 Power On/Off Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

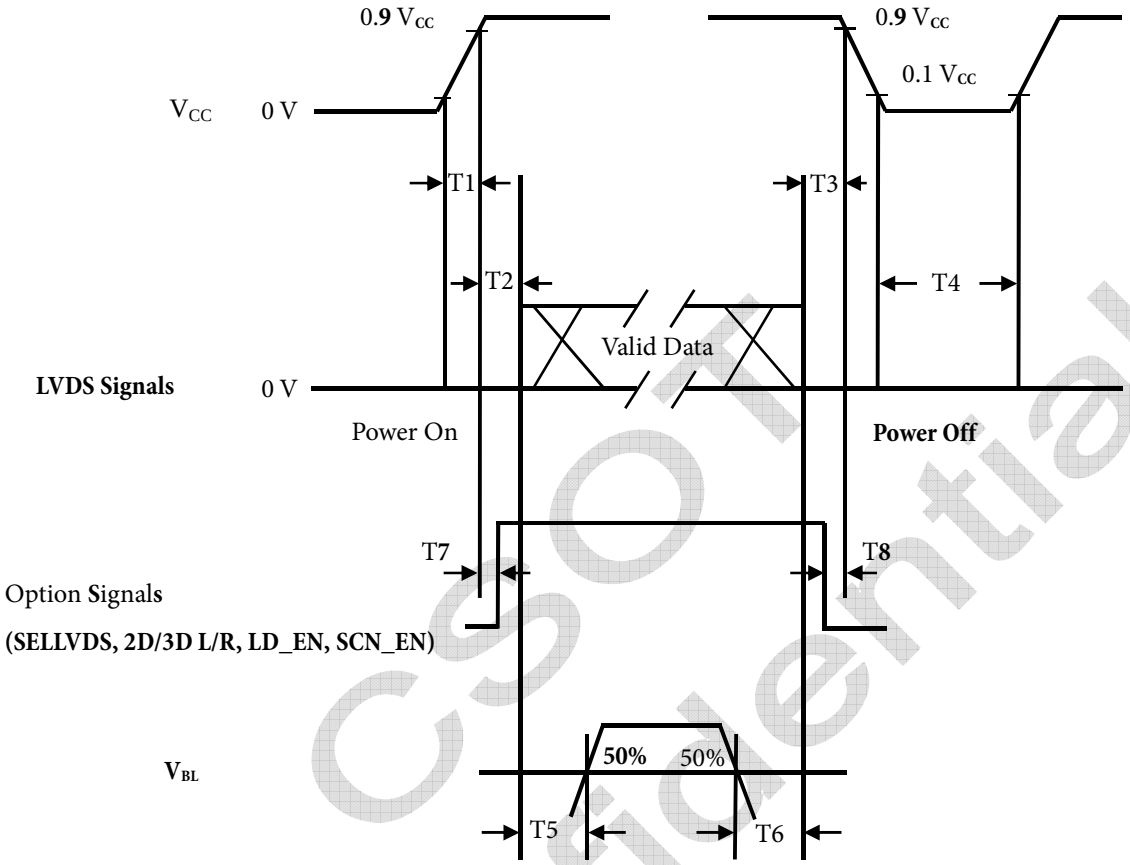


Fig. 5.3 Power on/off sequence

5.2.2 2D/3D Change Signal Sequence without Vcc Turn off and Turn on

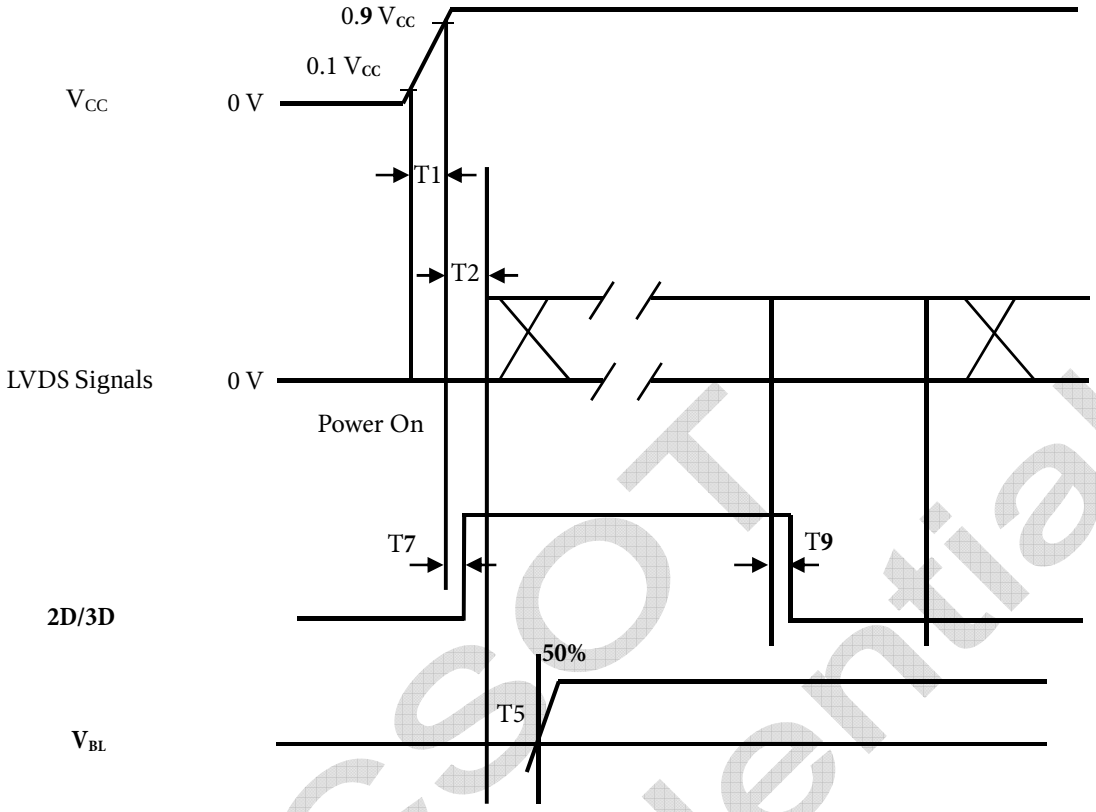


Fig. 5.4 2D/3D Power on/off sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	Min.
T1	0.5	-	10.0	ms
T2	0.0	-	-	ms
T3	0.0	-	-	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms
T7	-	-	T2	ms
T8	-	-	T3	ms
T9	0.0	-	10.0	ms

Attention:

(1)While system turn from 2D/3D function to 3D/2D function,the V_{BL} signal should be always high .

(2) The supply voltage of the external system for the module input should follow the definition of V_{CC}.

(3) Apply the lightbar voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(4) In case that V_{CC} is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.

(5) T4 should be measured after the module has been fully discharged between power off and on period.

(6) Interface signal shall not be kept at high impedance when the power is on.

6. Optical Characteristics

6.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25 ± 2	°C
Ambient Humidity	H_A	50 ± 10	% RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Light Source Current (Each Unit)	I_L	120	mA
Vertical Refresh Rate	F_R	120	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 45 minutes after lighting the backlight and in the windless environment.

To measure the LCD module, it is suggested to set up the standard measurement system as Fig. 7.1. The measuring area S should contain at least 500 pixels of the LCD module as illustrated in Fig. 7.2 (A means the area allocated to one pixel). In this model, for example, the minimum measuring distance Z is 370 mm when θ is 2 degree. Hence, 500 mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

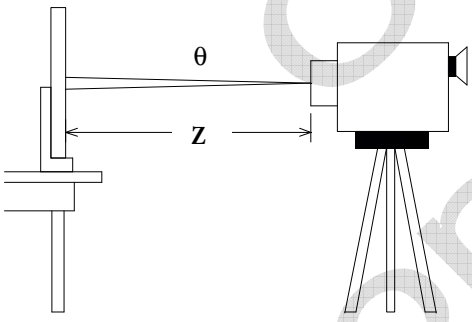


Fig. 6.1 The standard set-up system of measurement

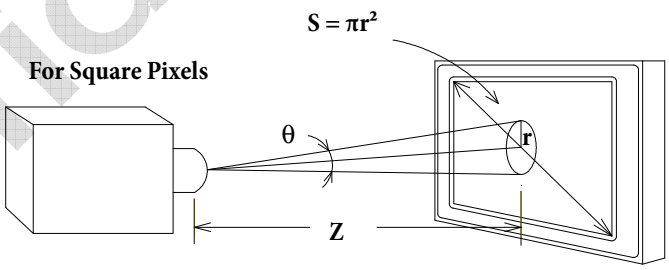


Fig. 6.2 The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant \textbf{500 pixels}$$

N means the actual number of the pixels in the area S.

6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTI Scope-SA and ELDIM EZ contrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	$\theta_H = 0°$, $\theta_V = 0°$ Normal direction at center point of the LCD module.	-	4000	-	-	(1) (2)
Response Time		T_L		-	6.5	-	ms	(3) OPTI Scope-SA
Center Luminance		L_{W-2D}		320	400	-	cd/m^2	(2) (4)
		L_{W-3D}		-	50	-	-	(8)
3D Crosstalk		CT-3D		-	TBD	-	-	(8)
Uniformity of White Screen		-		75	-	-	%	(2) (5)
Color Chromaticity (CIE1931)	Red	R_X		Typ. - 0.03	0.639	Typ. + 0.03	-	(2) (6)
		R_Y			0.335		-	
	Green	G_X			0.319		-	
		G_Y			0.626		-	
	Blue	B_X			0.155		-	
		B_Y			0.052		-	
	White	W_X			0.280		-	
		W_Y			0.290		-	
	Color Gamut	CG		-	72	-	% NTSC	
Viewing Angle	Horizontal	θ_{H+}	CR ≥ 10	-	89	-	Deg.	(7) ELDIM EZ Contrast
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\textbf{CR-W}}{\textbf{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 7.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000, (TOPCON) SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7

could be involved after being calibrated with a spectroradiometer on each stage of a product.

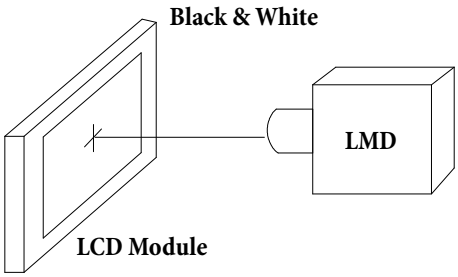


Fig. 6.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X\ to\ Y}$ is the transition time from luminance ratio X to Y. X and Y are two different luminance ratios among 0%, 25%, 50%, 75%, and 100% luminance. The transition time $t_{X\ to\ Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X < Y) as illustrated in Fig.3. When X > Y, the definition of $t_{X\ to\ Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate F_R = 60Hz.

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\%\ to\ 0\%}$	$t_{50\%\ to\ 0\%}$	$t_{75\%\ to\ 0\%}$	$t_{100\%\ to\ 0\%}$
	25%	$t_{0\%\ to\ 25\%}$		$t_{50\%\ to\ 25\%}$	$t_{75\%\ to\ 25\%}$	$t_{100\%\ to\ 25\%}$
	50%	$t_{0\%\ to\ 50\%}$	$t_{25\%\ to\ 50\%}$		$t_{75\%\ to\ 50\%}$	$t_{100\%\ to\ 50\%}$
	75%	$t_{0\%\ to\ 75\%}$	$t_{25\%\ to\ 75\%}$	$t_{50\%\ to\ 75\%}$		$t_{100\%\ to\ 75\%}$
	100%	$t_{0\%\ to\ 100\%}$	$t_{25\%\ to\ 100\%}$	$t_{50\%\ to\ 100\%}$	$t_{75\%\ to\ 100\%}$	

$t_{X\ to\ Y}$ means the transition time from luminance ratio X to Y.

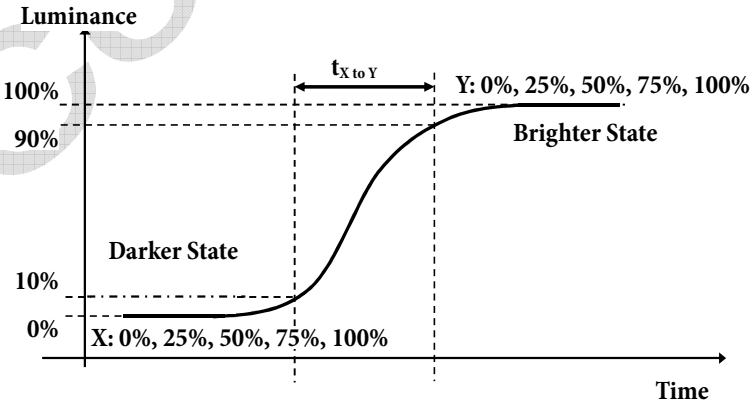


Fig. 6.4 The definition of $t_{X\ to\ Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center luminance (L_W):

The luminance is measured at the center point of the LCD module with full-screen displaying white. Fig. 7.5 shows the standard setup of luminance measurement.

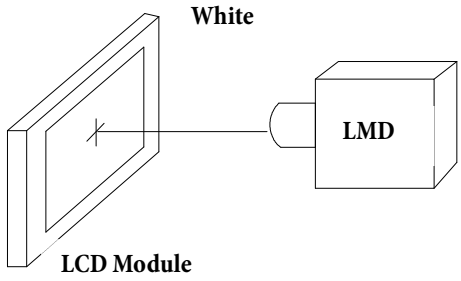


Fig. 6.5 The standard setup of luminance measurement

(5) Definition of uniformity of white screen:

The luminance Li (i from 1 to 5) is measured at the 5 points defined in Fig. 7.6. H and V indicate active area.

From the measured set of luminance values Li (i from 1 to 5), the minimum luminance is denoted as L_{min} and the maximum luminance is denoted as $L_{max.}$.The uniformity of white screen is defined according to

Uniformity = L_{min} / L_{max} x 100%.

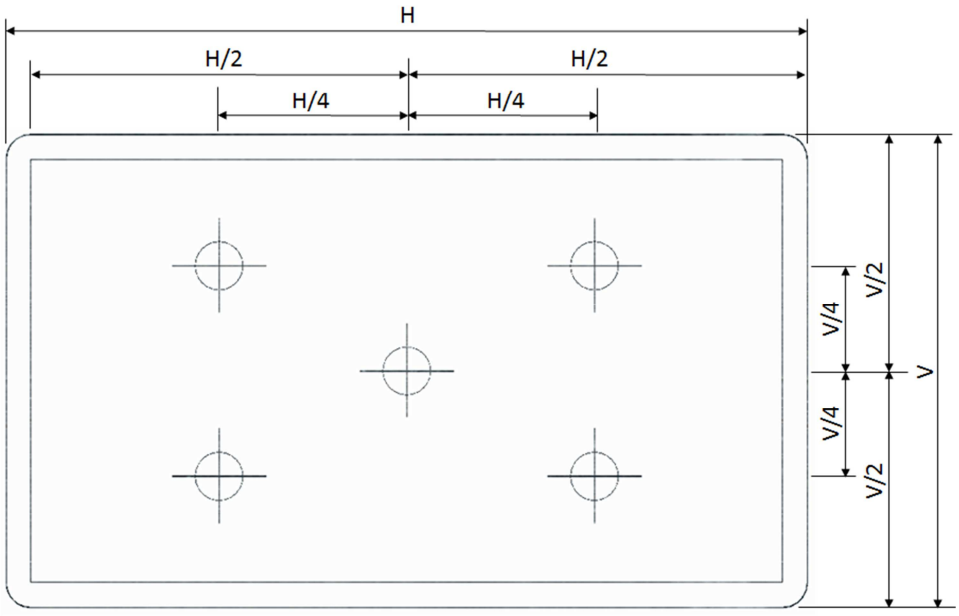


Fig. 6.6 Symbol "+ " defines the 5 measuring locations (1), (2), (3) ··· (5)

(6) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 7.7.

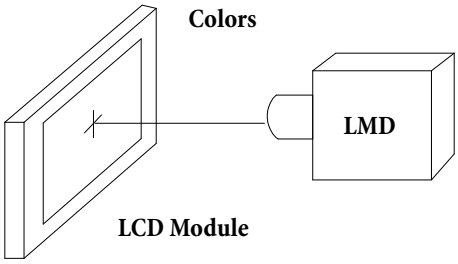


Fig. 6.7 The standard setup of color chromaticity measurement

(7) Definition of viewing angle coordinate system (θ_H, θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up θ_{V+} and down θ_{V-}; and two horizontal angles: right θ_{H+} and left θ_{H-}) as illustrated in Fig. 7.8. The contrast ratio is measured by ELDIM EZ Contrast.

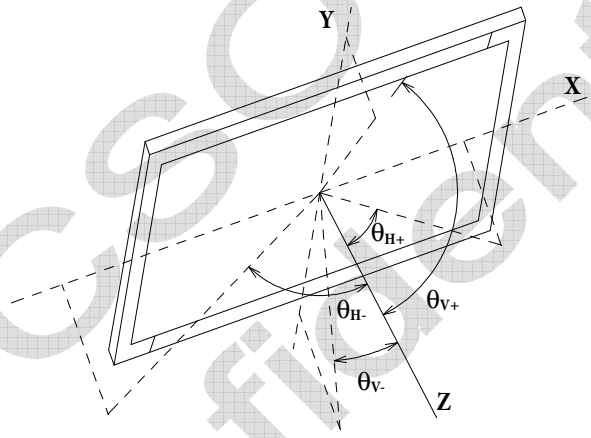
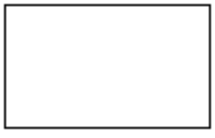
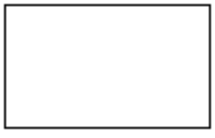


Fig. 6.8 Viewing angle coordination system

(8) Definition of the 3D mode performance:

Test pattern

Pattern	Left eye image	Right eye image	remark
WW			Left eye image: L255 Right eye image:L255 L(WW) is denoted as the luminance of "WW"
WB			Left eye image: L255 Right eye image:L0 L(WB) is denoted as the luminance of "WB"
BW			Left eye image: L0 Right eye image:L255 L(BW) is denoted as the luminance of "BW"

BB			Left eye image: L0 Right eye image:L0 L(BB) is denoted as the luminance of "BB"

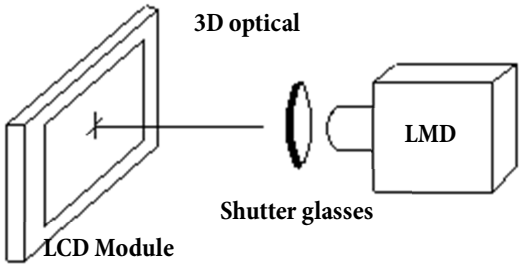


Fig. 6.9 3D optical measurement system

Measure the center point of the LCD module through the shutter glasses under 3D mode operation.

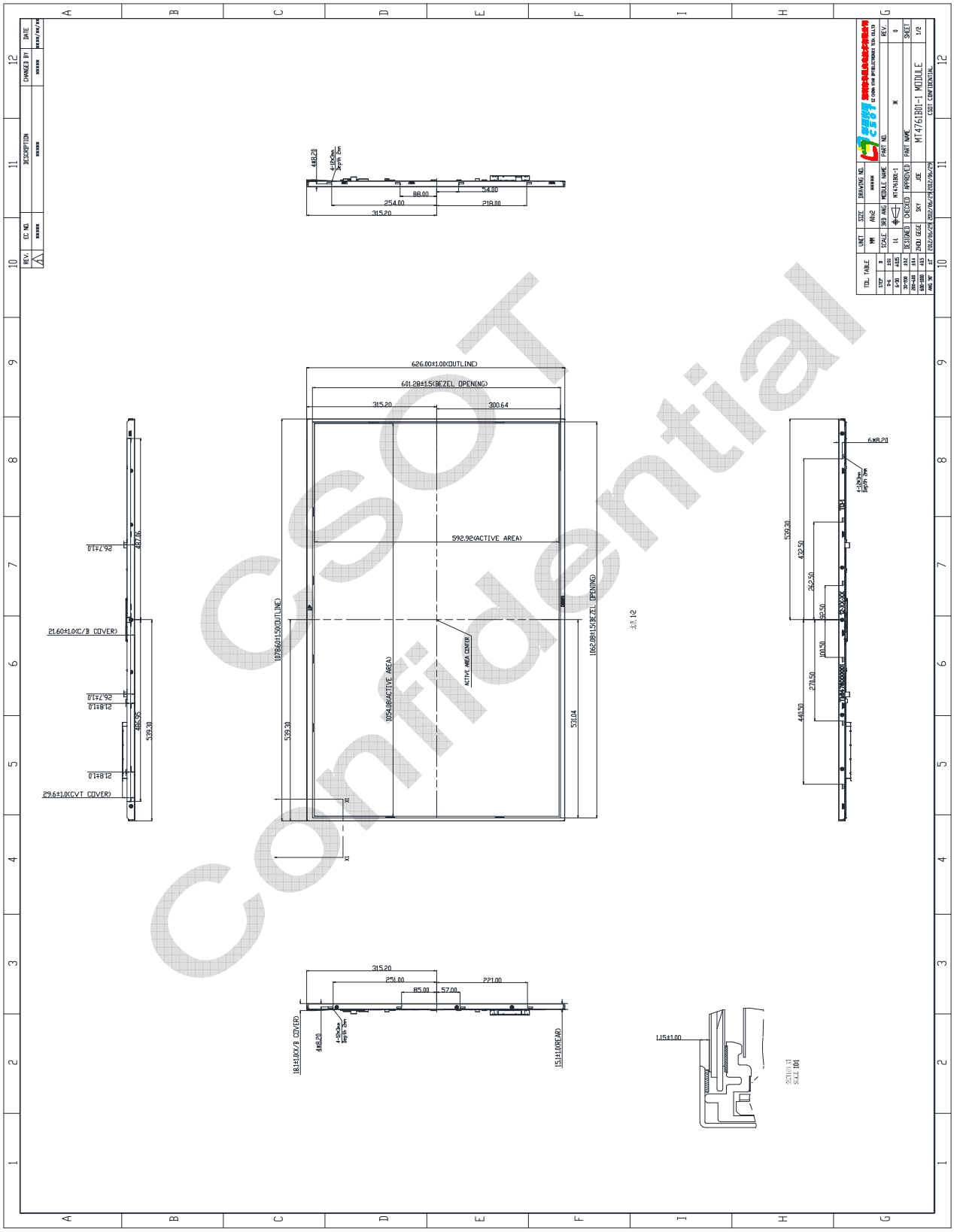
The 3D luminance (Lw-3D) is the luminance measured by LMD with well controlled shutter glasses at the center point of the LCD module with test pattern L(WW).

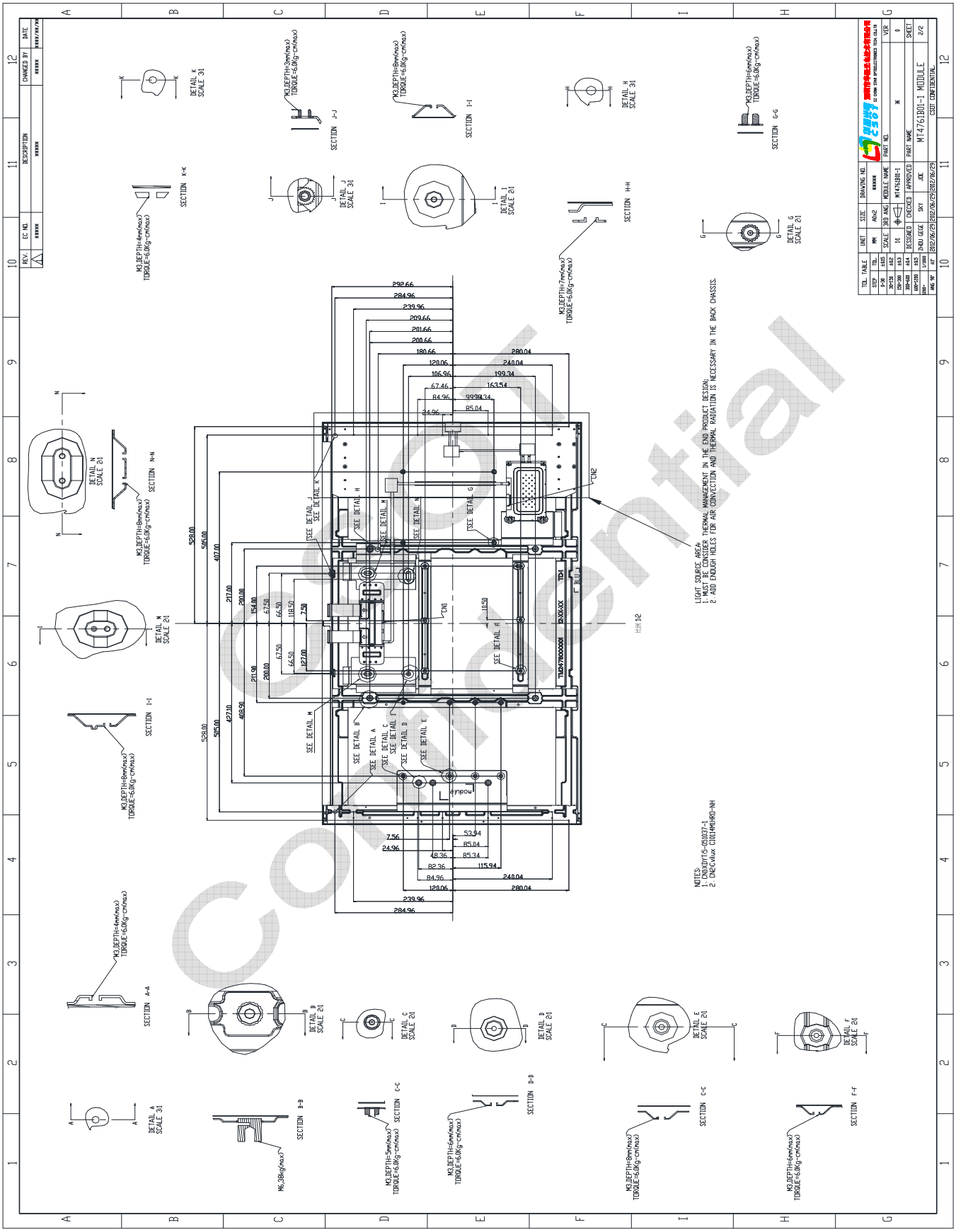
The 3D crosstalk is measured at the center point of the LCD module through right-eye glasses..

Definition of the 3D mode crosstalk: $\mathbf{CT\text{-}3D} = \frac{\mathbf{L(WB)\text{-}L(BB)}}{\mathbf{L(BW)\text{-}L(BB)}}$

7. Mechanical Characteristics

7.1 Measurement Conditions





7.2 Packing

7.2.1 Packing Specifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	22pcs / box	1175.0 (L) x 1066.0 (W) x 691.0 (H)	Net Weight: 198.0 Gross Weight: 209.7
Pallet	1	1200 (L) x 1100 (W) x 175 (H)	Net Weight: 19
Stack Layer	3		
Boxes per Pallet	1 box / pallet		
Pallet after Packing	22 pcs / pallet	1200 (L) x 1100 (W) x 866(H)	Gross Weight: 228.7

7.2.2 Packing Method

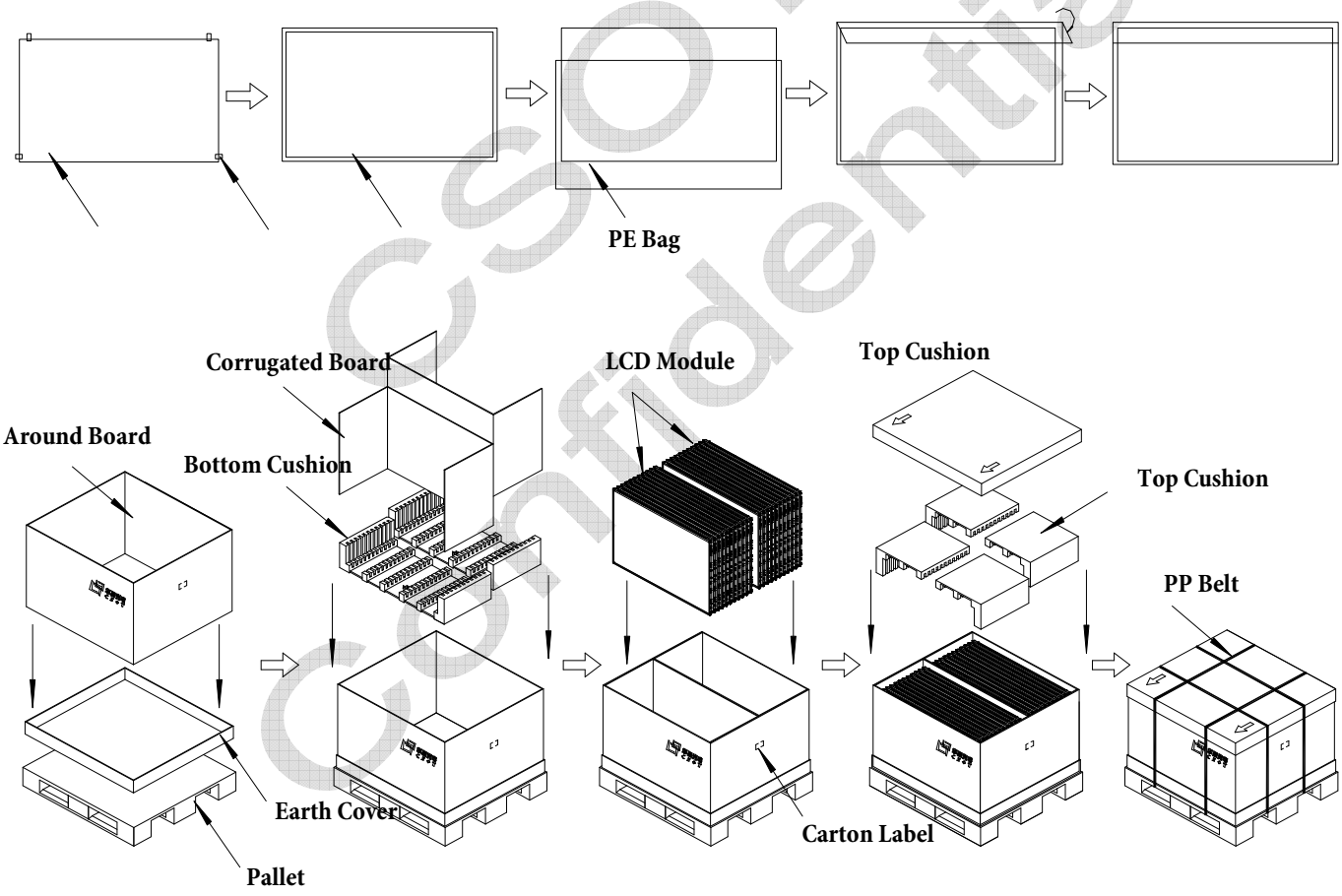
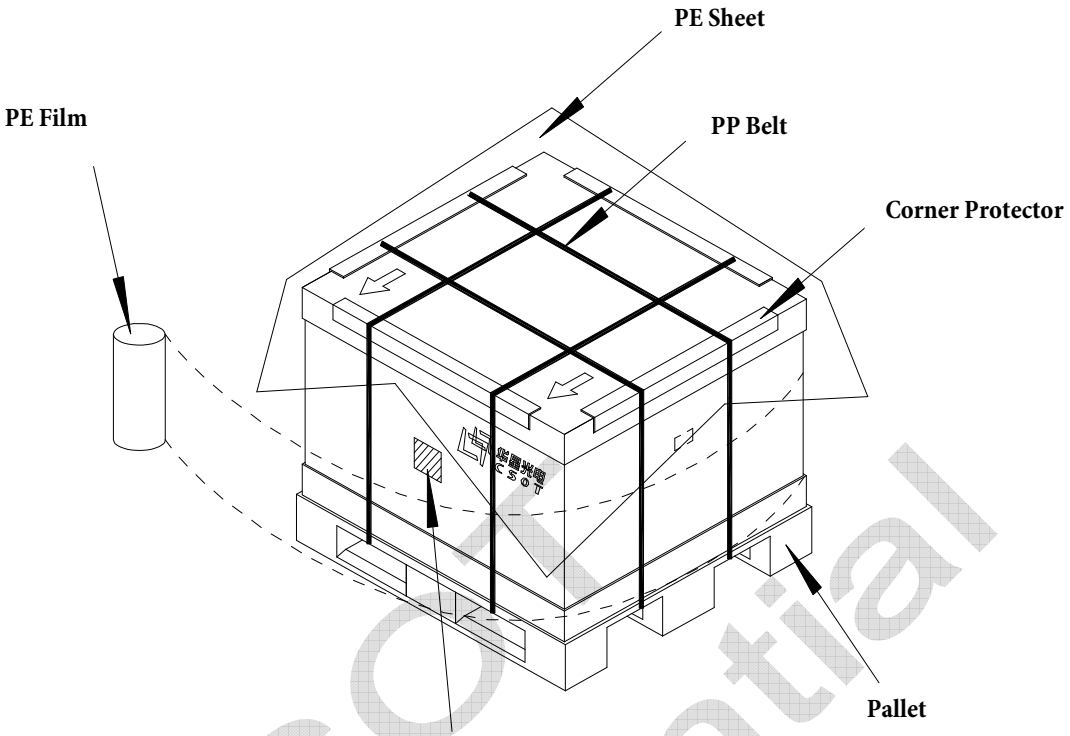


Fig. 7.1 Packing method (protector film stick on the front of the LCD module)



Pallet Label

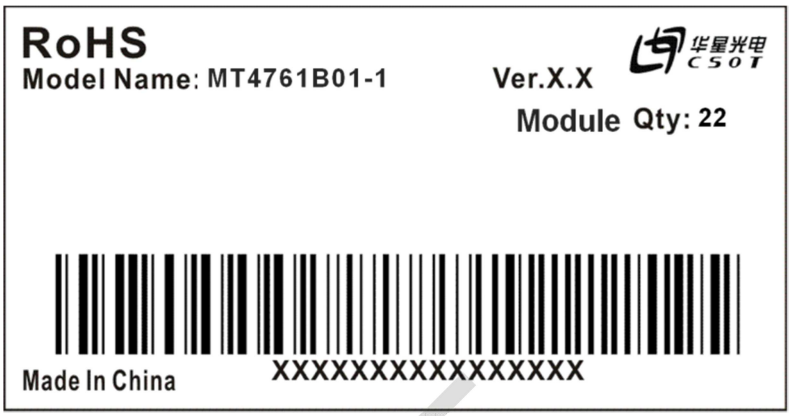
2 pcs Pallet label stick on the PE Film.

Relative to the two sides.

Fig. 7.2 Shipping method

8. Definition of Labels

8.1 Module Label



For RoHs compatible products, CSOT will add RoHS for identification.

Model Name: MT4761B01-1

Ver.X.X: Version, for example: 0.1, 0.2, … , 1.1, 1.2, …, 2.1, 2.2, …

WC (Week Code): XX XX

→ Week

→ Year

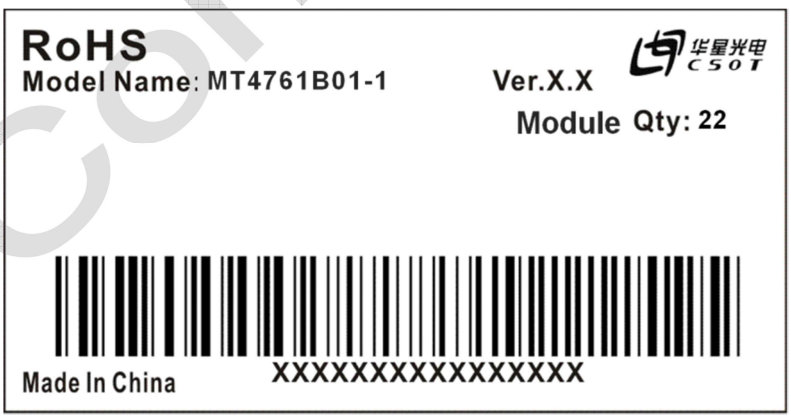
Year: 2010 = 10, 2011 = 11 … 2020 = 20, 2021 = 21…

Week: 01, 02, 03 …

Serial Number: XXXXXXXXXXXX XXXXXXXX

→ CSOT Internal Use

8.2 Carton Label



Serial Number: XXXXX XX XXXXX XXXXX

→ CSOT Internal Use

→ Year, Month, Date

→ Model Version Code

→ CSOT Internal Use

Manufactured Date:

Year: 2010 = 10, 2011 = 11…2020 = 20, 2021 = 21…

Month: 1~9, A~C, for Jan. ~ Dec.

Date: 01~31, for 1st to 31st

Model Version Code: Version of product, for example: 0.1, 0.2, 1.1, 1.2…

8.3 Pallet Label

Serial Number: XXX XX XXX XXXXX

- XXX → CSOT Internal Use
- XX → Year, Month
- XXX → Model Version Code
- XXXXX → CSOT Internal Use

9. Precautions

9.1 Assembly and Handling Precautions

(1) Do not apply rough force such as bending or twisting to the LCD module during assembly.

(2) It is recommended to assemble or install a LCD module into the user's system in clean working areas. The dust and oil may cause electrical short or damage the polarizer.

(3) Do not apply pressure or impulse to the LCD module to prevent the damage to LCD panel and backlight.

(4) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the LSI chips.

(5) Do not plug in or pull out the interface connector while the module is in operation.

(6) Do not disassemble the LCD module.

(7) Use soft dry cloth without chemicals for cleaning because the surface of polarizer is very soft and easily be scratched.

(8) Moisture can easily penetrate into the LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of the LCD module. Please store LCD modules in the specified storage conditions.

(10)When ambient temperature is lower than 10ºC, the display quality might be deteriorated. For example, the response time will become slow, and the starting voltage of LED light bar will be higher than that in room temperature.