

# MT4903

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

PRODUCT SUMMARY		
$V_{DSS}$	$I_D$	$R_{DS(ON)}$ (m $\Omega$ ) Typ
-30V	-3.0A	100@ $V_{GS}=-4.5V$
		67@ $V_{GS}=-10V$

### Features

- Super high dense cell design for low  $R_{DS(ON)}$
- Rugged and reliable
- Simple drive requirement
- Sot-23-6 package

### Applications

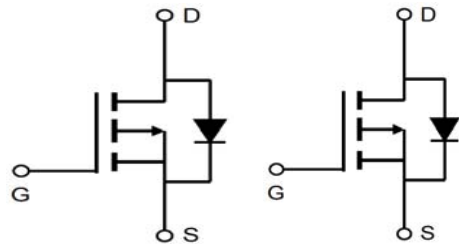
- Portable battery packs
- Load switch



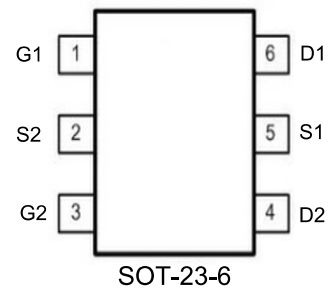
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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



### Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-3.0	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	-13	A
Maximum Power Dissipation	$P_D$	1.0	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	125	$^{\circ}C/W$
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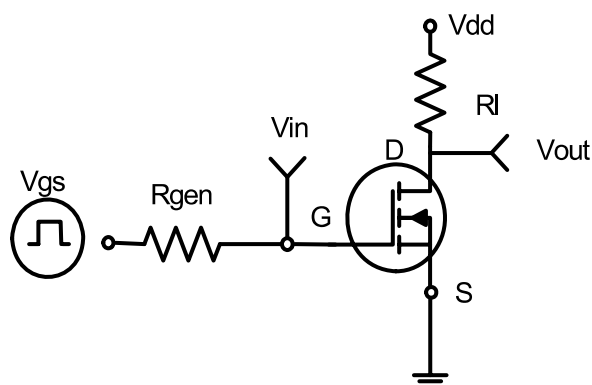
## Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>• Static Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.2	-1.8	-2.2	V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V	-	-	-1	μA
		V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 85°C	-	-	-30	
R <sub>DS(on)</sub>	Drain Source On State Resistance <sup>3</sup>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A	-	100	-	mΩ
		V <sub>GS</sub> =-10V, I <sub>D</sub> =-2A	-	67	-	
g <sub>fs</sub>	Forward Transconductance <sup>3</sup>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-2A	5	-	-	S
V <sub>SD</sub>	Diode Forward Voltage <sup>3</sup>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -2.6A	-	-0.8	-1.2	V
<b>• Dynamic Characteristics<sup>4</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10V, V <sub>GS</sub> =0V, f=1MHz	-	325	-	pF
C <sub>oss</sub>	Output Capacitance		-	63	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	37	-	
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A	-	3.2	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	0.6	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	0.9	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -10V, R <sub>L</sub> = 1.5Ω I <sub>D</sub> = -1.0A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 3Ω	-	11	-	nSec
t <sub>r</sub>	Rise Time		-	5.5	-	
T <sub>d(off)</sub>	Turn-Off Delay Time		-	22	-	
t <sub>f</sub>	Fall Time		-	8	-	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0, V <sub>DS</sub> =0, f=1MHz	-	3	-	Ω
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> = -2A, di/dt = 100A/μs	-	25	-	nSec
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	10	-	nC

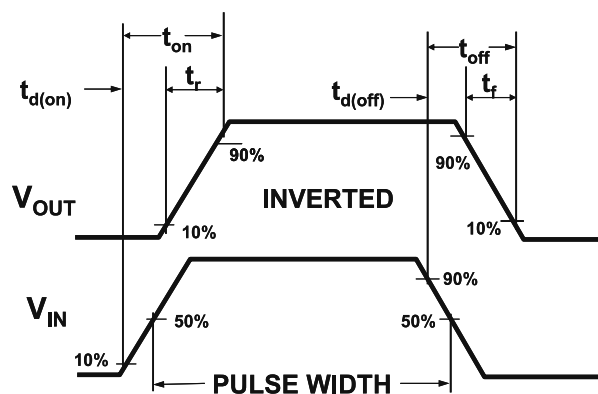
### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

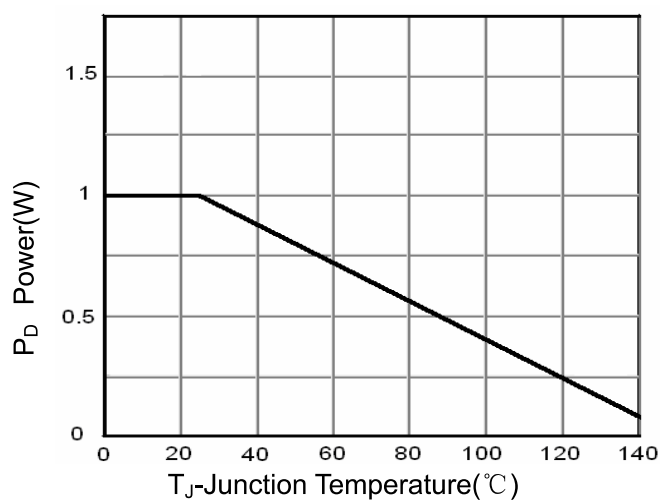
## Typical Electrical and Thermal Characteristics



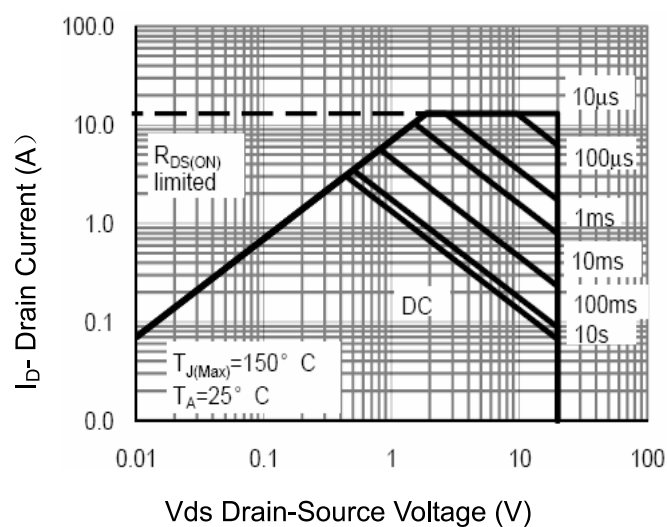
### Figure 1: Switching Test Circuit



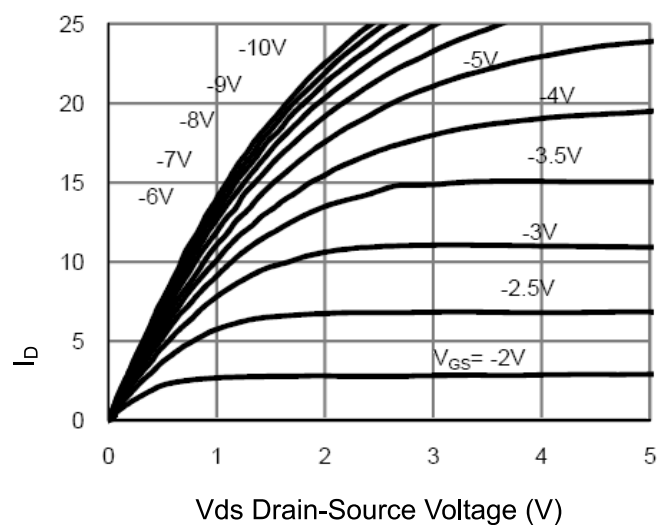
### Figure 2: Switching Waveforms



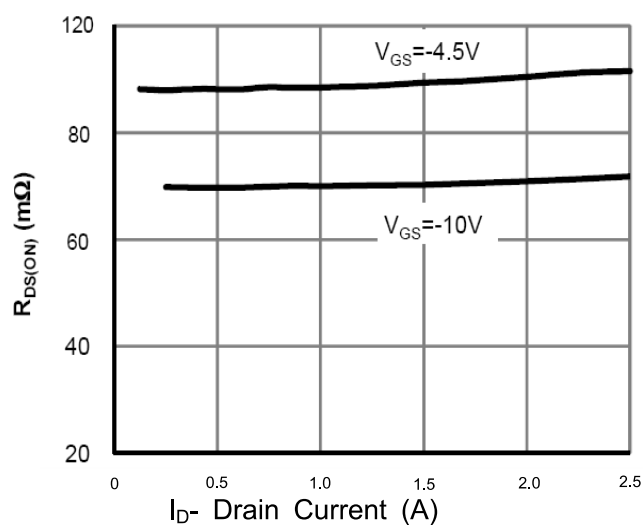
### Figure 3 Power Dissipation



### Figure 4 Safe Operation Area



### Figure 5 Output Characteristics



### Figure 6 Drain-Source On-Resistance

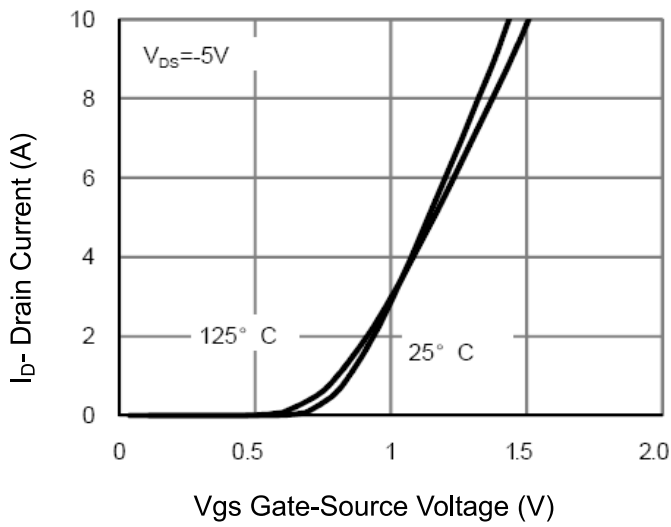


Figure 7 Transfer Characteristics

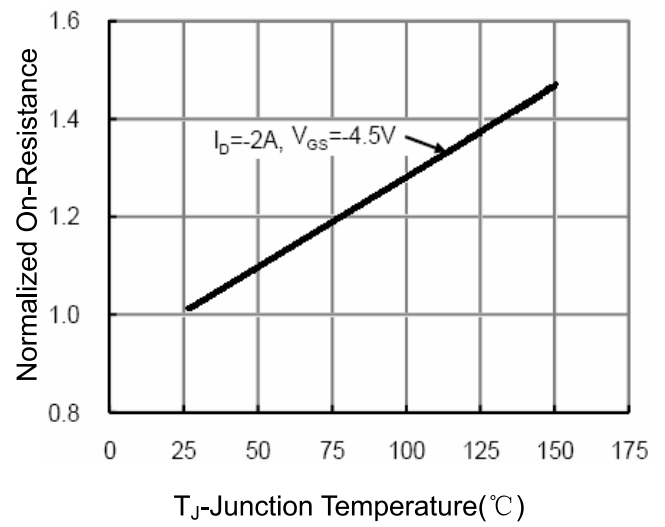


Figure 8 Drain-Source On-Resistance

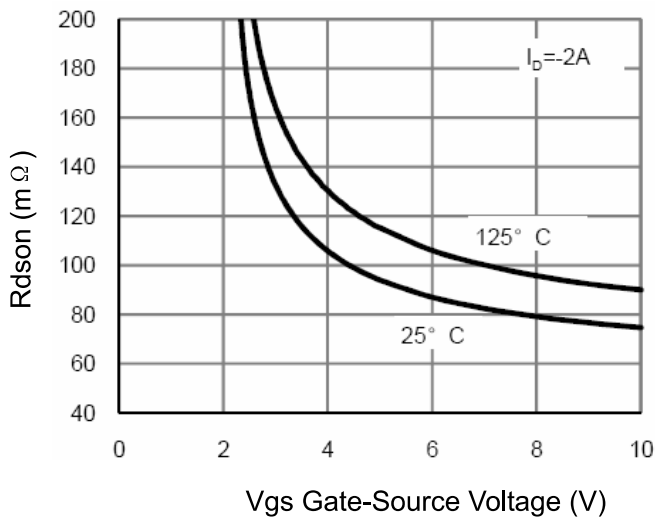
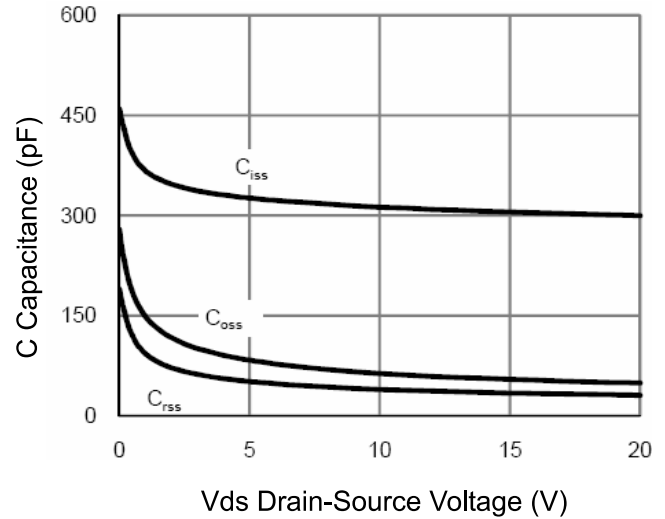
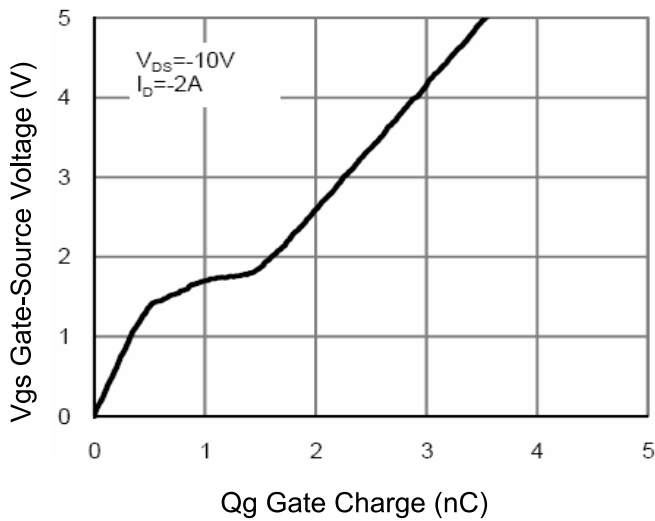
Figure 9  $R_{DS(on)}$  vs  $V_{GS}$ Figure 10 Capacitance vs  $V_{DS}$ 

Figure 11 Gate Charge

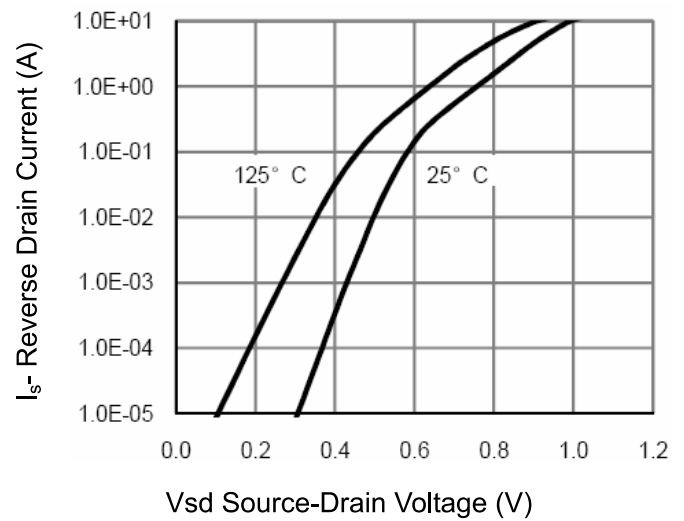
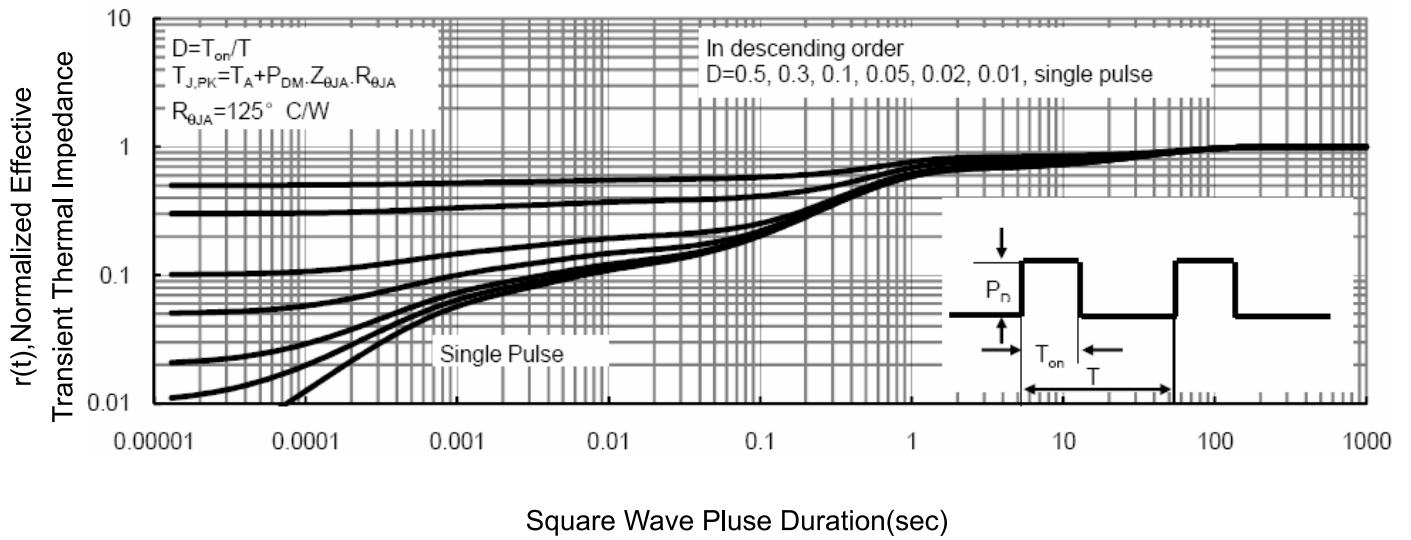


Figure 12 Source- Drain Diode Forward



**Figure 13 Normalized Maximum Transient Thermal Impedance**

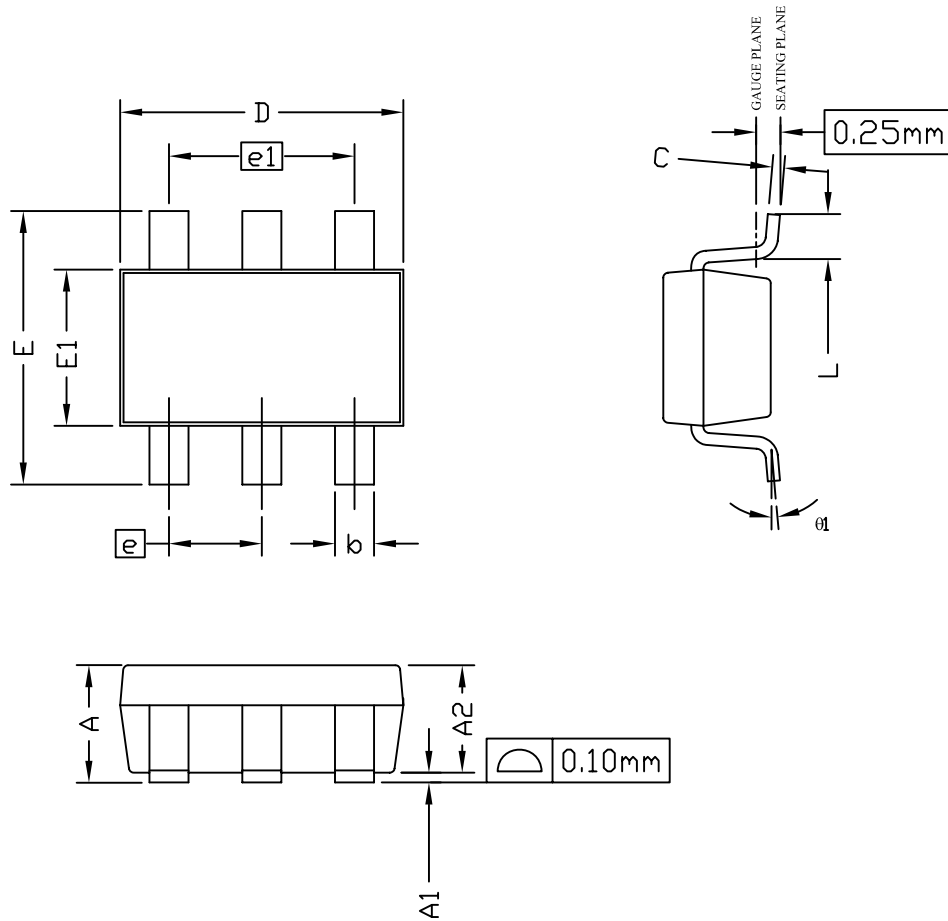
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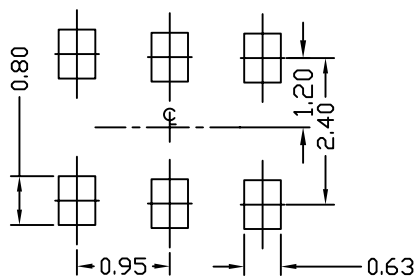
Version

rev B

## SOT23\_6 PACKAGE OUTLINE



## RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	—	1.25	0.035	—	0.049
A1	0.00	—	0.15	0.00	—	0.006
A2	0.70	1.10	1.20	0.028	0.043	0.047
b	0.30	0.40	0.50	0.012	0.016	0.020
C	0.08	0.13	0.20	0.003	0.005	0.008
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.50	2.80	3.10	0.098	0.110	0.122
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95 BSC.			0.037BSC.		
e1	1.90 BSC.			0.075 BSC.		
L	0.30	—	0.60	0.012	—	0.024
$\theta 1$	$0^\circ$	—	$8^\circ$	$0^\circ$	—	$8^\circ$

## NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
2. DIMENSION "L" IS MEASURED IN GAGE PLANE.
3. TOLERANCE  $\pm 0.100\text{ mm}$  (4 mil) UNLESS OTHERWISE SPECIFIED.
4. FOLLOWED FROM JEDEC MO-178C & MO-193C.
5. CONTROLLING DIMENSIONS IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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