MOS-TECH Semiconductor Co.,LTD
臺灣茂鈿半導體股份有限公司

MT4976

60V Complementary Power MOSFET

General Description

This complementary MOSFET device is produced using Mos-tech's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC/DC converter
- Power management
- LCD backlight inverter

Features

- **Q1**: **N-Channel**

  4.5 A, 60 V $R_{DS(on)}$ = 40 mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ = 45 mΩ @ V_{GS} = 4.5V

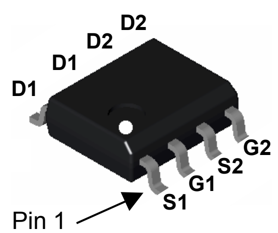
- **Q2**: **P-Channel**

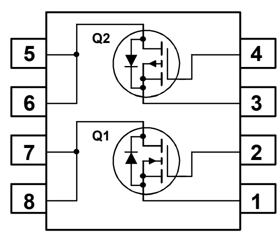
  –3.5 A, –60 V $R_{DS(on)}$ = 70 mΩ @ V_{GS} = –10V

  $R_{DS(on)}$ = 81 mΩ @ V_{GS} = –4.5V

- RoHS Compliant

SO-8





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DSS}	Drain-Source Voltage	60	–60	V
V_{GSS}	Gate-Source Voltage	±20	±20	V
I_D	Drain Current - Continuous (Note 1a)	4.5	–3.5	A
	- Pulsed	20	–20	
P_D	Power Dissipation for Dual Operation	2.3		W
	Power Dissipation for Single Operation (Note 1a)	1.8		
	(Note 1b)	1.4		
	(Note 1c)	2.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	79	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	41	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT4976	MT4976	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

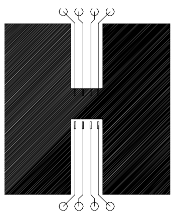
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)							
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 30 V, I_D = 4.5 A	Q1			93	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		Q1			4.5	A
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = –250 μA	Q1 Q2	60 –60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	Q1 Q2		59 –47		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V V_{DS} = –48 V, V_{GS} = 0 V	Q1 Q2			1 –1	μA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±20 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = –250 μA	Q1 Q2	1 –1	2.0 –2.0	3 –3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	Q1 Q2		–5.6 4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.5 A V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 4 A	Q1		40 52 45	50 64 55	mΩ
		V_{GS} = –10 V, I_D = –3.5 A V_{GS} = –10 V, I_D = –3.5 A, T_J = 125°C V_{GS} = –4.5 V, I_D = –3.1 A	Q2		70 90 81	85 100 91	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V V_{GS} = –10 V, V_{DS} = –5 V	Q1 Q2	20 –20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.5 A V_{DS} = –5 V, I_D = –3 5 A	Q1 Q2		15 10		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz Q2 V_{DS} = –30 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		680 770		pF
C_{oss}	Output Capacitance		Q1 Q2		86 94		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		37 39		pF
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 30 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω Q2 V_{DD} = –30 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω	Q1 Q2		13 7	23 17	ns
t_r	Turn-On Rise Time		Q1 Q2		8 12	19 23	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		19 19	39 37	ns
t_f	Turn-Off Fall Time		Q1 Q2		6 12	17 25	ns
Q_g	Total Gate Charge	Q1 V_{DS} = 30 V, I_D = 4.5 A, V_{GS} = 10 V Q2 V_{DS} = –30 V, I_D = –3.5 A, V_{GS} = –10V	Q1 Q2		15.5 18	19 24	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		2.6 2.7		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		2.7 3.3		nC

Electrical Characteristics **(continued)** T_A = 25°C unless otherwise noted

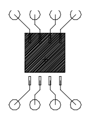
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			1.4 –1.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = –1.3 A (Note 2)	Q1 Q2		0.8 –0.8	1.1 –1.1	V

Notes:

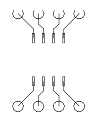
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a .02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: Q2

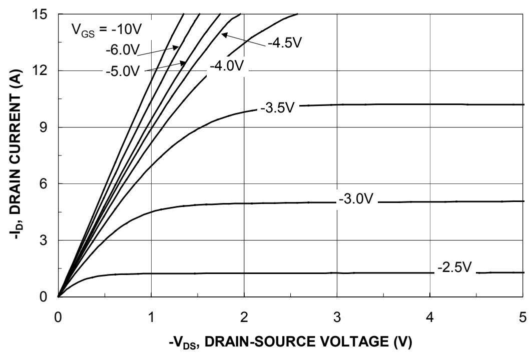


Figure 1. On-Region Characteristics.

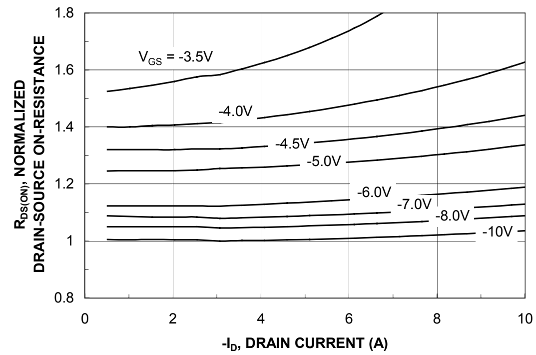


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

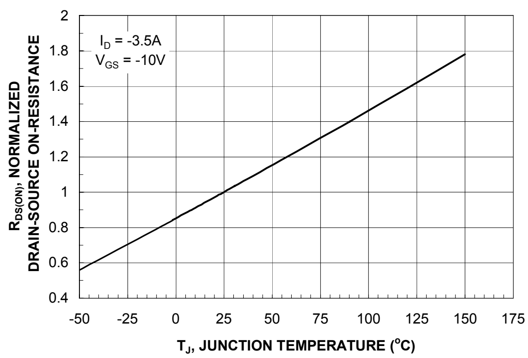


Figure 3. On-Resistance Variation with Temperature.

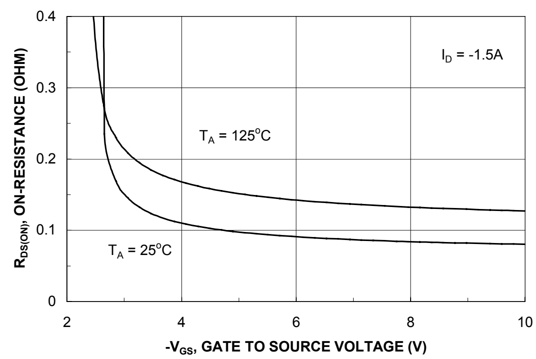


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

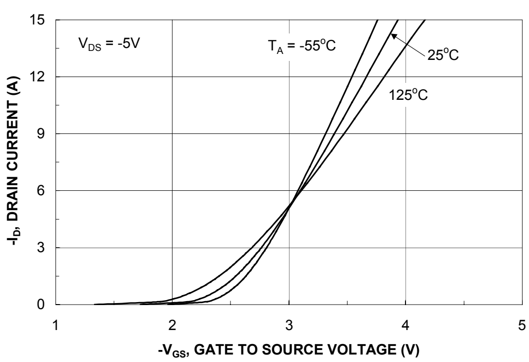


Figure 5. Transfer Characteristics.

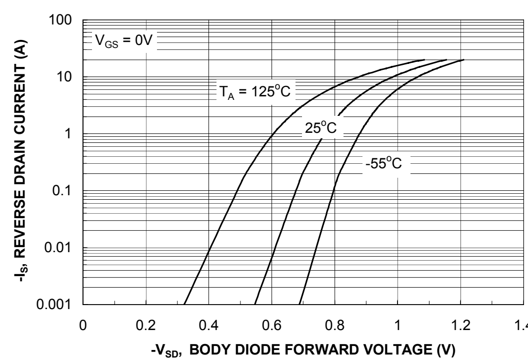


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

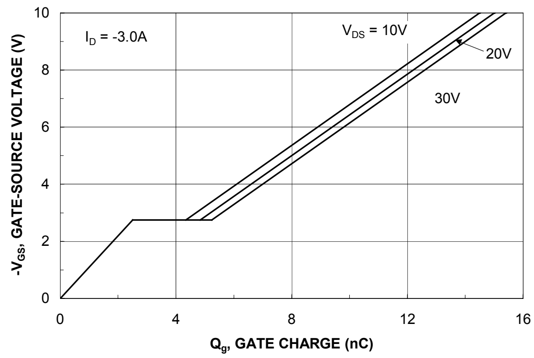


Figure 7. Gate Charge Characteristics.

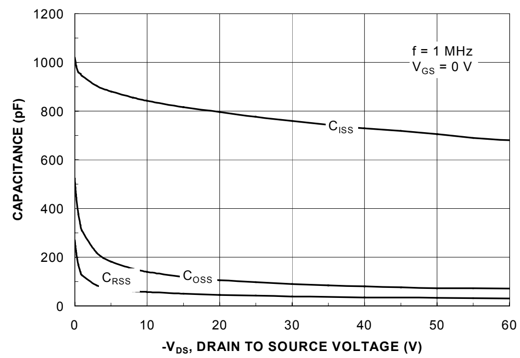


Figure 8. Capacitance Characteristics.

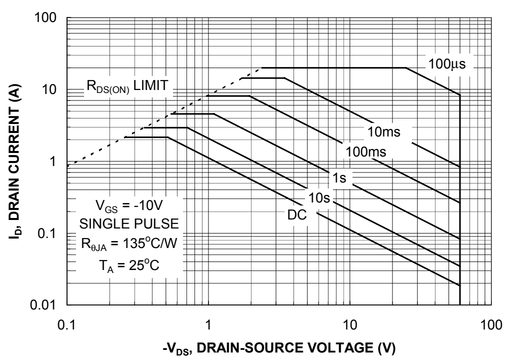


Figure 9. Maximum Safe Operating Area.

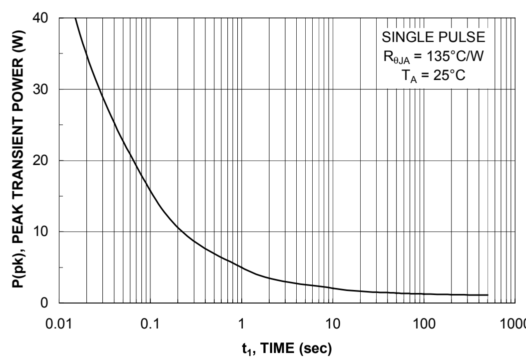


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

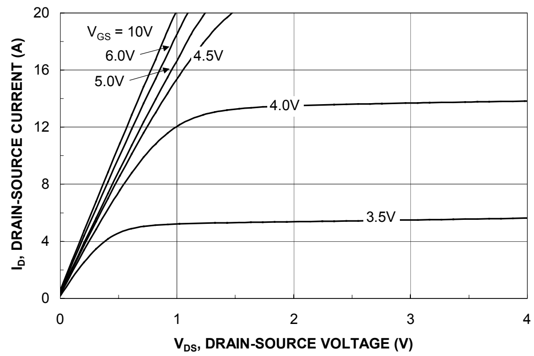


Figure 11. On-Region Characteristics.

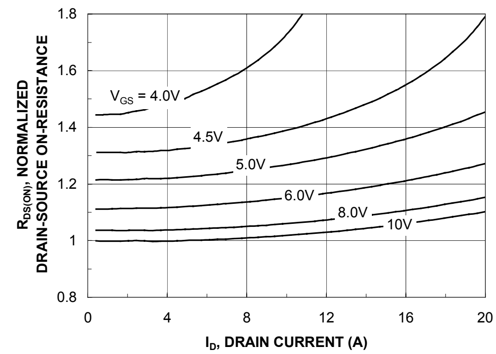


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

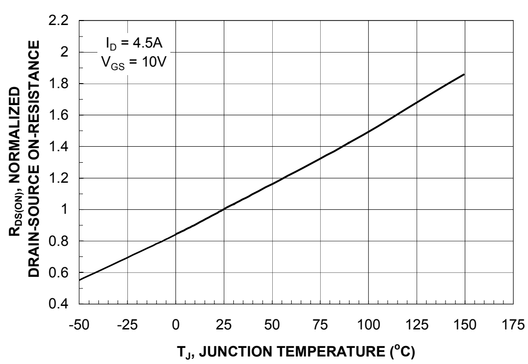


Figure 13. On-Resistance Variation with Temperature.

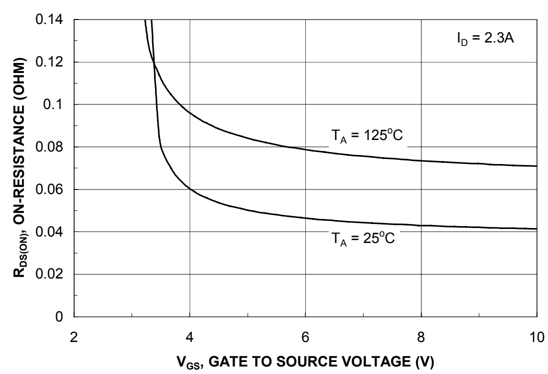


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

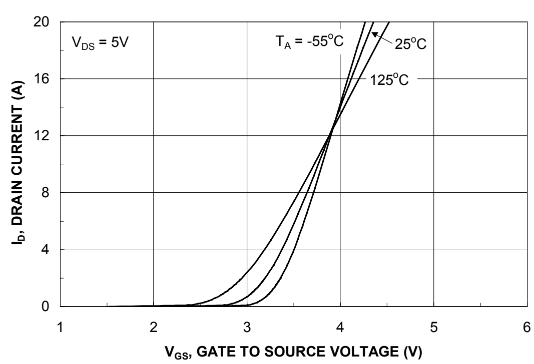


Figure 15. Transfer Characteristics.

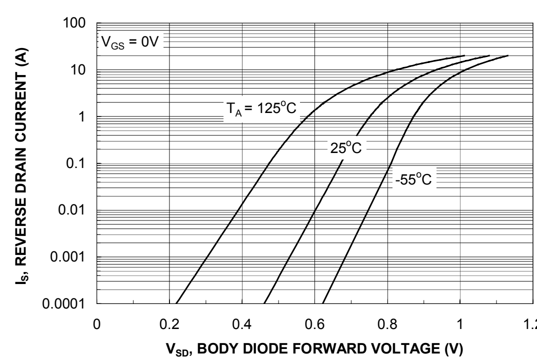


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

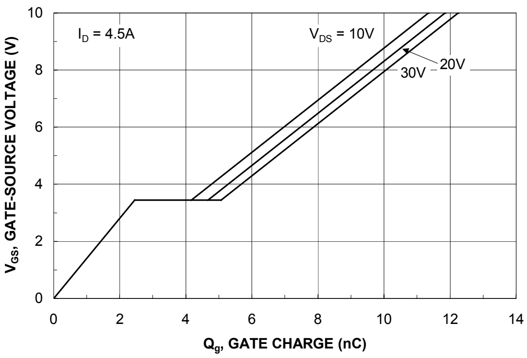


Figure 17. Gate Charge Characteristics.

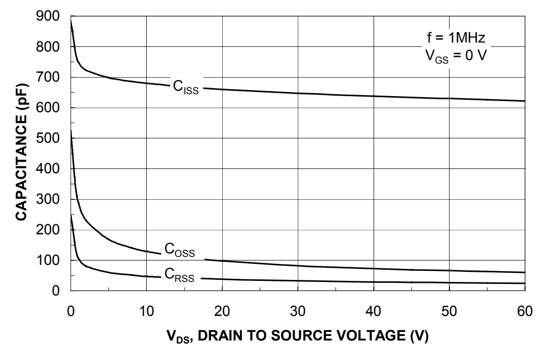


Figure 18. Capacitance Characteristics.

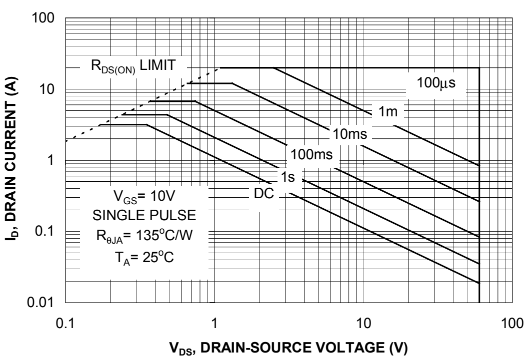


Figure 19. Maximum Safe Operating Area.

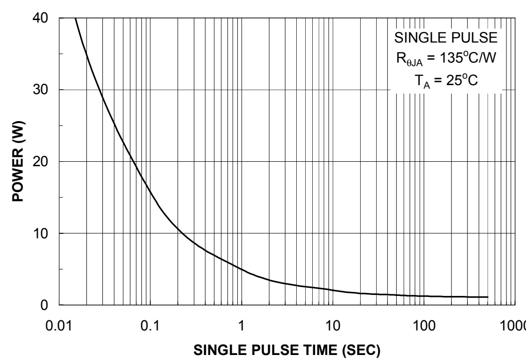


Figure 20. Single Pulse Maximum Power Dissipation.

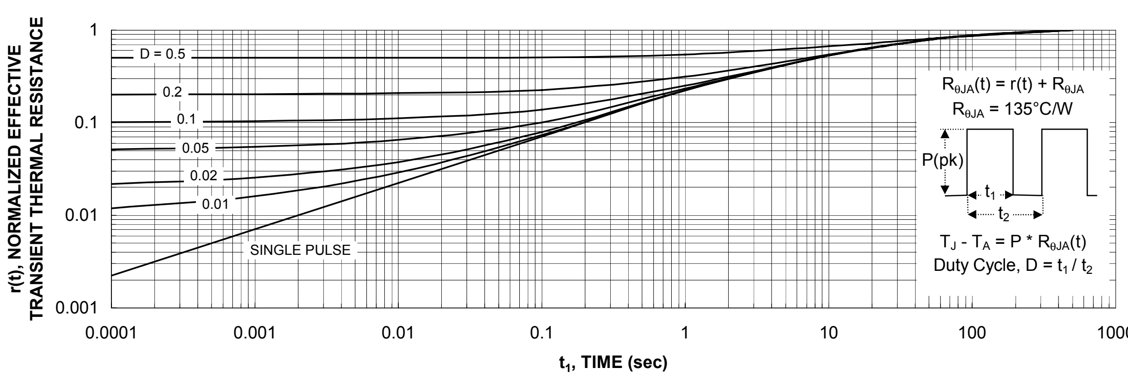


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.