



DRAM

4 MEG x 1 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-90622
- MIL-STD-883

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V $\pm 10\%$ power supply
- Low-power, 2.5mW standby; 300mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR), and HIDDEN
- FAST PAGE MODE access cycle
- CBR with $\overline{\text{WE}}$ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS

- Timing
- 70ns access
- 80ns access
- 100ns access
- 120ns access

MARKING

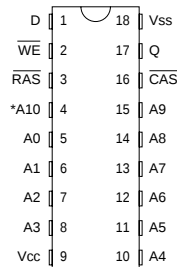
- 7		
- 8		
-10		
-12		
• Packages		
Ceramic DIP (300 mil)	CN	No. 101
Ceramic DIP (400 mil)	C	No. 102
Ceramic LCC	ECN	No. 202
Ceramic SOJ	ECJ	No. 504
Ceramic ZIP	CZ	No. 400
Ceramic Gull Wing	ECG	No. 600

GENERAL DESCRIPTION

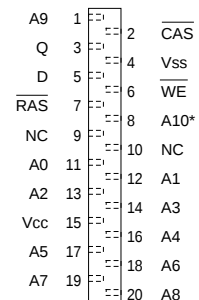
The MT4C1004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{\text{RAS}}$ is used to latch the first 11 bits and $\overline{\text{CAS}}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the

PIN ASSIGNMENT (Top View)

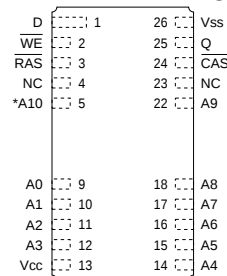
18-Pin DIP



20-Pin ZIP



20-Pin SOJ 20-Pin LCC 20-Pin Gull Wing



*Address not used for $\overline{\text{RAS}}$ -ONLY REFRESH

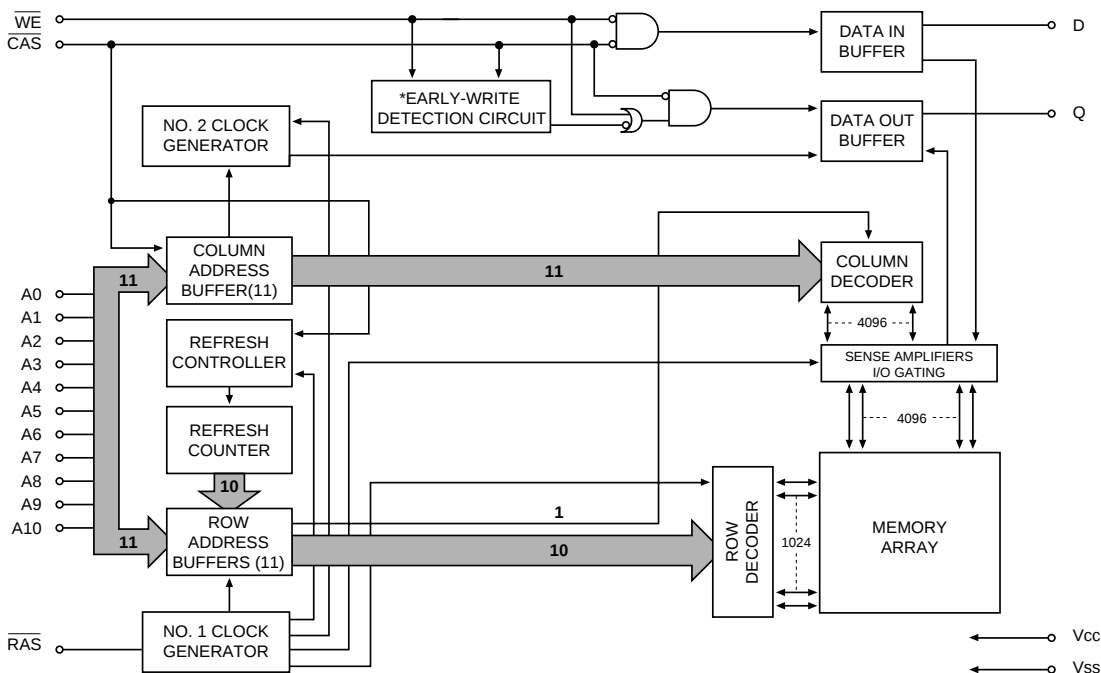
falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin remains open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This LATE- $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address (A0-A10) defined page



boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$ followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also,

the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ cycle will invoke the refresh counter for automatic $\overline{\text{RAS}}$ addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: $\overline{\text{WE}}$ LOW prior to $\overline{\text{CAS}}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
 $\overline{\text{CAS}}$ LOW prior to $\overline{\text{WE}}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)



TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES		DATA	
					'R	'C	D (Data In)	Q (Data Out)
Standby		H	H→X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
$\overline{\text{RAS}}$ -ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH		H→L	L	H	X	X	Don't Care	High-Z

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any pin Relative to V_{SS} -1.0V to +7.0V
 Power Dissipation 1W
 Short Circuit Output Current 50mA
 Lead Temperature (Soldering 5 Seconds)..... 270°C
 Storage Temperature -65°C to +150°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} + .5	V	
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-.5	0.8	V	
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ 5.5V V _{CC} =5.5V (All other pins not under test = 0V)	I _I	-5	5	μA	
OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ V _{OUT} ≤ 5.5V) V _{CC} =5.5V	I _{OZ}	-5	5	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX				UNITS	NOTES
		-7	-8	-10	-12		
STANDBY CURRENT (TTL) (R _{AS} = C _{AS} = V _{IH})	I _{CC1}	4	4	4	4	mA	
STANDBY CURRENT (CMOS) (R _{AS} = C _{AS} = V _{CC} -0.2V; all other inputs = V _{CC} -0.2V)	I _{CC2}	2	2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average Power-Supply Current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC3}	85	75	65	65	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average Power-Supply Current (R _{AS} = V _{IL} , C _{AS} , Address Cycling: t _{PC} = t _{PC} (MIN))	I _{CC4}	60	50	45	40	mA	3, 4
REFRESH CURRENT: R _{AS} -ONLY Average Power-Supply Current (R _{AS} Cycling, C _{AS} = V _{IH} : t _{RC} = t _{RC} (MIN))	I _{CC5}	85	75	65	65	mA	3
REFRESH CURRENT: C _{AS} -BEFORE-R _{AS} Average Power-Supply Current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC6}	85	75	65	65	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C _{I1}		7	pF	2
Input Capacitance: RAS, CAS, WE	C _{I2}		7	pF	2
Output Capacitance: Q	C _O		8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ 125; V_{CC} = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t _{RC}	130		150		180		220		ns	
READ-WRITE cycle time	t _{RWC}	155		175		210		255		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	40		45		55		70		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t _{PRWC}	65		70		85		140		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		70		80		90		120	ns	14
Access time from $\overline{\text{CAS}}$	t _{CAC}		20		20		25		30	ns	15
Access time from column address	t _{AA}		35		40		45		60	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45		60	ns	
RAS pulse width	t _{RAS}	70	10,000	80	10,000	100	10,000	120	100,000	ns	
RAS pulse width (FAST PAGE MODE)	t _{RASP}	70	100,000	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	t _{RSH}	20		20		25		30		ns	
RAS precharge time	t _{RP}	50		60		70		90		ns	
CAS pulse width	t _{CAS}	20	10,000	20	10,000	25	10,000	30	10,000	ns	
CAS hold time	t _{CSH}	70		80		100		120		ns	
CAS precharge time	t _{CPN}	10		10		12		15		ns	16
CAS precharge time (FAST PAGE MODE)	t _{CP}	10		10		12		15		ns	
RAS to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	50	20	60	25	75	25	90	ns	17
CAS to RAS precharge time	t _{CRP}	5		5		5		10		ns	
Row address setup time	t _{ASR}	0		0		0		0		ns	
Row address hold time	t _{RAH}	10		10		15		15		ns	
RAS to column address delay time	t _{RAD}	15	35	15	40	20	50	20	60	ns	18
Column address setup time	t _{ASC}	0		0		0		0		ns	
Column address hold time	t _{CAH}	15		20		25		25		ns	
Column address hold time (referenced to RAS)	t _{AR}	50		60		70		85		ns	
Column address to RAS lead time	t _{RAL}	35		40		50		60		ns	
Read command setup time	t _{RCS}	0		0		0		0		ns	
Read command hold time (referenced to CAS)	t _{RCH}	0		0		0		0		ns	19
Read command hold time (referenced to RAS)	t _{RRH}	0		0		0		0		ns	19
CAS to output in Low-Z	t _{CLZ}	0		0		0		0		ns	
Output buffer turn-off delay	t _{OFF}	0	20	0	20	0	20	0	20	ns	20
WE command setup time	t _{WCS}	0		0		0		0		ns	21

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	t_{WCH}	15		15		20		25		ns	
Write command hold time (referenced to RAS)	t_{WCR}	50		60		70		85		ns	
Write command pulse width	t_{WP}	15		15		20		25		ns	
Write command to RAS lead time	t_{RWL}	20		20		25		30		ns	
Write command to CAS lead time	t_{CWL}	20		20		25		30		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	22
Data-in hold time	t_{DH}	12		15		18		25		ns	22
Data-in hold time (referenced to RAS)	t_{DHR}	50		60		70		90		ns	
RAS to WE delay time	t_{RWD}	70		80		100		120		ns	21
Column address to WE delay time	t_{AWD}	35		40		50		60		ns	21
CAS to WE delay time	t_{CWD}	20		20		25		30		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh period (1,024 cycles)	t_{REF}		16		16		16		16	ms	
RAS to CAS precharge time	t_{RPC}	0		0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	t_{CSR}	10		10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	t_{CHR}	10		15		20		25		ns	5
WE hold time (CAS-BEFORE-RAS REFRESH)	t_{WRH}	10		10		10		10		ns	24, 25
WE setup time (CAS-BEFORE-RAS REFRESH)	t_{WRP}	10		10		10		10		ns	24, 25
WE hold time (WCBR test cycle)	t_{WTH}	10		10		10		10		ns	24, 25
WE setup time (WCBR test cycle)	t_{WTS}	10		10		10		10		ns	24, 25

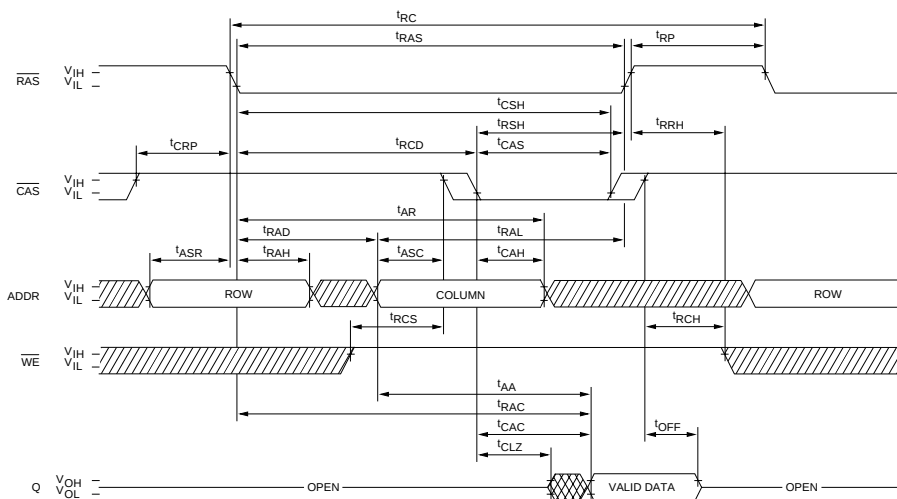


NOTES

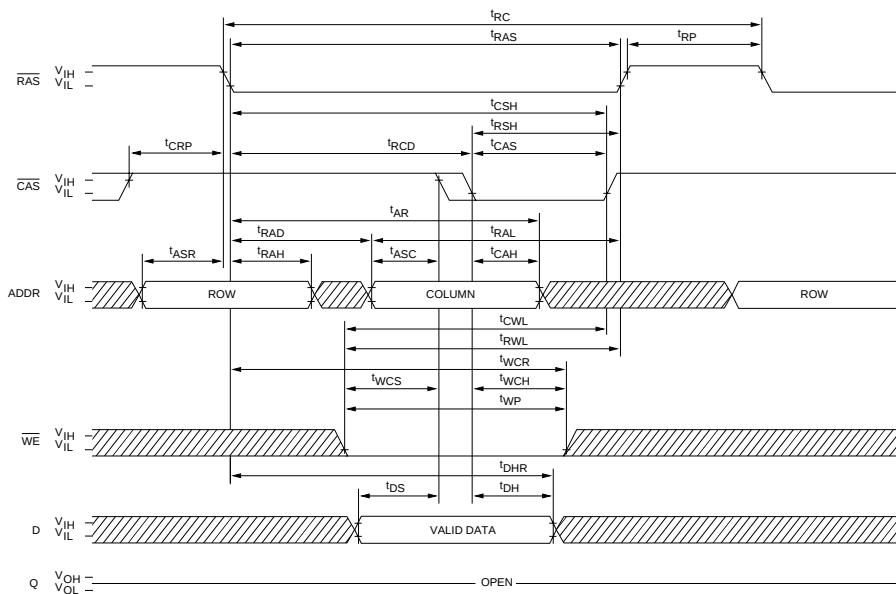
1. All voltages referenced to V_{SS} .
2. This parameter is sampled, not 100% tested.
Capacitance is measured with $V_{CC} = 5V$, $f = 1\text{ MHz}$ at less than $50mV_{rms}$, $T_A = 25^\circ C \pm 3^\circ C$, $V_{bias} = 2.4V$ applied to each input and output individually with remaining inputs and outputs open.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55^\circ C \leq T_A \leq 125^\circ C$) is assured.
7. An initial pause of $100\mu s$ is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and $100pF$.
14. Assumes that $t_{RCD} < t_{RCD} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD} (MAX)$.
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RCD} (MAX)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS} (MIN)$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD} (MIN)$, $t_{AWD} \geq t_{AWD} (MIN)$ and $t_{CWD} \geq t_{CWD} (MIN)$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE} = LOW$.
24. t_{WTS} and t_{WTH} are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of t_{WRP} and t_{WRH} in the CBR REFRESH cycle.
25. JEDEC test mode only.



READ CYCLE



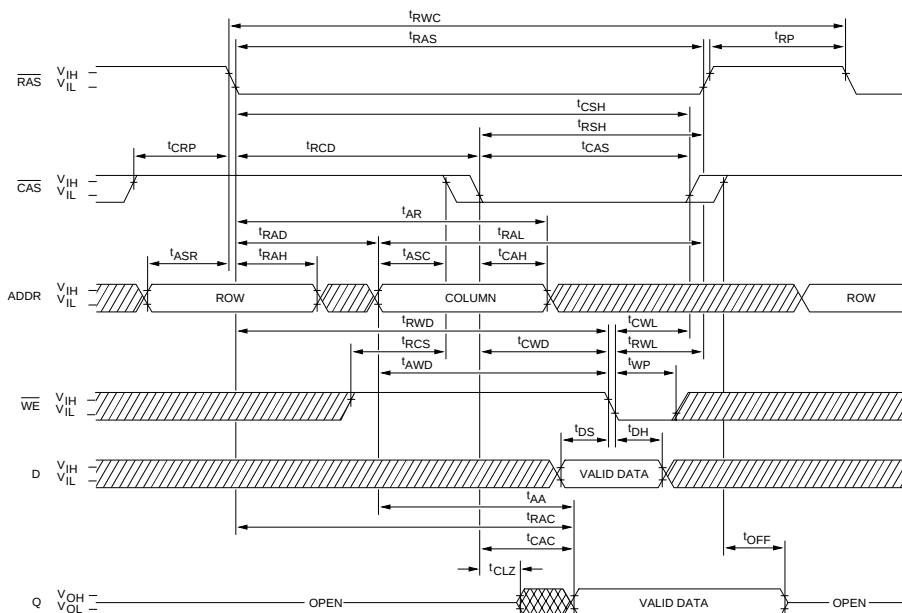
EARLY-WRITE CYCLE



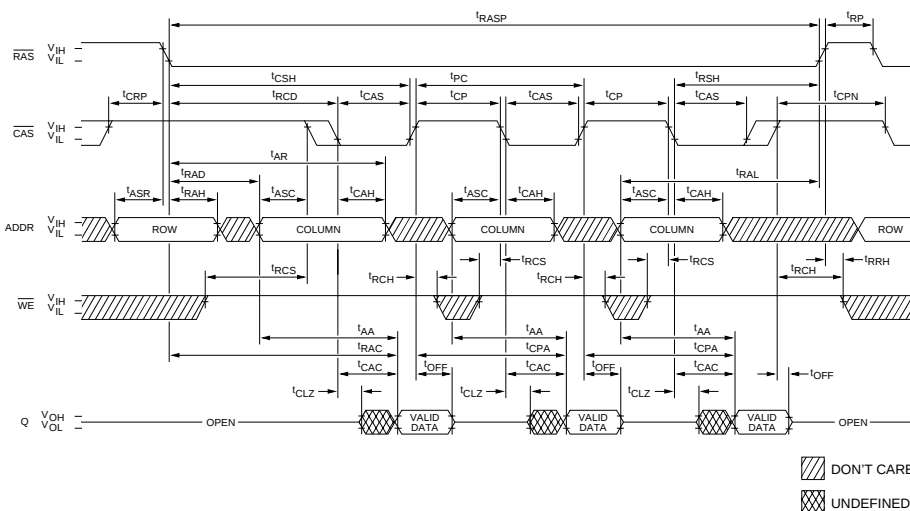
▨ DON'T CARE

▩ UNDEFINED

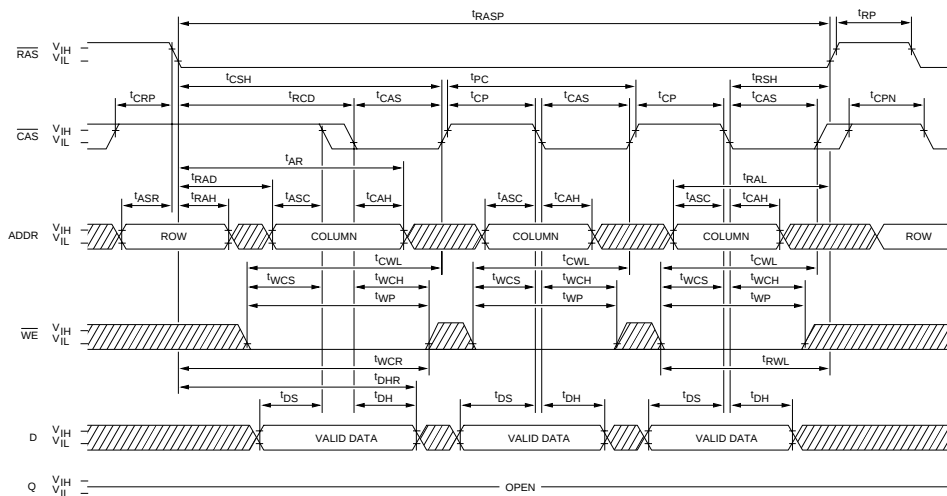
READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



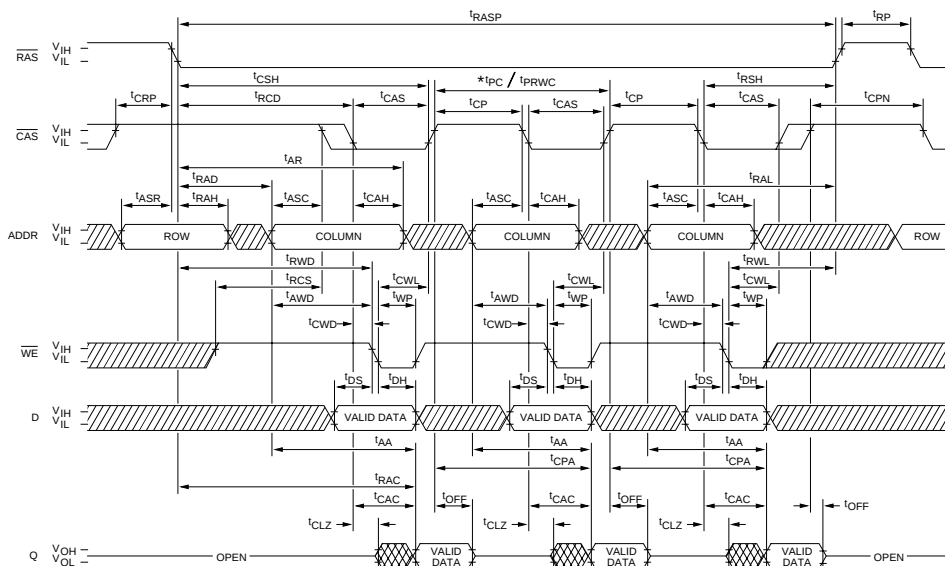
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

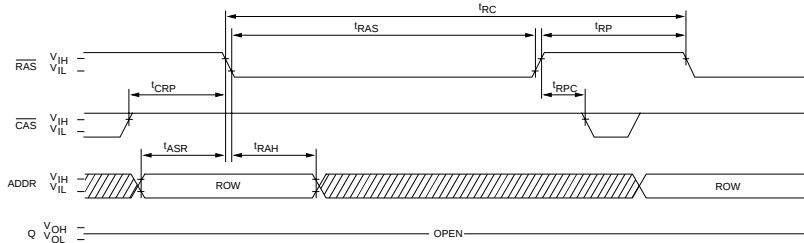


*t_{PC} = LATE-WRITE Cycle

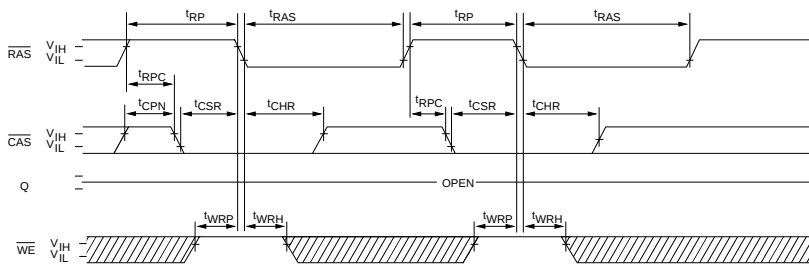
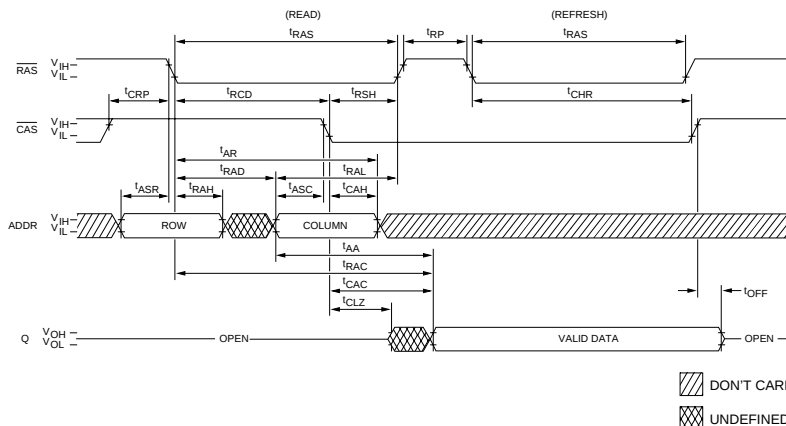
^tPRWC = FAST READ-MODIFY-WRITE Cycle

 DON'T CARE

UNDEFINED

 **$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE**(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE) **$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE**

(A0-A10 = DON'T CARE)

**HIDDEN REFRESH CYCLE ²³**($\overline{\text{WE}}$ = HIGH)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA / JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR (CAS-BEFORE-RAS) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

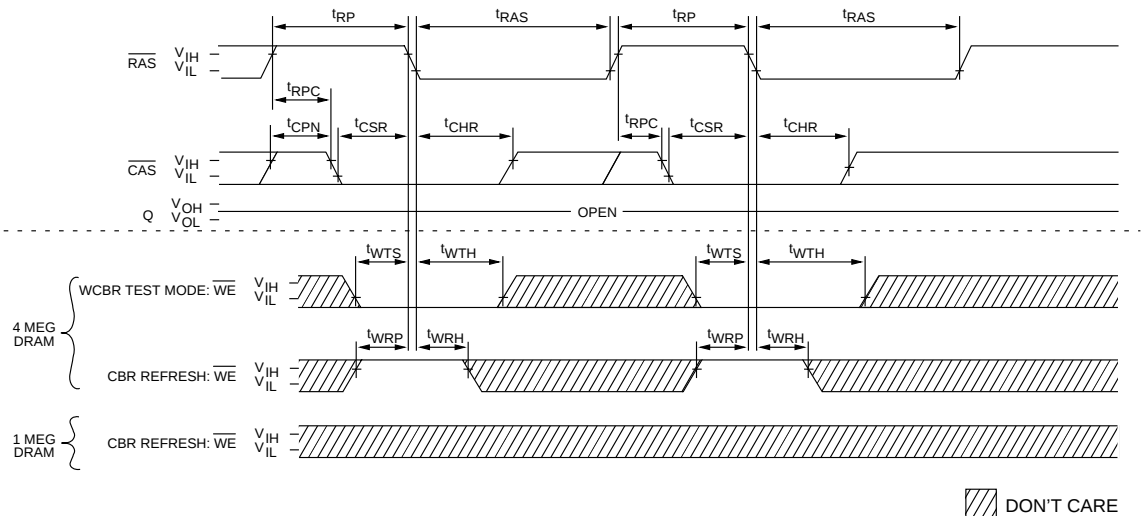
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100 μ s delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$ -ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$ -ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$ -ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

**ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

