DRAM

1 MEG x 1 DRAM

LOW POWER, FAST PAGE MODE

FEATURES

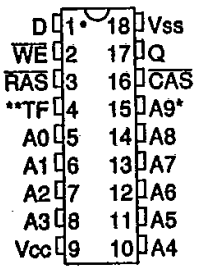
- Industry standard x1 pinout, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 1.0mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512-cycle refresh in 64ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, and HIDDEN
- Optional FAST PAGE MODE access cycle
- Low CMOS STANDBY CURRENT, 200µA maximum

OPTIONS

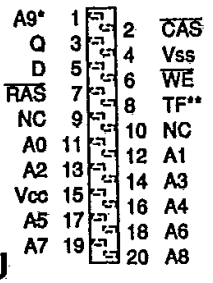
	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300mil)	None
Ceramic DIP (300mil)	C
Plastic ZIP (350mil)	Z
Plastic SOJ (300mil)	DJ
Plastic TSOP (***)	VG
• Operating Temperature, TA	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT

PIN ASSIGNMENT (Top View)

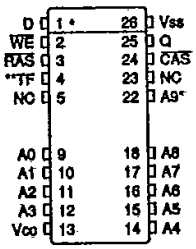
18-Pin DIP (A-3, B-2)



20-Pin ZIP (C-2)



20-Pin SOJ (E-1)



*Address not used for RAS-ONLY refresh
**TF = Test Function, VIN must not exceed Vcc+1V for normal operation
***Consult factory on availability of TSOP packages

GENERAL DESCRIPTION

The MT4C1027 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin, data out (Q), remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CAS-BEFORE-RAS refresh will increment the refresh counter for automatic RAS addressing.

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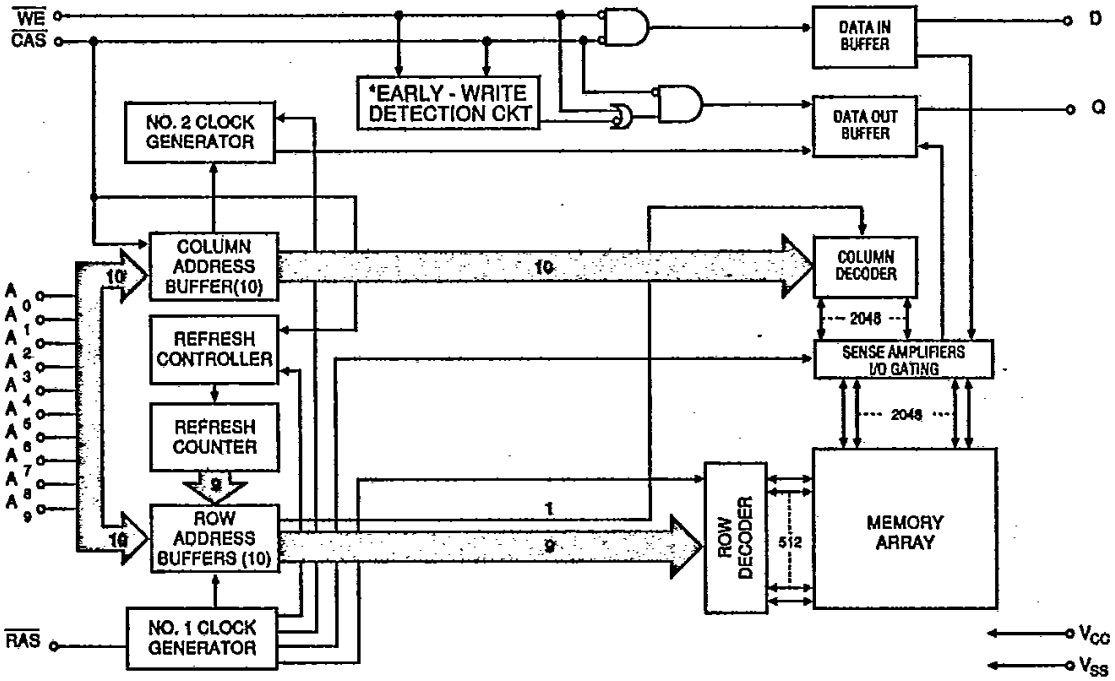
FUNCTIONAL BLOCK DIAGRAM
LOW POWER, FAST PAGE MODE



*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection CKT output is a HIGH (EARLY WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection CKT output is a LOW (LATE WRITE)

TRUTH TABLE

Function		RAS	CAS	WE	Address tR	Address tC	DATA D (Data In)	DATA Q (Data Out)
Standby		H	X	X	X	X	Don't Care	High-Z
READ		L	L	H	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Valid Data In	Valid Data Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Don't Care	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Don't Care	Valid Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Valid Data In	Valid Data Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Valid Data In	Valid Data Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	Don't Care	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Don't Care	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In	High-Z
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH		H→L	L	X	X	X	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-55°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (soldering 10 sec) .....260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-2.0	0.8	V	1, 25
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	MAX -10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	1	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	75	65	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))	I_{CC4}	55	45	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	200	200	200	µA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	75	65	60	mA	3, 5
BATTERY BACKUP REFRESH CURRENT Average power supply current during battery backup refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) of 1µs; $\overline{WE}$, A0-A9 and D in = Vcc -0.2V or 0.2V (D in may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	200	200	200	µA	5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ-WRITE cycle time	t_{RWC}	155		175		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	65		70		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column address	t_{AA}		35		40		50	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column-address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	20
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

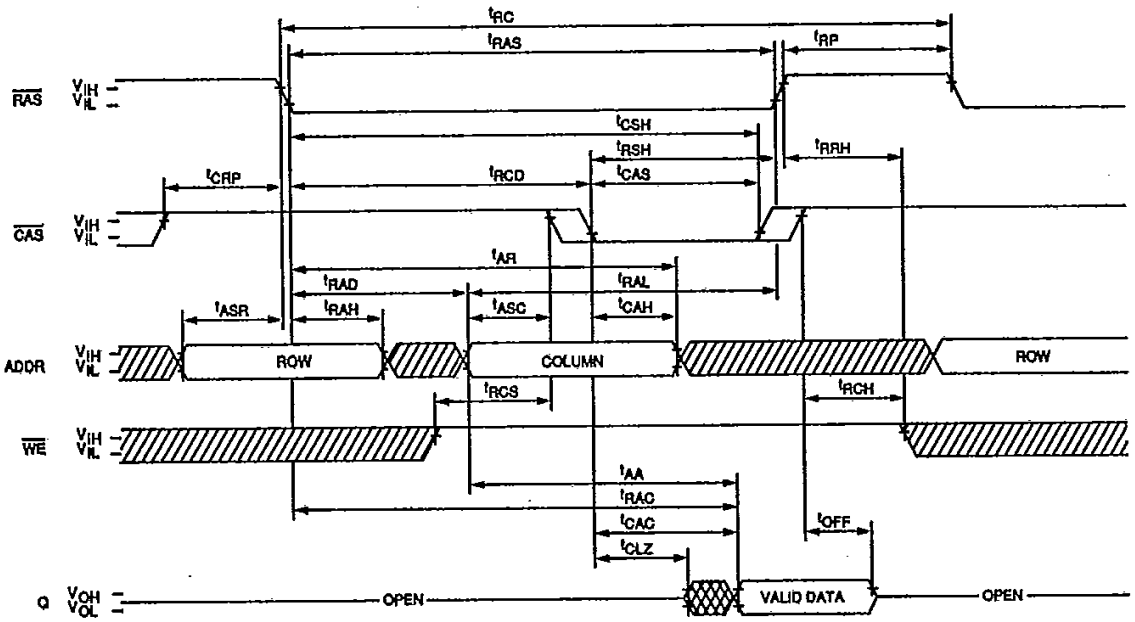
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	55		60		75		ns	
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70		80		100		ns	21
Column address to $\overline{WE}$ delay time	t_{AWD}	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20		20		25		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (512-cycles)	t_{REF}		64		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	5

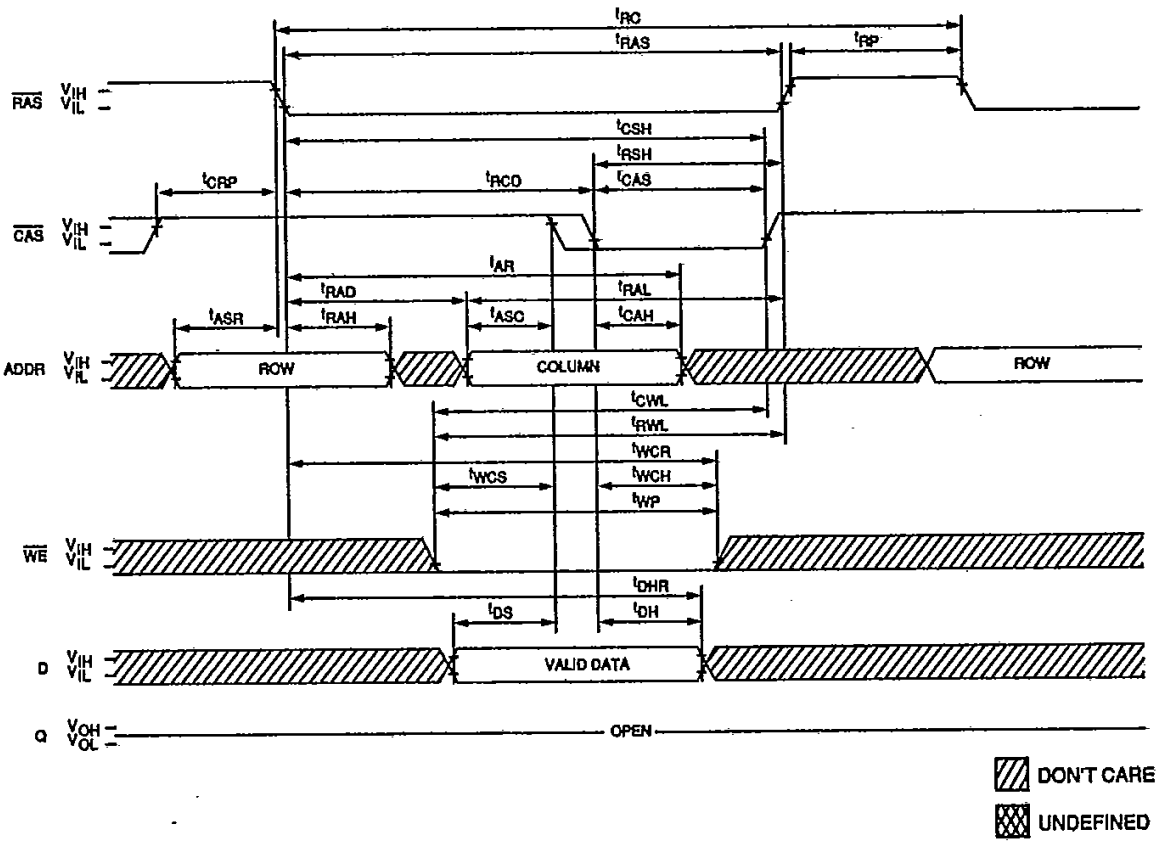
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = I\,{}^{dt}/_{dv}$ with dv = 3V and Vcc = 5V.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 64ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate. (at access time and until $\overline{CAS}$ goes back to V_{IH})
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -02V.
25. The device shall meet all functional requirements when a -2.0 signal is applied provided the signal is not more negative than -1.5V for a period of less than 20ns and the signal's total duration is 25ns or less; or a -0.3V signal of any duration is presented (DC).

READ CYCLE



EARLY-WRITE CYCLE



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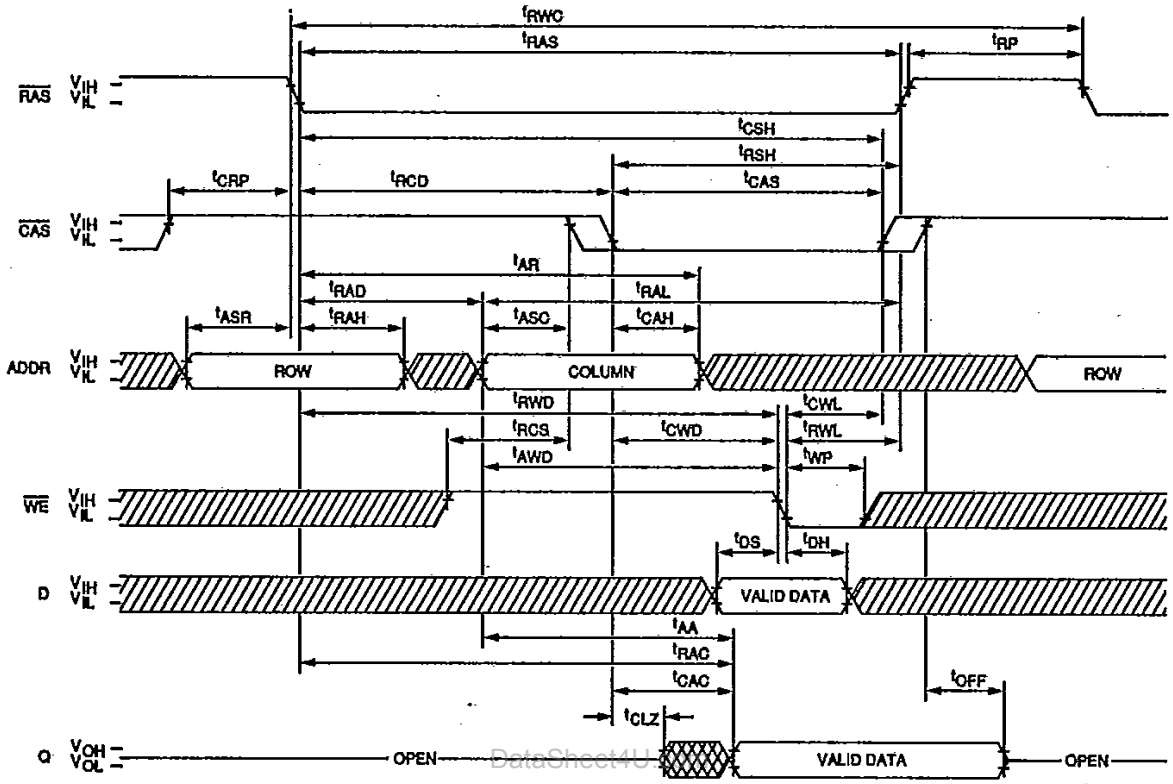
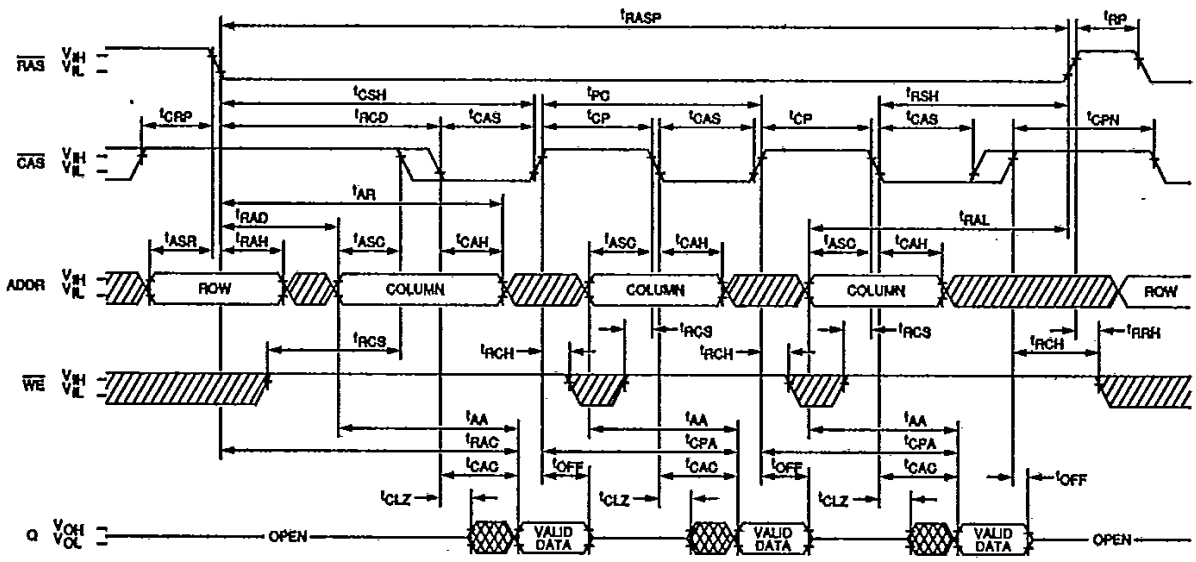
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



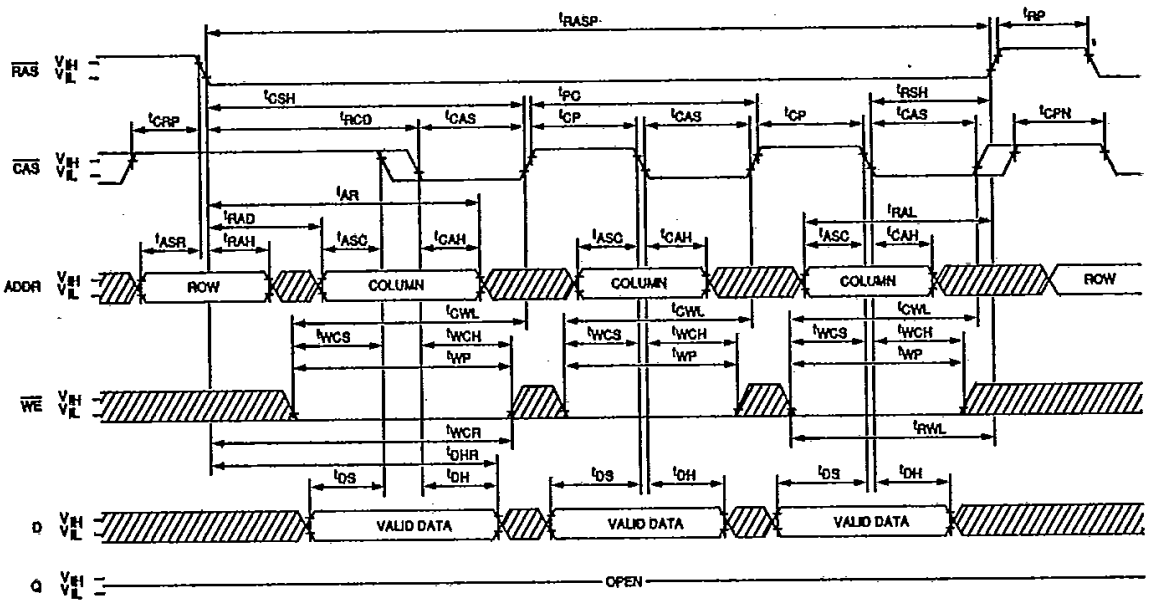
FAST-PAGE-MODE READ CYCLE



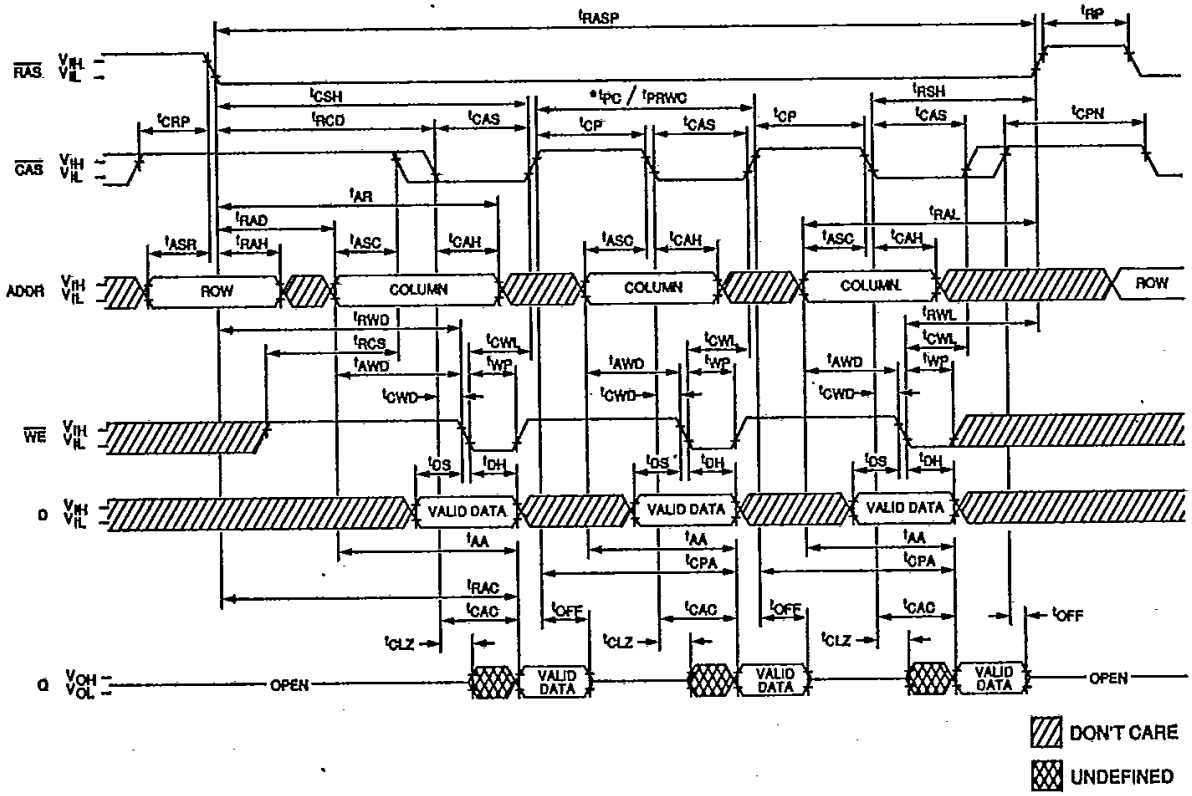
DON'T CARE

UNDEFINED

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE-WRITE only.

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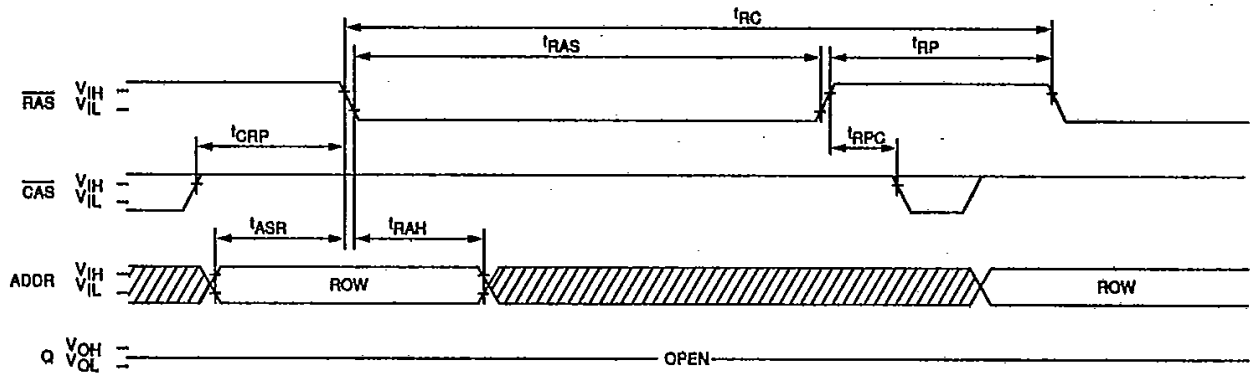
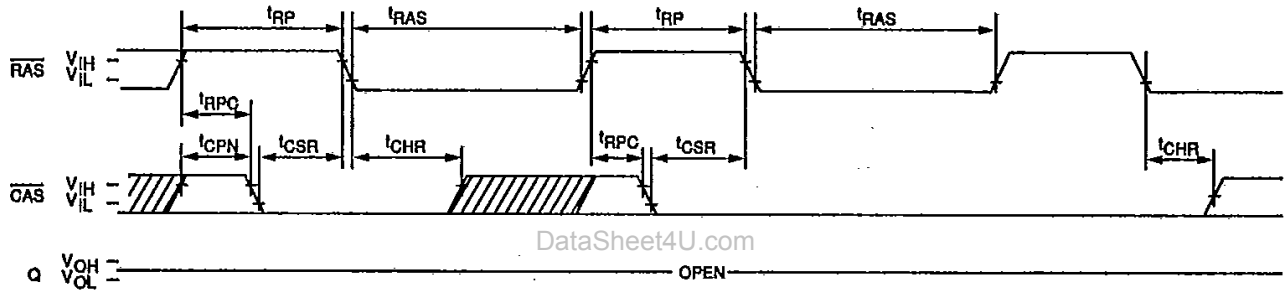
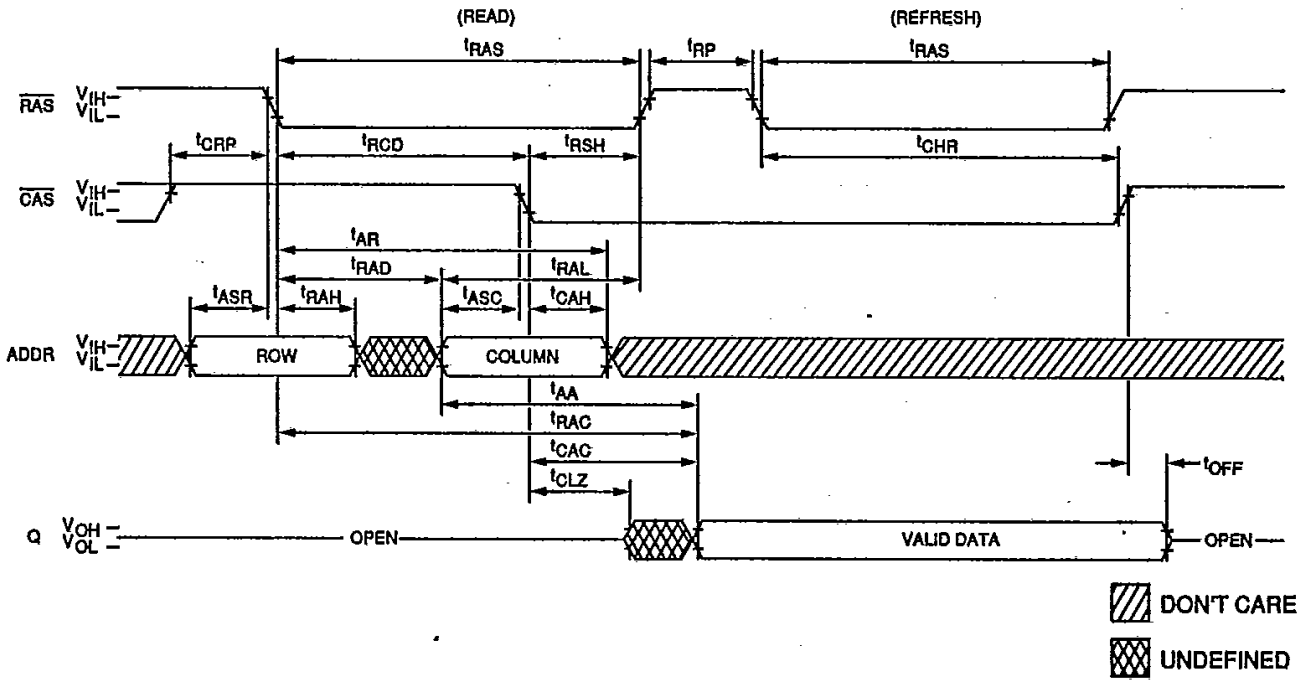
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_8; A_9 and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH) [23]



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HIDDEN REFRESH CYCLE
($\overline{WE}$ = LOW)