1 MEG x 4 DRAM

Fast Page Mode DRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-90847
- MIL-STD-883

FEATURES

- Industry standard x4 pinout, timing, functions, and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low-power, 2.5mW standby; 300mW active, typical
- All inputs, outputs, and clocks are fully TTL and CMOS compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS\-ONLY, CAS\-BEFORE-RAS\ (CBR), and HIDDEN
- FAST PAGE MODE access cycle
- CBR with WE\ a HIGH (JEDEC test mode capable via WCBR)

OPTIONS — MARKING

- Timing

70ns access	-7
80ns access	-8
100ns access	-10
120ns access	-12

- Packages

Ceramic DIP (300 mil)	CN	No. 103
Ceramic DIP (400 mil)	C	No. 104
Ceramic LCC*	ECN	No. 202
Ceramic ZIP	CZ	No. 400
Ceramic SOJ	ECJ	No. 504
Ceramic Gull Wing	ECG	No. 600

***NOTE:** If solder-dip and lead-attach is desired on LCC packages, lead-attach must be done prior to the solder-dip operation.*

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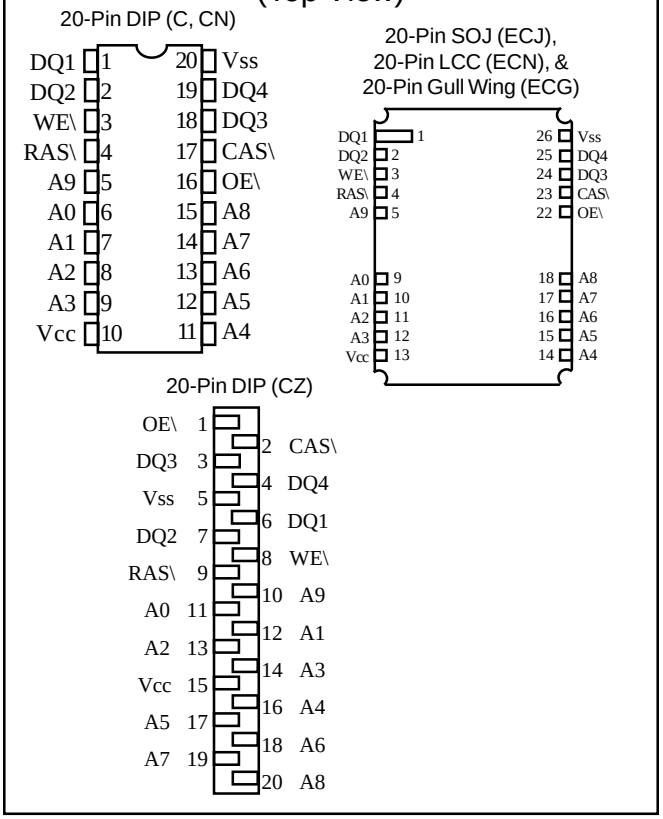
PIN ASSIGNMENT
(Top View)



GENERAL DESCRIPTION

The MT4C4001J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS\ is used to latch the first 10 bits and CAS\ the later 10 bits. A READ or WRITE cycle is selected with the WE\ input. A logic HIGH on WE\ dictates READ mode while a logic LOW on WE\ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE\ or CAS\, whichever occurs last. If WE\ goes LOW prior to CAS\ going LOW, the output pin(s) remain open (High-Z) until the next CAS\ cycle. If WE\ goes LOW after data reaches the output pin(s), Qs are activated and retain the selected cell data as long as CAS\ remains low (regardless of WE\ or RAS\). This LATE WE\ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE\ and OE\. FAST-PAGE-MODE operations allow faster data operations (READ, WRITE, or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE

(continued)

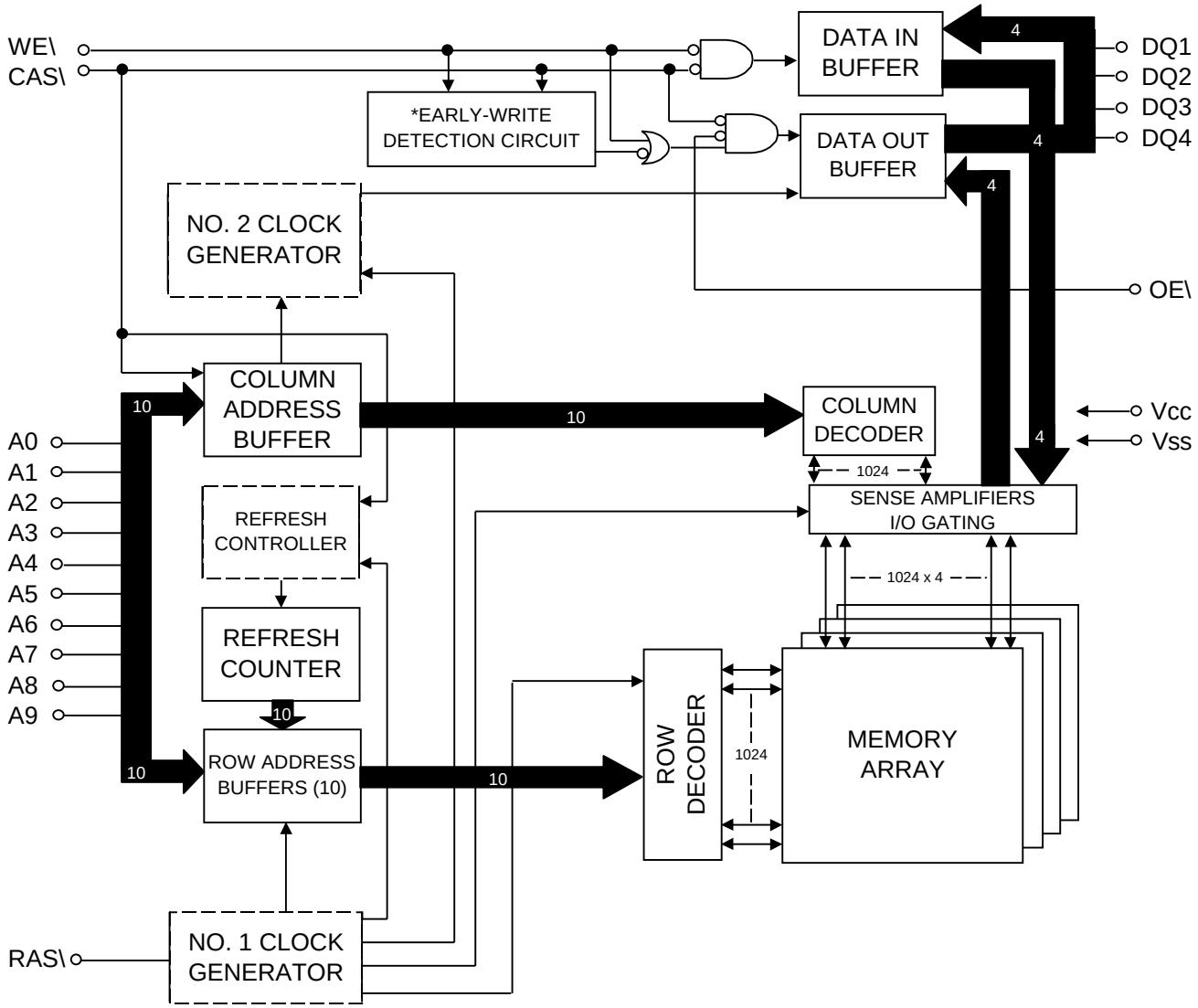
GENERAL DESCRIPTION (cont.)

cycle is always initiated with a row address strobe-in by RAS\ followed by a column address strobed-in by CAS\. CAS\ may be toggled-in by holding RAS\ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS\ HIGH terminates the FAST PAGE MODE operation.

Returning RAS\ and CAS\ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS\ HIGH time. Memory cell data is retained in its corrected stated by maintaining power and executing any RAS\ cycle (READ, WRITE, RAS\-ONLY, CAS\-BEFORE-RAS\, or HIDDEN REFRESH) so that all 1,024 combinations of RAS\ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS\ addressing.

FUNCTIONAL BLOCK DIAGRAM

FAST PAGE MODE



NOTE: WE\ LOW prior to CAS\ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS\ LOW prior to WE\ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		RAS\	CAS\	WE\	OE\	ADDRESSES		DATA IN/OUT
						^{t}R	^{t}C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out/Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out/Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out/Data In
RAS\-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS\-BEFORE-RAS\ REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss.....-1.0V to +7.0V
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....50mA
Lead Temperature (soldering 5 seconds).....+270°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(NOTES: 1, 3, 4, 6, 7) (-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+0.5	V	
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ 5.5V Vcc = 5.5V (All other pints not under test = 0V)	I_I	-5	5	µA	
OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ V_{OUT} ≤ 5.5V) Vcc = 5.5V	I_{OZ}	-5	5	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYM	-7	-8	-10	-12	UNITS	NOTES
STANDBY CURRENT (TTL) (RAS\ = CAS\ = V_{IH})	I_{CC1}	4	4	4	4	mA	
STANDBY CURRENT (CMOS) (RAS\ = CAS\ = V_{CC} -0.2V; all other inputs = V_{CC} -0.2V)	I_{CC2}	2	2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average Power-Supply Current (RAS\, CAS\, Address Cycling: t_{RC} = t_{RC}(MIN))	I_{CC3}	85	75	65	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average Power-Supply Current (RAS\ = V_{IL}, CAS\, Address Cycling: t_{PC} = t_{PC} (MIN))	I_{CC4}	60	50	45	40	mA	3, 4
REFRESH CURRENT: RAS\-ONLY Average Power-Supply Current (RAS\ Cycling, CAS\ = V_{IH}: t_{RC} = t_{RC} (MIN))	I_{CC5}	85	75	65	70	mA	3
REFRESH CURRENT: CAS\-BEFORE-RAS\ Average Power-Supply Current (RAS\, CAS\, Address Cycling: t_{RC} = t_{RC} (MIN))	I_{CC6}	85	75	65	70	mA	3, 5

CAPACITANCE

PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		7	pF	2
Input Capacitance: RAS\, CAS\, WE\, OE\	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(NOTES: 6, 7, 8, 9, 10, 11, 12, 13) ($-55°C \le T_C \le 125°C$; V_{CC} = 5V ±10%)

		-7		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		190		220		ns	
READ-WRITE cycle time	t_{RWC}	180		200		240		255		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	40		45		55		70		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	90		90		110		140		ns	
Access time from RAS\	t_{RAC}		70		80		90		120	ns	14
Access time from CAS\	t_{CAC}		20		20		25		30	ns	15
Access time from column address	t_{AA}		35		40		45		60	ns	
Access time from CAS\ precharge	t_{CPA}		35		40		45		60	ns	
RAS\ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	120	100,000	ns	
RAS\ pulse width (FAST PAGE MODE)	t_{RASP}	70	100,000	80	100,000	100	100,000	120	100,000	ns	
RAS\ hold time	t_{RSH}	20		20		25		30		ns	
RAS\ precharge time	t_{RP}	50		60		70		90		ns	
CAS\ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	30		ns	
CAS\ hold time	t_{CSH}	70		80		100		120		ns	
CAS\ precharge time	t_{CPN}	10		10		12		15		ns	16
CAS\ precharge time (FAST PAGE MODE)	t_{CP}	10		10		12		15		ns	
RAS\ to CAS\ delay time	t_{RCD}	20	50	20	60	25	75	25	90	ns	17
CAS\ to RAS\ precharge time	t_{CRP}	5		5		5		10		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		15		ns	
RAS\ to column address delay time	t_{RAD}	15	35	15	40	20	50	20	60	ns	18
Column address setup time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		25		ns	
Column address hold time (referenced to RAS\)	t_{AR}	50		60		70		85		ns	
Column address to RAS\ lead time	t_{RAL}	35		40		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		0		ns	
Read command hold time (referenced to CAS\)	t_{RCH}	0		0		0		0		ns	19
Read command hold time (referenced to RAS\)	t_{RRH}	0		0		0		0		ns	19
CAS\ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	20
WE\ command setup time	t_{WCS}	0		0		0		0		ns	21, 27

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

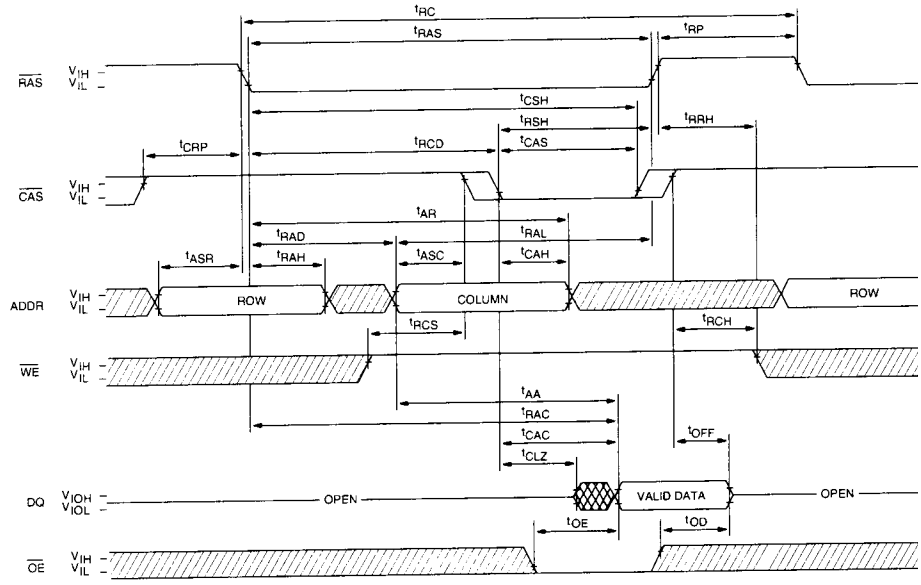
(NOTES: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ±10%)

		-7		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	t_{WCH}	15		15		20		25		ns	
Write command hold time (referenced to RAS\)	t_{WCR}	50		60		70		80		ns	
Write command pulse width	t_{WP}	15		15		20		25		ns	
Write command to RAS\ lead time	t_{RWL}	20		20		25		30		ns	
Write commend to CAS\ lead time	t_{CWL}	20		20		25		30		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	22
Data-in hold time	t_{DH}	12		15		18		25		ns	22
Data-in hold time (referenced to RAS\)	t_{DHR}	50		60		70		90		ns	
RAS\ to WE\ delay time	t_{RWD}	95		105		130		140		ns	21
Column address to WE\ delay time	t_{AWD}	60		65		80		90		ns	21
CAS\ to WE\ delay time	t_{CWD}	45		45		55		60		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh period (1,024 cycles)	t_{REF}		16		16		16		16	ms	
RAS\ to CAS\ precharge time	t_{RPC}	0		0		0		0		ns	
CAS\ setup time (CAS\-BEFORE-RAS\ REFRESH)	t_{CSR}	5		10		10		10		ns	5
CAS\ hold time (CAS\-BEFORE-RAS\ REFRESH)	t_{CHR}	10		15		20		25		ns	5
WE\ hold time (CAS\-BEFORE-RAS\ REFRESH)	t_{WRH}	10		10		10		10		ns	25, 28
WE\ setup time (CAS\-BEFORE-RAS\ REFRESH)	t_{WRP}	10		10		10		10		ns	25, 28
WE\ hold time (WCBR test cycle)	t_{WTH}	10		10		10		10		ns	25, 28
WE\ setup time (WCBR test cycle)	t_{WTS}	10		10		10		10		ns	25, 28
OE\ setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		0		ns	
Output disable	t_{OD}		15		20		25		25	ns	27
Output enable	t_{OE}		15		20		25		25	ns	23
OE\ hold time from WE\ during READ-MODIFY-WRITE cycle	t_{OEH}	20		20		25		25		ns	26

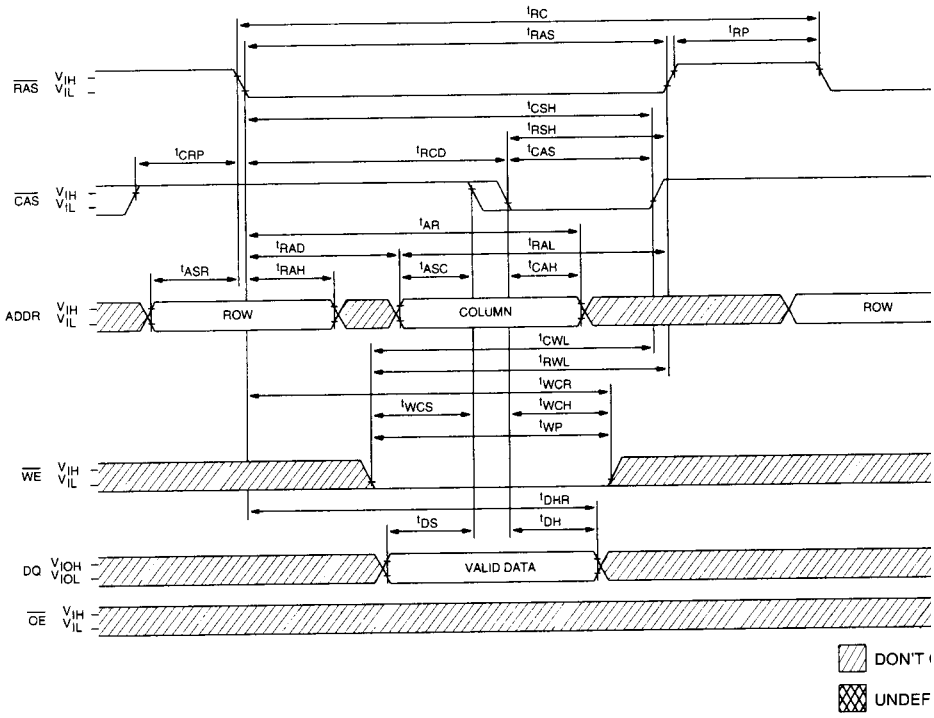
NOTES:

1. All voltages referenced to Vss.
2. This parameter is sampled, not 100% tested. Capacitance is measured with Vcc=5V, f=1 MHz at less than 50mVrms, T_A = 25°C ±3°C, Vbias = 2.4V applied to each input and output individually with remaining inputs and outputs open.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C < T_A < 125°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS\ refresh cycles (RAS\-ONLY or CBR with WE\ HIGH) before proper device operation is assured. The eight RAS\ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume t_T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS\ = V_{IH}, data outputs (DQs) are High-Z.
12. If CAS\ = V_{IL}, data outputs (DQs) may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $t_{RCD} < t_{RCD}$ (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} > t_{RCD}$ (MAX)
16. If CAS\ is LOW at the falling edge of RAS\, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS\ must be pulsed HIGH for t_{CPN}.
17. Operation within the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, then access time is controlled exclusively by t_{CAC}.
18. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, then access time is controlled exclusively by t_{AA}.
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. t_{OFF} (MAX) defines the time at which the output achieves the open circuit conditions and is not referenced to V_{OH} or V_{OL}.
21. t_{WCS}, t_{RWD}, t_{AWD}, and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY-WRITE cycles. t_{RWD}, t_{AWD}, and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} > t_{WCS}$ (MIN), the cycle is an EARLY-WRITE cycles and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} > t_{RWD}$ (MIN), $t_{AWD} > t_{AWD}$ (MIN) and $t_{CWD} > t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate. OE\ held HIGH and WE\ taken LOW after CAS\ goes LOW results in a LATE-WRITE (OE\ controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to CAS\ leading edge in EARLY-WRITE cycle and WE\ leading edge in LATE-WRITE cycles and WE\ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycle.
23. If OE\ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE\=LOW and OE\=HIGH.
25. t_{WTS} and t_{WTH} are setup and hold specifications for the WE\ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of t_{WRP} and t_{WRH} in the CBR REFRESH cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met (OE\ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS\ remains LOW and OE\ is taken back LOW after t_{OEH} is met. If CAS\ goes HIGH prior to OE\ going back LOW, the DQs will remain open.
27. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If CAS\ goes HIGH first, OE\ becomes a “don’t care.” If OE\ goes HIGH and CAS\ stays LOW, OE\ is not a “don’t care;” and the DQs will provide the previously read data if OE\ is taken back LOW (while CAS\ remains LOW).
28. JEDEC test mode only.

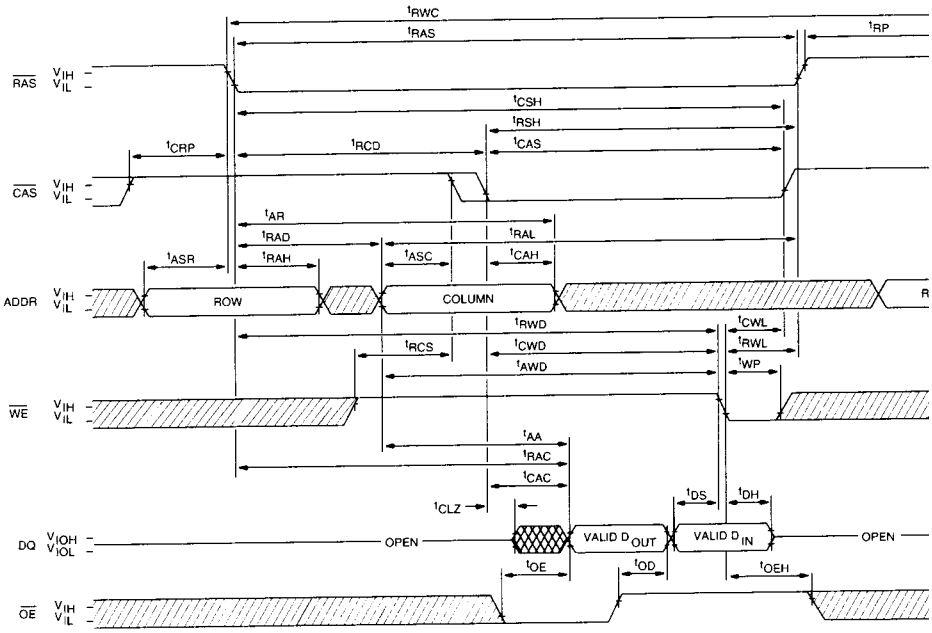
READ CYCLE



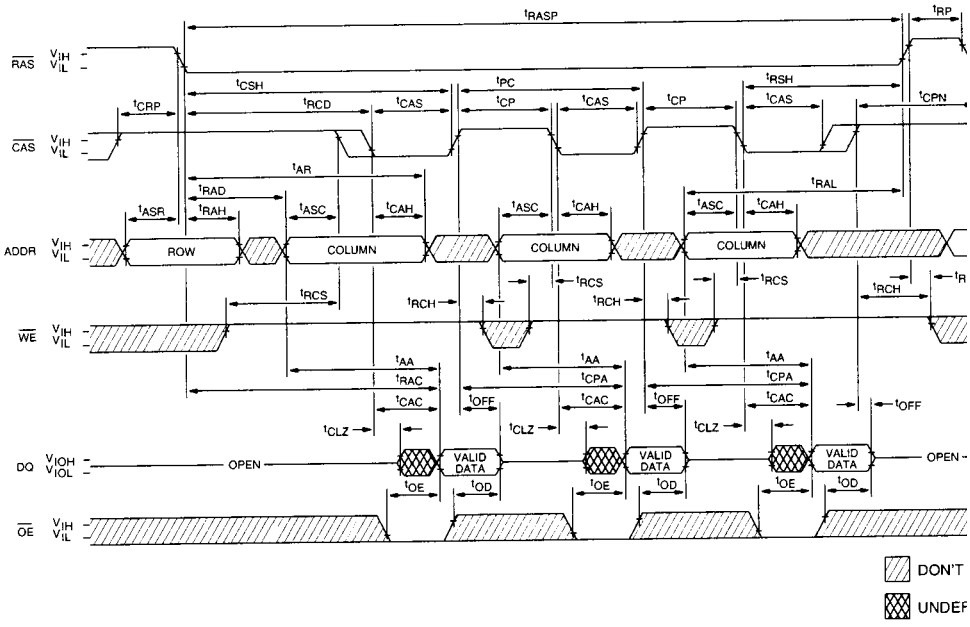
EARLY-WRITE CYCLE



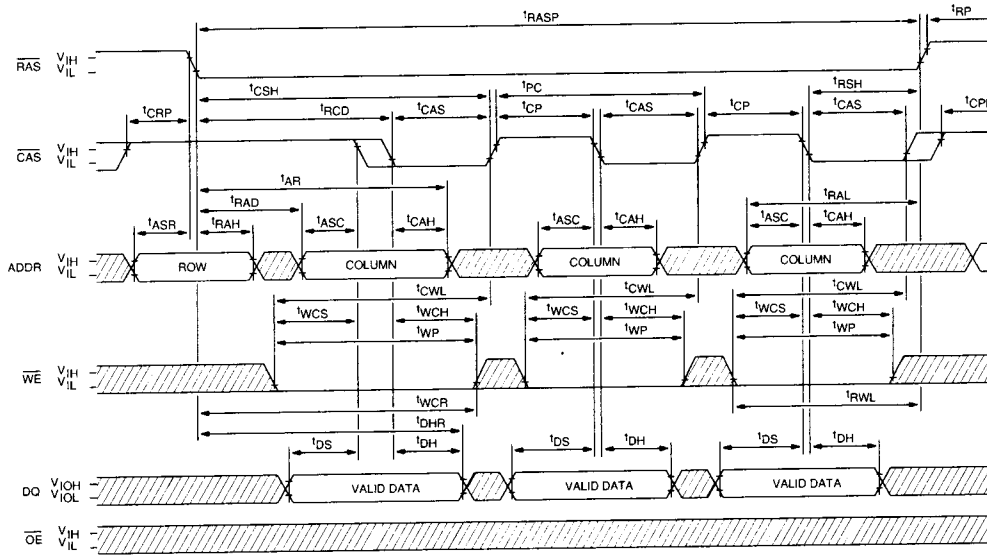
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



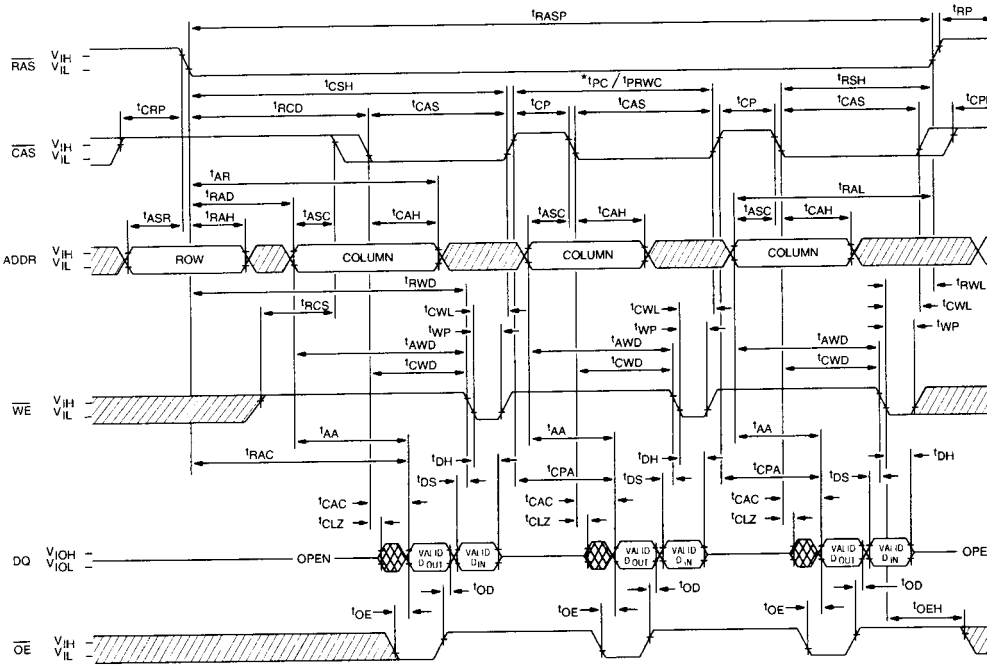
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

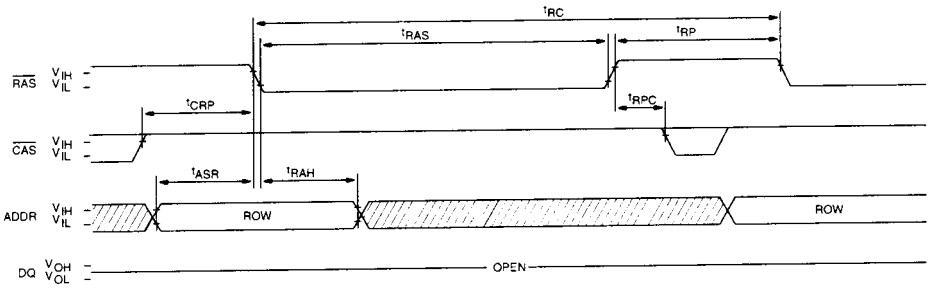


*t_{PC} = LATE-WRITE cycle
t_{PRWC} = FAST READ-MODIFY-WRITE cycle

DON'T CARE
UNDEFINED

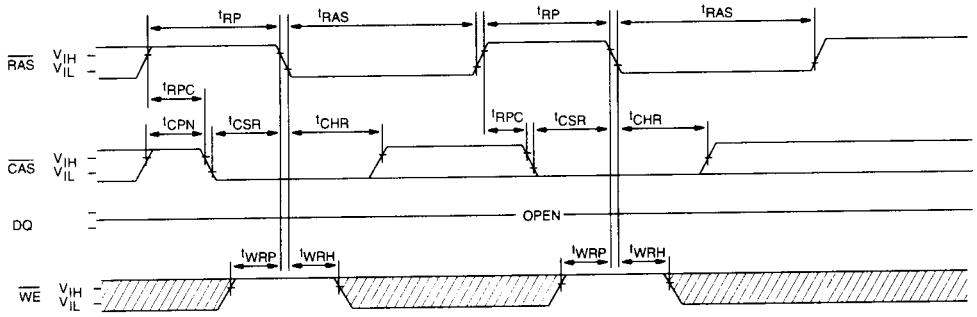
RAS\-ONLY REFRESH CYCLE

(ADDR = A0-A9; WE\ = Don't Care)



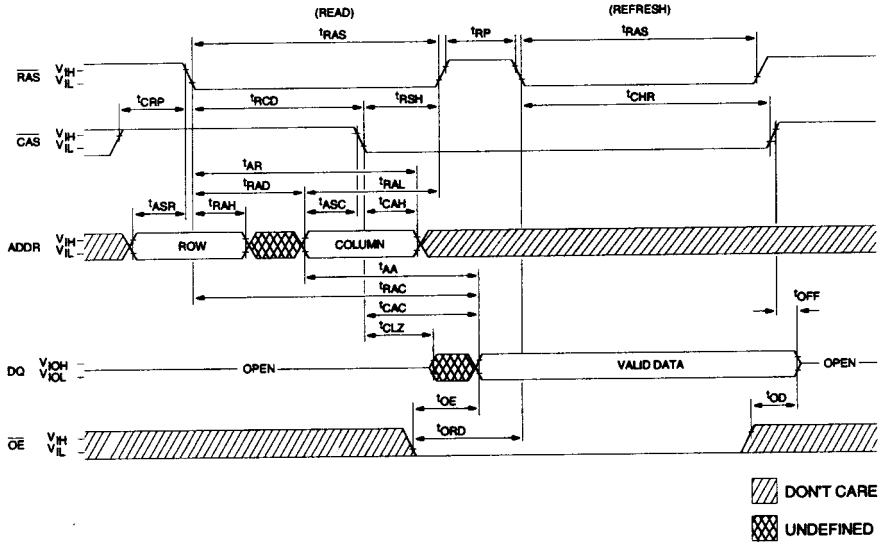
CAS\-BEFORE-RAS\ REFRESH CYCLE

(A0-A9, and OE\ = DON'T CARE)



HIDDEN REFRESH CYCLE[24]

(WE\ = HIGH, OE\ = LOW)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR (CAS\-BEFORE-RAS\) REFRESH cycle. The CBR for the 1 Meg specifies the WE\ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE\ pin held at a voltage HIGH level.

A CBR cycle with WE\ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

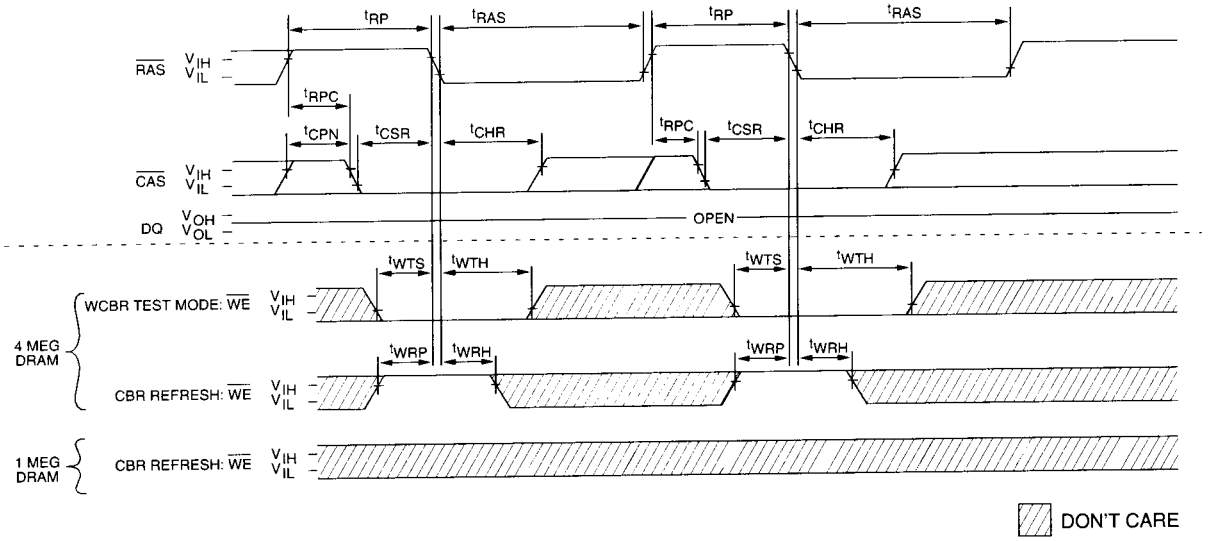
POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS\ cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS\-ONLY or CBR REFRESH (WE\ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a RAS\-ONLY or a CBR REFRESH cycle (WE\ held HIGH).

SUMMARY

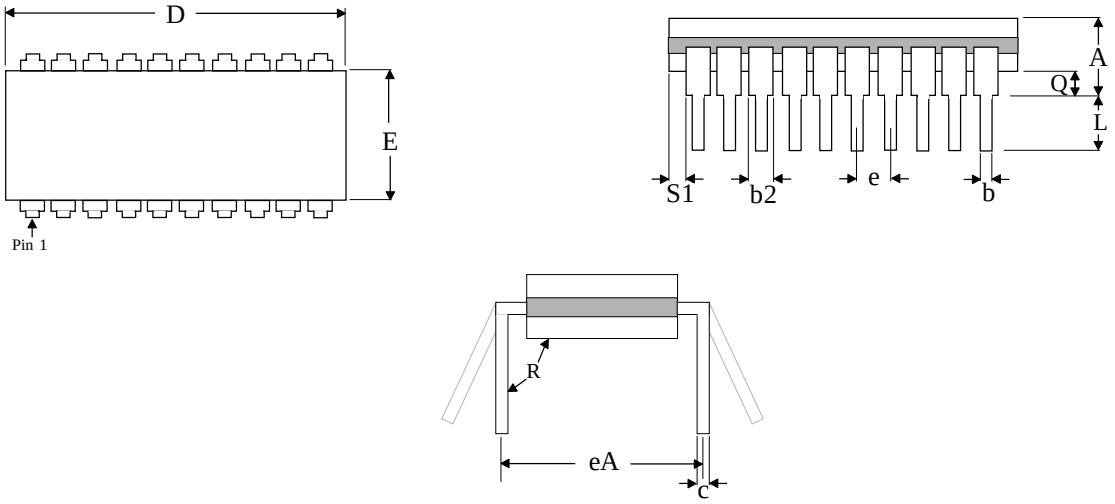
1. The 1 Meg CBR REFRESH allows the WE\ pin to be "don't care" while the 4 Meg CBR requires WE\ to be HIGH.
2. The eight RAS\ wake-up cycles on the 1 Meg may be any valid RAS\ cycle while the 4 Meg may only use RAS\-ONLY or CBR REFRESH cycles (WE\ held HIGH).

COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



MECHANICAL DEFINITIONS*

ASI Case #103 (Package Designator CN)
SMD 5962-90847, Case Outline R



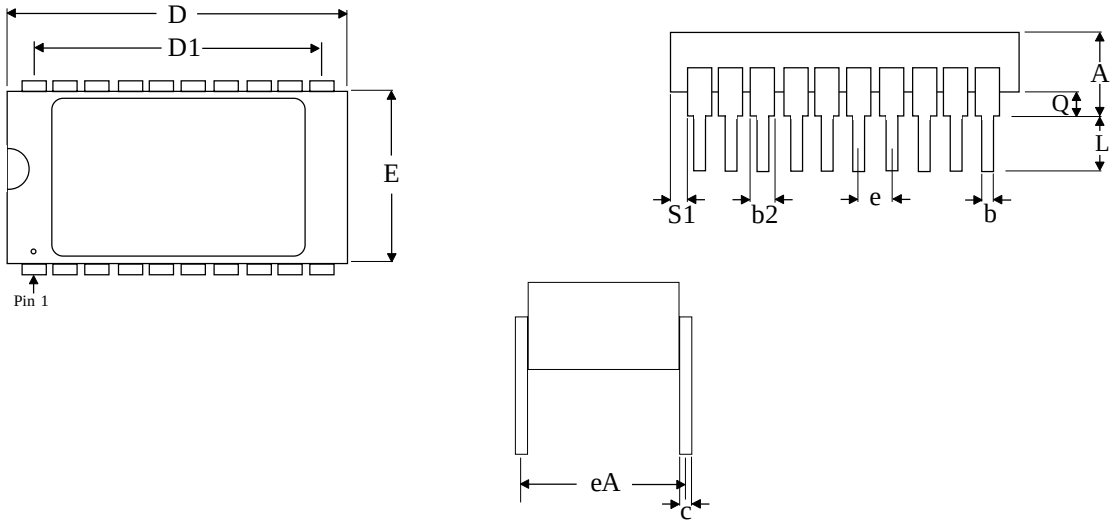
SYMBOL	SMD Specifications	
	MIN	MAX
A	---	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
Q	0.015	0.070
L	0.125	0.200
S1	0.005	---
R	90°	105°

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #104 (Package Designator C)
SMD 5962-90847, Case Outline U



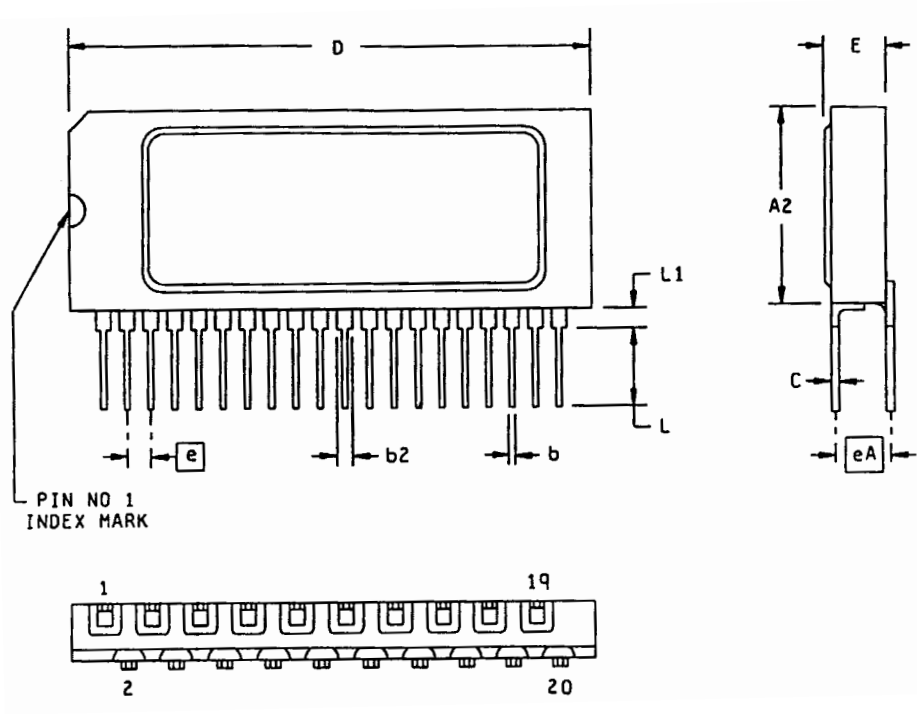
SYMBOL	SMD Specifications	
	MIN	MAX
A	---	0.175
b	0.015	0.021
b2	0.045	0.065
c	0.008	0.014
D	0.980	1.030
D1	0.890	0.910
E	0.380	0.410
eA	0.385	0.420
e	0.100 BSC	
Q	0.015	0.060
L	0.125	0.200
S1	---	0.070

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #400 (Package Designator CZ)
SMD 5962-90847, Case Outline N

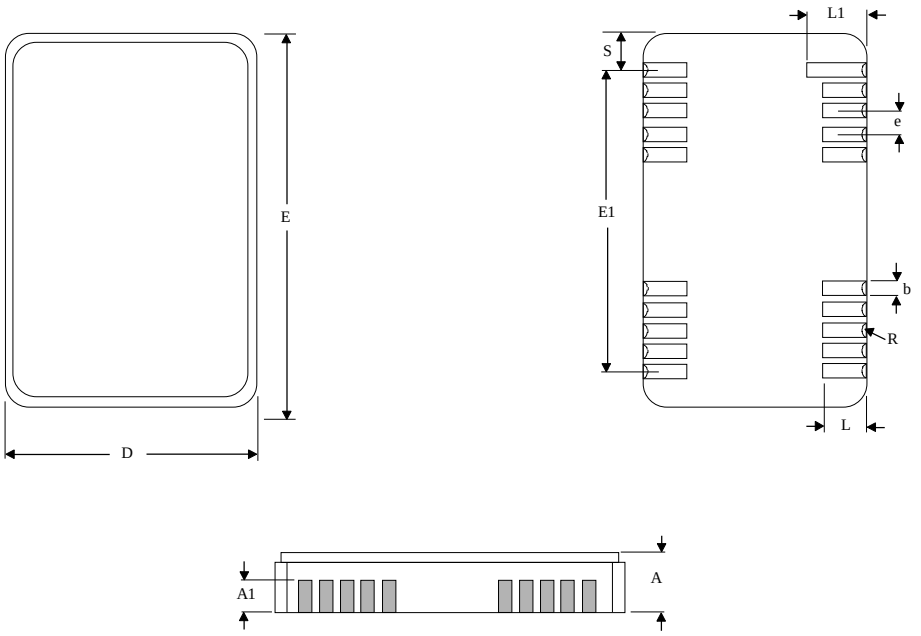


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.355	0.405
b	0.016	0.023
b2	0.035	0.045
c	0.008	0.015
e	0.045	0.055
eA	0.085	0.115
D	1.035	1.065
E	0.100	0.130
L	0.125	0.200
L1	0.015	0.050

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

ASI Case #202 (Package Designator ECN)
SMD 5962-90847, Case Outline T



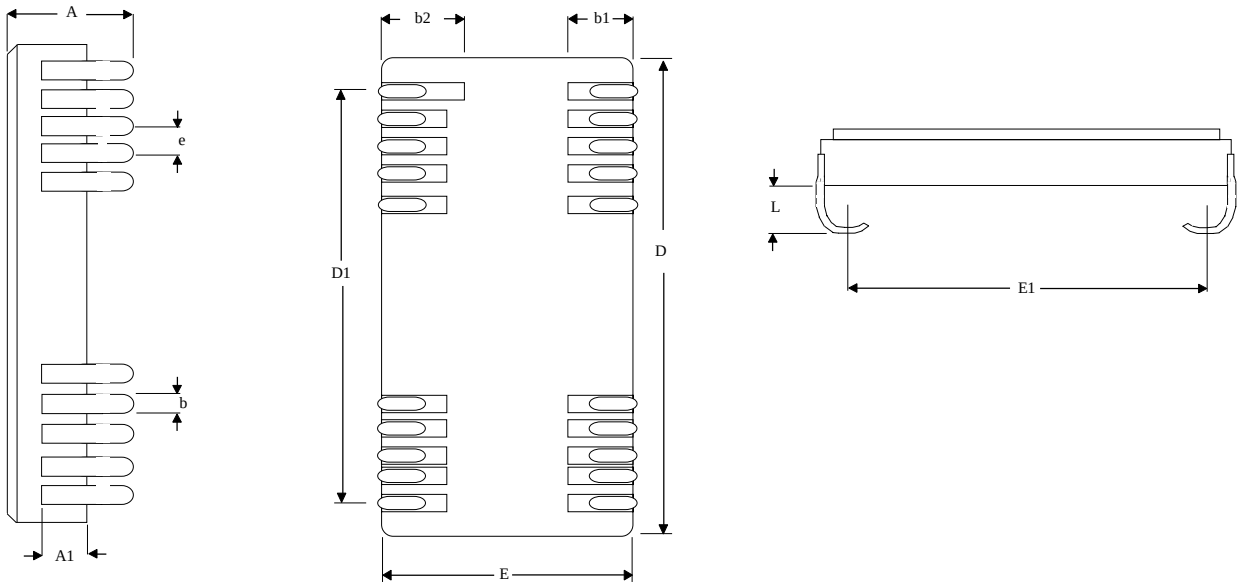
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.080
A1	0.035 TYP	
b	0.022	0.028
D	0.343	0.357
E	0.665	0.685
E1	0.590	0.610
e	0.050 TYP	
L	0.045	0.055
L1	0.080	0.100
R	0.006	0.010
S	0.025	0.050

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITION*

ASI Case #504 (Package Designator ECJ)

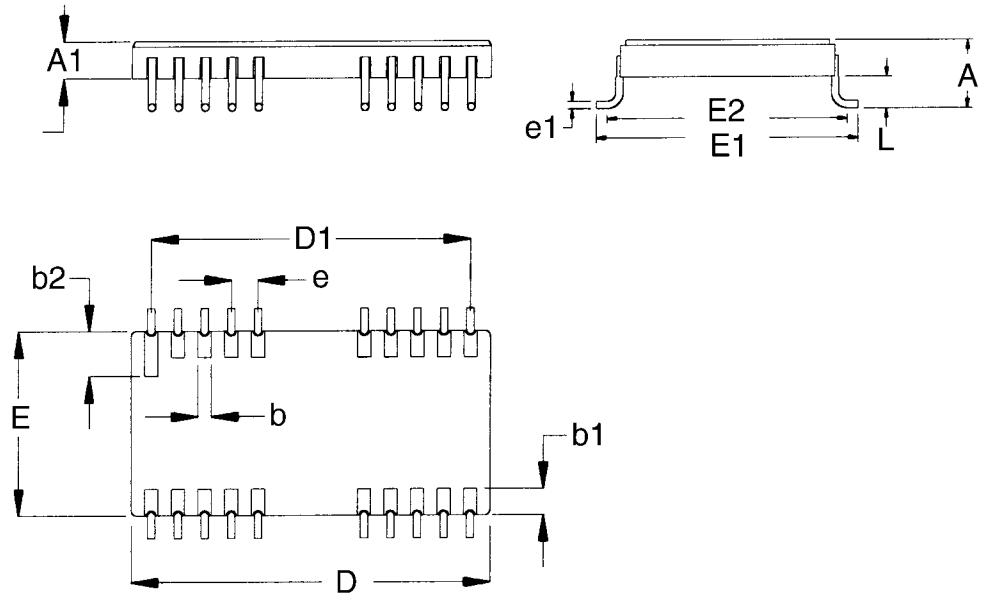


SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.120	0.140
A1	0.066	0.078
b	0.022	0.028
b1	0.050 TYP	
b2	0.090	0.11
D	0.665	0.685
D1	0.592	0.608
E	0.345	0.355
E1	0.345	0.360
e	0.045	0.055
L	0.057	0.063

All measurements are in inches.

MECHANICAL DEFINITION*

ASI Case #600 (Package Designator ECG)



SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.120	0.140
A1	0.066	0.078
b	0.022	0.028
b1	0.050 TYP	
b2	0.090	0.110
D	0.665	0.685
D1	0.592	0.608
E	0.345	0.355
E1	0.482	0.498
E2	0.442	0.458
e	0.045	0.055
e1	0.014 Dia. TYP	
L	0.057	0.063

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT4C4001JCN-8/883C

Device Number	Package Type	Speed ns	Process
MT4C4001J	CN	-7	/*
MT4C4001J	CN	-8	/*
MT4C4001J	CN	-10	/*
MT4C4001J	CN	-12	/*

EXAMPLE: MT4C4001JC-12/883C

Device Number	Package Type	Speed ns	Process
MT4C4001J	C	-7	/*
MT4C4001J	C	-8	/*
MT4C4001J	C	-10	/*
MT4C4001J	C	-12	/*

EXAMPLE: MT4C4001JCZ-7/883C

Device Number	Package Type	Speed ns	Process
MT4C4001J	CZ	-7	/*
MT4C4001J	CZ	-8	/*
MT4C4001J	CZ	-10	/*
MT4C4001J	CZ	-12	/*

EXAMPLE: MT4C4001JECN-10/XT

Device Number	Package Type	Speed ns	Process
MT4C4001J	ECN	-7	/*
MT4C4001J	ECN	-8	/*
MT4C4001J	ECN	-10	/*
MT4C4001J	ECN	-12	/*

EXAMPLE: MT4C4001JECJ-7/IT

Device Number	Package Type	Speed ns	Process
MT4C4001J	ECJ	-7	/*
MT4C4001J	ECJ	-8	/*
MT4C4001J	ECJ	-10	/*
MT4C4001J	ECJ	-12	/*

EXAMPLE: MT4C4001JECG-12/IT

Device Number	Package Type	Speed ns	Process
MT4C4001J	ECG	-7	/*
MT4C4001J	ECG	-8	/*
MT4C4001J	ECG	-10	/*
MT4C4001J	ECG	-12	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range	-40°C to +85°C
XT = Extended Temperature Range	-55°C to +125°C
883C = Full Military Processing	-55°C to +125°C

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator CZ

ASI Part #	SMD Part #
MT4C4001JCZ-8/883C	5962-9084703MNA
MT4C4001JCZ-10/883C	5962-9084702MNA
MT4C4001JCZ-12/883C	5962-9084701MNA

ASI Package Designator C

ASI Part #	SMD Part #
MT4C4001JC-8/883C	5962-9084703MUA
MT4C4001JC-10/883C	5962-9084702MUA
MT4C4001JC-12/883C	5962-9084701MUA

ASI Package Designator CN

ASI Part #	SMD Part #
MT4C4001JCN-8/883C	5962-9084703MRA
MT4C4001JCN-10/883C	5962-9084702MRA
MT4C4001JCN-12/883C	5962-9084701MRA

ASI Package Designator ECN

ASI Part #	SMD Part #
MT4C4001JECN-8/883C	5962-9084703MTA
MT4C4001JECN-10/883C	5962-9084702MTA
MT4C4001JECN-12/883C	5962-9084701MTA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*