

DRAM

1 MEG x 4 DRAM

5V, EDO PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- Single +5V $\pm 10\%$ power supply
- JEDEC-standard pinout and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- Extended Data-Out (EDO) PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- EDO PAGE MODE cycle times, 25-35ns

OPTIONS

- Timing
 - 60ns access
 - 70ns access
- Refresh Rate
 - Standard 16ms period
 - SELF REFRESH and 128ms period
- Packages
 - Plastic SOJ (300 mil)
- Part Number Example: MT4C4007JDJ-7

MARKING

-6
-7

None
S

DJ

KEY TIMING PARAMETERS

SPEED	$\overline{\text{t}}_{\text{RC}}$	$\overline{\text{t}}_{\text{RAC}}$	$\overline{\text{t}}_{\text{PC}}$	$\overline{\text{t}}_{\text{AA}}$	$\overline{\text{t}}_{\text{CAC}}$	$\overline{\text{t}}_{\text{CAS}}$
-6	110ns	60ns	25ns	30ns	18ns	10ns
-7	130ns	70ns	33ns	35ns	22ns	15ns

GENERAL DESCRIPTION

The MT4C4007J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a $\times 4$ configuration with optional SELF REFRESH. During READ or WRITE cycles, each of the 4 memory bits (1 bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ latches the first 10 bits and $\overline{\text{CAS}}$ latches the latter 10 bits.

A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last, however, only EARLY WRITE cycles are supported. LATE WRITE cycles should not be attempted

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1)

DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{\text{WE}}$	3	24	DQ3
$\overline{\text{RAS}}$	4	23	$\overline{\text{CAS}}$
A9	5	22	OE
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

as the results are not predictable. When $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW (EARLY WRITE cycle), the output pins remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and OE.

PAGE ACCESS

PAGE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

The PAGE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates PAGE operation.

EDO PAGE MODE

The MT4C4007J provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{\text{CAS}}$ goes back HIGH. EDO provides for $\overline{\text{CAS}}$ precharge time ($\overline{\text{t}}_{\text{CP}}$) to occur without the output data going invalid. This elimination of $\overline{\text{CAS}}$ output control provides for pipeline READs.

PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{\text{CAS}}$. EDO

EDO PAGE MODE (continued)

operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{\text{CAS}}$ goes HIGH, as long as $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are held LOW and $\overline{\text{WE}}$ is held HIGH. $\overline{\text{OE}}$ can be brought LOW or HIGH while $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{\text{OE}}$, there are two methods to disable the outputs and keep them disabled during the $\overline{\text{CAS}}$ HIGH time. The first method is to have $\overline{\text{OE}}$ HIGH when $\overline{\text{CAS}}$ transitions HIGH and keep $\overline{\text{OE}}$ HIGH for t_{OEHC} . This will tristate the DQs and they will remain tristate, regardless of $\overline{\text{OE}}$, until $\overline{\text{CAS}}$ falls again. The second method is to have $\overline{\text{OE}}$ LOW when $\overline{\text{CAS}}$ transitions HIGH. Then $\overline{\text{OE}}$ can pulse

HIGH for a minimum of t_{OEP} anytime during the $\overline{\text{CAS}}$ HIGH period and the DQs will tristate and remain tristate, regardless of $\overline{\text{OE}}$, until $\overline{\text{CAS}}$ falls again (please reference Figure 1 for further detail on the toggling $\overline{\text{OE}}$ condition). During cycles other than PAGE-MODE READ, the outputs are disabled at t_{OFF} time after $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are HIGH, or t_{WHZ} after $\overline{\text{WE}}$ transitions LOW. The t_{OFF} time is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last. $\overline{\text{WE}}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 2.

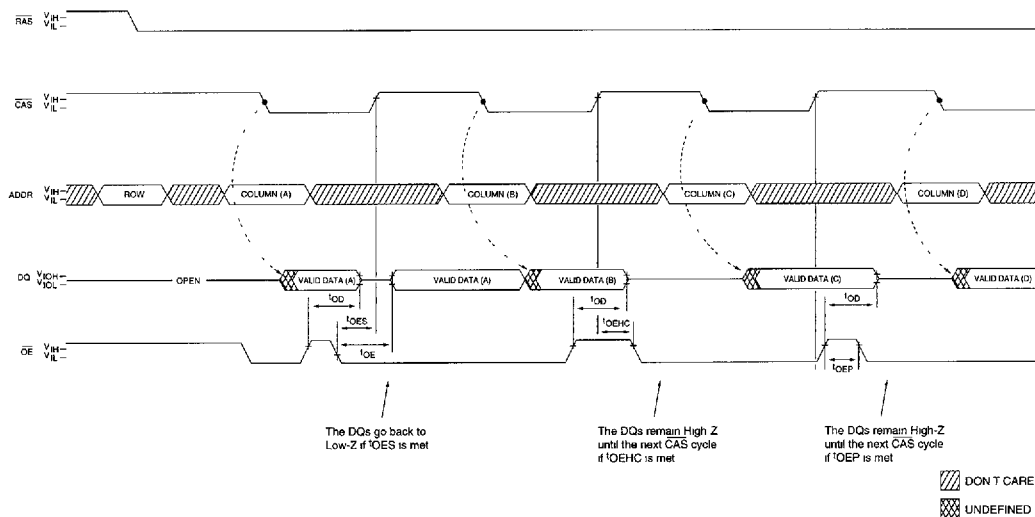


Figure 1
OUTPUT ENABLE AND DISABLE

REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed within $t_{\text{REF max}}$, regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

An optional SELF REFRESH mode is also available on the MT4C4007J(S). The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding $\overline{\text{RAS}}$ LOW for the specified t_{RASS} . Additionally, the "S" version allows for an extended refresh period of 128ms, or 125 μ s per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving $\overline{\text{RAS}}$ HIGH for a minimum time of t_{RPS} . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{\text{RAS}}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes $\overline{\text{RAS}}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time.

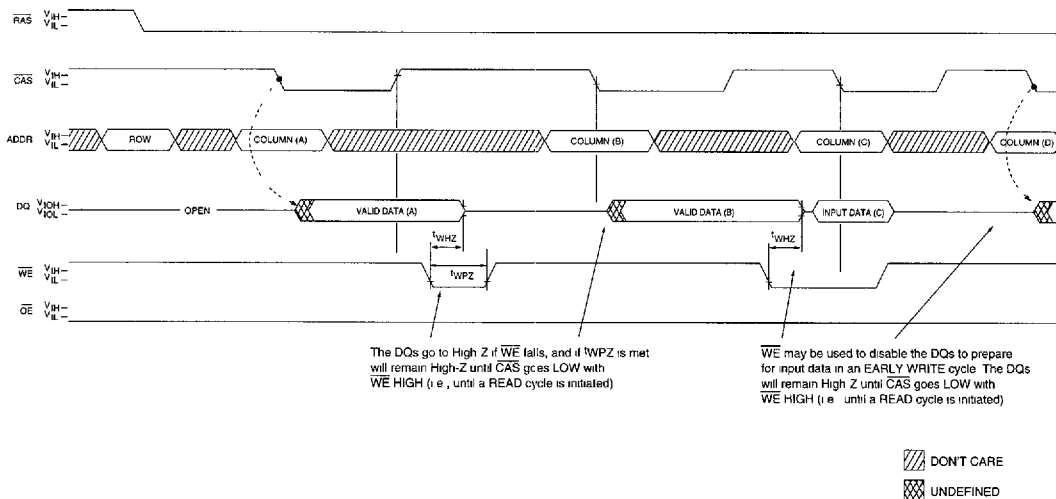
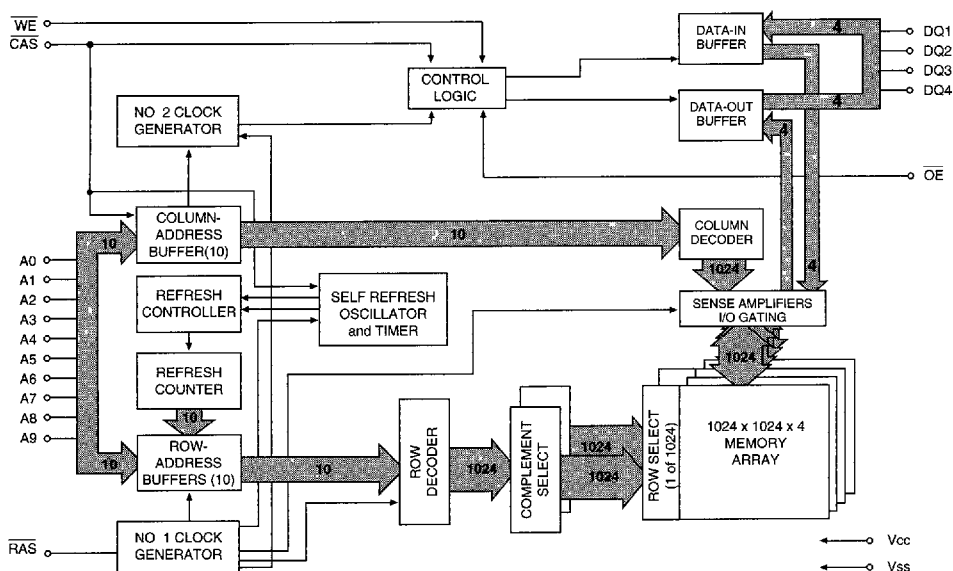


Figure 2
OUTPUT ENABLE AND DISABLE USING $\overline{\text{WE}}$

FUNCTIONAL BLOCK DIAGRAM
EDO PAGE MODE

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA-IN/OUT
						'R	'C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V _{SS}	-1.0V to +7V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	V _{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 6.5V (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
TTL OUTPUT LEVELS	High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4	V	
	Low Voltage (I _{OUT} = 4.2mA)	V _{OL}	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 (Notes: 1, 6, 7) ($V_{CC} = +5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-6	-7		
STANDBY CURRENT: (TTL) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS} = \overline{CAS} = \text{Other Inputs} = V_{CC} - 0.2V$)	I_{CC2}	1	1	μA	
	I_{CC2} (S only)	200	200	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC} = t_{RC} [MIN]$)	I_{CC3}	110	100	mA	3, 4, 30
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling: $t_{PC} = t_{PC} [MIN]$)	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC} [MIN]$)	I_{CC5}	110	100	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC} = t_{RC} [MIN]$)	I_{CC6}	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: $\overline{CAS} = 0.2V$ or CBR cycling; $\overline{RAS} = t_{RAS} (MIN)$; $\overline{WE} = V_{CC} - 0.2V$; $A0-A9$ and $D_{IN} = V_{CC} - 0.2V$ or $0.2V$ (D_{IN} may be left open); $t_{RC} = 125\mu s$ (1,024 rows at $125\mu s = 128ms$)	I_{CC7} (S only)	300	300	μA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $t_{RAS} \geq t_{RASS} (MIN)$ and $\overline{CAS}$ held LOW; $\overline{WE} = V_{CC} - 0.2$; $A0-A9$ and $D_{IN} = V_{CC} - 0.2V$ or $0.2V$ (D_{IN} may be left open)	I_{CC8} (S only)	300	300	μA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: $A0-A9$	C_{i1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{i2}	7	pF	2
Input/Output Capacitance: DQ	C_{iO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t_{AA}		30		35	ns	
Column-address setup to CAS precharge during WRITE	t_{ACH}	15		15		ns	
Column-address hold time (referenced to RAS)	t_{AR}	45		50		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Access time from CAS	t_{CAC}		18		22	ns	15
Column-address hold time	t_{CAH}	10		15		ns	
CAS pulse width	t_{CAS}	10	10,000	15	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH cycle	t_{CHD}	10		10		ns	28
CAS hold time (CBR REFRESH)	t_{CHR}	10		10		ns	5
CAS to output in Low-Z	t_{CLZ}	3		3		ns	
Data output hold after CAS LOW	t_{COH}	5		5		ns	
CAS precharge time	t_{CP}	10		10		ns	16
Access time from CAS precharge	t_{CPA}		35		40	ns	
CAS to RAS precharge time	t_{CRP}	10		10		ns	
CAS hold time	t_{CSH}	50		55		ns	
CAS setup time (CBR REFRESH)	t_{CSR}	10		10		ns	5
Write command to CAS lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	10		13		ns	22
Data-in hold time (referenced to RAS)	t_{DHR}	45		55		ns	
Data-in setup time	t_{DS}	0		0		ns	22
Output disable	t_{OD}		15		20	ns	26
Output Enable time	t_{OE}		15		20	ns	23
OE HIGH hold time from CAS HIGH	t_{OEHC}	10		10		ns	
OE HIGH pulse width	t_{OEP}	10		10		ns	
OE LOW to CAS HIGH setup time	t_{OES}	5		5		ns	
Output buffer turn-off delay	t_{OFF}	3	15	3	20	ns	20
OE setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	25		33		ns	
Access time from RAS	t_{RAC}		60		70	ns	14
RAS to column-address delay time	t_{RAD}	15	30	15	35	ns	18
Row-address hold time	t_{RAH}	10		10		ns	
Column-address to RAS lead time	t_{RAL}	30		35		ns	

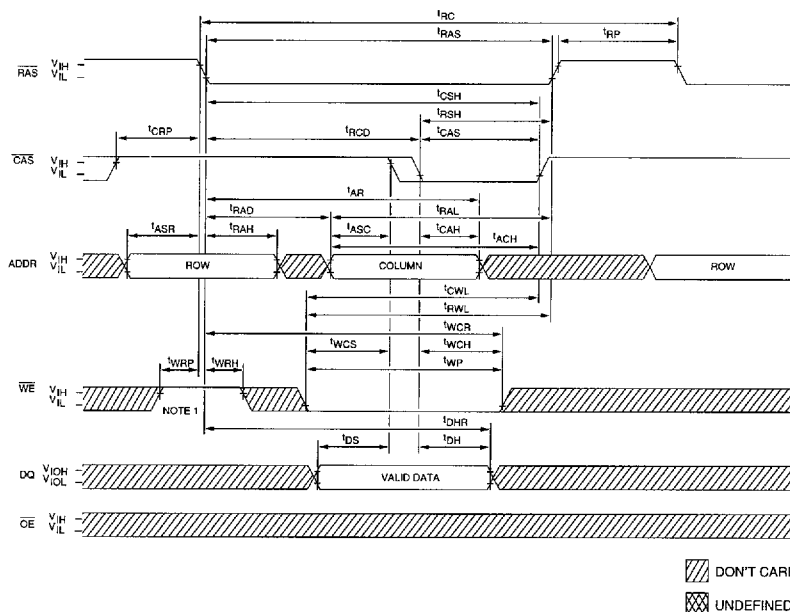
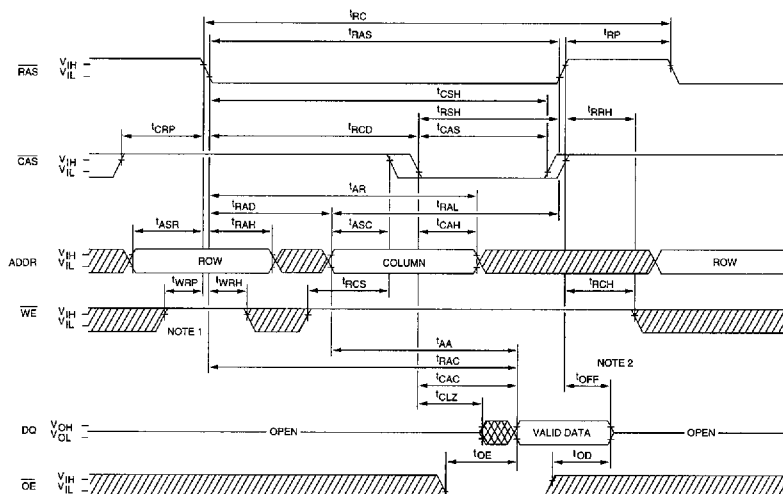
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
RAS pulse width	t_{RAS}	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	t_{RASP}	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH cycle	t_{RASS}	100		100		μs	28
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
RAS to CAS delay time	t_{RCD}	20	45	20	50	ns	17
Read command hold time (referenced to CAS)	t_{RCH}	0		0		ns	19
Read command setup time	t_{RCS}	0		0		ns	
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
Refresh period (1,024 cycles) S version	t_{REF}		128		128	ms	
RAS precharge time	t_{RP}	40		50		ns	
RAS to CAS precharge time	t_{RPC}	0		0		ns	
RAS precharge time during SELF REFRESH cycle	t_{RPS}	110		130		ns	28
Read command hold time (referenced to RAS)	t_{RRH}	0		0		ns	19
RAS hold time	t_{RSH}	15		20		ns	
Write command to RAS lead time	t_{RWL}	15		20		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	9, 10
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to RAS)	t_{WCR}	45		55		ns	
WE command setup time	t_{WCS}	0		0		ns	21, 26
Output disable delay from WE (CAS HIGH)	t_{WHZ}	3	15	3	20	ns	
Write command pulse width	t_{WP}	10		15		ns	
WE pulse width for output disable when CAS HIGH	t_{WPZ}	10		10		ns	
WE hold time (CBR REFRESH)	t_{WRH}	10		10		ns	25
WE setup time (CBR REFRESH)	t_{WRP}	10		10		ns	25

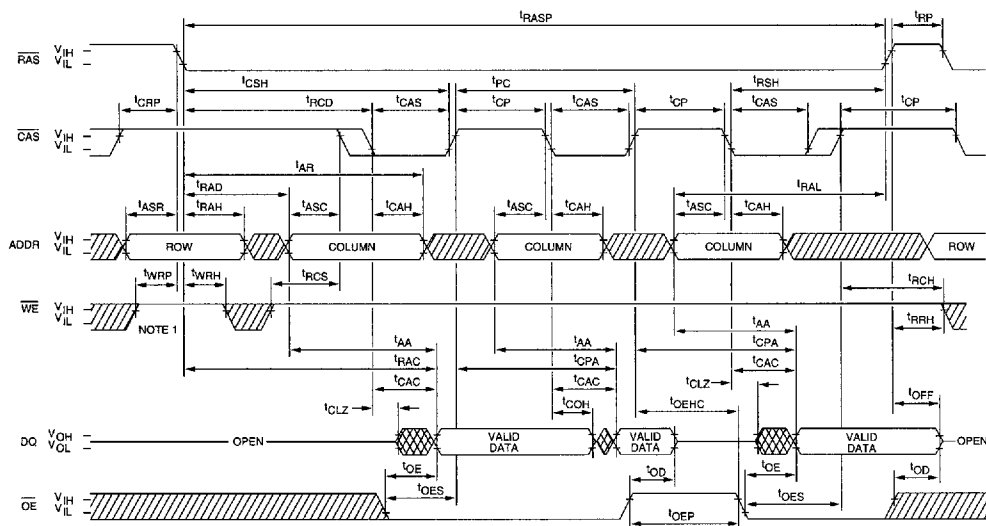
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +5V$; $f = 1\text{ MHz}$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of $100\mu s$ is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $\overline{REF}$ refresh requirement is exceeded.
8. AC characteristics assume $T = 2.5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS} = V_{IH}$, data output is High-Z.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and $100pF$.
14. Assumes that $t_{RCD} < t_{RCD}(\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD}(\text{MAX})$.
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CP} .
17. Operation within the $t_{RCD}(\text{MAX})$ limit ensures that $t_{RAC}(\text{MAX})$ can be met. $t_{RCD}(\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{MAX})$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD}(\text{MAX})$ limit ensures that $t_{RCD}(\text{MAX})$ can be met. $t_{RAD}(\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{MAX})$ limit, access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. If the cycle is a READ-MODIFY-WRITE, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$ -controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
23. Even if $\overline{OE}$ is HIGH, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.
25. t_{WTS} and t_{WTH} are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of t_{WRP} and t_{WRH} in the CBR REFRESH cycle.
26. The DQs open during READ cycles once t_{OD} or t_{OFF} occur.
27. Extended refresh current is reduced as t_{RAS} is reduced from its maximum specification during the extended refresh cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
29. Column-address changed once each cycle.

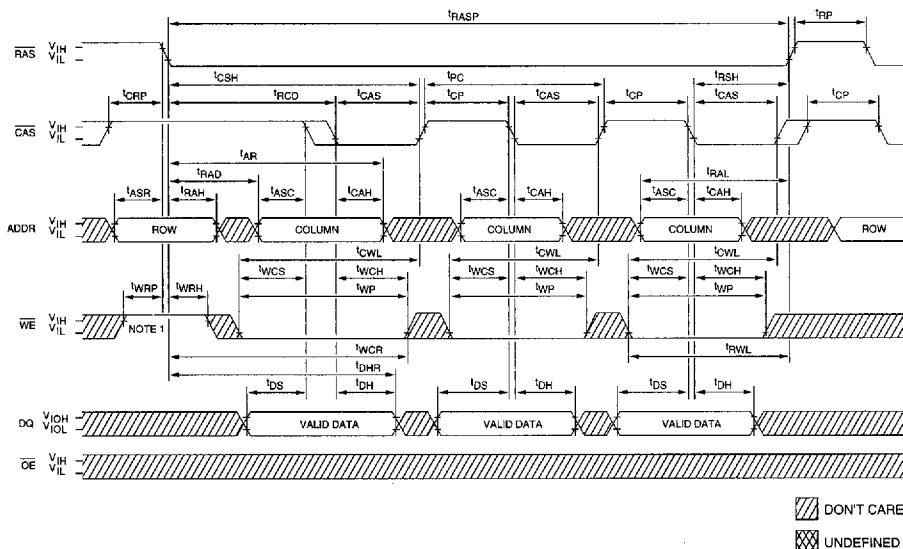


UNDEFINED

EDO-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



 DON'T CARE

 UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a “don’t care” at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH . This design implementation will facilitate compatibility with future EDO DRAMs.

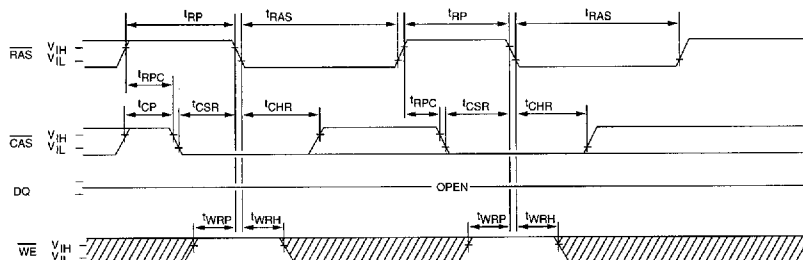
The timing diagram illustrates the relationship between several signals: RAS, CAS, ADDR, WE, DO, and OE. It defines the following timing parameters:

- t_{RASP} : RAS pulse width
- t_{CRP} : RAS to CAS setup time
- t_{CSH} : RAS to CAS hold time
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{CP} : CAS to output delay
- t_{PC} : CAS to output delay (for column A)
- t_{RSH} : RAS to output delay
- t_{CAS} : CAS to output delay (for column N)
- t_{CP} : CAS to output delay (for column N)
- t_{AR} : Address to output delay
- t_{ASC} : Address to output delay (for column A)
- t_{CAH} : Address to output delay (for column A)
- t_{ASC} : Address to output delay (for column B)
- t_{CAH} : Address to output delay (for column B)
- t_{ASC} : Address to output delay (for column N)
- t_{CAH} : Address to output delay (for column N)
- t_{WRP} : Write pulse width
- t_{WRH} : Write pulse hold time
- t_{RCS} : RAS to output delay
- t_{RCH} : RAS to output delay (for column A)
- t_{WCS} : Write to output delay
- t_{WCH} : Write to output delay (for column A)
- t_{AA} : Address to output delay
- t_{RAC} : RAS to output delay
- t_{CAC} : CAS to output delay
- t_{CPA} : CAS to output delay
- t_{CAC} : CAS to output delay
- t_{COH} : CAS to output delay
- t_{WHZ} : Write to output delay
- t_{DS} : Data to output delay
- t_{DH} : Data to output delay
- t_{OE} : Output enable pulse width

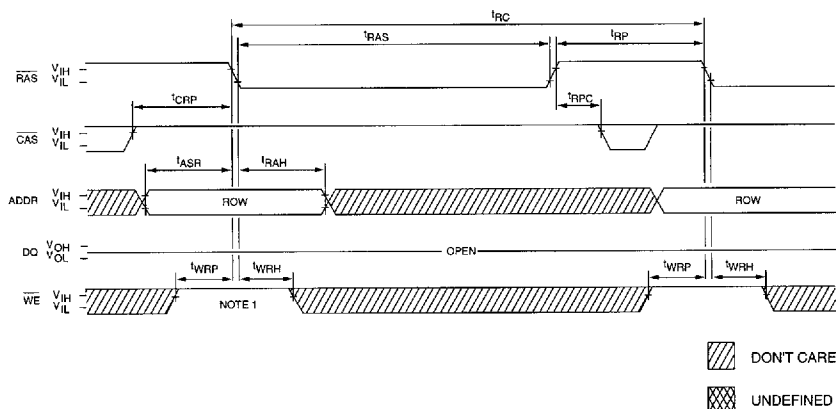
Timing diagram for a 64K16 static CMOS RAM. The diagram illustrates the relationship between RAS, CAS, ADDR, DQ, and OE signals during (READ) and (REFRESH) operations. Key timing parameters are labeled, including t_{RAS} , t_{RP} , t_{RCD} , t_{RSH} , t_{CRP} , t_{CHR} , t_{AR} , t_{RAD} , t_{RAH} , t_{ASC} , t_{CAH} , t_{ASR} , t_{AA} , t_{RAC} , t_{CAC} , t_{CLZ} , t_{OE} , t_{OD} , and t_{OFF} . The data bus DQ shows 'OPEN' and 'VALID DATA' states. Address lines are labeled 'ROW' and 'COLUMN'. A legend indicates that hatched areas are 'DON'T CARE' and cross-hatched areas are 'UNDEFINED'.

6111549 0012022 T04

CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



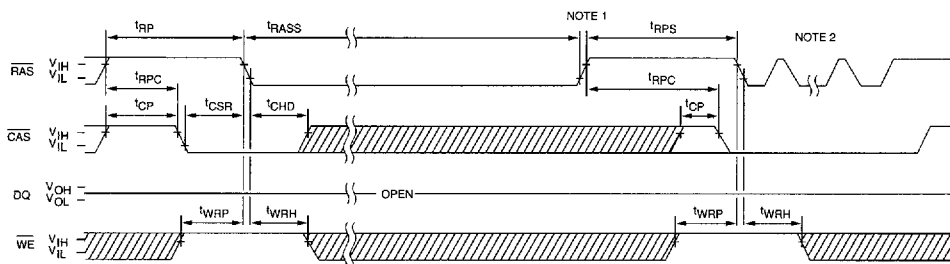
RAS-ONLY REFRESH CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

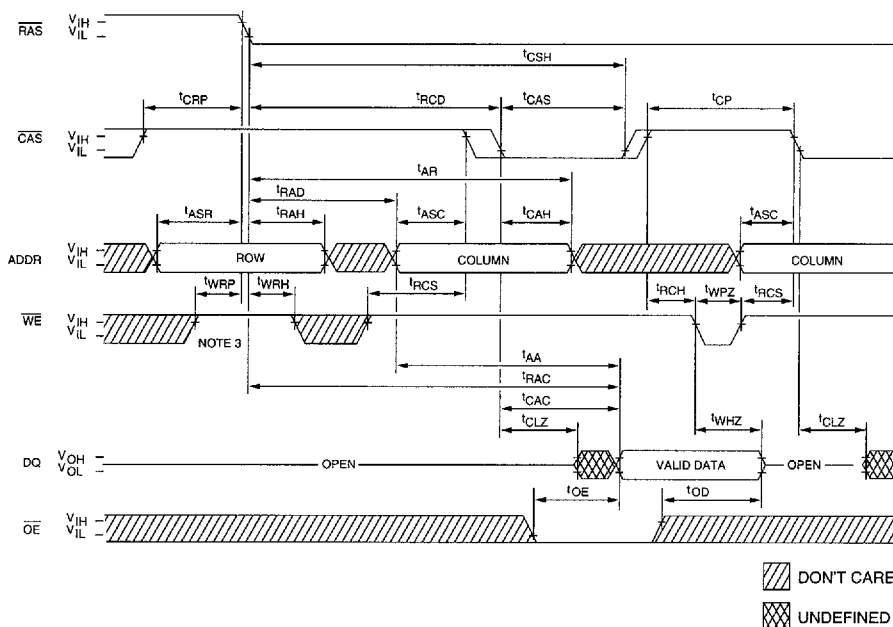
SELF REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



READ CYCLE

(with $\overline{WE}$ -controlled disable)



- NOTE:**
1. Once t_{RASS} (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
 2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed.
 3. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.