DRAM

MT4LC2M8B1

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC- and industry-standard x8 pinouts, timing, functions and packages
- High-performance, low-power CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Optional self refresh (S) for low-power data retention
- 2,048-cycle refresh (11 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) access

OPTIONS — MARKING

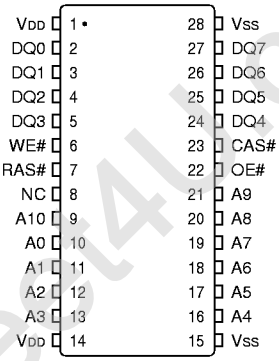
- Packages
  - Plastic 28-pin SOJ (300 mil) — DJ
  - Plastic 28-pin SOJ (400 mil) — DW
  - Plastic 28-pin TSOP (300 mil) — TG
- Timing
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh (32ms period) — None
  - Self Refresh (128ms period) — S*

NOTE: 1. The # symbol indicates signal is active LOW.

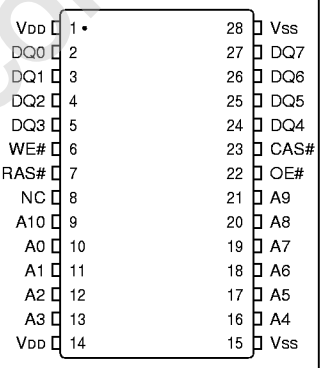
*Contact factory for availability

PIN ASSIGNMENT (Top View)

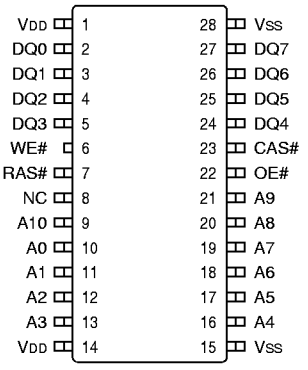
28-Pin SOJ



28-Pin SOJ



28-Pin TSOP



KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

2 MEG x 8 FPM DRAM PART NUMBERS

PART NUMBER	PACKAGE	REFRESH
MT4LC2M8B1DJ-6	SOJ	Standard
MT4LC2M8B1DJ-6 S	SOJ	Self
MT4LC2M8B1TG-6	TSOP	Standard
MT4LC2M8B1TG-6 S	TSOP	Self

GENERAL DESCRIPTION

The 2 Meg x 8 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x8 configuration. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS# latching 11 bits (A0-A10) and then CAS# latching 10 bits (A0-A9).

The CAS# control also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS# goes LOW.

READ or WRITE cycles are selected by WE#. A logic HIGH on WE# dictates read mode while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. Taking WE# LOW will initiate a WRITE cycle, selecting DQ0-DQ7. If WE# goes LOW prior to CAS#

GENERAL DESCRIPTION (continued)

going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle. If WE# goes LOW after CAS# goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# and OE# remain LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by OE# and WE#.

The MT4LC2M8B1 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS# followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR, or HIDDEN) so that all 2,048 combinations of RAS# addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed within ^{t}REF (MAX), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

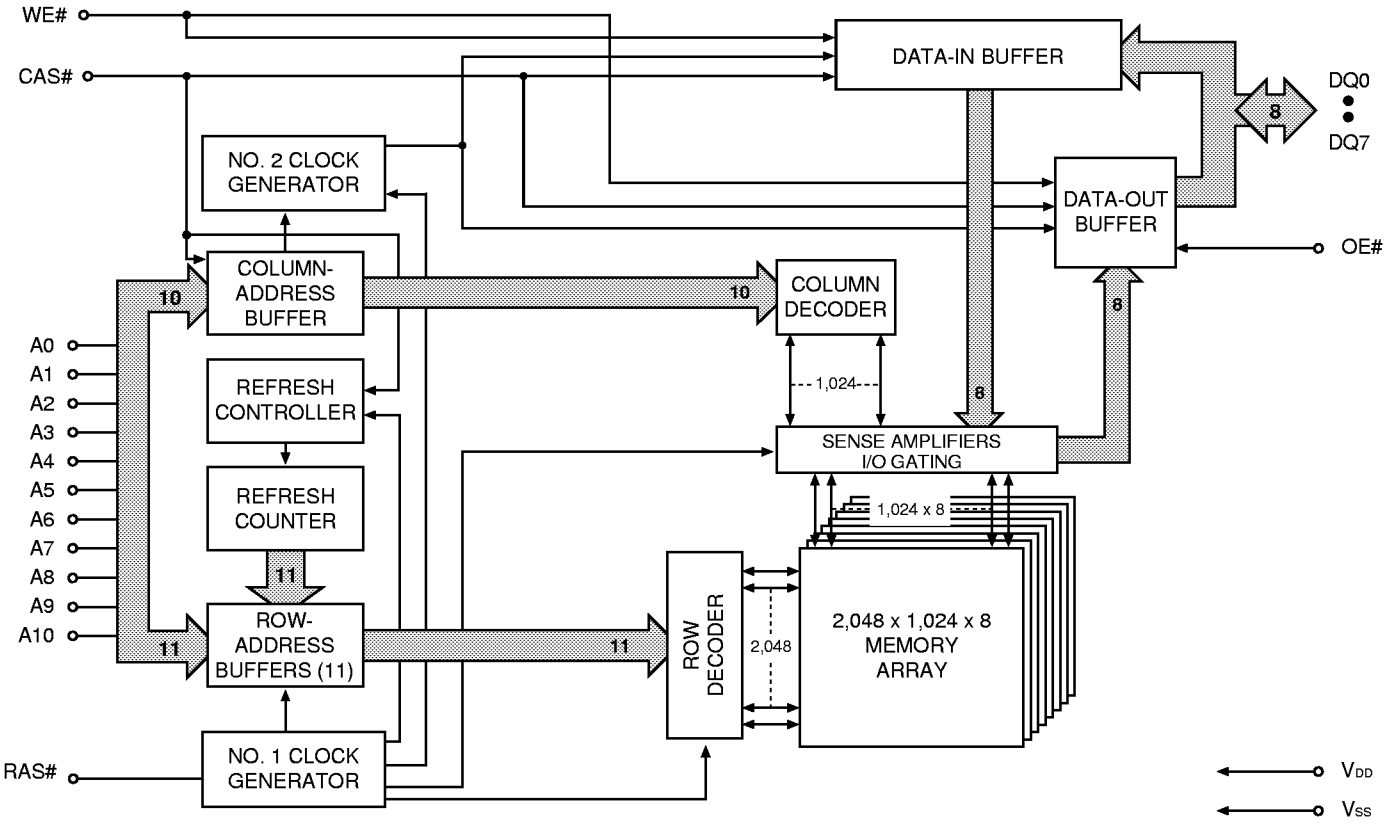
An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 62.5µs per row, if using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all 2,048 rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on NC, Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	5.5	V	24
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-0.5	0.8	V	24
INPUT LEAKAGE CURRENT: Any input at V_{IN} ($0V \le V_{IN} \le V_{DD} + 0.3V$); All other pins not under test = 0V	I_I	-2	2	µA	
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} ($0V \le V_{OUT} \le V_{DD} + 0.3V$); DQ is disabled and in High-Z state	I_{OZ}	-5	5	µA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SPEED	MAX	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	-6	1	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	-6	1	mA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	-6	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	-6	100	mA	22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC4}	-6	80	mA	22
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC5}	-6	100	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	-6	100	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^{t}RAS (MIN); WE# = V_{DD} - 0.2V; A0-A11, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open); ^{t}RC = 31.25µs	I_{CC7}	-6	300	µA	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# ≥ $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{DD} - 0.2V; A0-A11, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	-6	300	µA	4, 7

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Column address to WE# delay time	^tAWD	55		ns	18
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		ns	
CAS# hold time (CBR Refresh)	^tCHR	10		ns	4
CAS# to output in Low-Z	^tCLZ	3		ns	23
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	5		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		ns	4
CAS# to WE# delay time	^tCWD	40		ns	18
WRITE command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	19
Data-in setup time	^tDS	0		ns	19
Output disable	^tOD	3	15	ns	23
Output enable	^tOE		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	15		ns	
Output buffer turn-off delay	^tOFF	3	15	ns	17, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	125,000	ns	
RAS# pulse width during Self Refresh	^tRASS	100		µs	
Random READ or WRITE cycle time	^tRC	110		ns	

AC ELECTRICAL CHARACTERISTICS

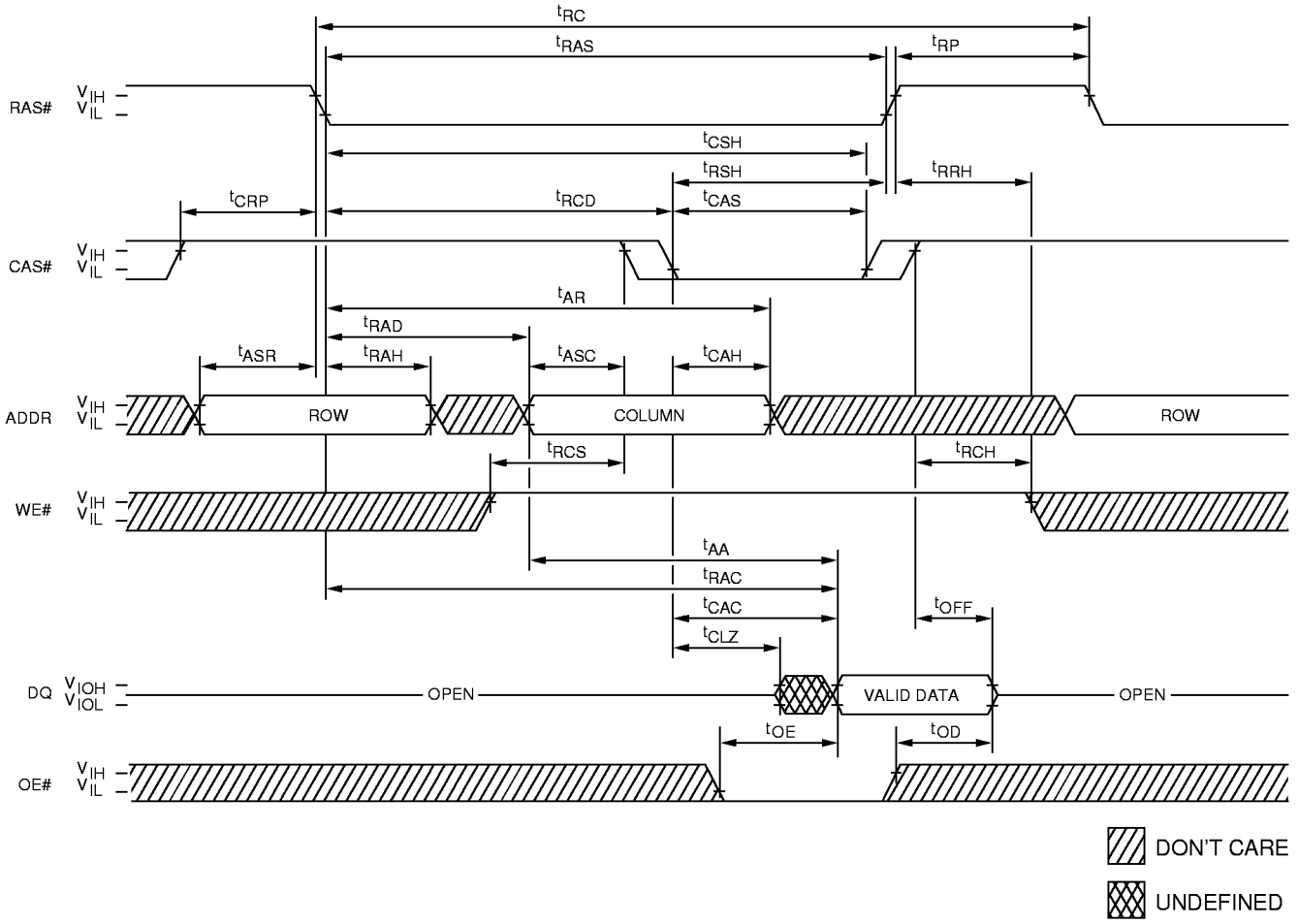
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
RAS# to CAS# delay time	^{t}RCD	20		ns	14
READ command hold time (referenced to CAS#)	^{t}RCH	0		ns	16
READ command setup time	^{t}RCS	0		ns	
Refresh period (2,048 cycles)	^{t}REF		32	ms	
Refresh period (2,048 cycles) "S" version	^{t}REF		128	ms	
RAS# precharge time	^{t}RP	40		ns	
RAS# to CAS# precharge time	^{t}RPC	0		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	110		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	
READ-WRITE cycle time	^{t}RWC	155		ns	
RAS# to WE# delay time	^{t}RWD	85		ns	18
WRITE command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
WRITE command hold time	^{t}WCH	10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	18
WRITE command pulse width	^{t}WP	10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#- ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. Column address changed once each cycle.
23. The 3ns minimum is guaranteed by design.
24. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE

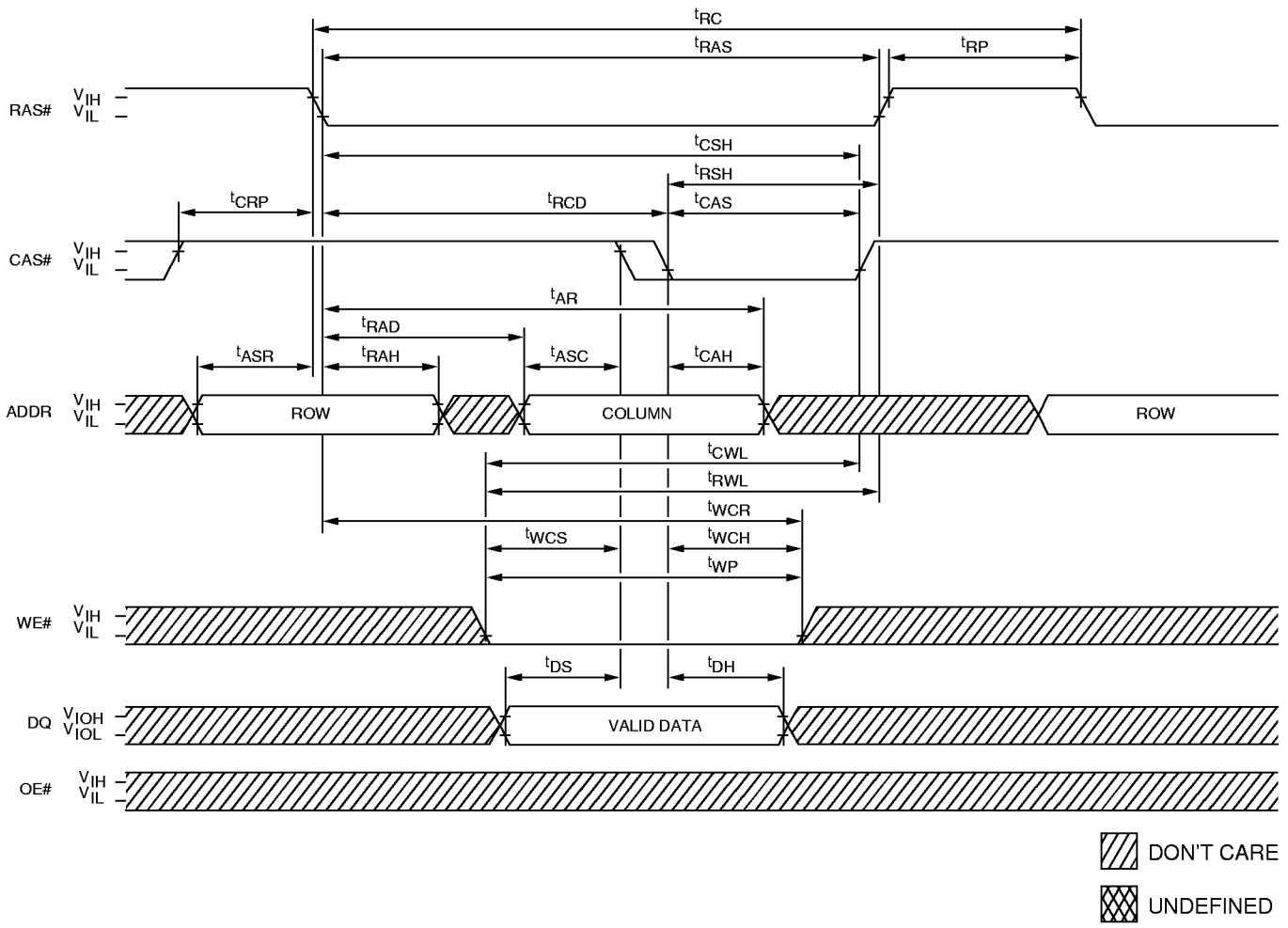


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCRP	5		ns
tCSH	60		ns
tOD	3	15	ns
tOE		15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EARLY WRITE CYCLE

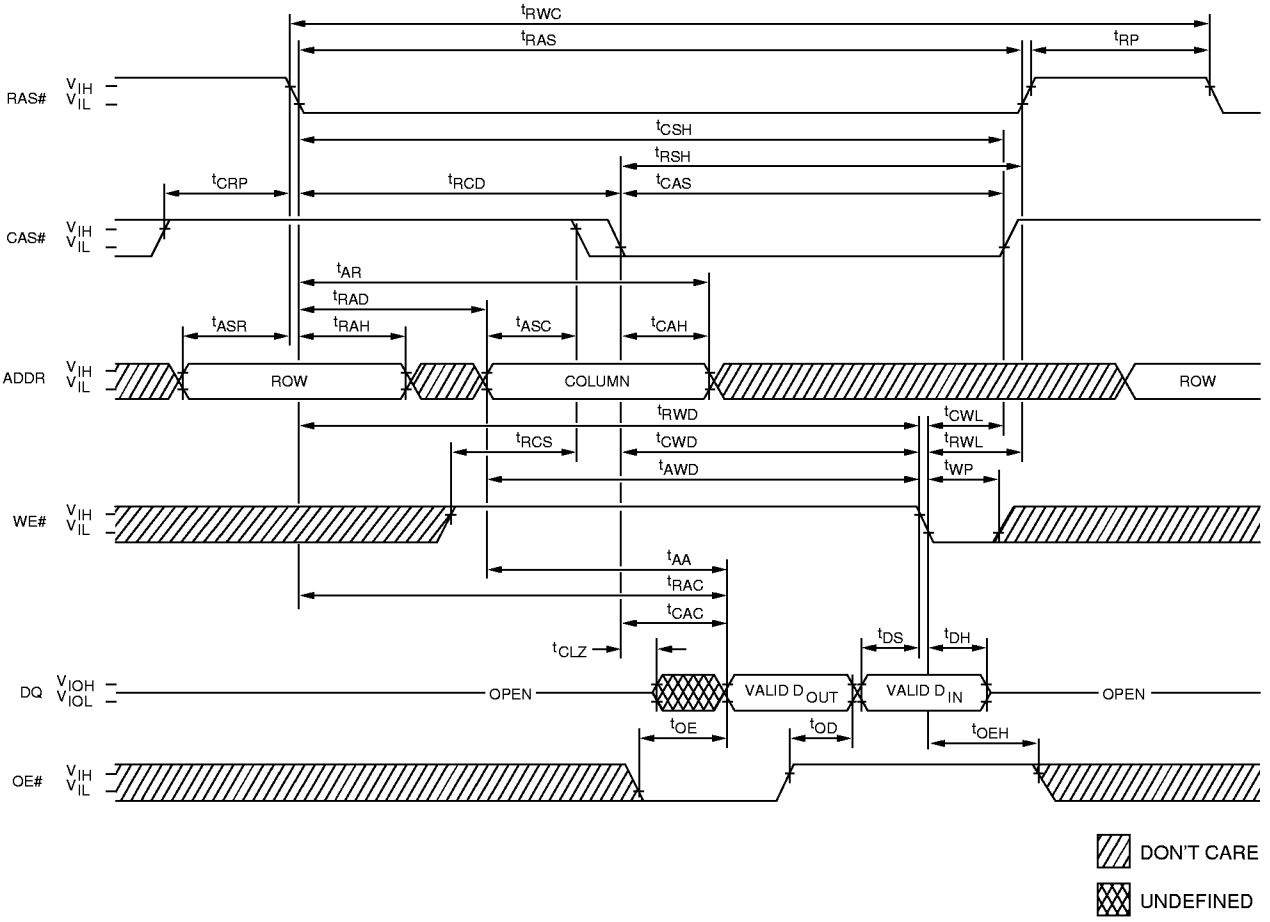


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tRAD	15		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

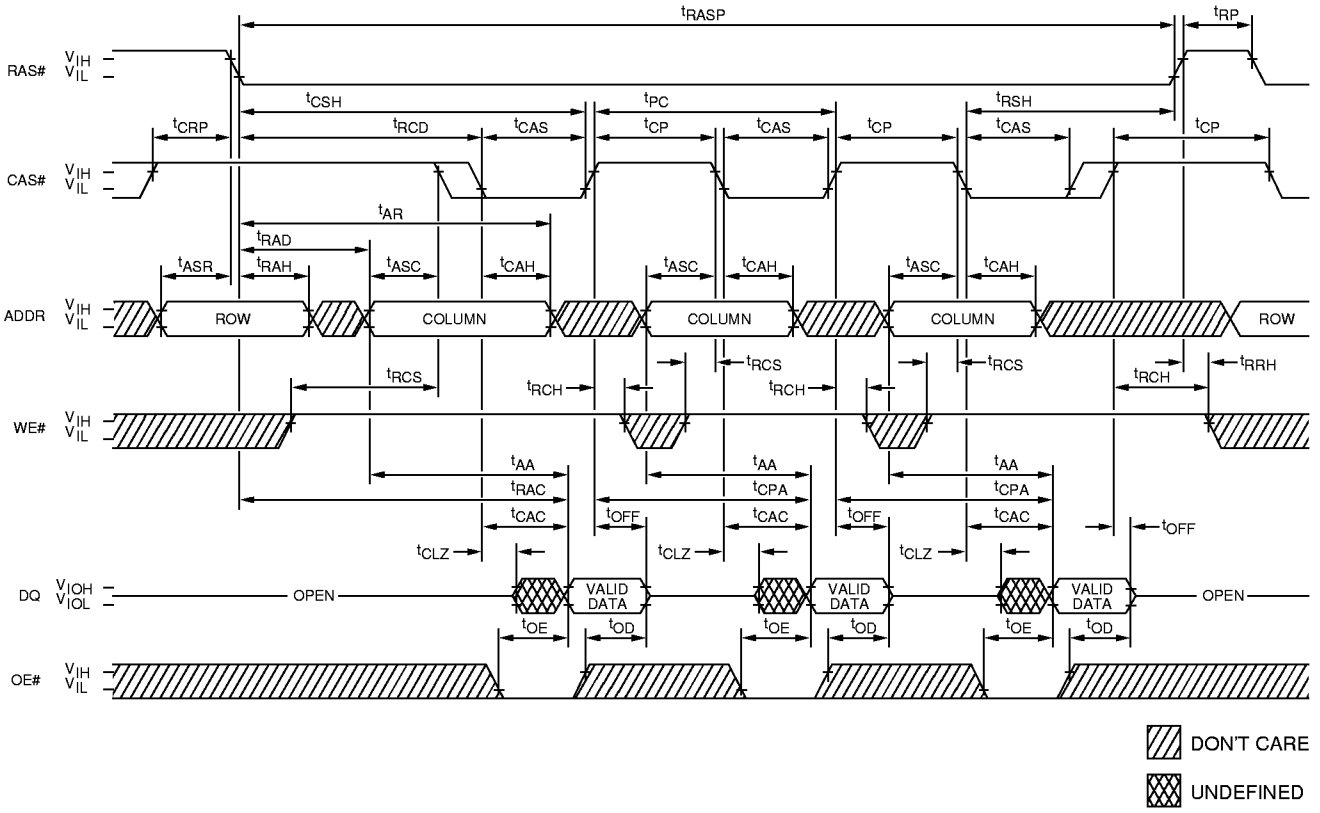


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tAWD	55		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCRP	5		ns
tCSH	60		ns
tCWD	40		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOD	3	15	ns
tOE		15	ns
tOEH	15		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWC	155		ns
tRWD	85		ns
tRWL	15		ns
tWP	10		ns

FAST-PAGE-MODE READ CYCLE

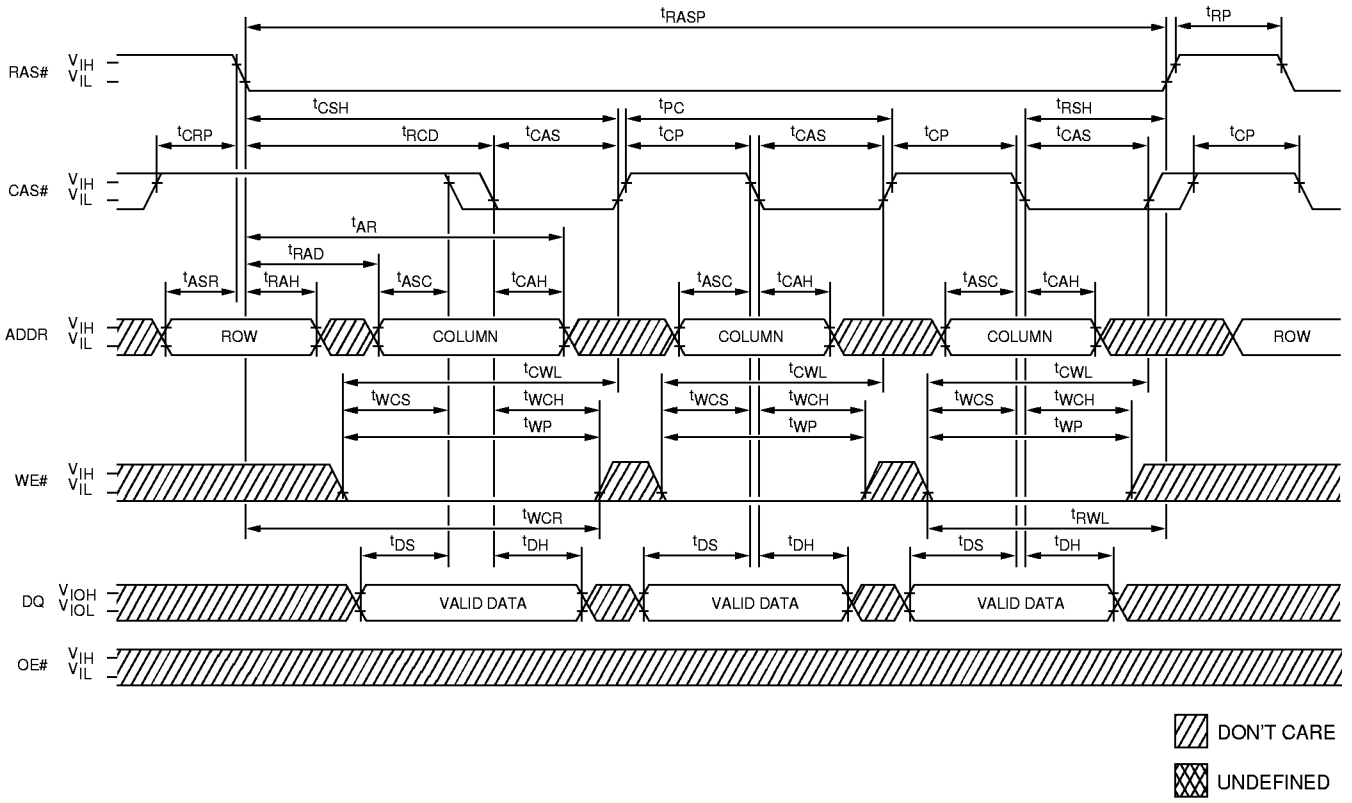


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	5		ns
tCSH	60		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE

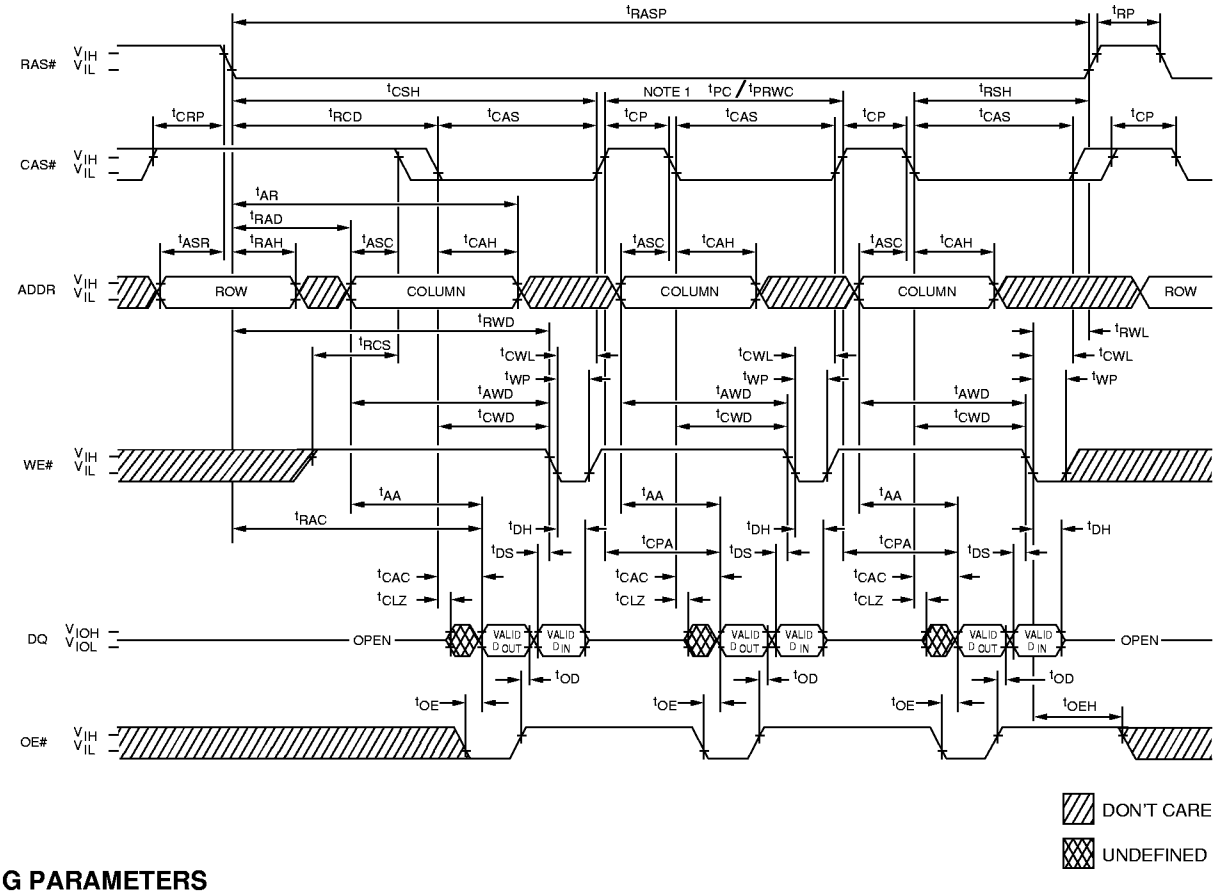


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCP	10		ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tPC	35		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



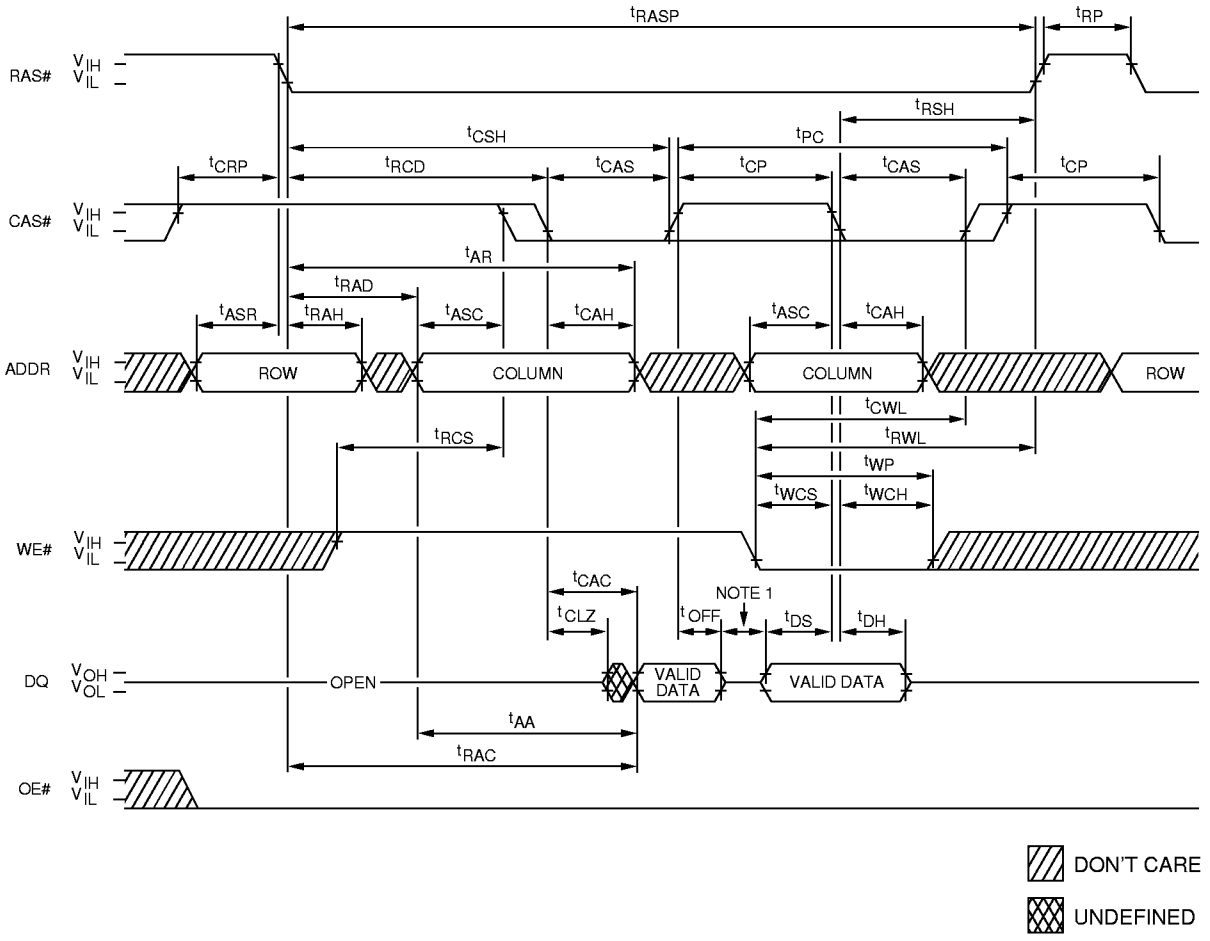
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tAWD	55		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	5		ns
tCSH	60		ns
tCWD	40		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOD	3	15	ns
tOE		15	ns
tOEH	15		ns
tPC	35		ns
tPRWC	85		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWD	85		ns
tRWL	15		ns
tWP	10		ns

NOTE: 1. tPC is for LATE WRITE only.

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



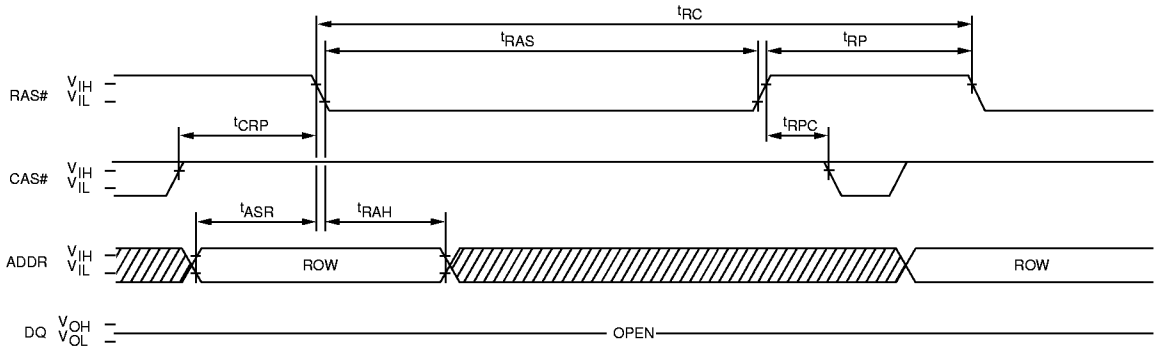
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

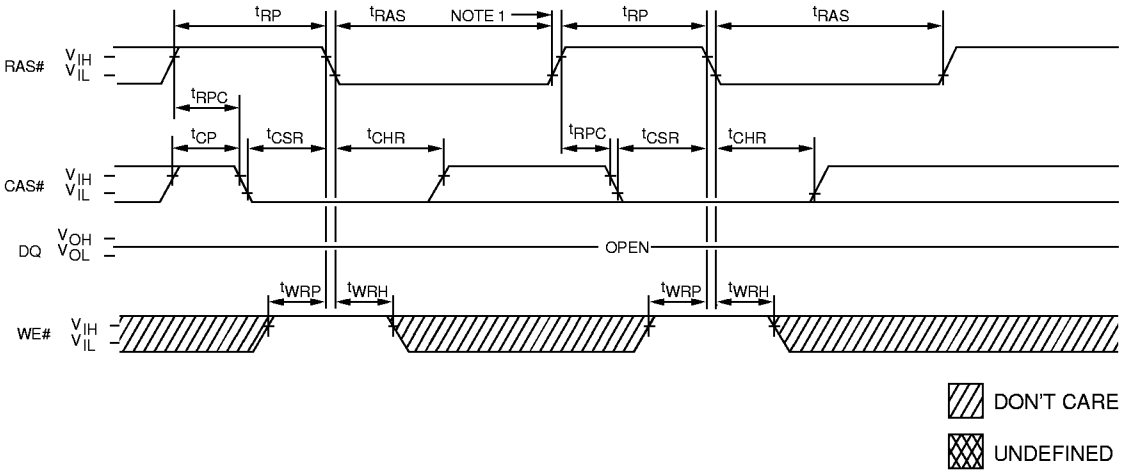
SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to High-Z.

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



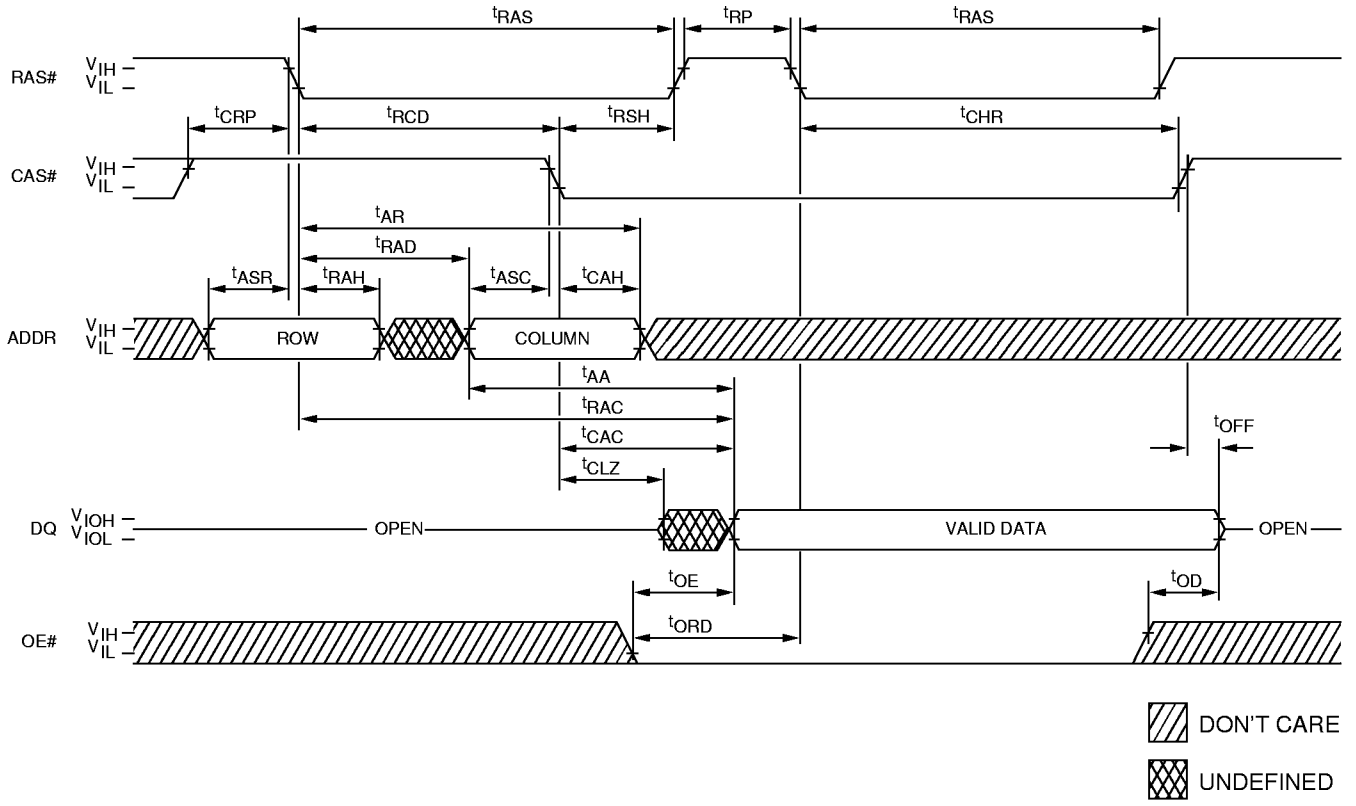
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tASR	0		ns
tCHR	10		ns
tCP	10		ns
tCRP	5		ns
tCSR	5		ns
tRAH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAS	60	10,000	ns
tRC	110		ns
tRP	40		ns
tRPC	0		ns
tWRH	10		ns
tWRP	10		ns

NOTE: 1. End of CBR REFRESH cycle.

HIDDEN REFRESH CYCLE [21]
(WE# = HIGH; OE# = LOW)

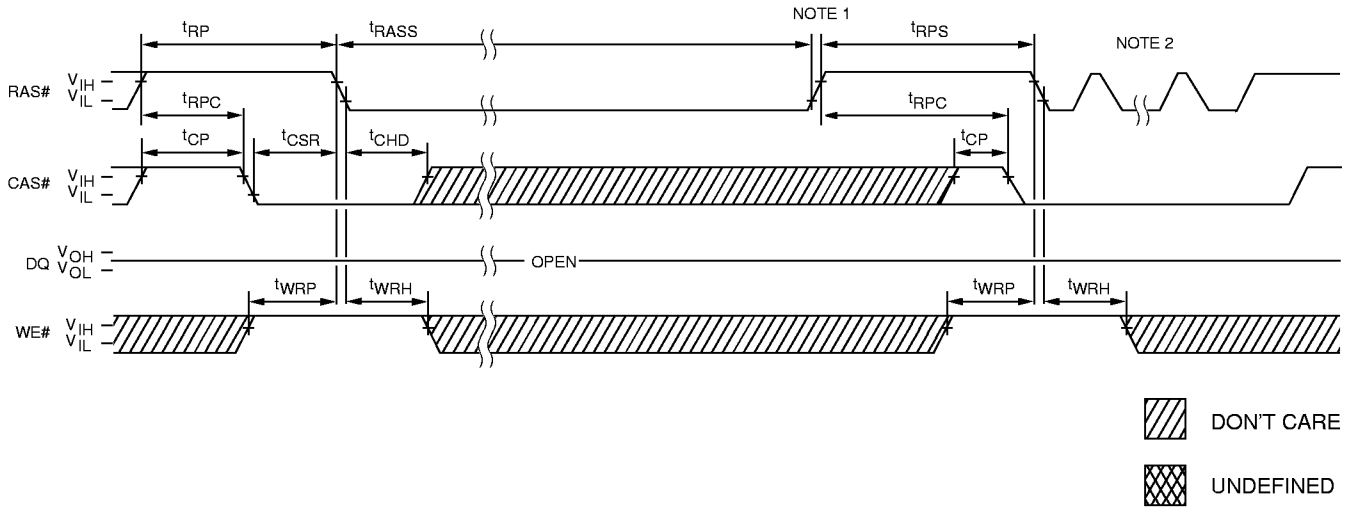


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCHR	10		ns
tCLZ	3		ns
tCRP	5		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tORD	0		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

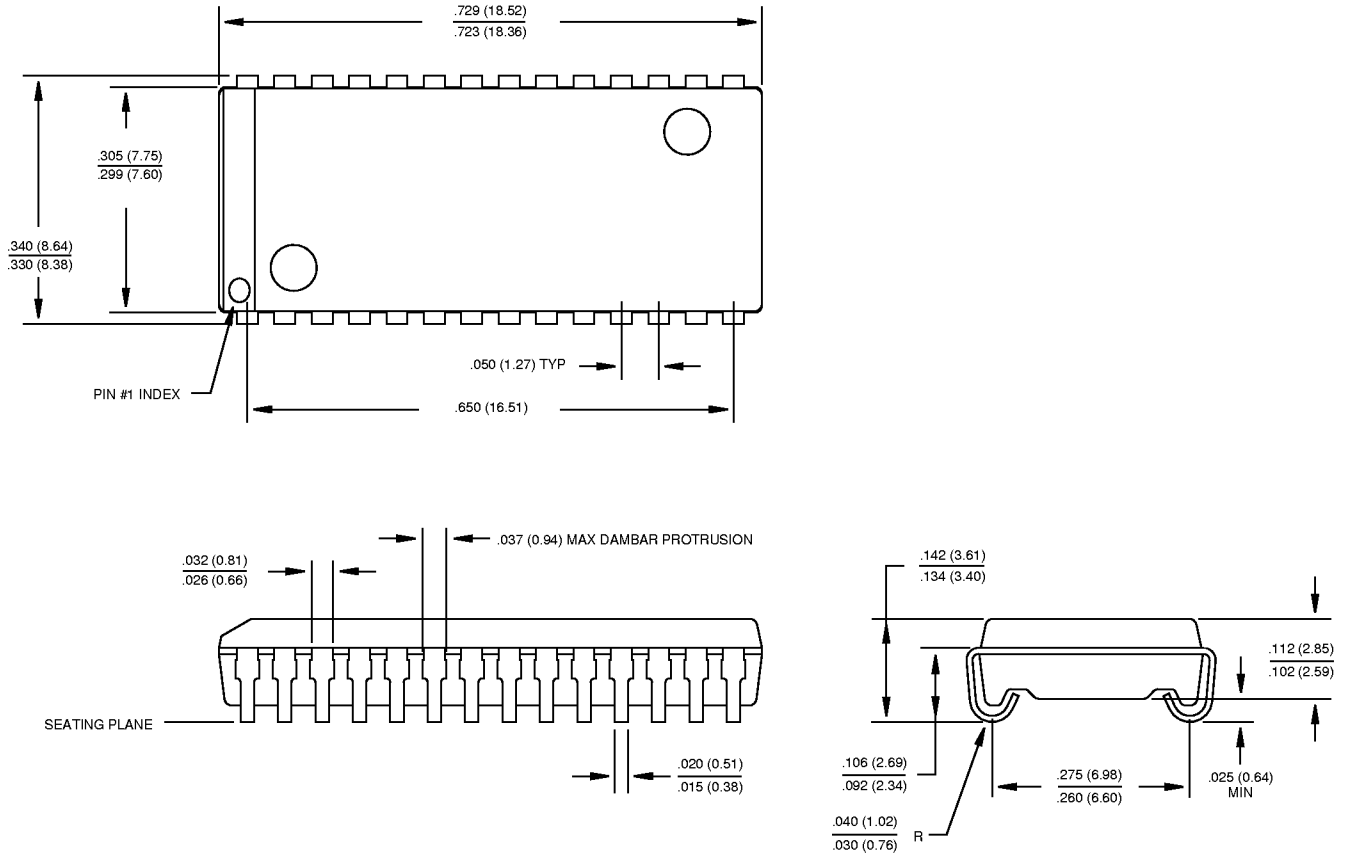
SYMBOL	-6 MIN	-6 MAX	UNITS
tCHD	15		ns
tCP	10		ns
tCSR	5		ns
tRASS	100		µs
tRP	40		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRPC	0		ns
tRPS	110		ns
tWRH	10		ns
tWRP	10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

28-PIN PLASTIC SOJ (300 mil)

DA-2

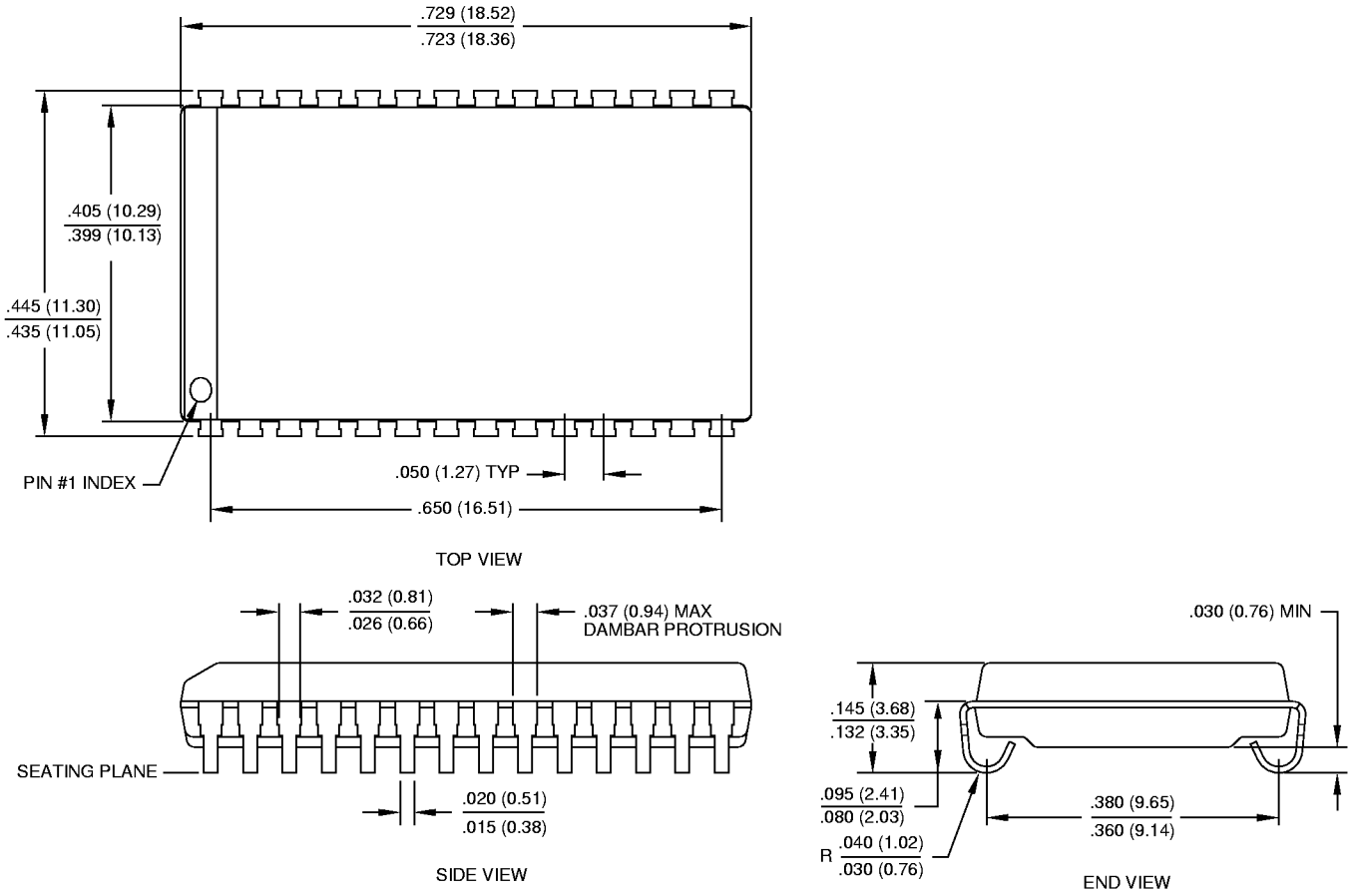


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ (400 mil)

DA-3

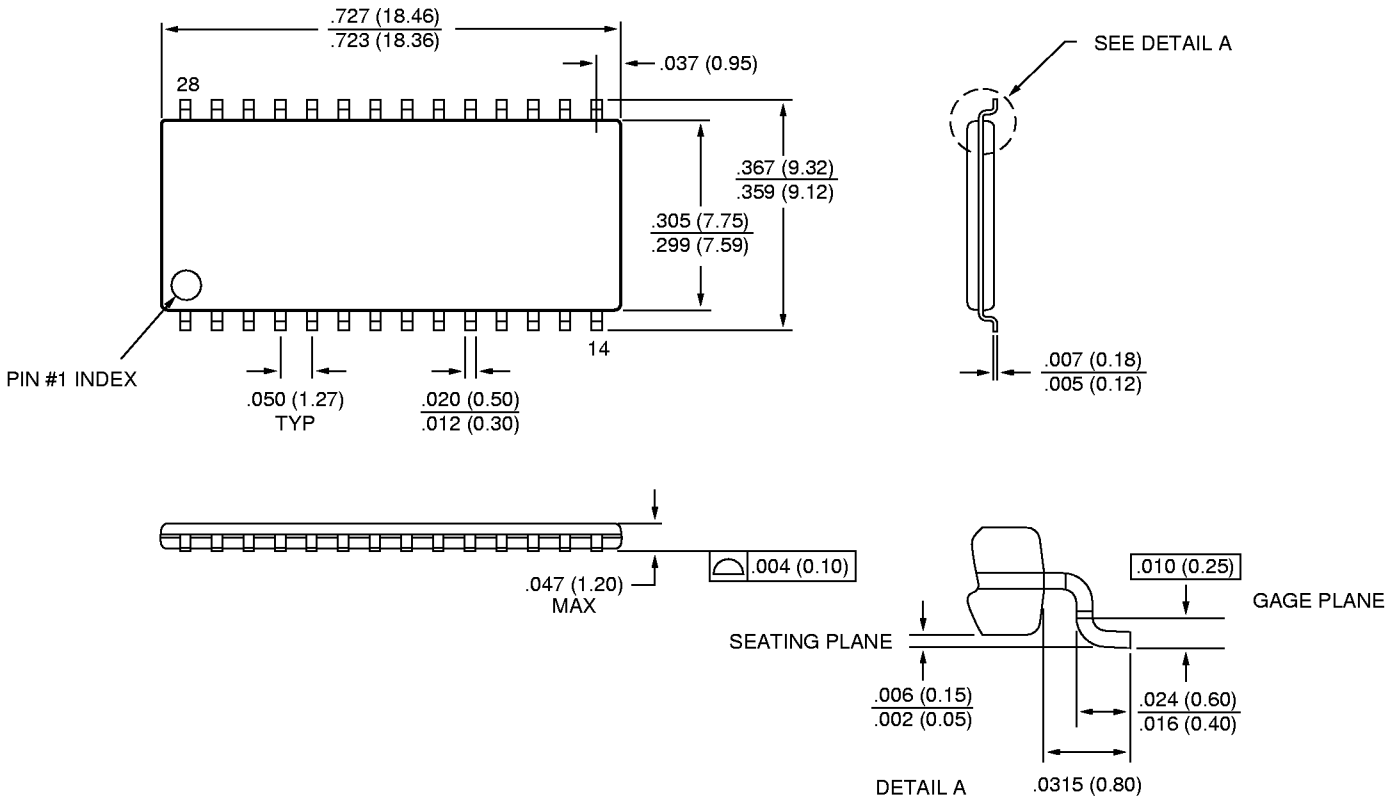


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC TSOP (300 mil)

DB-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992