NEW BURST EDO DRAM

DRAM

2 MEG x 8

3.3V, BURST EDO

FEATURES

- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- Single +3.3V ±5% power supply
- All inputs and outputs are LVTTL-compatible with 5V input/output tolerance
- Industry-standard x8 pinout and packages
- High-performance CMOS silicon-gate process
- Refresh: $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) or $\overline{\text{RAS}}$ ONLY
- 2,048-cycle refresh (11 row-, 10 column-addresses)
- Four-cycle Extended Data-Out (EDO) burst accesses

OPTIONS MARKING

- Timing
  52ns access; 15ns cycle -52
  60ns access; 16.6ns cycle -60
- Packages
  Plastic SOJ (300 mil) DJ
- Refresh
  Standard (2,048 cycles at 32ms) None
- Part Number Example: MT4LC2M8F4DJ-52

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(DA-3)

Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
$\overline{\text{WE}}$	6	23	$\overline{\text{CAS}}$
$\overline{\text{RAS}}$	7	22	$\overline{\text{OE}}$
NC	8	21	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

KEY TIMING PARAMETERS

SPEED	^{t}RAC	^{t}PC	^{t}CAC	^{t}COH	^{t}DS	^{t}DH
-52	52ns	15ns	10ns	3ns	0ns	5ns
-60	60ns	16.6ns	11ns	3ns	0ns	5ns

GENERAL DESCRIPTION

The MT4LC2M8F4 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 21 address bits, which are entered 11 bits (A0-A10) at $\overline{\text{RAS}}$ time and 10 bits (A0-A9) at $\overline{\text{CAS}}$ time.

The MT4LC2M8F4 is a burst access DRAM in which all READ and WRITE cycles occur in bursts of four. The bursts wrap around on a 4-byte boundry. This means only the two least significant bits of the $\overline{\text{CAS}}$ address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle with address A0 set to either HIGH or LOW. A0 LOW will program the device to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information (0010 000x) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{\text{RAS}}$-ONLY or CBR REFRESH cycle to exit this programming mode.

A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input during the first $\overline{\text{CAS}}$ LOW pulse of the burst. During the burst cycle the $\overline{\text{WE}}$ input must remain constant for the burst to continue. Transition of the $\overline{\text{WE}}$ input during a burst causes the burst to terminate and places the outputs in a High-Z state. After a terminated burst, the next falling edge of $\overline{\text{CAS}}$ will start a new burst access at the address present on the external address bus.

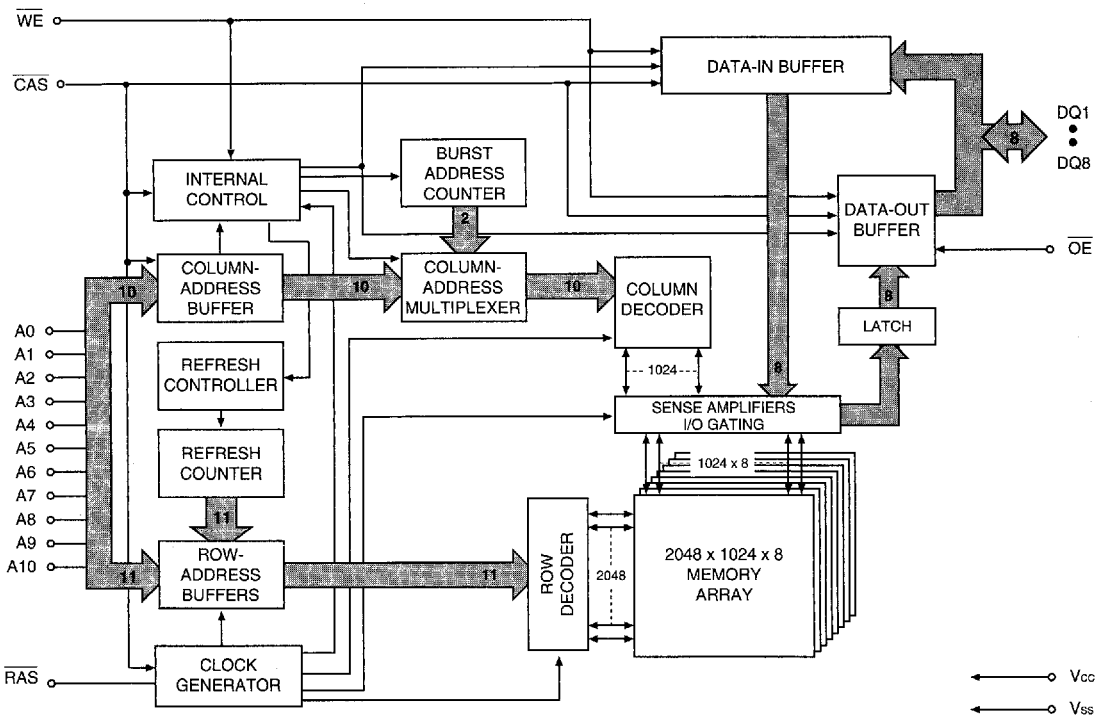
During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{CAS}}$. $\overline{\text{WE}}$ must be LOW prior to $\overline{\text{CAS}}$ going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. $\overline{\text{WE}}$ must remain LOW during the burst operation for the burst to complete. $\overline{\text{WE}}$ going HIGH after ^{t}WCH from $\overline{\text{CAS}}$ LOW and before ^{t}WCS of the next $\overline{\text{CAS}}$ LOW terminates the burst operation and places the DQ pins in the High-Z state.

GENERAL DESCRIPTION (continued)

During a READ cycle $\overline{WE}$ must be HIGH prior to $\overline{CAS}$ going LOW. $\overline{WE}$ must remain HIGH during the burst operation for the burst to complete. $\overline{WE}$ going LOW after ^{t}RCH from $\overline{CAS}$ LOW and before ^{t}RCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the DQ pins in the High-Z state.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. The chip is precharged for the next access during the $\overline{RAS}$ HIGH time.

FUNCTIONAL BLOCK DIAGRAM
Burst EDO



EDO BURST MODE TRUTH TABLE

PRESENT STATE	RESULTING STATE	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA
						Row	Column	DQ
Any	Idle	L→H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	H	X	X	X	High-Z
Row Open	$\overline{RAS}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	COL	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE Using CBR REFRESH	H→L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE Using $\overline{RAS}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR cycle determines the burst sequence. A0=LOW sets the burst sequence to linear, A0=HIGH set the burst sequence to interleave. A8 through A10 are "don't cares." A7-A0 should contain the sequence (0010 000x where x=A0) to ensure future compatability. A refresh cycle ($\overline{RAS}$ ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

	ADDRESSES USED		
OPERATION	**A10 - A2**	**A1**	**A0**
First access, register external CAS address	A10 - A2	A1	A0
Second access, (first burst address)	registered A10 - A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A10 - A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A10 - A2	registered $\overline{A1}$	registered $\overline{A0}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss ..... -1.0V to +4.6V
Voltage on Inputs, NC or I/O pins
Relative to Vss ..... -1.0V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 11) (Vcc = +3.3V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.13	3.47	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	5.5	V	2
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -52	MAX -60	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	500	500	µA	
OPERATING CURRENT: CLOSED ROW BURST READ/WRITE Average power supply current; (^tPC = ^tPC [MIN]; 50% duty cycle on $\overline{RAS}$; open row, four cycle burst, close row)	ICC3	110	100	mA	4, 5
OPERATING CURRENT: OPEN ROW BURST READ/WRITE Average power supply current (alternating four cycle burst followed by four cycles inactivity; ^tPC = ^tPC [MIN])	ICC4	70	65	mA	4, 5
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current (address cycling; $\overline{RAS}$ cycling; $\overline{CAS}$ = VIH; ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	ICC5	140	130	mA	4, 5
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling: ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	ICC6	140	130	mA	5, 6

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: Addresses, $\overline{WE}$, $\overline{OE}$	C_{I1}		5	pF	3
Input Capacitance: $\overline{RAS}$	C_{I2}		6	pF	3
Input Capacitance: $\overline{CAS}$	C_{I3}		4	pF	3
Input/Output Capacitance: DQ	C_{IO}		7	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (V_{CC} = +3.3V ±5%)

AC CHARACTERISTICS		-52		-60			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{CAS}$	^tAA		25		28.2	ns	12
Column-address setup time	^tASC	1.5		1.5		ns	
Row-address setup time	^tASR	1.5		1.5		ns	
Burst terminate hold time	^tBTH	3		3		ns	
Output disable from burst terminate	^tBTHZ	7	13	7	13	ns	13, 16
Access time from $\overline{CAS}$	^tCAC		10		11	ns	
Column-address hold time	^tCAH	8.5		8.5		ns	
$\overline{CAS}$ pulse width	^tCAS	5	10,000	5	10,000	ns	
$\overline{CAS}$ hold time (CBR or WCBR)	^tCHR	15		15		ns	6
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	13
Data hold time from $\overline{CAS}$ LOW	^tCOH	3		3		ns	
$\overline{CAS}$ precharge time	^tCP	5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	^tCPN	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	^tCRW	15		16.6		ns	
$\overline{CAS}$ setup time (CBR or WCBR)	^tCSR	10		10		ns	6
Data-in hold time	^tDH	5		5		ns	
Data-in setup time	^tDS	0		0		ns	17
Ouput disable	^tOD	4	10	4	10	ns	13
Ouput enable access time	^tOEA		10		12	ns	
Ouput enable hold (only near $\overline{CAS}$)	^tOEH	5		5		ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	3		3		ns	13
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		ns	
Ouput enable setup (only near $\overline{CAS}$)	^tOES	3		3		ns	
Output buffer turn-off delay	^tOFF	4	13	4	13	ns	13
Burst EDO cycle time	^tPC	15		16.6		ns	
Access time from $\overline{RAS}$	^tRAC		52		60	ns	
Row-address hold time	^tRAH	8.5		8.5		ns	
$\overline{RAS}$ pulse width	^tRAS	52	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	90		110		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD1$	20		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD2$	40		45		ns	
Read command hold time	^tRCH	5		5		ns	
Read command setup time	^tRCS	3		4		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS		-52		-60			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	tRP	30		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	
$\overline{RAS}$ hold time	tRSH	0		0		ns	
Transition time (rise or fall)	tT	1.5	50	1.5	50	ns	
Burst terminate pulse width	tTP	6		6		ns	14
Write command hold time	tWCH	5		5		ns	
$\overline{WE}$ command setup time	tWCS	3		4		ns	
Ouput disable from $\overline{WE}$ LOW	tWHZ	4	10	4	10	ns	13, 16
$\overline{WE}$ hold time (CBR or WCBR)	tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR or WCBR)	tWRP	10		10		ns	

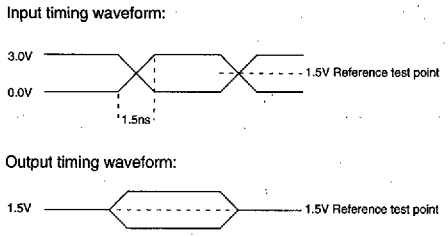


Figure 1
TIMING SPECIFICATIONS

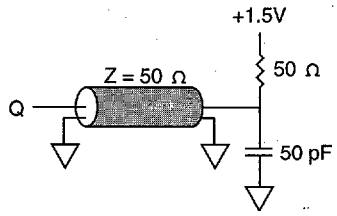


Figure 3
AC TIMING OUTPUT LOAD EQUIVALENT

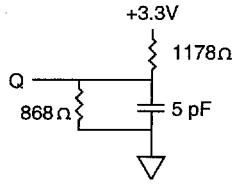


Figure 2
HIGH-Z OUTPUT LOAD

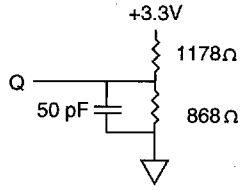
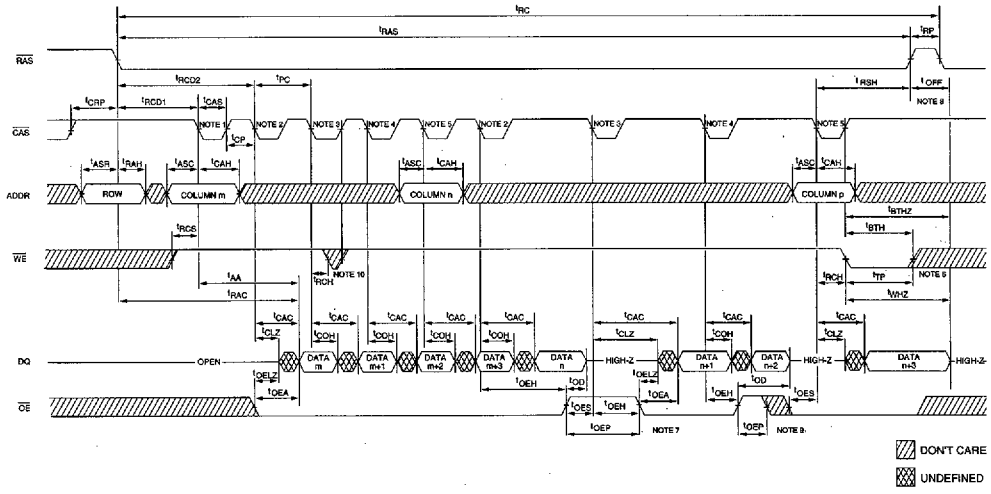


Figure 4
OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss.
2. Input Power-up: $V_{IH} \leq +5.5V$ and $V_{CC} \leq +3.13V$ for $t \leq 200ms$
3. This parameter is sampled. $V_{CC} = 3.13V$ f = 1 MHz.
4. Address transitions once per burst access.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum ^tPC and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle.
8. AC characteristics assume $^tT = 1.5ns$.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. ^tAA is a calculated specification which is the sum of ^tPC and ^tCAC.
13. Output loading is specified with $C_L = 5pF$ as in Figure 2. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with $C_L = 50pF$ as in Figure 3. Figure 4 is shown for reference. Transition is measured at the 1.5V reference level.
16. The DQs will continue to drive data out until ^tBTHZ (MIN) and ^tWHZ (MIN) have both been satisfied and will reach the High-Z state once ^tBTHZ (MAX) and ^tWHZ (MAX) have both been satisfied.
17. Valid data-in is referenced from when a valid logic level (V_{IH}, V_{IL}) has been achieved.

BURST EDO READ CYCLE



NOTE:

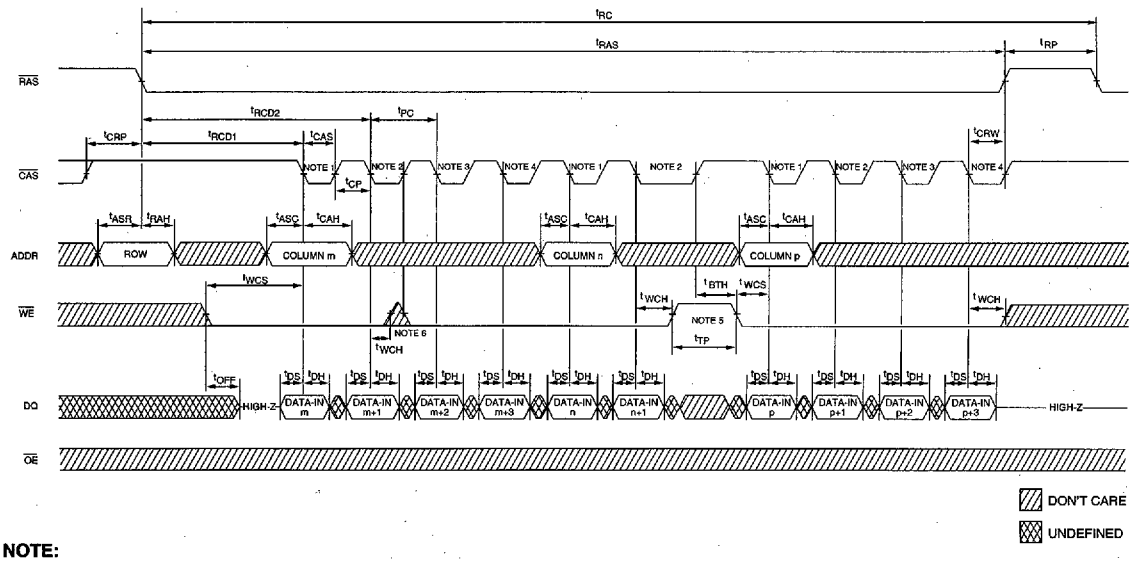
1. Latch column address; start READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start READ cycle.
6. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
7. Once $\overline{OE}$ transitions LOW after $\overline{CAS}$ transitions LOW, Note 9 applies if $\overline{OE}$ transitions back HIGH.
8. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQs in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
9. When $\overline{OE}$ transitions HIGH, the DQ pins are placed in the High-Z state and will remain in the High-Z state until another $\overline{CAS}$ LOW transition occurs, regardless of the state of $\overline{OE}$.
10. $\overline{WE}$ transitioning LOW and returning HIGH prior to $\overline{CAS}$ going HIGH will not terminate the burst.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		28.2	ns
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
$^{t}BTHZ$	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}CLZ	3		3		ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}OD	4	10	4	10	ns
^{t}OEA		10		12	ns
^{t}OEH	5		5		ns
$^{t}OELZ$	3		3		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}OEP	10		10		ns
^{t}OES	3		3		ns
^{t}OFF	4	13	4	13	ns
^{t}PC	15		16.6		ns
^{t}RAC		52		60	ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
$^{t}RCD1$	20		20		ns
$^{t}RCD2$	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}RSH	0		0		ns
^{t}TP	6		6		ns
^{t}WHZ	4	10	4	10	ns

BURST EDO WRITE CYCLE



NOTE:

1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied.
6. $\overline{WE}$ transitioning HIGH and returning LOW prior to $\overline{CAS}$ going HIGH will not terminate the burst.

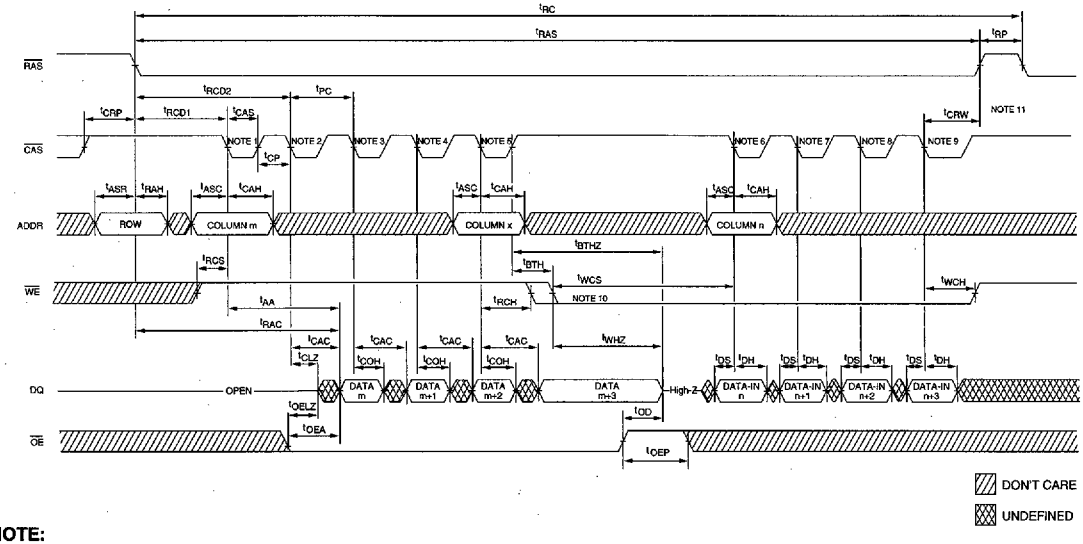
TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASC	1.5		1.5		ns
tASR	1.5		1.5		ns
tBTH	3		3		ns
tCAH	8.5		8.5		ns
tCAS	5	10,000	5	10,000	ns
tCP	5		5		ns
tCRP	10		10		ns
tCRW	15		16.6		ns
tDH	5		5		ns
tDS	0		0		ns
tOFF	4	13	4	13	ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tPC	15		16.6		ns
tRAH	8.5		8.5		ns
tRAS	52	125,000	60	125,000	ns
tRC	90		110		ns
tRCD1	20		20		ns
tRCD2	40		45		ns
tRP	30		40		ns
tTP	6		6		ns
tWCH	5		5		ns
tWCS	3		4		ns

NEW BURST EDO DRAM

BURST EDO READ/WRITE CYCLE



NOTE:

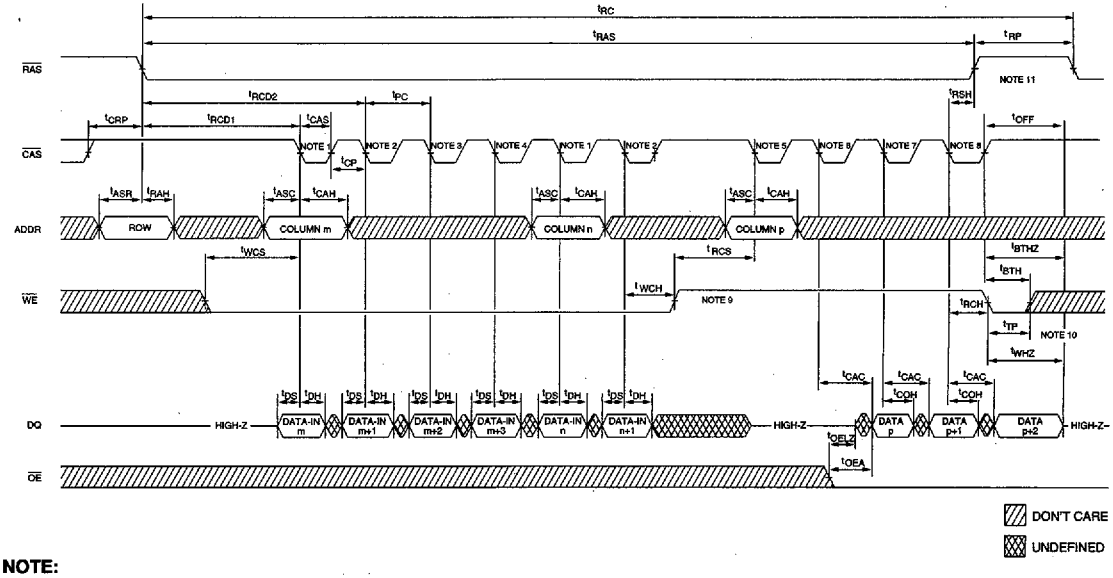
1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. ^{t}TP is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		28.2	ns
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
$^{t}BTHZ$	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}CLZ	3		3		ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}CRW	15		16.6		ns
^{t}DH	5		5		ns
^{t}DS	0		0		ns
^{t}OD	4	10	4	10	ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}OEA		10		12	ns
$^{t}OELZ$	3		3		ns
^{t}OEP	10		10		ns
^{t}PC	15		16.6		ns
^{t}RAC		52		60	ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
$^{t}RCD1$	20		20		ns
$^{t}RCD2$	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}WCH	5		5		ns
^{t}WCS	3		4		ns
^{t}WHZ	4	10	4	10	ns

BURST EDO WRITE/READ CYCLE



NOTE:

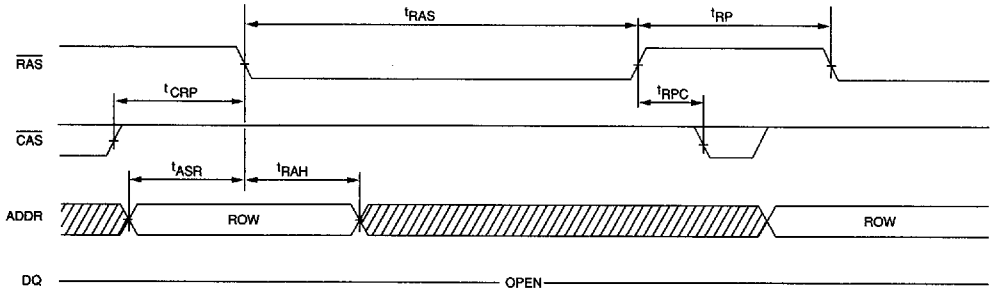
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter. The ^{t}BTH time is not required as it is satisfied by ^{t}RCS; ^{t}TP is met by the WRITE burst being terminated by a READ burst.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.

TIMING PARAMETERS

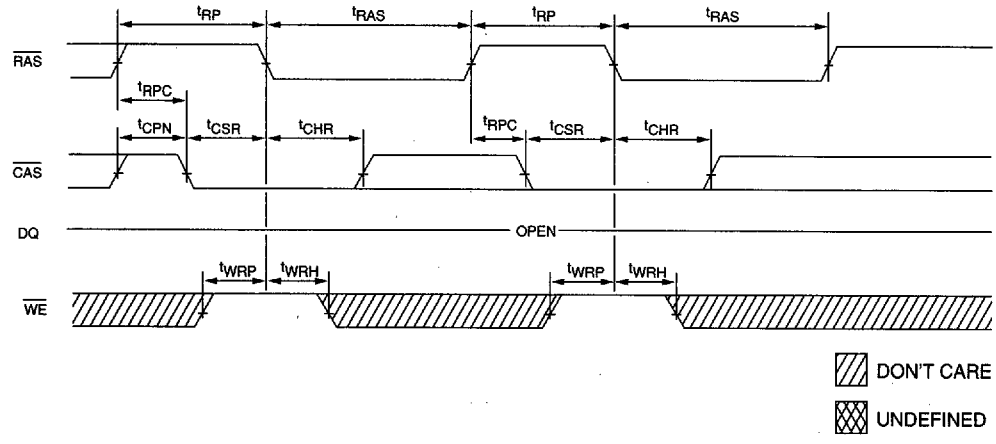
	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
^{t}BTHZ	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}DH	5		5		ns
^{t}DS	0		0		ns
^{t}OEA		10		12	ns
^{t}OELZ	3		3		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}PC	15		16.6		ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
^{t}RCD1	20		20		ns
^{t}RCD2	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}RSH	0		0		ns
^{t}TP	6		6		ns
^{t}WCH	5		5		ns
^{t}WCS	3		4		ns
^{t}WHZ	4	10	4	10	ns

RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE



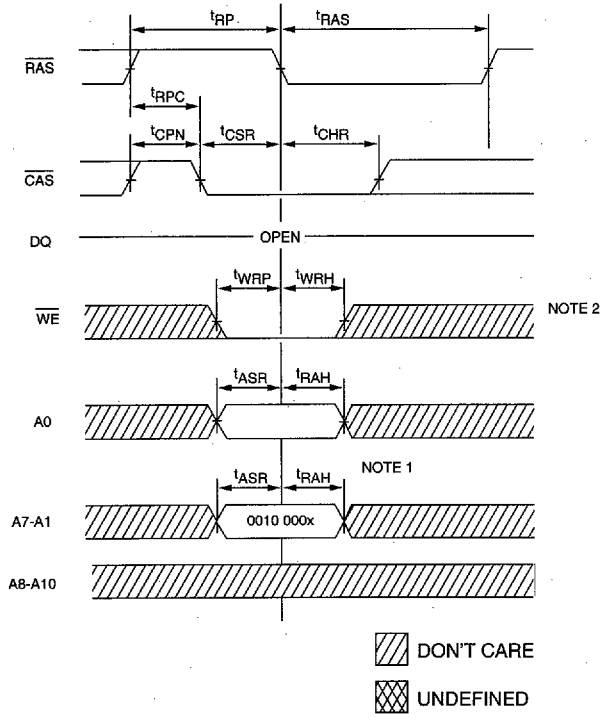
NOTE: 1. CBR REFRESH is recommended for all new designs to ensure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASR	1.5		1.5		ns
tCHR	15		15		ns
tCPN	10		10		ns
tCRP	10		10		ns
tCSR	10		10		ns
tRAH	8.5		8.5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAS	52	125,000	60	125,000	ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	10		10		ns
tWRP	10		10		ns

WCBR PROGRAM CYCLE



NOTE:
1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A1 should contain the state of (0010 000x where x=A0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A $\overline{RAS}$-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASR	1.5		1.5		ns
tCHR	15		15		ns
tCPN	10		10		ns
tCSR	10		10		ns
tRAH	8.5		8.5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAS	52	125,000	60	125,000	ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	10		10		ns
tWRP	10		10		ns