95% Efficient 1.2MHz Synchronous Step-up Converter With 6A Switches

DESCRIPTION

The MT5030 devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer battery. The converter generates a stable output voltage that is either adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 2.1A at 5.3V at a supply voltage down to 2.9V. The maximum peak current in the step-up switch is limited to a value of 6A. The MT5030 operates at 1.2MHz switching frequency and enters pulse-skip-mode (PSM) operation at light load currents to maintain high efficiency over the entire load current range. The PSM mode extends the battery life by reducing the quiescent current to 50μA (typ) during light load operation. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery.

FEATURES

- **95% Efficient Synchronus Step-up Converter with 2A Output Current From 2.9V Input**
- **Wide V_{BAT} Range From 2.5V to 5.5V**
- **Fixed and Adjustable Output Voltage**
- **Built-in Output Over-voltage Protection**
- **Light-Load Pulse Skip Mode with 50μA Quiescent Current**
- **Low Battery Comparator**
- **Low EMI-Converter (Integrated Anti-ringing Switch)**
- **Load Disconnect During Shutdown**
- **Thermal Shutdown and Overload Protection**
- **Available in a Small 4 mm x 4 mm QFN-16**

APPLICATIONS

- **Tablet PC and Notebook**
- **Power Bank**
- **USB Charging Port (5V)**
- **DC/DC Micro Modules**

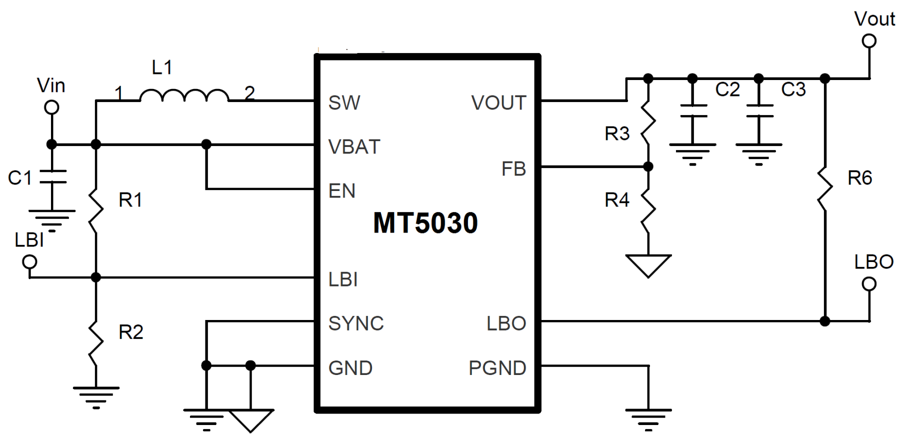
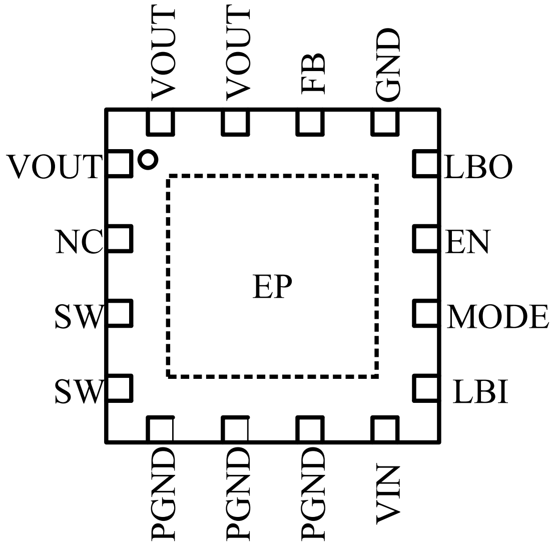


Figure 1. MT5030 Typical Operating Circuit

Ordering Information

Part No.	Marking	Temp. Range	Package	Remark
MT5030NQBR	MT5030 xxxxx	-40℃ ~+85℃	QFN16L 4x4	

Pin Configuration



MT5030 (TOP View)

Pin Description

NAME	PIN NO.	DESCRIPTION
EN	11	Enable input. (1: V_{BAT} enabled, 0: GND disabled)
FB	14	Voltage feedback of adjustable versions. Connect FB to GND and set fixed 5.125V output voltage.
GND	13	Analog Ground pin. Connect GND to PGND under EP.
LBI	9	0.5V Threshold Low battery comparator input (comparator enabled with EN)
LBO	12	Low battery comparator output (open drain)
NC	2	Not connected
MODE	10	Enable/disable pulse skip mode (1: V_{BAT} disabled, 0: GND enabled)
SW	3, 4	Step-up and rectifying switch input
PGND	5, 6, 7	Power Ground pin.
V_{BAT}	8	Input Supply voltage
VOUT	1, 15, 16	Step-up convert output
EP		Exposed pad must be soldered to achieve appropriate power dissipation. Connect EP to GND.

Absolute Maximum Rating (1)

Supply Voltage (V_{BAT}) ……………… -0.3V to +6V

Output Voltage (V_{OUT}) ……………… -0.3V to +6V

Input Voltage (LBI, LBO, SW) ……….. -0.3V to +6V

Input Voltage (MODE, EN, FB) …….. -0.3V to +6V

Peak output current ………………… Internally limited

Lead Temperature …………………………… 260℃

Junction temperature range, T_J …… -40℃ ~+135℃

Storage temperature range, T_{stg} …… -55℃~+155℃

Thermal information

Maximum Power Dissipation(T_A=+25℃) ……2.2W

Thermal resistance(θ_{JA})…………………………..45℃/W

Recommend Operating Conditions (2)

Input Voltage (V_{BAT}) ………………… +2.5V to +5.5V

Output Voltage (V_{OUT}) ……………… +2.5V to +5.5V

Operating Temperature Range …… -40℃ to +85℃

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

T_A = +25℃, 2.5V ≤ V_{BAT} ≤ 5.5V, unless otherwise noted. Typical values are at V_{BAT}= V_{EN} =3.6V and V_{OUT}=5V.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage range V_{BAT}			2.5		5.5	V
Input Under voltage lockout threshold	V_{BAT} voltage decreasing			2.2		V
Output voltage adjustable range V_{OUT}			2.5		5.5	V
Fixed Output Voltage	FB=GND	T_A = +25℃	4.90	5.00	5.10	V
		T_A = –40℃ to +85℃	4.85		5.15	
Feedback voltage V_{FB}	T_A = +25℃		490	500	510	mV
Oscillator frequency f_{OSC}			1.0	1.2	1.4	MHz
NCH Switch Current Limit	V_{OUT}= 5V			5.5		A
NCH Switch on resistance	V_{OUT}= 5V			60		mΩ
PCH Switch on resistance	V_{OUT}= 5V			60		mΩ
Shutdown Current	V_{EN} = 0V, V_{BAT} = 3.6V			0.1	1	μA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Current	V_{BAT}	V_{FB} =0.55V		50		µA
	V_{OUT}	V_{FB} =0.55V V_{OUT} = 5 V		5		
Low Battery LBI voltage threshold		V_{LBI} voltage decreasing	485	500	515	mV
LBI input hysteresis				10		mV
LBI input Bias Current		LBI = V_{BAT} or GND	-0.1		0.1	µA
LBO output low voltage		V_{OUT}=5V and V_{LBI}=0V, sink 100µA		0.04	0.4	V
LBO output leakage current		V_{LBI}=0.6V and V_{LBO} = 5V			0.1	µA
EN, MODE logic low voltage					0.4	V
EN, MODE logic high voltage			1.4			V
EN, MODE leakage current		Clamped on GND or V_{BAT}	-1		1	µA
Thermal Shutdown				150		℃
Thermal Shutdown Hysteresis				20		℃

Functional Block Diagram

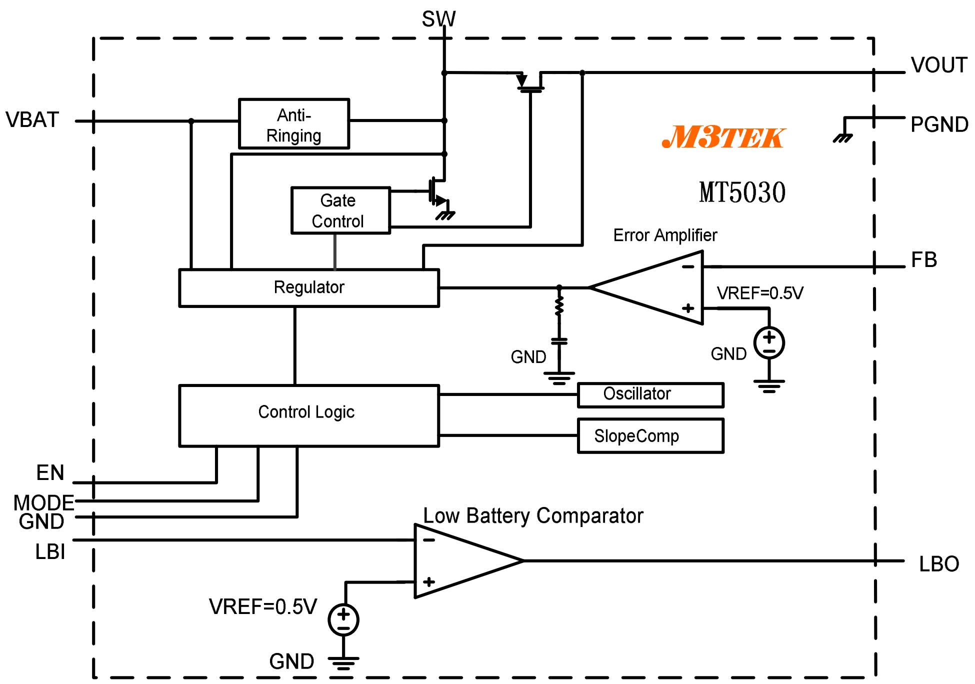


Figure 2. MT5030 Functional Block Diagram

Detailed Description

The MT5030 is based on a fixed frequency current mode pulse width modulation topology. The peak current of the NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 6A. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

The MODE pin can be used to select different operation modes. Set MODE pin low to enable pulse skip mode and improve efficiency at light load. In pulse skip mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and returns pulse skip mode once the output voltage exceeds the set threshold voltage. This pulse skip mode can be disabled by setting the MODE to V_{BAT}.

The low-battery detector circuit LBI/LBO is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is only active when the device is enabled (EN=Hi). When the device is disabled, the LBO pin is high-impedance. The LBI trip threshold is 500 mVI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV. The low battery voltage can be programmed with a resistive divider connected to the LBI pin.

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated anti-ringing switch clamps this voltage to V_{BAT} and therefore dampens ringing.

Application Information

Because of the high integration of MT5030, the application circuit is simple. Only input capacitor C1, output capacitor C2, C3, inductor L, output feedback resistors R3, R4, LBI Battery voltage divider R1,R2, LBO pull-up resistor R6 need to be selected for the targeted applications specifications.

Setting the Output Voltage

The MT5030 output voltage can be adjusted with an external resistor divider (See Figure 1. MT5030 Typical Operating Circuit). The typical value of the voltage on the FB pin is 500mV. The maximum allowed value for the output voltage is 5.5 V. Choose the bottom resistor R4 in the 100kΩ~500kΩ range to set the divider current at 1µA or higher. The value of resistor R3, depending on the needed output voltage V_{OUT}, can be calculated using Equation 1:

$$R3 = R4 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = 200k\Omega \times \left(\frac{V_{OUT}}{500mV} - 1 \right)$$ (Equation 1)

Setting the LBI/LBO Threshold Voltage

The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage V_{BAT}, can be calculated using Equation 2:

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI}} - 1 \right) = 500k\Omega \times \left(\frac{V_{BAT}}{500mV} - 1 \right)$$ (Equation 2)

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The LBO output requires a pull-up resistor with a recommended value of 1MegΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the MT5030 output voltage. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

The inductor DC current rating should be greater (by some margin) than the maximum input average current. The highest peak current through the inductor and the switch depends on the output load, converter efficiency η, the input voltage (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 3:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times \eta}$$ (Equation 3)

For example, for an output current of 2A at 5V with 85% efficiency, at least 4.7A of average current flows through the inductor at a minimum input voltage of 2.5V.

The MT5030 step-up converters have been optimized to operate with an effective inductance in the range of 1µH to 3.3µH and with output capacitors in the range of 20µF to 200µF. The internal compensation is optimized for an output filter of L = 1.2µH and C_{OUT} = 100µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions.

Input Capacitor

Place at least a 10 µF input ceramic capacitor close to the IC is to improve transient behavior of the regulator and EMI behavior of the total power supply circuit.

Output Capacitor

For the output capacitor, it is recommended to use X7R ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. A recommended output capacitance value is around 20~200µF. Note that high capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. A 10 V rated 0805 capacitor with 10μF can have an effective capacitance of less 5μF at an output voltage of 5 V.

Layout consideration

Use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

Thermal information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

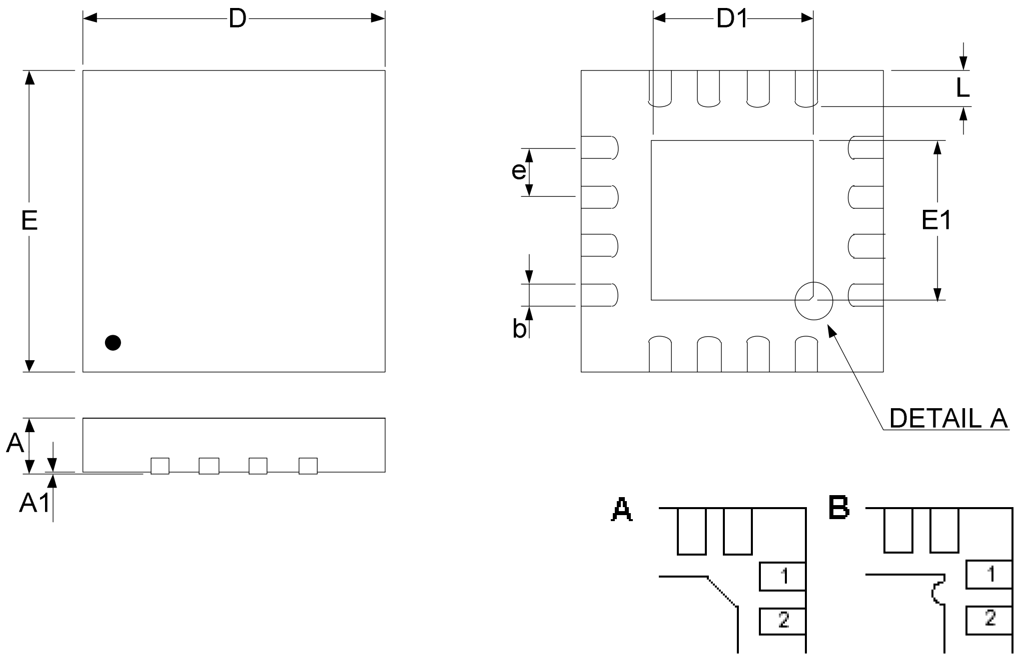
Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design
- Improve the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the MT5030 devices is 125℃.The thermal resistance of the 16-pin QFN package is θ_{JA} = 45℃/W, if the Exposed PAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of +50℃. Therefore, the maximum power dissipation for the 16-pin QFN package it is about 1.67W. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125^{\circ}\text{C-}50^{\circ}\text{C}}{45^{\circ}\text{C/W}} = 1.67W$$

MT5030 QFN 16L 4x4 mm PACKAGE OUTLINE DIMENSIONS



DETAIL A

Thermal Pad Option

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
E	3.90	4.10	0.154	0.161
D	3.90	4.10	0.154	0.161
D1	2.20		0.087	
E1	2.20		0.087	
e	0.65		0.026	
L	0.30	0.60	0.012	0.024

Datasheet Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED