



MT58LC64K18A6 64K x 18 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY, FULLY REGISTERED I/O AND
LINEAR BURST COUNTER

FEATURES

- Fast access times: 7, 10, 12 and 15ns
- Fast \overline{OE} : 5, 6, 7 and 8ns
- Single +3.3V $\pm 5\%$ power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (linear burst sequence)
- High density, high-speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS

- Timing

7ns access/15ns cycle	- 7
10ns access/20ns cycle	-10
12ns access/25ns cycle	-12
15ns access/30ns cycle	-15
- Packages

52-pin PLCC	EJ
100-pin TQFP	LG
- Part Number Example: MT58LC64K18A6EJ-10

MARKING

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

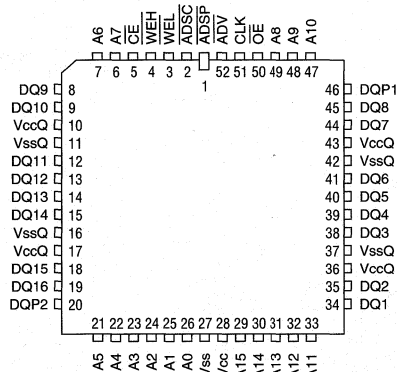
GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

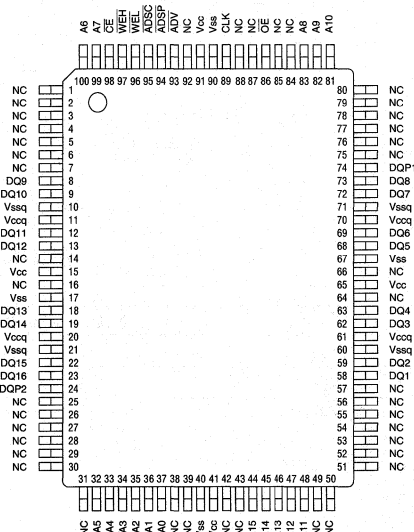
The MT58LC64K18A6 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry, a 2-bit burst counter and output register. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (\overline{CE}), burst control inputs (\overline{ADSC} , \overline{ADSP} , \overline{ADV}) and the byte write enables (\overline{WEH} , \overline{WEL}).

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SB-1)



100-Pin TQFP (SC-1)



NEW
3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

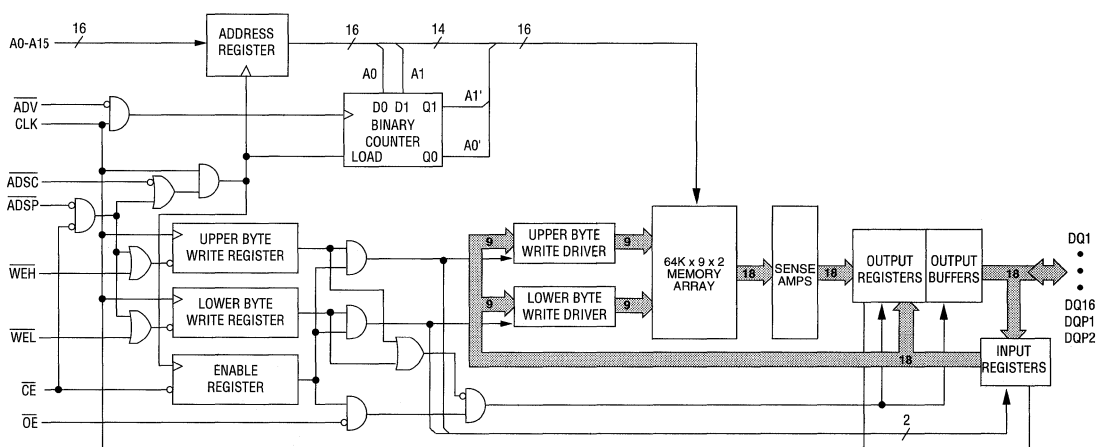
Asynchronous inputs include the output enable (\overline{OE}) and the clock (CLK). The data-out (Q), enabled by \overline{OE} , is also asynchronous. The output register is controlled by the clock. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor (ADSP) or address status controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by \overline{OE} to improve cache system response.

The MT58LC64K18A6 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for PowerPC™ and linear burst pipelined applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{\text{WEH}}, \text{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. WEL controls DQ1-DQ8 and DQP1. WEH controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{\text{CE}}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{\text{OE}}$	Input	Output Enable: This active LOW asynchronous input enables the Data I/O output drivers.
52	93	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{\text{ADSP}}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{\text{ADSP}}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{\text{ADSC}}$ but dependent upon $\overline{\text{CE}}$ being LOW.
2	95	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{\text{CE}}$ is LOW. $\overline{\text{ADSC}}$ is also used to place the chip into power-down state when $\overline{\text{CE}}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V $\pm 5\%$
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V $\pm 5\%$

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	CE	ADSP	ADSC	ADV	WRITE	OE	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

- NOTE:**
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{\text{WRITE}}=\text{L}$ means any one or more byte write enable signals ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$) are LOW. $\overline{\text{WRITE}}=\text{H}$ means all byte write enable signals are HIGH.
 2. $\overline{\text{WEL}}$ enables writes to DQ1-DQ8 and DQP1. $\overline{\text{WEH}}$ enables writes to DQ9-DQ16 and DQP2.
 3. All inputs except $\overline{\text{OE}}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
 4. Wait states are inserted by suspending burst.
 5. For a write operation following a read operation, $\overline{\text{OE}}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
 6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
 7. ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WE_s}$	OPERATION	\overline{CE}	$\overline{WE_s}$	\overline{OE}	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carryover from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1); data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1); data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carryover from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{CC} Supply Relative to V _{SS}	-0.5V to +4.6V
V _{IN}	-0.5V to +6V
Storage Temperature (plastic)	-55°C to +150°C
Junction Temperature	+150°C
Power Dissipation	1.6W
Short Circuit Output Current	100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-1	1	μA	
Output Leakage Current	Output(s) disabled, 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-1	1	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	MAX				UNITS	NOTES
				-7	-10	-12	-17		
Power Supply Current: Operating	Device selected; all inputs ≤ V _{IL} OR ≥ V _{IH} ; cycle time ≥ 1KC min; V _{CC} = MAX; outputs open	I _{CC}	150	225	200	175	160	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{\text{ADSC}}, \overline{\text{ADSP}}, \overline{\text{ADV}} \geq \text{V}_{\text{IH}}$; all inputs ≤ V _{IL} OR ≥ V _{IH} ; V _{CC} = MAX; cycle time ≥ 1KC min	I _{SB1}	45	65	55	50	45	mA	12, 13
CMOS Standby	Device deselected; V _{CC} = MAX; all inputs ≤ V _{SS} +0.2 or ≥ V _{CC} -0.2; all inputs static; CLK frequency = 0	I _{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V _{IL} OR ≥ V _{IH} ; all inputs static; V _{CC} = MAX; CLK frequency = 0	I _{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V _{IL} OR ≥ V _{IH} ; V _{CC} = MAX; CLK cycle time ≥ 1KC min	I _{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1 MHz V _{CC} = 3.3V	C _I	3	4	pF	4
Input/Output Capacitance (DQ)		C _O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ _{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ _{JC}	15	6	°C/W	
Maximum Case Temperature		T _C	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 3.3\text{V} \pm 5\%$)

DESCRIPTION		-7		-10		-12		-15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^t KC	15		20		25		30		ns	
Clock HIGH time	^t KH	5		7		9		11		ns	
Clock LOW time	^t KL	5		7		9		11		ns	
Output Times											
Clock to output valid	^t KQ		7		10		12		15	ns	
Clock to output invalid	^t KQX	3		3		3		3		ns	
Clock to output in Low-Z	^t KQLZ	2		2		2		2		ns	6, 7
Clock to output in High-Z	^t KQHZ		5		6		6		6	ns	6, 7
\overline{OE} to output valid	^t OEQ		5		6		7		8	ns	9
\overline{OE} to output in Low-Z	^t OELZ	0		0		0		0		ns	6, 7
\overline{OE} to output in High-Z	^t OEHZ		5		6		6		6	ns	6, 7
Setup Times											
Address	^t AS	2.5		3		3		3		ns	8, 10
Address Status (ADSC, ADSP)	^t ADSS	2.5		3		3		3		ns	8, 10
Address Advance (\overline{ADV})	^t AAS	2.5		3		3		3		ns	8, 10
Byte Write Enables (WEH, WEL)	^t WS	2.5		3		3		3		ns	8, 10
Data-in	^t DS	2.5		3		3		3		ns	8, 10
Chip Enable (\overline{CE})	^t CES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^t AH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status (ADSC, ADSP)	^t ADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance (\overline{ADV})	^t AAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables (\overline{WEH} , \overline{WEL})	^t WH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^t DH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable (\overline{CE})	^t CEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

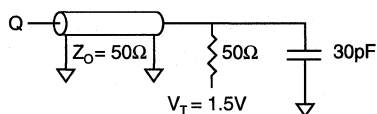


Fig. 1 OUTPUT LOAD EQUIVALENT

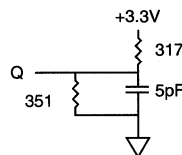
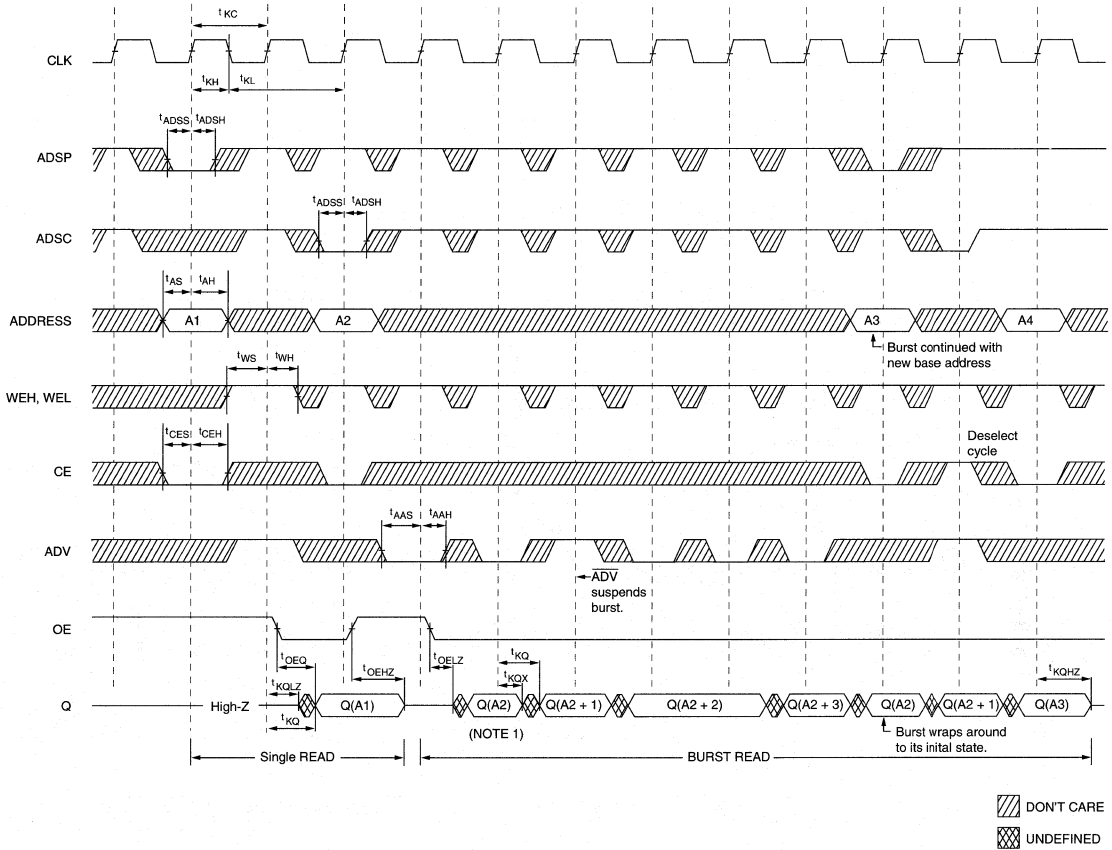


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

- All voltages referenced to Vss (GND).
- Overshoot: $V_{IH} \leq +6.0V$ for $t \leq t_{KC} / 2$.
Undershoot: $V_{IL} \geq -2.0V$ for $t \leq t_{KC} / 2$.
Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
- Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- Output loading is specified with $CL = 5pF$ as in Fig. 2. Transition is measured $\pm 500mV$ from steady state voltage.
- At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEZH} is less than t_{OELZ} .
- A READ cycle is defined by byte write enables all HIGH or \overline{ADSP} LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and \overline{ADSP} HIGH for the required setup and hold times.
- \overline{OE} is a "don't care" when a byte write enable is sampled LOW.
- This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either \overline{ADSP} or \overline{ADSC} is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either \overline{ADSP} or \overline{ADSC} is LOW) to remain enabled.
- Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds $110^\circ C$. Care should be taken to limit case temperature to acceptable levels.
- "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
- Typical values are measured at 3.3V, $25^\circ C$ and 20ns cycle time.

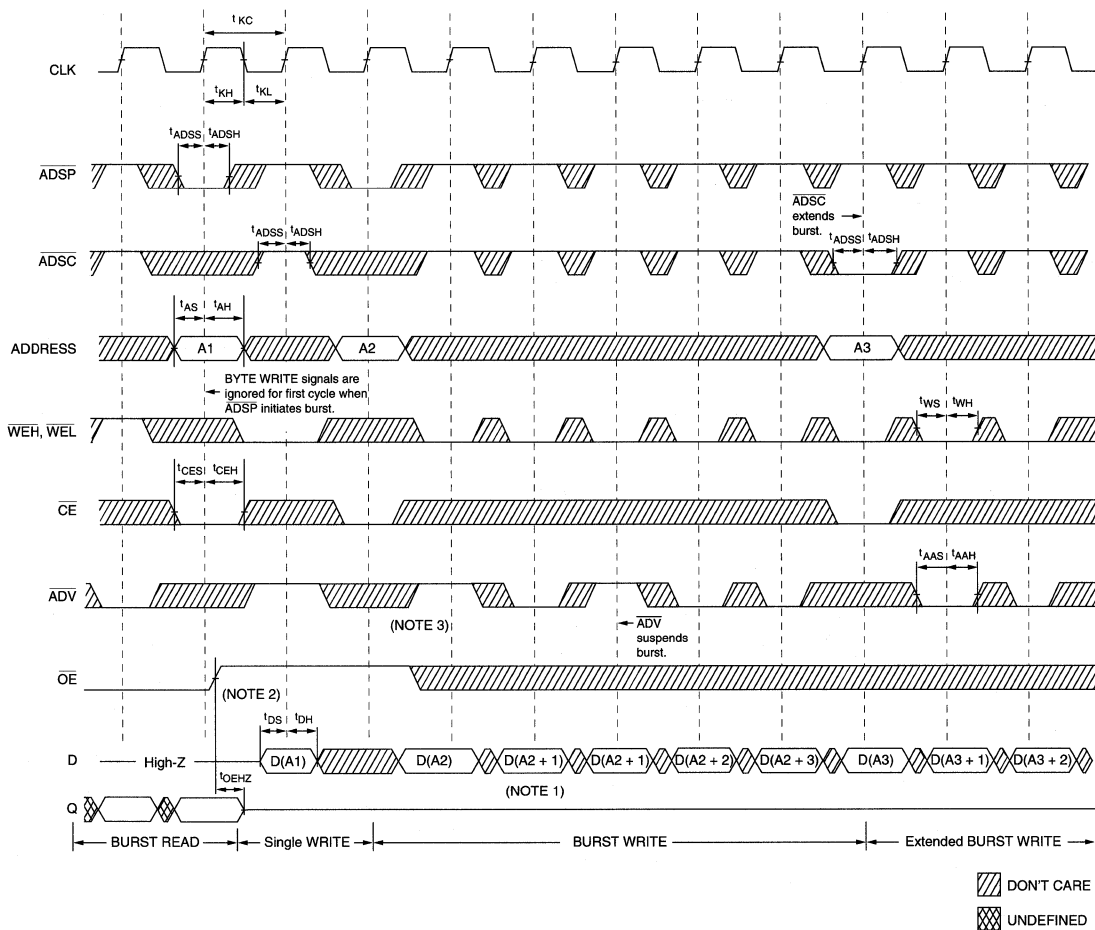
READ TIMING



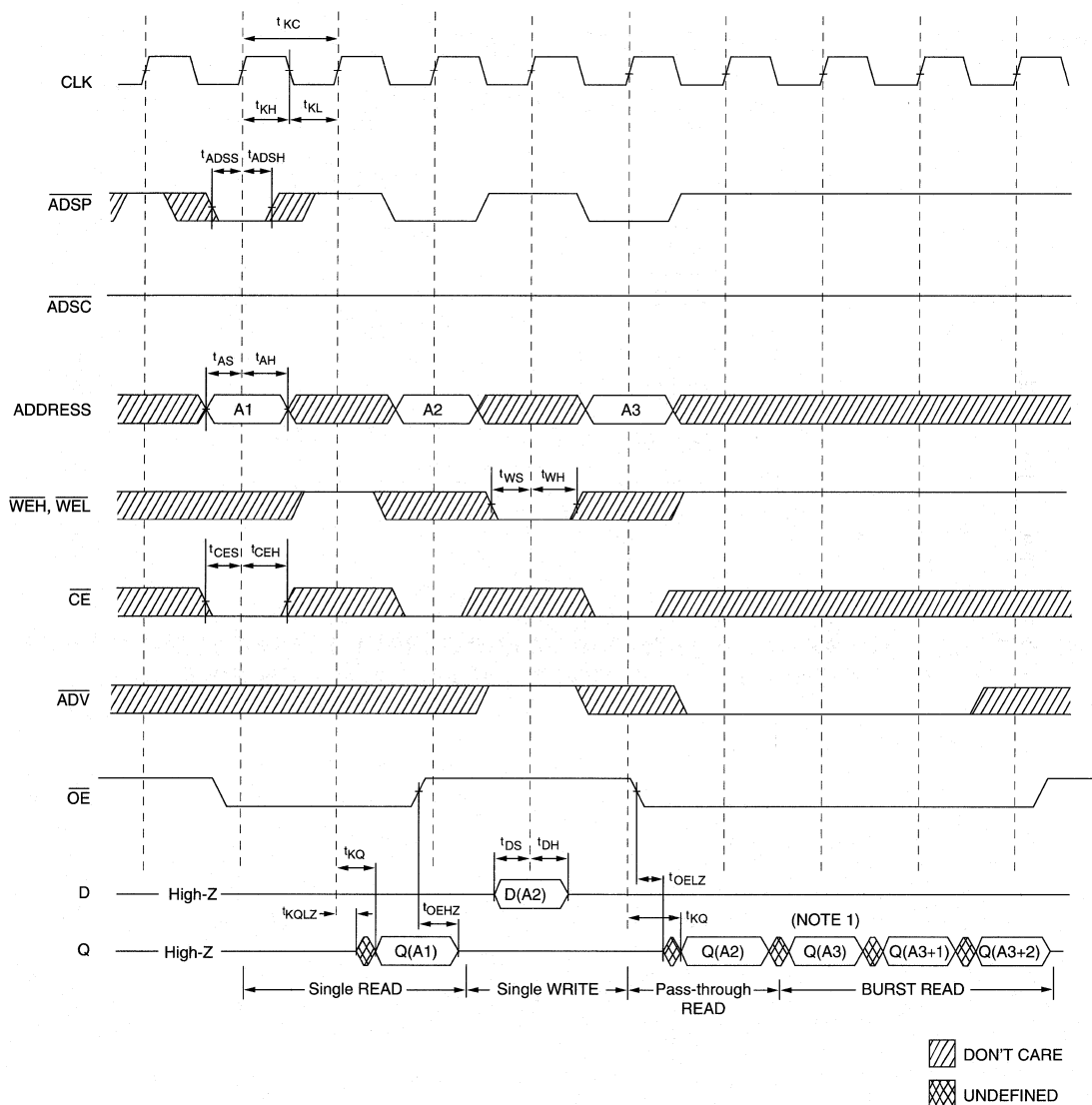
NEW
3.3 VOLT SYNCHRONOUS SRAM

NOTE: 1. $Q(A2)$ refers to output from address $A2$. $Q(A2+1)$ refers to output from the next internal burst address following $A2$.

WRITE TIMING



- NOTE:**
1. D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.
 2. Although a LOW on any one of the byte write inputs will tristate the data outputs, \overline{OE} must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being latched.
 3. \overline{ADV} must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING


NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

APPLICATION EXAMPLE

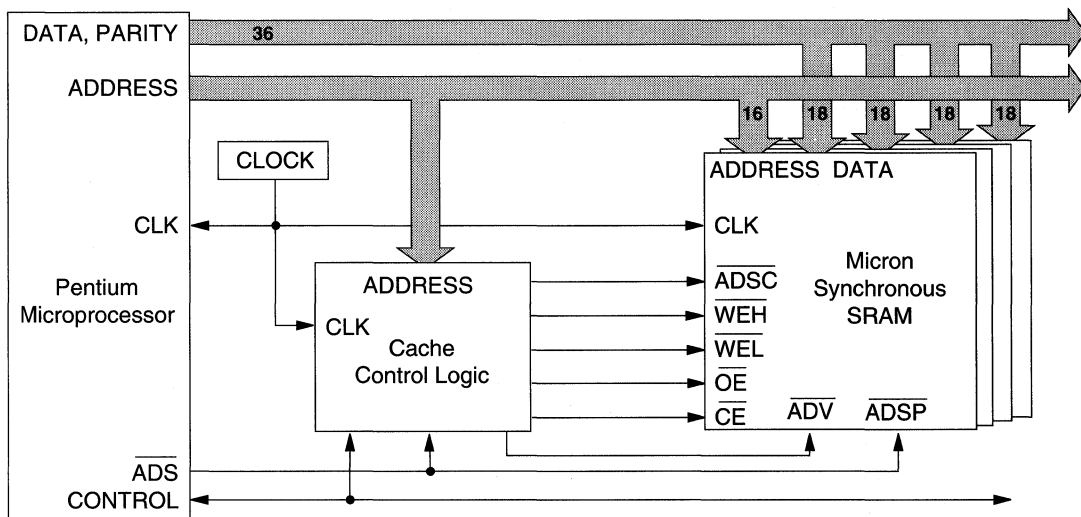


Figure 3

512K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz PENTIUM™ OR POWERPC™ USING FOUR MT58LC64K18A6EJ-10 SYNCHRONOUS SRAMs