SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND LINEAR BURST COUNTER

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{\text{OE}}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (linear burst sequence)
- High density, high-speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS

OPTIONS	MARKING
• Timing	
9ns access/15ns cycle	- 9
10ns access/15ns cycle	-10
12ns access/20ns cycle	-12
17ns access/25ns cycle	-17
• Packages	
52-pin PLCC	EJ
100-pin TQFP	LG

- Part Number Example: MT58LC64K18M1EJ-12

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

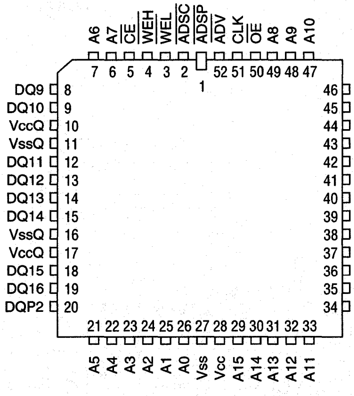
The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18M1 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{\text{CE}}$), burst control inputs ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$, $\overline{\text{ADV}}$) and byte write enables ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$).

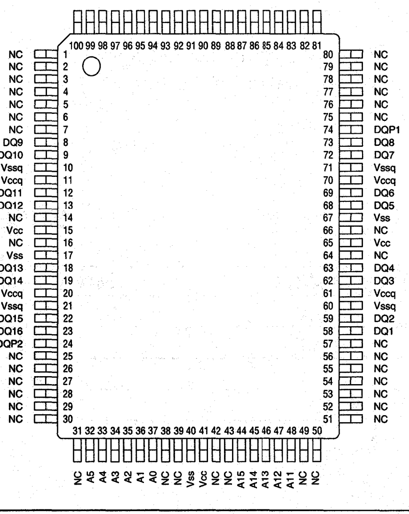
Asynchronous inputs include the output enable ($\overline{\text{OE}}$) and the clock (CLK). The data-out (Q), enabled by $\overline{\text{OE}}$, is also asynchronous. WRITE cycles can be from one to two bytes wide as controlled by the byte write enables.

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SB-1)



100-Pin TQFP
(SC-1)



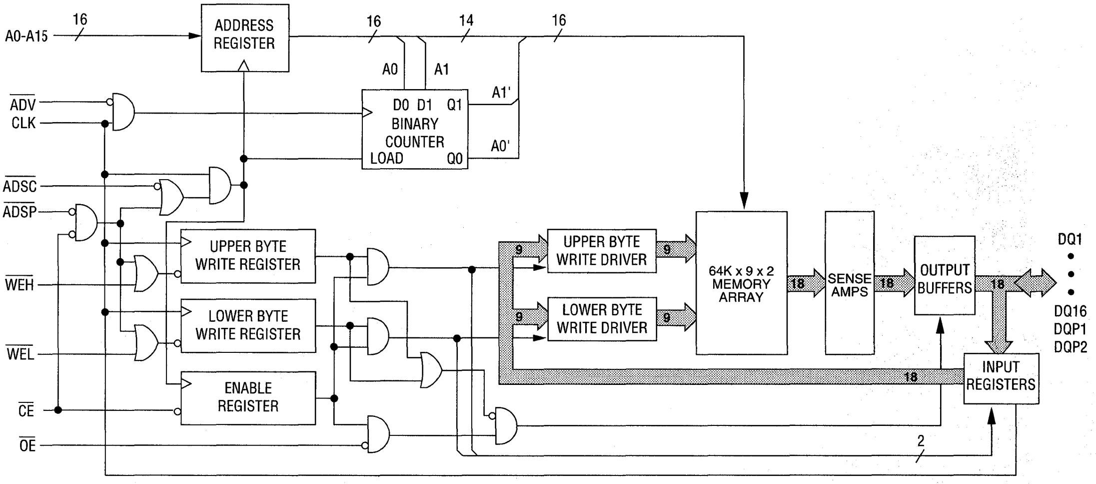
GENERAL DESCRIPTION (continued)

Burst operation can be initiated with either address status processor ($\overline{\text{ADSP}}$) or address status controller ($\overline{\text{ADSC}}$) input pins. Subsequent burst addresses can be internally generatedas controlled by the burst advance pin ($\overline{\text{ADV}}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{\text{WEL}}$ controls DQ1-DQ8 and DQP1. $\overline{\text{WEH}}$ controls DQ9-DQ16 and DQP2.

The MT58LC64K18M1 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for PowerPC™ and 680X0 systems and those systems which benefit from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

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PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 83, 82, 81, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	97, 96	$\overline{\text{WEH}}$, $\overline{\text{WEL}}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{\text{WEL}}$ controls DQ1-DQ8 and DQP1. $\overline{\text{WEH}}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{\text{CE}}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{\text{OE}}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	93	$\overline{\text{ADV}}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{\text{ADSP}}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	94	$\overline{\text{ADSP}}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{\text{ADSC}}$ but dependent upon $\overline{\text{CE}}$ being LOW.
2	95	$\overline{\text{ADSC}}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{\text{CE}}$ is LOW. $\overline{\text{ADSC}}$ is also used to place the chip into power down state when $\overline{\text{CE}}$ is HIGH.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	11, 20, 61, 71	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
11, 16, 37, 42	10, 21, 60, 71	VssQ	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 4, 5, 6, 7, 14, 16, 25, 26, 27, 28, 29, 30, 31, 38, 39, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 64, 66, 75, 76, 77, 78, 79, 80, 84, 85, 87, 88, 92	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{\text{CE}}$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{\text{WRITE}}$=L means any one or more byte write enable signals ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$) are LOW. $\overline{\text{WRITE}}$=H means all byte write enable signals are HIGH.
2. $\overline{\text{WEL}}$ enables writes to DQ1-DQ8 and DQP1. $\overline{\text{WEH}}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{\text{OE}}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{\text{OE}}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{\text{ADSP}}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ....-0.5V to +4.6V
V_{IN} ....-0.5V to +6V
Storage Temperature (plastic) ....-55°C to +150°C
Junction Temperature ....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYPICAL**	**-9**	**-10**	**-12**	**-17**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC min; V_{CC} = MAX; outputs open	I_{CC}	150	225	225	200	175	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ ^tKC min	I_{SB1}	45	65	65	55	50	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_I	3	4	pF	4
Input/Output Capacitance (DQ)		C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	45	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	6	°C/W	
Maximum Case Temperature		TC	110	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

DESCRIPTION	SYM	-9		-10		-12		-17		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time	^{t}KC	15		15		20		25		ns	
Clock HIGH time	^{t}KH	4		5		6		8		ns	
Clock LOW time	^{t}KL	4		5		6		8		ns	
Output Times											
Clock to output valid	^{t}KQ		9		10		12		17	ns	
Clock to output invalid	^{t}KQX	3		3		3		3		ns	
Clock to output in Low-Z	^{t}KQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^{t}KQHZ		5		5		6		6	ns	6, 7
$\overline{\text{OE}}$ to output valid	^{t}OEQ		5		5		6		7	ns	9
$\overline{\text{OE}}$ to output in Low-Z	^{t}OELZ	0		0		0		0		ns	6, 7
$\overline{\text{OE}}$ to output in High-Z	^{t}OEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	^{t}AS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$)	^{t}ADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{\text{ADV}}$)	^{t}AAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$)	^{t}WS	2.5		3		3		3		ns	8, 10
Data-in	^{t}DS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{\text{CE}}$)	^{t}CES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^{t}AH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$)	^{t}ADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{\text{ADV}}$)	^{t}AAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{\text{WEH}}$, $\overline{\text{WEL}}$)	^{t}WH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^{t}DH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{\text{CE}}$)	^{t}CEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

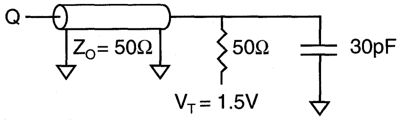


Fig. 1 OUTPUT LOAD EQUIVALENT

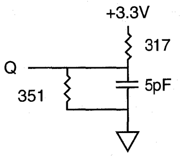
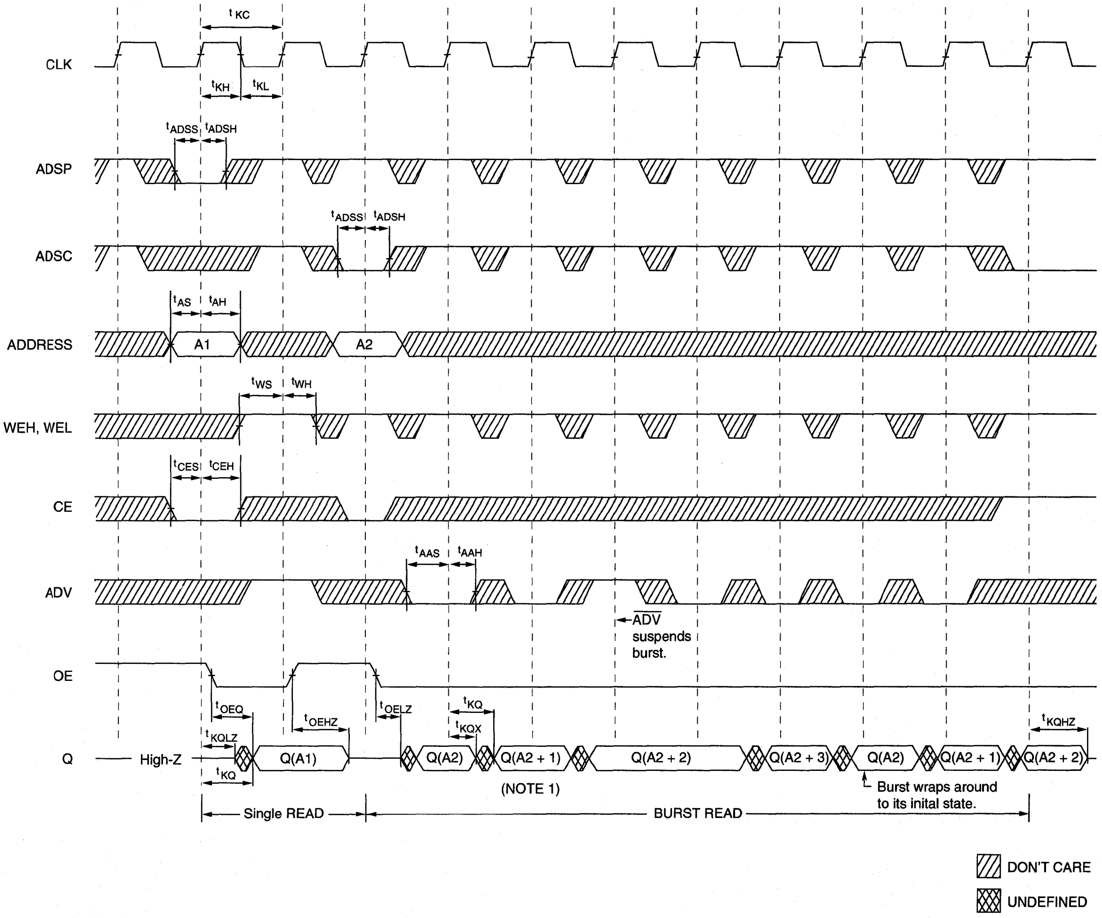


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

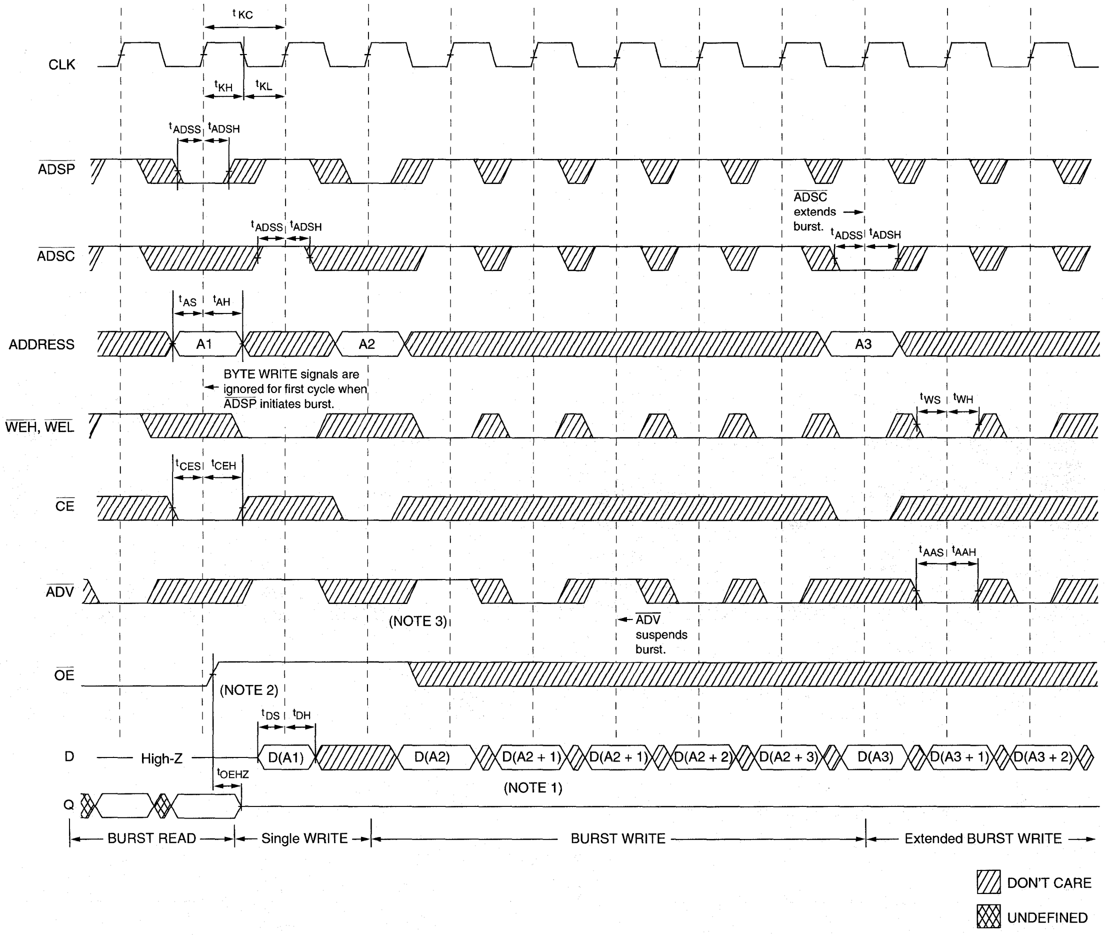
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le {}^tKC/2$.
   Undershoot: $V_{IL} \ge -2.0V$ for $t \le {}^tKC/2$.
   Power-up: $V_{IH} \le +6.0V$ and $V_{CC} \le 3.1V$ for $t \le 200$msec.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING



NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

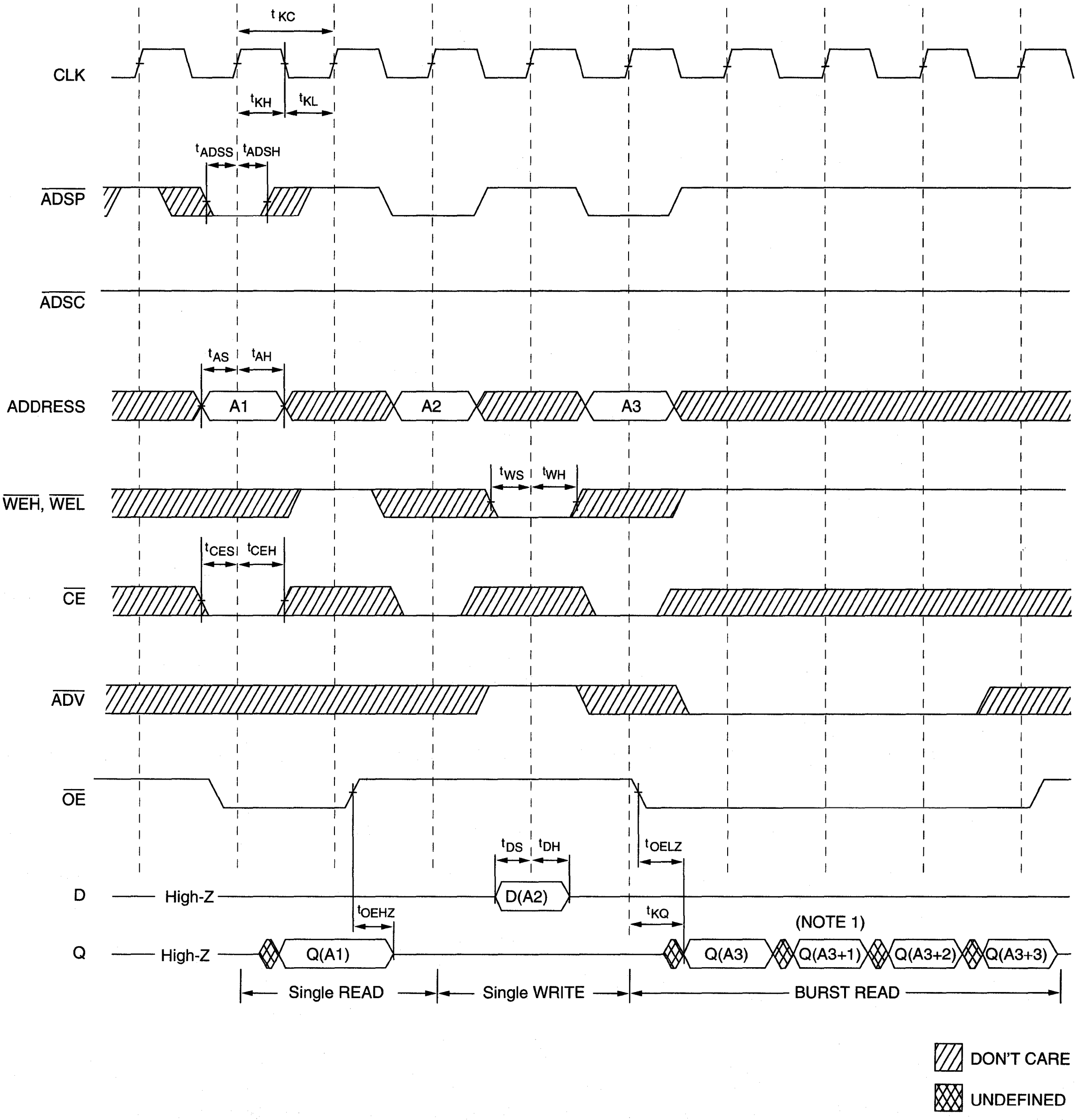
WRITE TIMING



NOTE: 1 D(A2) refers to input to address A2. D(A2+1) refers to input to the next internal burst address following A2.

2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE: 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

APPLICATION EXAMPLE

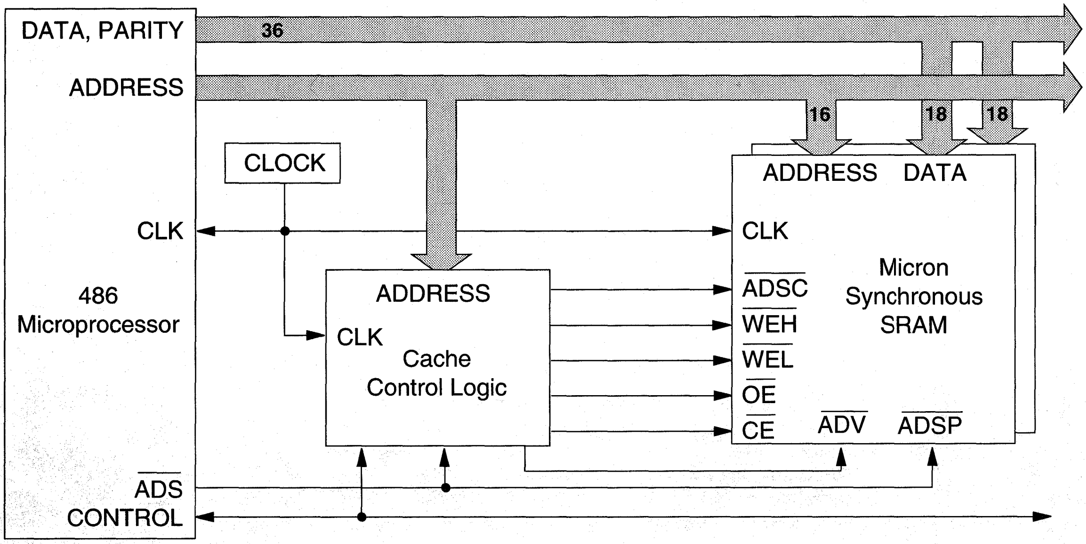


Figure 3
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 OR 680X0 USING TWO MT58LC64K18M1EJ-12 SYNCHRONOUS SRAMs