MEDIATEK

MT5931 Application Design Notice v1

2011.10.07





Update History

- 2011.09.04 : initial version 0.1
- 2011.10.07 : version 1.0

Outline -1

- MT5931 Block diagram and features
- MT5931 Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection (FP and SP)
  - System GPIO signals connection
  - WIFI BT co-existence signal connection (FP and SP)
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

Outline-2

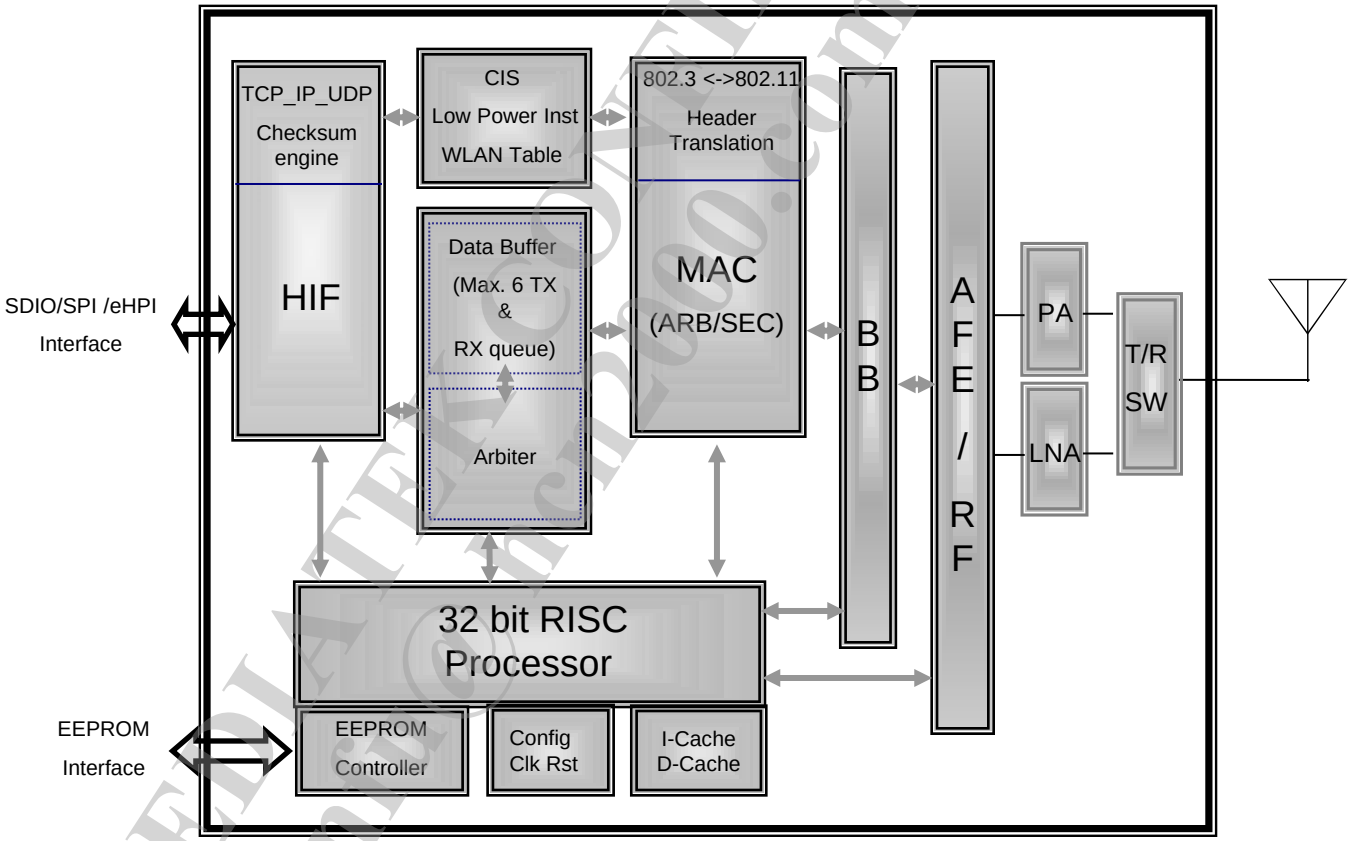
- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
- META Tool Usage
- ATE Setting
- WIFI MAC address

Outline

- MT5931 Block diagram and features
- MT5931 Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection (FP and SP)
  - System GPIO signals connection
  - WIFI BT co-existence signal connection (FP and SP)
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

MT5931 Block Diagram and Features

- Block Diagram



MT5931 Block Diagram and Features

- Feature
  - MT5931 is a WiFi device which includes
    - 802.11 b/g/n
    - PA
    - LNA
    - TRSW
    - Internal PMU
- Package
  - MT5931A (TFBGA) : 5.1mm* 5.3mm
    - Support EHPI 8 , EHPI 16 and SDIO.
  - MT5931P (WLCSP) : 2.9mm* 3.2mm
    - Support SDIO only.

Outline

- MT5931 Block diagram and features
- MT5931 TFBGA Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection
  - System GPIO signals connection
  - WIFI BT co-existence signal connection
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

MT5931 Schematic Design

- Interface mode selection : Strap mode

【ANTSEL_0】	【ANTSEL_1】	【GPIO_1】	Main clock frequency
0	1	0	26MHz

【WIFI_INT_B】	Main clock source
0	OSC / Co-clocking
1	XTAL

【GPIO_0】	32K source
1	Internal
0	External

【ANTSEL_2】	【ANTSEL_3】	Host interface
0	0	eHPI-8
1	0	eHPI-16
0	1	SPI
1	1	SDIO

MT5931 Schematic Design

- Interface mode selection : Strap mode

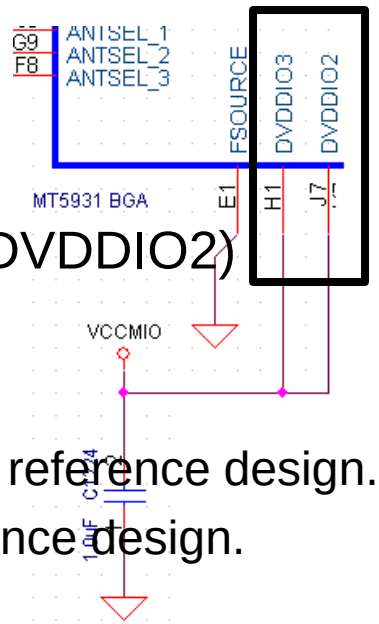
Pin Name	FP Phone HW configure (NFI 8 bit)	SP Phone HW configure (SDIO)	MT5931 E3 default Pull
GPIO_1	NC	NC	PD
GPIO_0	NC	NC	PD
ANTSEL_3	NC	external 10K resistor PU	PD
ANTSEL_2	NC	external 10K resistor PU	PD
ANTSEL_1	NC	NC	PU
ANTSEL_0	NC	NC	PD
WIFI_INT_B	connect to BB & external 10K resistor PD/PU	connect to BB & external 10K resistor PD/PU	No-pull

MT5931 Schematic Design

- Interface mode selection
  - MT5931 uses **strap-pin** to configure IC interface type, clock frequency and clock type setting. These pins are input mode at power-on stage and return to other function at normal operation stage.
  - MT5931 Antsel_0 , Antsel_1 , Antsel_2 , Antsel_3 , GPIO_0, and GPIO_1 pins support internal PU or PD pad design.
  - WIFI_INT_B pin doesn't support internal PU or PD pad design so needs external 10K resistor circuit.

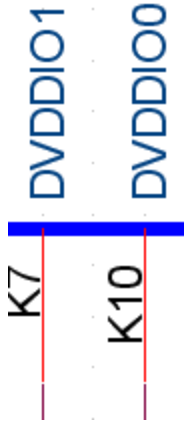
MT5931 Schematic Design (TFBGA)

- Host interface IO voltage domain setting
  - MT5931 supports different host interface IO voltage domain by connecting MT5931 IO voltage **pins J7 and pin H1** to different voltage according to different BB's requirement, like 2.8V or 1.8V.
  - MT5931 IO voltage pin H1(DVDDIO3)
    - HPI 8bit mode / SDIO IO domain.
  - MT5931 IO voltage pin H1(DVDDIO3) and J7(DVDDIO2)
    - HPI 16bit mode IO domain.
  - Example
    - Default 1.8V for MT6236/MT6276/MT6256 MTK reference design.
    - Default 2.8V for MT6235 or MT6513 MTK reference design.
    - Please take MTK official design as reference .



MT5931 Schematic Design (TFBGA)

- Interface IO voltage domain setting
  - MT5931 IO voltage pin K7(DVDDIO1)
    - BT_PRI IO domain
  - MT5931 IO voltage pin K10(DVDDIO0)
    - ANTSEL , GPIO , OSC_EN , RST_N and UART IO domain
  - Example
    - BT_PRI is 2.8V in MT6236/MT6256/MT6576
    - BT_PRI is 1.8V in MT6513+MT6626+MT5931 reference design.
    - Please take MTK official design as reference .



MT5931 Schematic Design

- Interface connection (Feature Phone, NFI)

		Pin name	MT5931 I/O屬性	MT5931 Default PU/PD	MT5931 IO domain	Note
MT5931 E3	Interface	NFI D0~7	I/O	no-pull	VDD_NFI	這些訊號皆同power domain (MT5931 DVDDIO3 for NFI8) (MT5931 DVDDIO2/3 for NFI16)
		/CS	I			
		EINT	O			
		OE_N	I			
		WE_N	I			
		LPA0	I			
	GPIO request	WIFI_EN	I	no-pull	2.8V	MT5931 internal PMU enable pin
		WIFI_RST	I	PU	2.8V	MT5931 reset signal
		WIFI_32K	I	no-pull	2.8V(default)	可透過MT5931 VRTC pin來調整.
		BT_PRI	I/O	PD	2.8V(default)	可透過MT5931 DVDDIO1 pin來調整
		OSC_EN	O	no-pull	2.8V	WIFI co-clock request pin

- Support Feature Phone BB
  - MT6235/36/52/56/76

MT5931 Schematic Design (MT6236 example)

- Interface connection
  - MT5931 shares NFI bus with NAND and LCM module so WiFi , NAND and LCM must have the same bus voltage domain.

MT5931 pin name	**MT6236 pin name**	Description
D0~D7	NLD0~NLD7	NFI , LCM and MT5931 should have the same NFI voltage domain setting.
D8~D15	Don't connect Keep NC	
OE_N	LRDB	
WE_N	LWRB	
A0	LPA0	
CS_N	LPCE1B	
INT_N	EINT0	**MUST connect WIFI EINT to MT6236 EINT0 !!** Because EINT0 power domain = DVDD_NFI EINT1~6 power domain = DVDD28 Only EINT0 meets MT5931 requirement.

MT5931 Schematic Design (MT6236 example)

- Interface connection
  - There are three **2.8V IO** signals
    - **WIFI_EN** signal would control MT5931 internal PMU. Please use default PD mode function GPIO.
      - High : Enable PMU
      - Low : Disable PMU
    - **WIFI_RST** signal would control MT5931 reset state.
    - **WIFI_32K** is MT5931's slow clock source.
  - All signals should belong to **BB DVDD28 power domain GPIO**. Please don't use other power domain IO, like CAM.

MT5931 pin name	MT6236 pin name	Power domain
XIN_32K	GPIO17	DVDD_KP=VIO case
	GPIO 8/42/58/63	DVDD28

MT5931 Schematic Design (MT6236 example)

- WIFI BT co-existence signal (Feature phone)
  - BT_PRI is **2.8V IO** signal .

MT5931 pin name	MT6236 pin name	Description
BT_PRI	bt2wifi_0(GPIO64)	**WiFi BT co-existence signal**

- Other platform

MT5931 pin name	BB or BT pin name	Description
BT_PRI	MT6256 pin B10 (GPIO3)	**WiFi BT co-existence signal**
	MT6276 pin AM33 (GPIO16)	
	MT6616/6622/6626 (GPIO4)	
	MT6611 (GPIO7)	

MT5931 Schematic Design

Interface connection (Smart Phone, SDIO)

		Pin name	MT5931 I/O屬性	MT5931 Default PU/PD	MT5931 IO domain	Note
MT5931 E3	Interface	D0 ~D3 (SDIO D0~D3)	I/O	no-pull	VDD_SDIO 2.8V for high speed	這些訊號皆同power domain (MT5931 DVDDIO3 for SDIO)
		EINT	O			
		OE_N (SDIO_CLK)	I			
		A0 (SD_CMD)	I/O			
	GPIO request	WIFI_EN	I	no-pull	2.8V	MT5931 Internal PMU enable pin
		WIFI_RST	I	PU	2.8V	MT5931 reset signal
		WIFI_32K	I	no-pull	2.8V(default)	可透過MT5931 VRTC pin來調整,
		BT_PRI	I/O	PD	1.8V (default in MT6513+MT6626+MT5931)	可透過MT5931 DVDDIO1 pin來調整,
		OSC_EN	O	no-pull	2.8V	WIFI co-clock request pin (output)

- Support Smart Phone BB
  - MT6513/MT6573

MT5931 Schematic Design (MT6513 example)

- Interface connection (Smart Phone)

MT5931 pin name	MT6513 pin name	Description
D0~D3	MC1DA0~3	SDIO bus
OE_N (SDIO_CLK)	MC1CK MC1CK_FB	
A0 (SD_CMD)	MC1CM0	
WIFI_INT_B	EINT15	Interrupt

MT5931 Schematic Design (MT6513 example)

- Interface connection
  - There are three **2.8V IO** signals
    - **WIFI_EN** signal would control MT5931 internal PMU. Please use default mode PD function GPIO.
      - High : Enable PMU
      - Low : disable PMU
    - **WIFI_RST** signal would control MT5931 reset state.
    - **WIFI_32K** is MT5931's slow clock source.
  - All signals should belong to **BB DVDD28 power domain GPIO**. Please don't use other power domain IO, like CAM.
  - Please take MTK official design as reference.

MT5931 Schematic Design (MT6513 example)

- WIFI BT co-existence signal (Smart phone)
  - BT_PRI is **1.8V IO** signal due to MT6626's 1.8V IO setting in MT6513+MT6626+MT5931 reference design.

MT5931 pin name	MT6626 pin name	Description
BT_PRI	bt2wifi(GPIO4)	**WiFi BT co-existence signal**

MT5931 Schematic Design

- System Power source connection
  - MT5931 needs four external power sources.
  - Please take MTK official design as reference .

MT5931 Pin name	MT6236 name	Description	Voltage range	Voltage tolerance	current
VBAT	---	Internal PMU power source	+3.6~+4.3V	---	>100mA
DVDDIO0	DVDD28	Digital IO power source 0	+2.8V	+/-10%	<5mA
DVDDIO1*	DVDD28/ DVDD18	Digital IO power source 1	+2.8V /+1.8V	+/-10%	<5mA
DVDDIO2/3*	DVDD28/ DVDD18	Digital IO power source 2/3	+2.8V /+1.8V	+/-10%	<5mA
VRTC**	VRTC	Digital power source	+2.8V	+/-10%	<1mA

*According to different BB platform, DVDDIO1~3 might have different design. Customers must take newest MTK BB+MT5931 design package as reference design.
** MT5931 use MT6235's pin B11 BAT_BACKUP as 2.8V VRTC power.

Outline

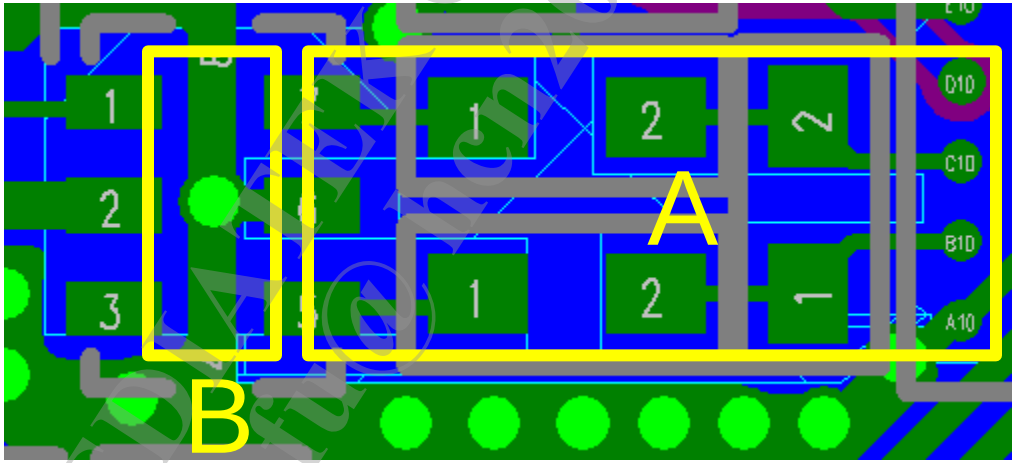
- MT5931 Block diagram and features
- MT5931 Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection (FP and SP)
  - System GPIO signals connection
  - WIFI BT co-existence signal connection (FP and SP)
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

MT5931A TFBGA Layout Guide

- RF Trace
  - RF traces keep as short as possible for reducing RF performance loss.
  - Reserving matching network between MT5931 IC differential RF trace and external passive balance-BPF component.
  - RF single and differential-end trace impedance is 50 Ohm and the route needs to keep equal length. Please use L2 as reference ground.
  - RF traces must route on the surface layer and far away from other high speed signal trace .
  - Digital traces shouldn't go through directly under RF trace layers.
  - All RF trace below should have solid ground plane.

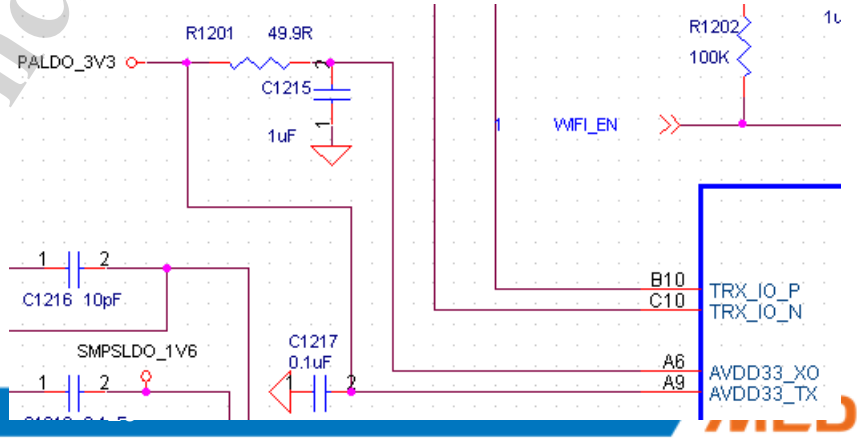
MT5931A TFBGA Layout Guide

- Example
  - RF differential-end trace needs to keep equal length and have solid ground plane, like A. Suggest to use L2 as RF 50 ohm reference ground.
  - Balanced filter should have solid ground, like B. GND via would effect filter performance degradation.



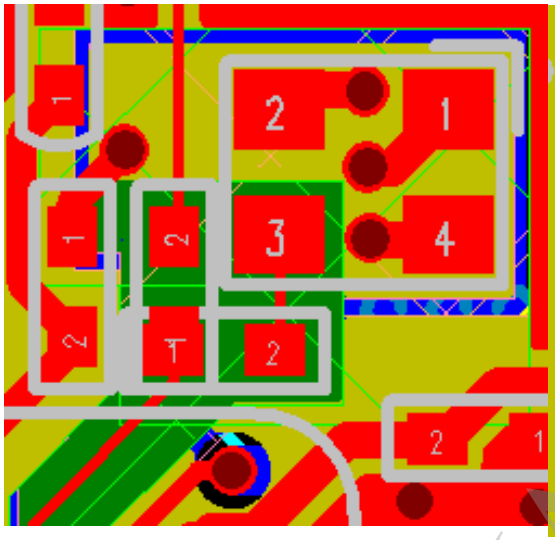
MT5931A TFBGA Layout Guide

- Clock Trace
  - Keep clock trace as short as possible.
  - Keep the noisy traces far away from clock trace.
  - Clock traces enclosed by PCB copper is recommended.
  - Please keep the empty ground plane under crystal component to reduce resident effect.
  - Suggest MT5931A A6 pin bypass capacitor GND pin to connects to crystal GND plate with via.

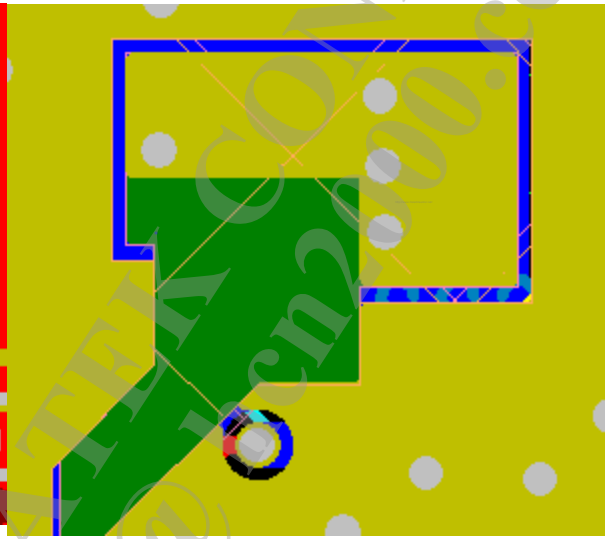


MT5931A TFBGA Layout Guide

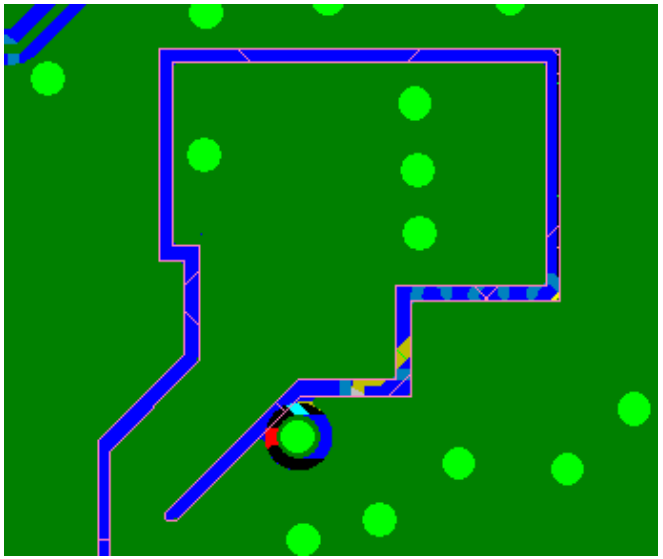
- Example
  - Crystal pad mapping reference



WS1556
L1



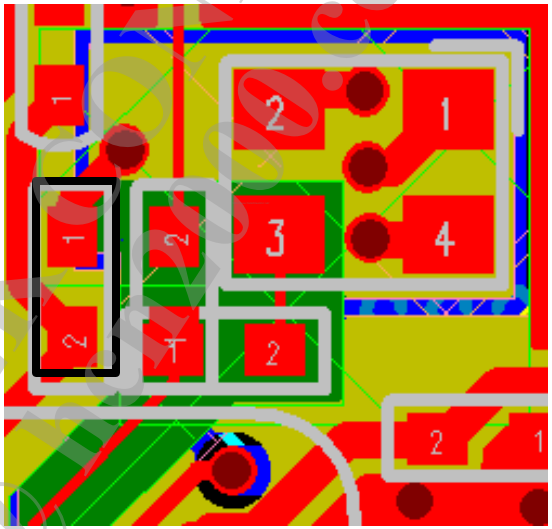
WS1556
L2



WS1556
L3

MT5931A TFBGA Layout Guide

- Example
  - MT5931A A6 pin bypass capacitor GND pin (black square) connects to crystal GND plate with via.

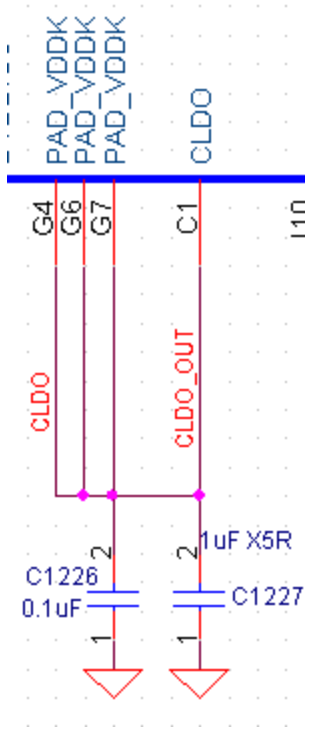


MT5931A TFBGA Layout Guide

- Power Trace
  - VBAT , PALDO , SMPSLDO and CLDO power trace width is at least 10 mil width.
  - Keep de-coupling capacitors close to the power pins.
  - Keep 10pF capacitor close to balanced filter DC feed point.
  - Power trace should connect to de-couple capacitors first and then connect to target input pins.
  - PALDO_FB and OUT_FB signal is 4 mil width.

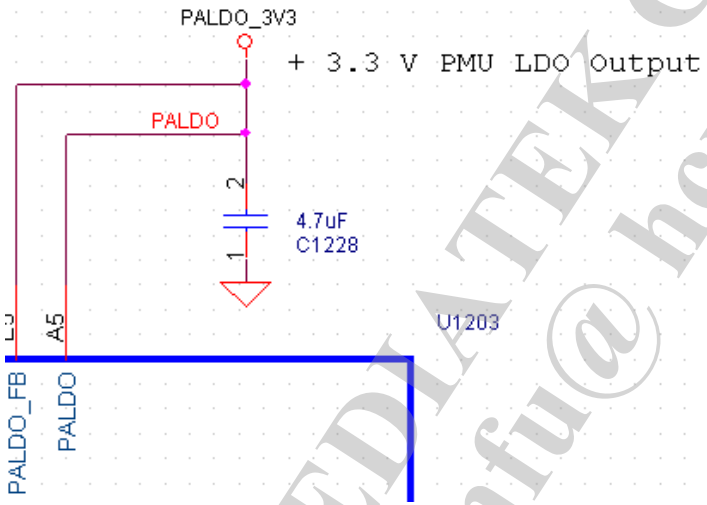
MT5931A TFBGA Layout Guide

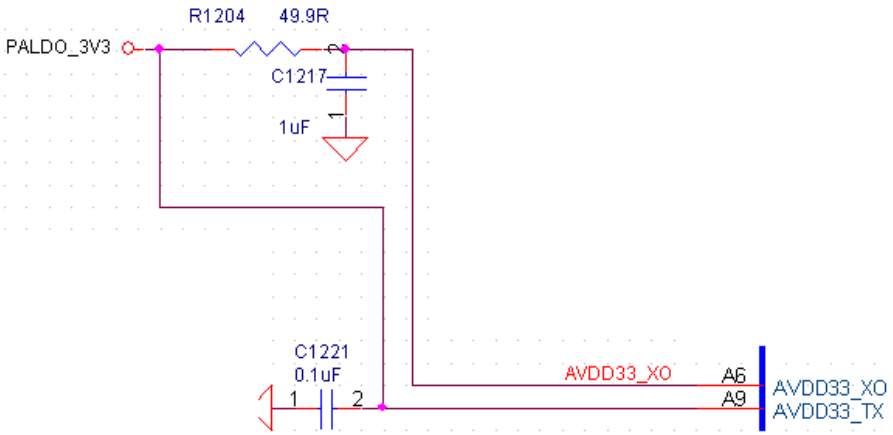
- Power Trace
  - Example (CLDO net)
  - Power trace should connect to C1227 first and then connect to C1226. Finally connect to Pin G4/G6/G7 target pins.



MT5931A TFBGA Layout Guide

- Power Trace
  - Example (PA LDO net)
  - Power trace should connect to C1228 first and then connect to C1221. Finally connect to Pin A9 target pins.

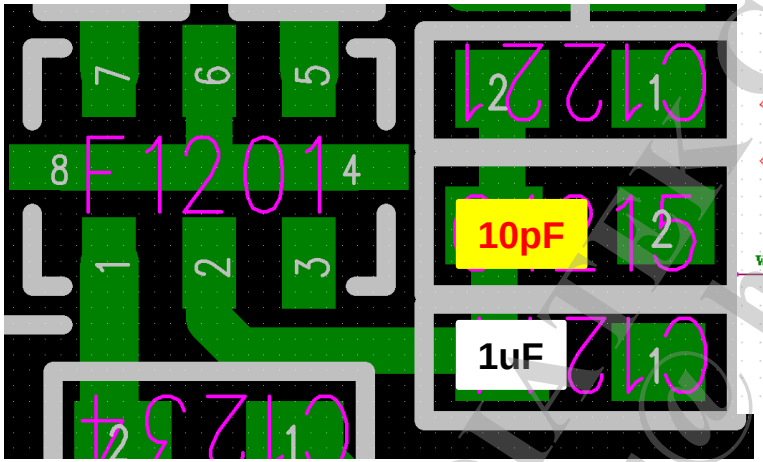


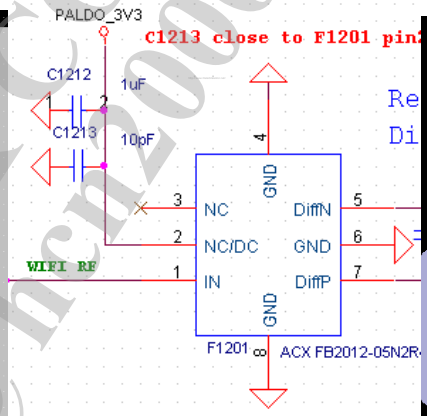


MT5931A TFBGA Layout Guide

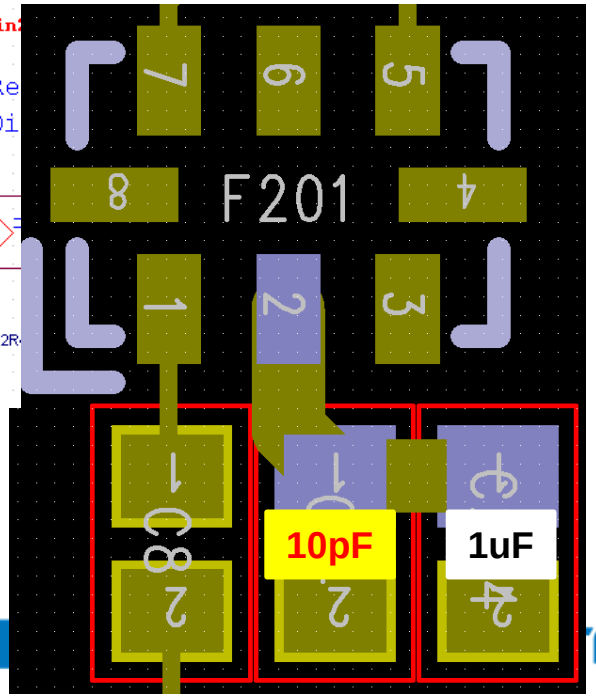
- Power Trace
  - Example (PA LDO net)
  - Keep 10pF capacitor close to balanced filter DC feed point.

Bad placement case



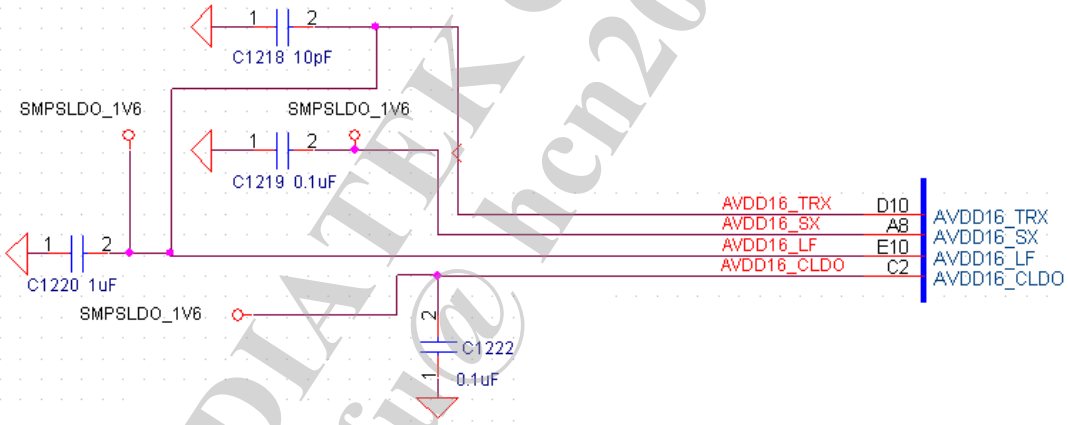


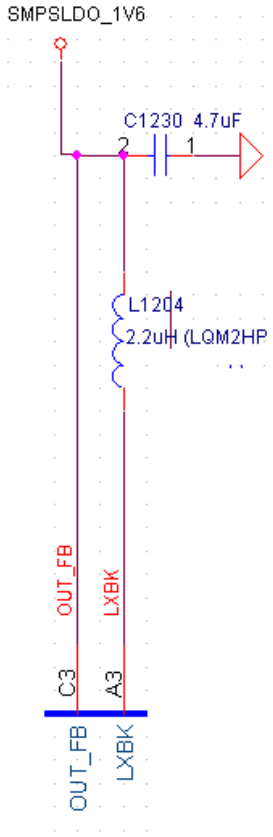
Good placement case



MT5931A TFBGA Layout Guide

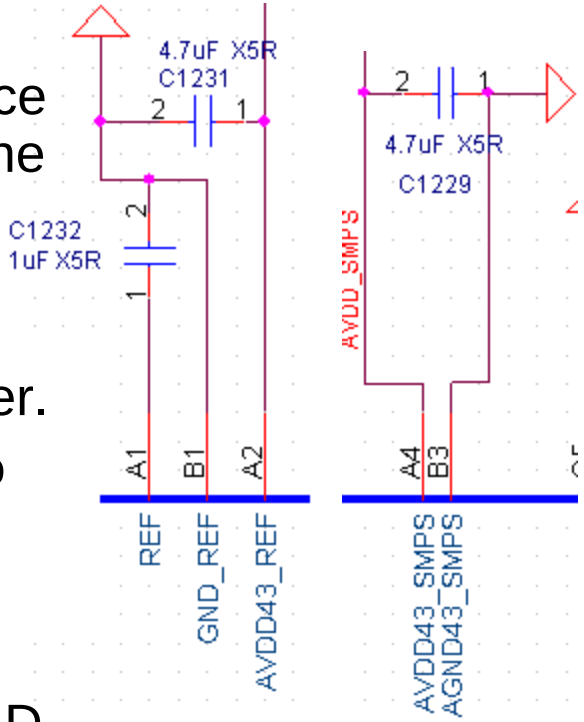
- Power Trace
  - Example (SMPSLDO_1V6 net)
  - Power trace should connect to C1230 first and then connect to C1218,C1219 , C1220 and C1222. Finally connect to target pins.





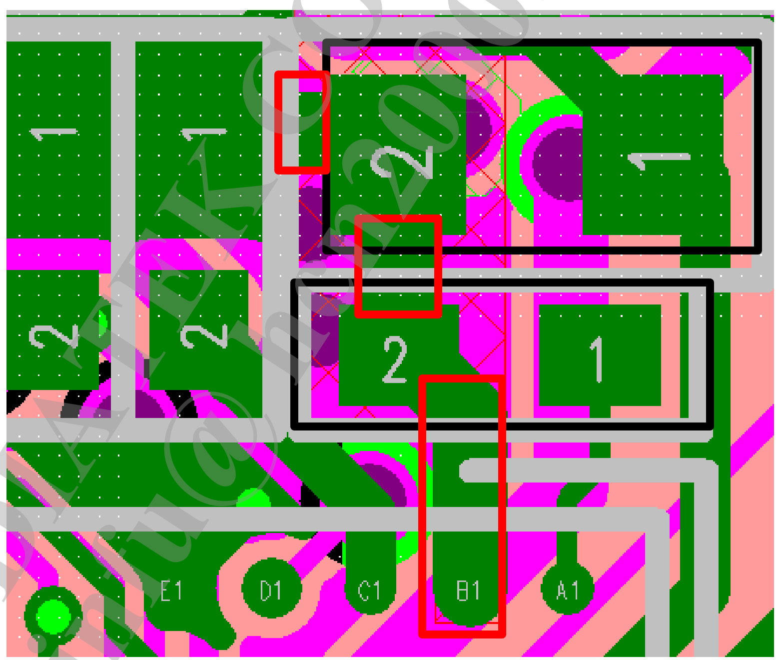
MT5931A TFBGA Layout Guide

- Ground Trace
  - MT5931 pinB1 should connect to C1231 and C1232 GND pin with limited width trace first and then connect to other ground plane or layer.
  - MT5931 pinB3 should connect to C1229 GND pin with limited width trace first and then connect to other ground plane or layer.
  - Don't connect pinB1 and pinB3 directly to GND plane.
  - Separate digital GND and RF GND plane.
  - Balun-filter and DC decoupling caps GND must been direct contact to PCB main GND with GND via.



MT5931A TFBGA Layout Guide

- Example
  - MT5931 pinB1 should connect to C1231 and C1232 GND pin with limited width trace first and then connect to other ground plane or layer.

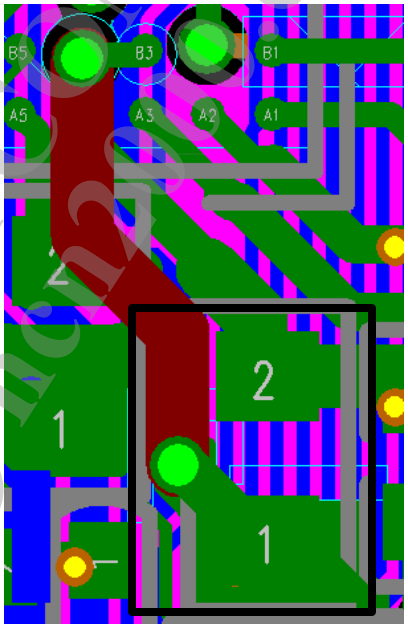


C1232

C1231

MT5931A TFBGA Layout Guide

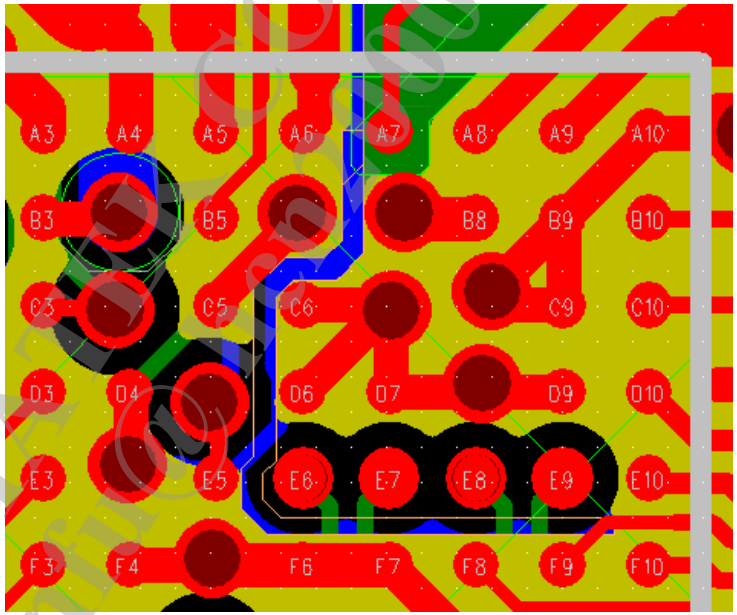
- Example
  - MT5931 pinB3 should connect to C1229GND pin with limited width trace first and then connect to other ground plane or layer.



C1229

MT5931A TFBGA Layout Guide

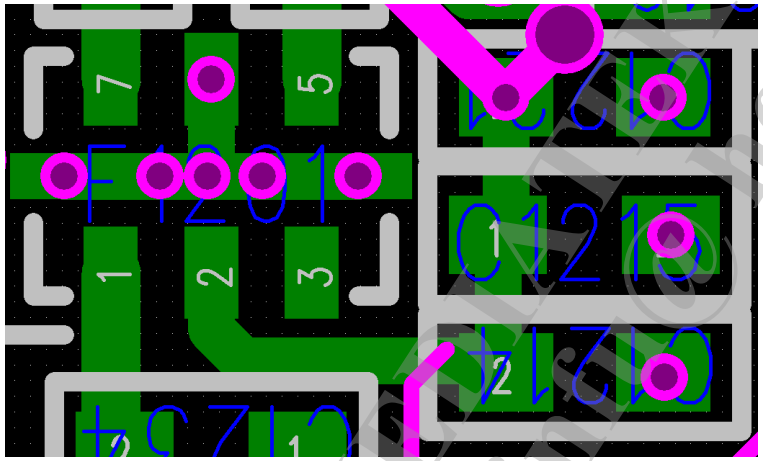
- Example
  - Like B9/C9/A10在L1連接後再到L2與GND 大地連
  - Like C6/D5/D7/D9在L1連接後再到L2與GND 大地連
  - 將RF 與數位地做切割至A7 pin(黃色虛線處)



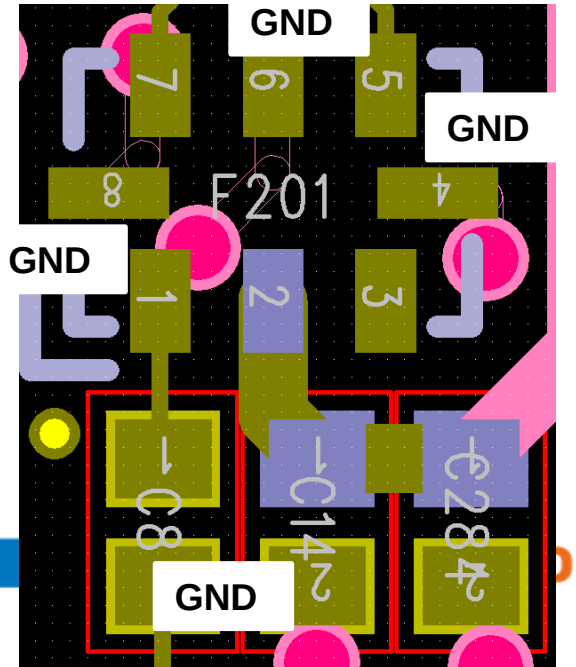
MT5931A TFBGA Layout Guide

- Example
  - Balun filter and DC decoupling caps GND must been direct contact to PCB main GND with GND via.

Bad via case
(only L1-2 GND via ,no near main GND via)



Good GND via case

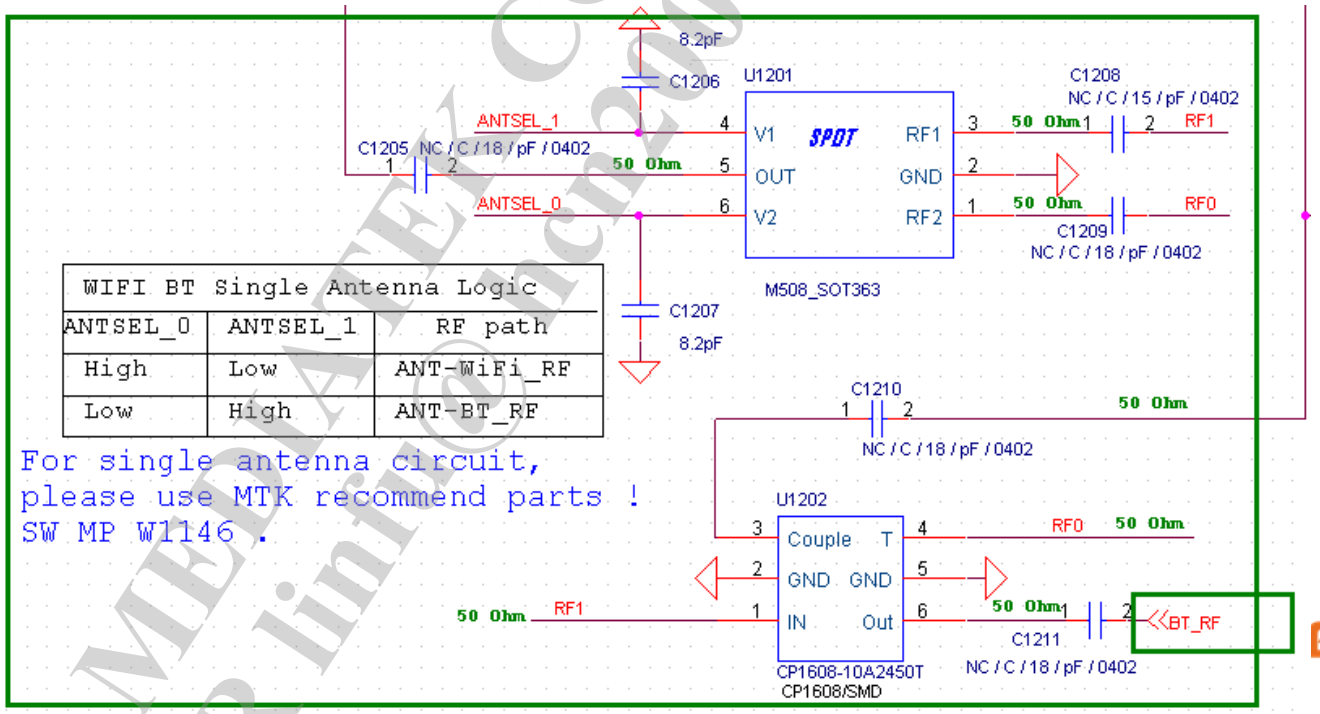


Outline

- MT5931 Block diagram and features
- MT5931 Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection (FP and SP)
  - System GPIO signals connection
  - WIFI BT co-existence signal connection (FP and SP)
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

MT5931 WIFI BT Single Antenna Structure

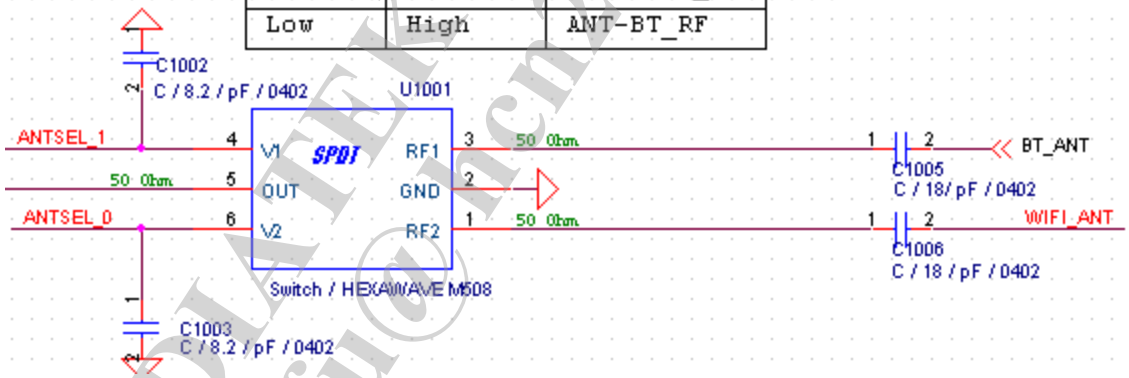
- MT5931 support
  - Dual Antenna : recommend default design in all platform
  - Mode 7 FDD single antenna :
    - All FP platforms support mode 7.
    - SP platforms don't support mode 7.



MT5931 WIFI BT Single Antenna Structure

- MT5931 support
  - Mode 8 TDD single antenna ：MT6256/MT6622/MT6626
  - Software MP schedule
    - FP : after W1208
    - SP : after W1146

ANTSEL_0	ANTSEL_1	RF path
High	Low	ANT-WiFi_RF
Low	High	ANT-BT_RF



MT5931 WIFI BT Single Antenna Structure

- Single antenna control logic table is as below.

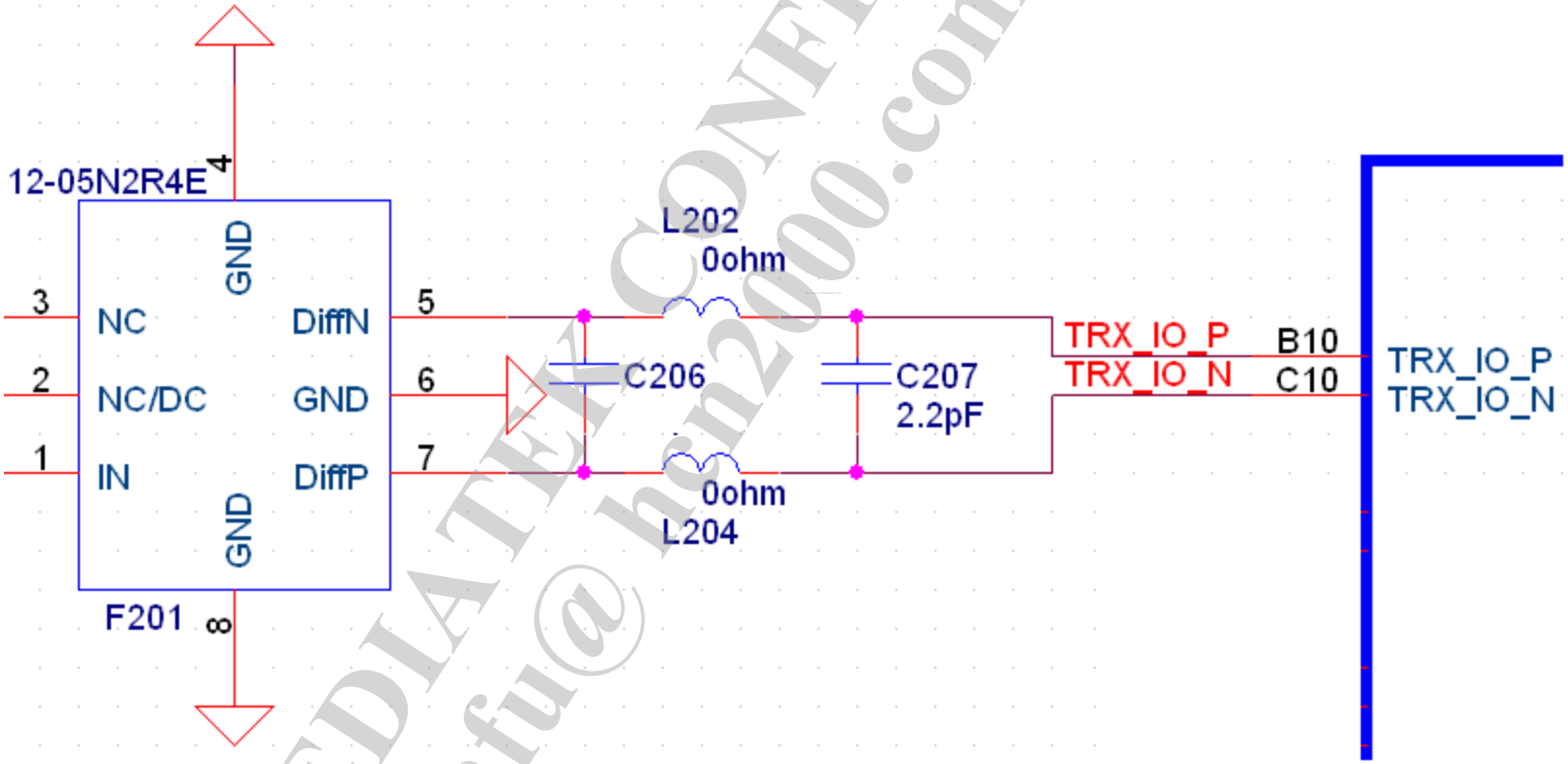
ANTSEL_0	ANTSEL_1	RF path
High	Low	ANT-WiFi_RF
Low	High	ANT-BT_RF

Outline

- MT5931 Block diagram and features
- MT5931 Schematic Design
  - Interface mode selection
  - Interface IO voltage domain setting
  - Interface connection (FP and SP)
  - System GPIO signals connection
  - WIFI BT co-existence signal connection (FP and SP)
  - System Power source connection
- MT5931A TFBGA Layout Guide
  - RF trace
  - Clock trace
  - Power trace
  - GND trace
- MT5931 WIFI BT Single Antenna Structure
- MT5931 RF Matching Skill

MT5931 Differential Matching topology

1. Different IC package or PCB may lead to different topologies.
2. Use RF Psat index to get the optimized point.



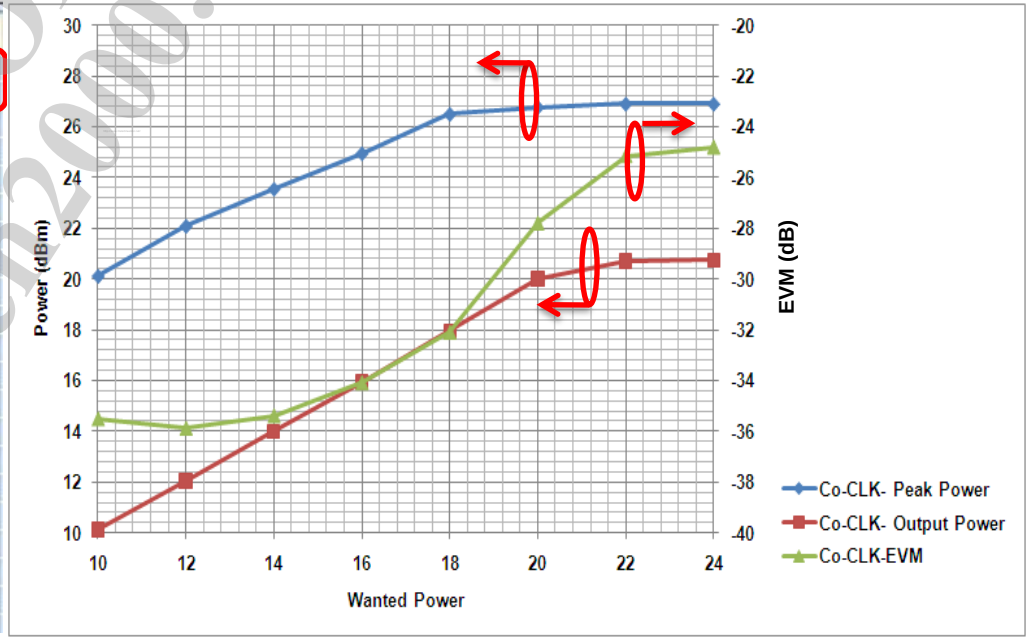
How to get Psat?

1. DUT set wanted power and then use WLAN tester to check peak power level.
2. Adjust wanted power rising and let peak power into saturation.
3. The saturated peak power level is the Psat level.
4. MT5931 target Psat is 26~27dBm level.

Output

Result Averaging 10

	Current	Average(10)	Maximum	Minimum	Unit
Peak Power	26.38	26.48	26.82	-12.70	dBm
Avg. Power (all)	16.09	16.10	16.97	-17.88	dBm
Avg. Power (no gap)	17.41	17.41	18.29	-16.60	dBm
EVM All	-32.47	-32.66	-31.06	-33.46	dB
	2.38	2.33	2.80	0.00	%
EVM Data	-32.40	-32.66	-30.92	-33.47	dB
	2.40	2.33	2.85	0.00	%
EVM Pilots	-33.53	-32.94	-31.48	-33.53	dB
	2.11	2.32	2.67	0.00	%
Amplitude Imb.	-0.02	-0.05	0.05	-0.09	dB
Phase Imb.	0.53	0.67	0.97	-0.07	deg
Freq. Error	-25.69	-25.36	-24.71	-27.57	kHz
Sym. Clock	-9.68	-10.37	-9.33	-12.56	ppm
RMS Phase Error	0.60	0.50	0.68	0.33	deg
Data Rate	54				M...
Number of Symbols	38				
Num. PSDU	1020				Byte
Coding Rate	0.75				
PSDU CRC	passed				



Check List table

Step	Check Item	Request	Unit
1	TX Psat request	26~27	dB
2	TX chip out avg. power at CCK 1M	21	dBm
3	TX EVM at OFDM 54M chip out 18dBm	<-30	dB
4	TX PA current at CCK 1M Chip out 21dBm	~160	mA
5	TX spectrum mask margin at CCK 1M Chip out 21dBm	>3	dB
6	TX 2nd harmonic at CCK 1M Chip out 21dBm	<-40	dB
7	RX sensitivity CCK 1M chip in -98.5dBm	+/-0.5	dB
8	RX sensitivity OFDM 54M chip in -77.5dBm	+/-0.5	dB
9	TX OFDM 54M target power channel variation	<0.5	dB
10	RX chip in sensitivity OFDM 54M channel variation	<0.5	dB

Note: All value means MT5931 chip in/out point , not Antenna port.

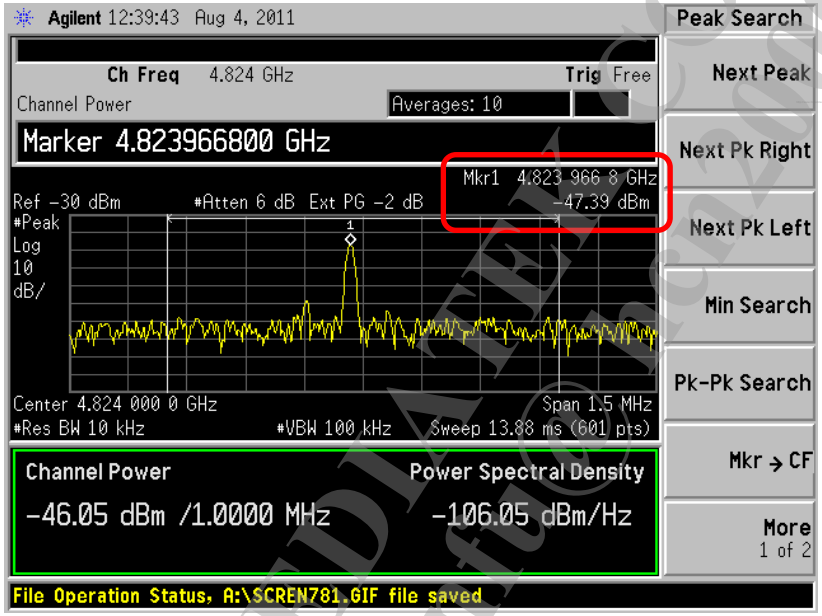
Example

C206+C207: Our target Psat is 26~27dBm, PA current @21dBm is around 160mA.

C206	C207	Psat	PA current (@Psat)	PA current (@21dBm)
1.8pF	1.2pF	26.025	337	
1.5pF	1.2pF	25.94	338	175
1.5pF	1.8pF	25.93	324	164
2.2pF	1.8pF	26.3	331	160
2.2pF	2.2pF	25.8	321	164
2.4pF	1.8pF	26.3	331	160
2.7pF	1.8pF	26.5	330	160
3.3pF	1.8pF	26.69	330	161
3.6pF	1.8pF	26.69	330	160
3.9pF	1.8pF	26.67	325	160
4.3pF	1.8pF	26.52	316	155

TRX performance check

- After re-fine matching component value
  - Check RX chip in sensitivity performance
  - Check TX 2nd harmonic level



2nd harmonic Target: <-40dBm

Outline

- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
- META Tool Usage
- ATE Setting

MT5931 DWS Setting

- MT6236 DWS Setting Example
  - Must Configure EINT0 as below setting in EINT and GPIO page !!

GPIO Setting | GPO Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting

	EINT Var	Debounce Time (10ms)	UEM EINT Str
EINT0	WIFI_EINT_NO	25	WIFI EINT
EINT1	NC	0	
EINT2	NC	0	
EINT3	NC	0	
EINT4	NC	0	

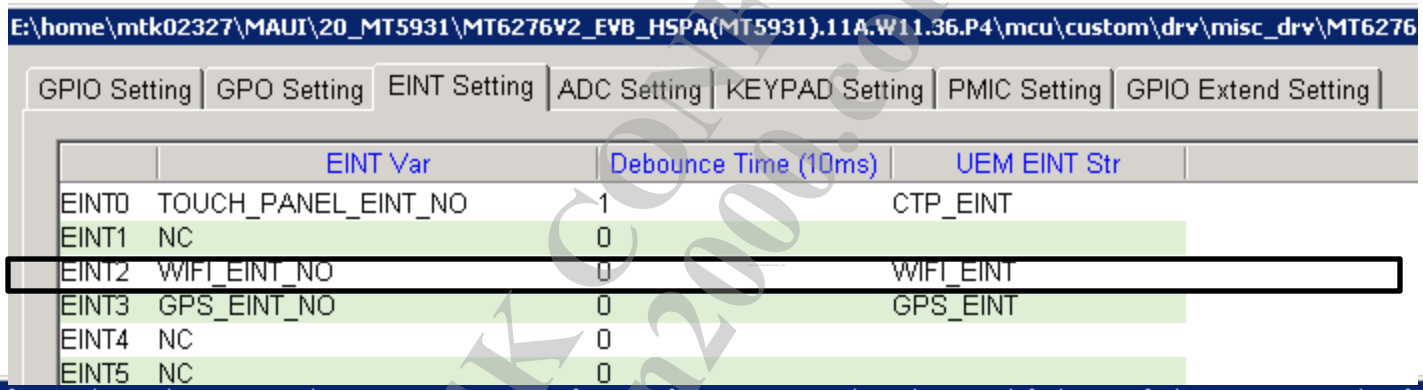
GPIO Setting | GPO Setting | EINT Setting | ADC Setting | KEYPAD Setting | PMIC Setting

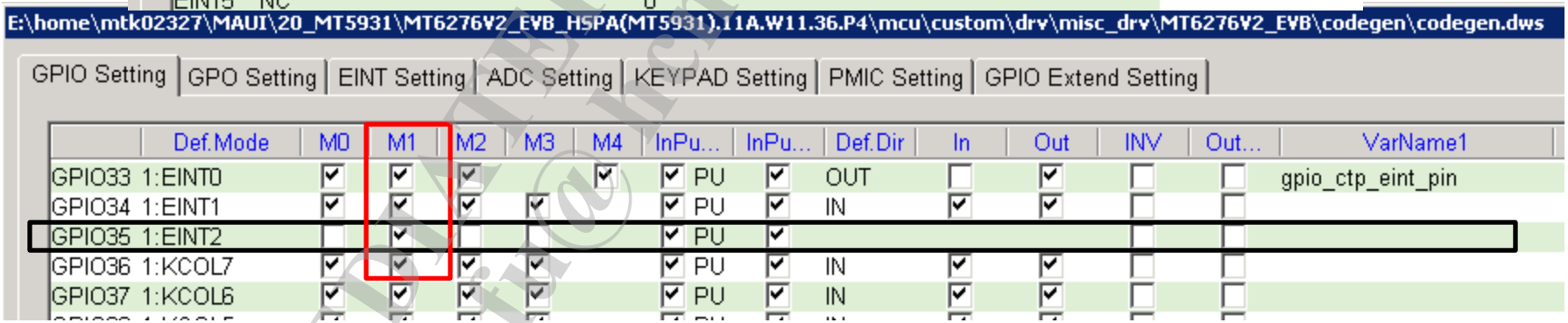
	Def.Mode	M0	M1	M2	M3	InPu...	InPu...	Def.Dir	In	Out	INV	Out...
GPIO39	1:URXD3	✔	✔	✔	✔	PU		IN	✔	✔		
GPIO40	0:GPIO40	✔	✔	✔	✔	PU		OUT	✔	✔		
GPIO41	1:EINT0		✔			✔ PU	✔					
GPIO42	1:EINT1	✔		✔	✔	PU		OUT	✔	✔		
GPIO43	0:GPIO43	✔	✔	✔	✔	PU		OUT	✔	✔		

Select “M1“ EINT0 function only !!

MT5931 DWS Setting

- MT6276 DWS Setting Example
  - Use EINT2 as below setting in EINT and GPIO page.





Select “M1“ EINT2 function only !!

MT5931 DWS Setting

- DWS Setting
  - Please configure setting as below.

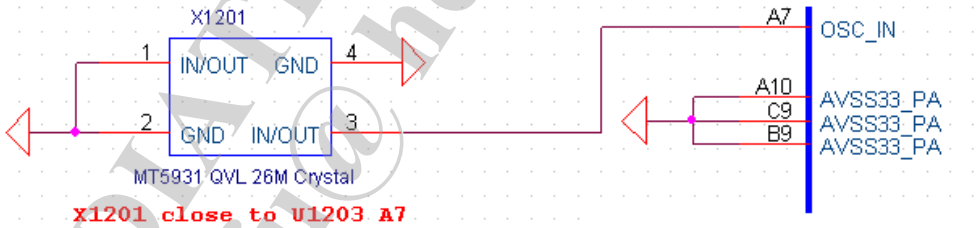
	Def.Mode	M0	M1	M2	M3	InPu...	InPu...	Def.Dir	In	Out	INV	Out...	VarName1
GPIO39	1:URXD3	✓	✓	✓	✓		PU	IN	✓	✓			
GPIO40	0:GPIO40	✓	✓	✓	✓		PU	OUT		✓			gpio_wifi_enable_pin
GPIO41	1:EINT0		✓			✓	PU						
GPIO42	1:EINT1	✓	✓	✓	✓		PU	OUT	✓	✓			
GPIO43	0:GPIO43	✓	✓	✓	✓		PU	OUT		✓		✓	gpio_wifi_ext_rst_pin
GPIO17	2:CLKM1	✓	✓	✓	✓		PD	OUT		✓			gpio_wifi_32k_pin

Outline

- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
  - Please visit MTK BBS site for newest QVL !!
  - WCPBBS > Shared Documents > Parts_Qualification_Lists > Wi-Fi
- META Tool Usage
- ATE Setting

MT5931 26MHz Crystal QVL -1

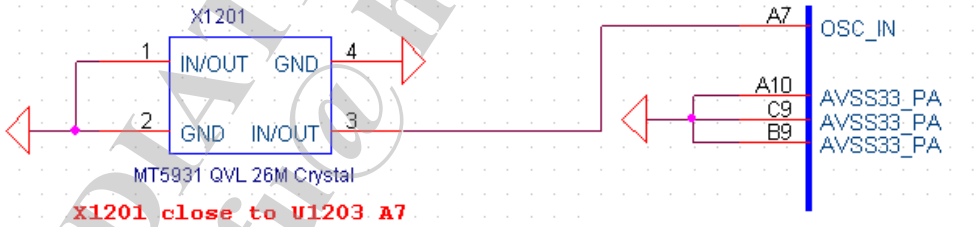
	台灣嘉碩	加高電子	希華晶體	台灣晶技
Part No	TZ2300A	X2B026000B71HZ	XTL581100-M118-051	8Z26090001
Frequency Tolerance	-7ppm ~ +7ppm	-7ppm ~ +7ppm	-7ppm ~ +7ppm	-10ppm ~ +3ppm
Load capacitance	11.5pF	11.5pF	11pF	11pF
Size	2.5*2.0mm	2.5*2.0mm	2.5*2.0mm	2.5*2.0mm
MP Capability /Month	5M	5M	5M	5M
Lead time	4 weeks	4~6 weeks	4 weeks	4 weeks



Note : Use crystal pin3 as clock pad

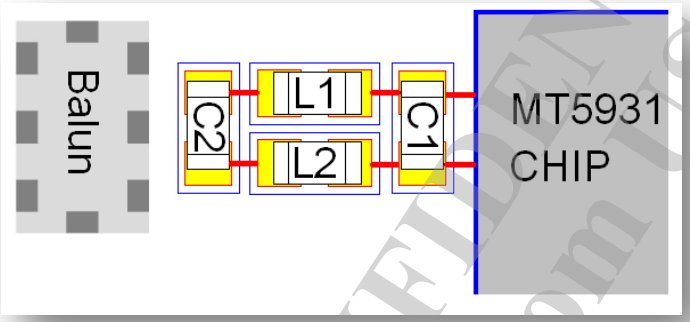
MT5931 26MHz Crystal QVL -2

	鴻星電子	安碁科技		
Part No	E2SB26.0000F11EG1M	CXA-026000-2F8F44		
Frequency Tolerance	-7ppm ~ +7ppm	-7ppm ~ +7ppm		
Load capacitance	11.5PF	10.5PF		
Size	2.5*2.0mm	2.5*2.0mm		
MP Capability /Month	2~3 M	6M		
Lead time	3~4 weeks	4 ~ 5 weeks		



Note : Use crystal pin3 as clock pad

MT5931 Balance Filter QVL



		璟德電子	華新科技	TDK(日)
		ACX	PSA	TDK
Part number		FB2012-05N2R4G	RFBPB2012090AM1T59	DEA202450BT-7116E1
Matching	C1	0402 / **2.2pF**	0402 / **2.2pF**	0402 / **1.8pF**
	C2	NC	NC	NC
	L1	0402/ 0R	0402/ 0R	0402/ 0R
	L2	0402/ 0R	0402/ 0R	0402/ 0R
MP Capability /Month		15M	10M	20M
Lead time		6~8 weeks	4 weeks	6~8 weeks

Note: Please reserve C1/C2/L1/L2 component for matching purpose

WIFI BT Single Antenna QVL

Component	Pin-to-Pin	Part Number	Package	Manufacturer	Lead Time
50 ohm SPDT Chip (Note)	Yes	M508 (50ohm terminated)	SOT-363	HEXAWAVE	4~6 weeks
		uPG2418TB (50ohm terminated)		NEC	4~6 weeks
Coupler	Yes	CP1608-10A2450	1608	ACX	4~6 weeks
		LTC-1608-2G4S1		Mag.Layers	4~6 weeks

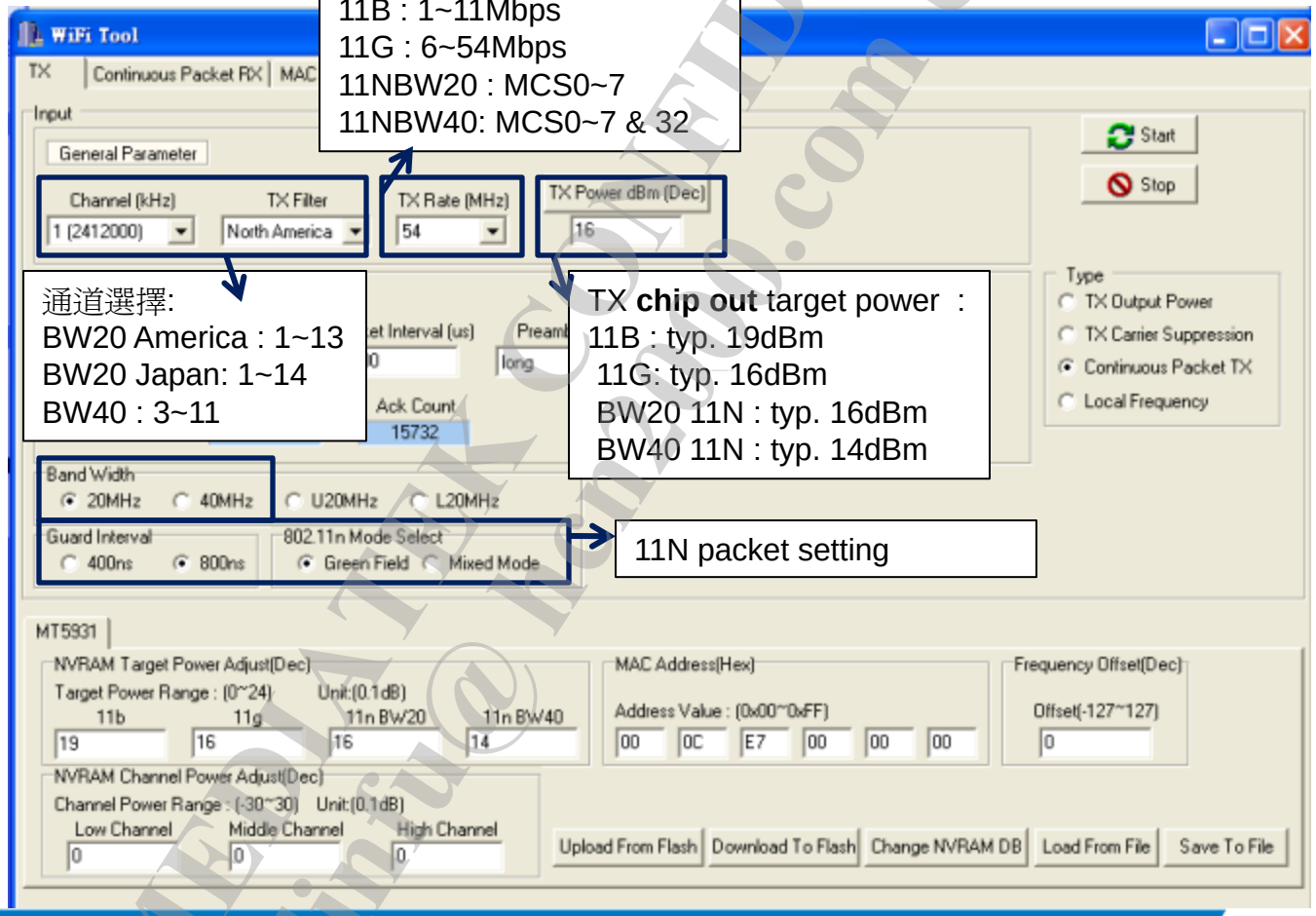
Note : Switch is special 50 ohm terminated component. For single-antenna designs, please follow MTK reference design schematic

Outline

- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
- META Tool Usage
  - Version W1146~
- ATE Setting

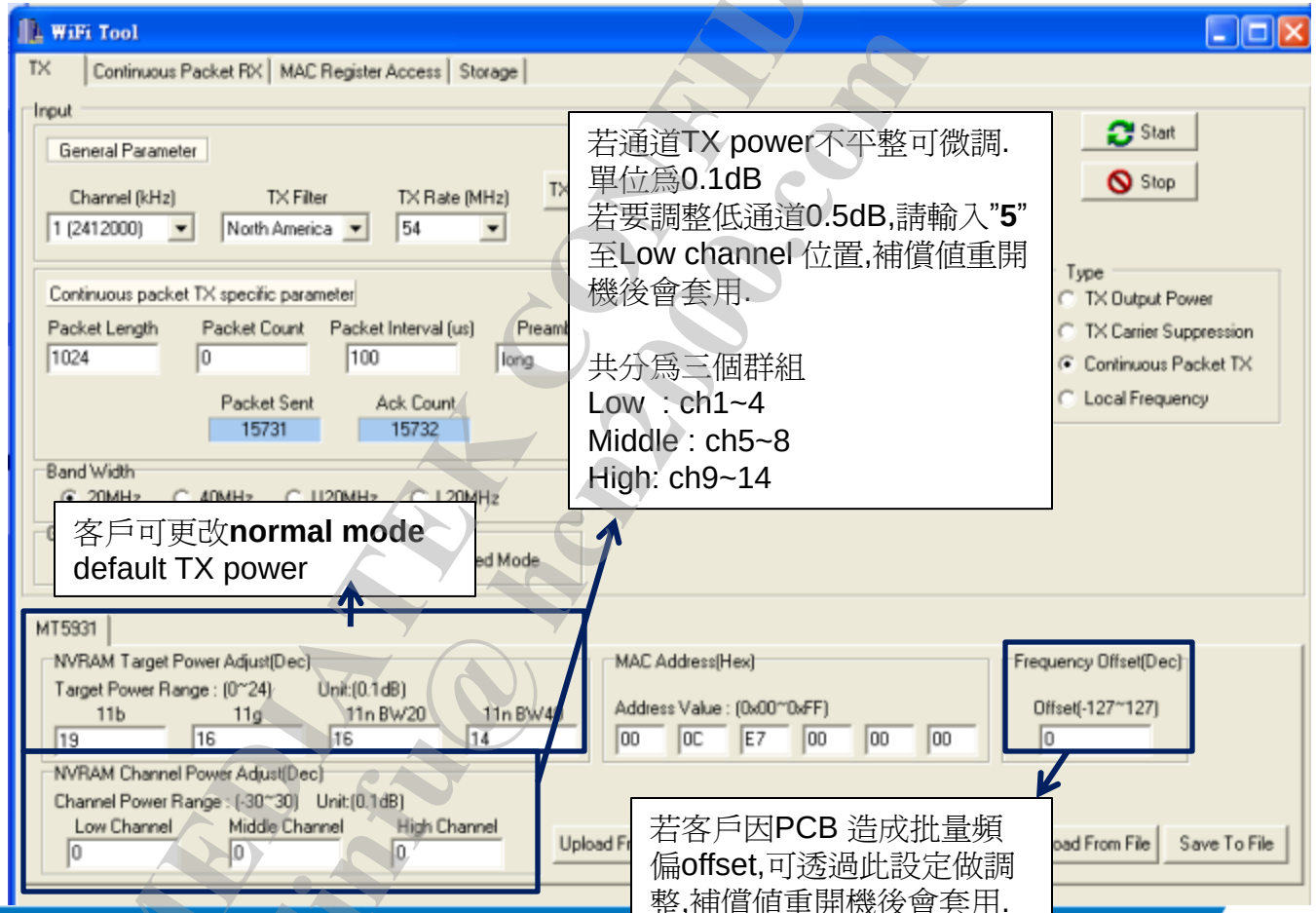
META Tool Usage

- TX page



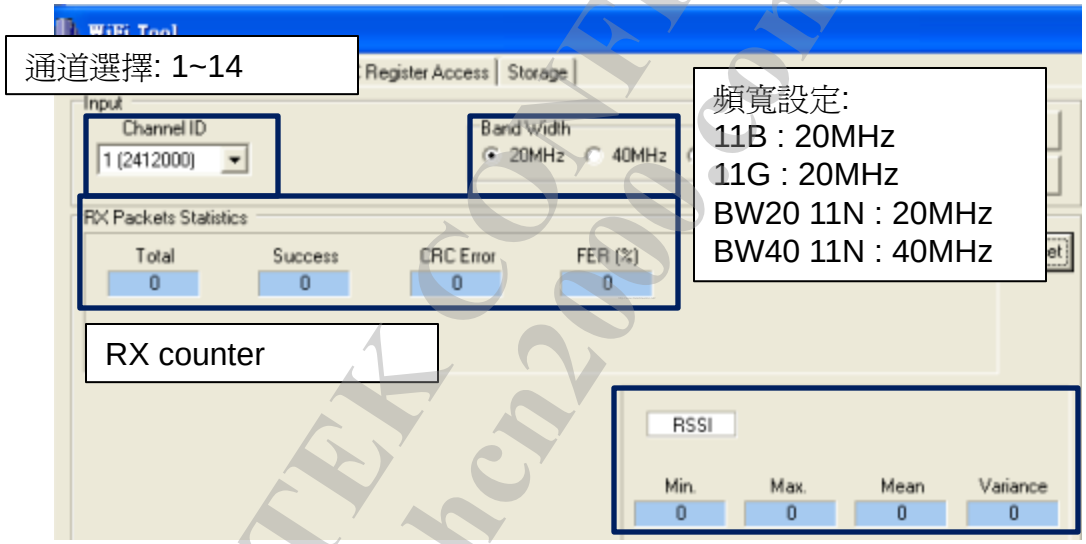
META Tool Usage

- TX page



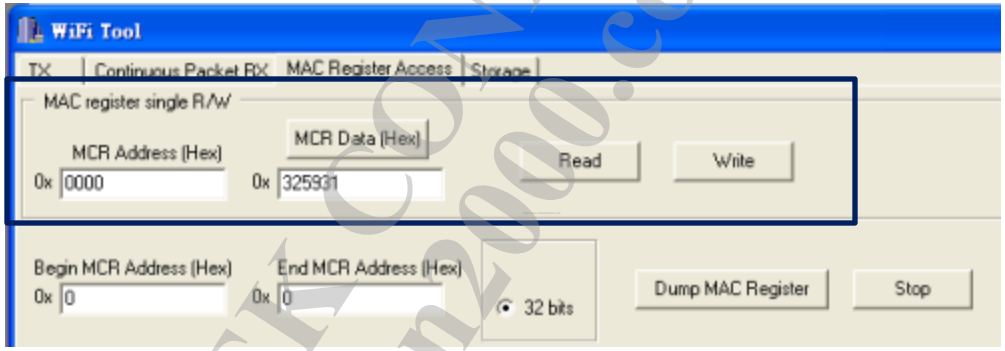
META Tool Usage

- RX page



META Tool Usage

- MCR page for debug usage



Outline

- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
- META Tool Usage
- ATE Setting
- WIFI MAC address

ATE Setting

- MT5931 supports internal TX power calibration so MP line could reduce test time.
- Suggest ATE Test item :
  - Select “RF check“ bottom and it contains
  - TX performance test
    - EVM
    - Mask
    - Frequency error
    - Central frequency leakage
  - RX performance test
    - Sensitivity

ATE CFG File Setting

- MT5931 ATE CFG setting
  - [WiFi common]
    - WiFi_Support = 0x06 ➔ Suggest to use 11g setting
  - [WiFi TX power table]
    - CCK_MAX_P = 18 -> This means antenna port power and suffers 2.5dB BPF loss.
    - CCK_WANTED_P = 19 -> This mean chip out power
    - CCK_MIN_P = 15 -> This means antenna port power and suffers 2.5dB BPF loss.
    - CCK_C = 2
    - CCK_Delta = 0.5
    - 802.11B_CAL_CHANNEL = 2412,2442,2472, => don't use 2484 to test 11B
    - 802.11B_CHECK_CHANNEL = 2412,2442,2472, => don't use 2484 to test 11B
    - CCK_CAL_RATE = 11
    - CCK_CHECK_RATE = 11
    - OFDM_MAX_P = 15 -> This means antenna port power and suffers 2.5dB BPF loss.
    - OFDM_WANTED_P = 16 →This mean chip out power
    - OFDM_MIN_P = 12 -> This means antenna port power and suffers 2.5dB BPF loss.
    - OFDM_C = 2
    - OFDM_Delta = 0.5
    - 802.11G_CAL_CHANNEL = 2412,2442,2472,
    - 802.11G_CHECK_CHANNEL = 2412,2442,2472,
    - OFDM_CAL_RATE = 54
    - OFDM_CHECK_RATE = 54

Outline

- DWS Setting
  - EINT setting
  - Other setting
- QVL Status
- META Tool Usage
- ATE Setting
- WIFI MAC address

WiFi IEEE MAC Address Application

- 爲何需要申請MAC address ?
  - MAC address又稱MAC位址、硬體位址，用來定義網路設備的位置,若出現與別人MAC address重複的現象，AP(熱點)也許會認爲被攻擊,因此出現無預警的斷線或是導致網路裝置錯失大量封包，導致難以追查的問題， 因此MAC address必須具有唯一性，不可重複。
- MAC位址定義
  - 共48位元（6個位元組），以十六進位表示。
  - 高24位元由貴司與IEEE組織申請，低24位元由貴司實際生產時自行產生。
  - 舉例來說: 假設貴司申請到的IEEE OUI是0x00-0x01-0x02 ，貴司可以使用0x00-0x01-0x02-XX-YY-ZZ當作完整MAC address，只要生產時能確定產品XX-YY-ZZ流水號具惟一性，則此MAC address一定不會發生與他人MAC address產生衝突問題，進而可避免導致網路功能異常。
- 適用對象
  - 任何有WiFi產品生產之公司.
- 寫入方式
  - WiFi CoB客戶：請利用MTK SN writer tool.
  - WiFi module客戶：請利用ATE “EEPROM copy" function.

WiFi IEEE MAC Address Application

- 申請步驟
  - http://standards.ieee.org/regauth/oui/forms/
    - 1.填寫線上表單
    - https://standards.ieee.org/cgi-bin/wtp/request?rt=OUI
    - 2.繳費
    - 選擇 (支票/ 匯款/ 採購單/ 信用卡)
    - 3.費用
    - Publicly Registered OUI (company name and address on the public listing)費用爲$1,650.00(US) ; 相當於一組OUI費用爲美金USD $1,650，每組OUI可有256*256*256 = 16777216個address。相當於一塊美金就可以擁有壹萬個MAC address.
  - 完成繳費後,七日內可透過電郵收到IEEE指派給貴司之OUI號碼.
  - 其他相關資訊可至下列網站查找.
  - http://standards.ieee.org/regauth/oui/index.shtml

MTK SN Writer Tool 可支援Write MAC Address功能