

SRAM

128K x 8 SRAM

WITH OUTPUT ENABLE

5 VOLT SRAM

FEATURES

- High speed: 12, 15, 17, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and \overline{OE} options
- All inputs and outputs are TTL-compatible
- Fast \overline{OE} access time: 8ns

OPTIONS

- Timing

12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
35ns access	-35
- Packages

Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Plastic SOJ (300 mil)	SJ
- 2V data retention L
- 2V data retention, low power LP
- Temperature

Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

MARKING

- Part Number Example: MT5C1008DJ-25 LP

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

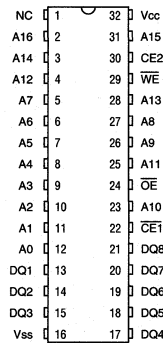
GENERAL DESCRIPTION

The MT5C1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

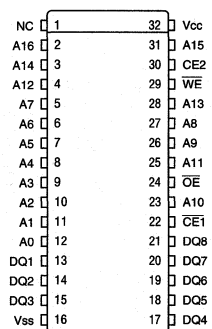
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable (\overline{OE}). This enhancement can place the outputs in High-Z for additional flexibility in system design.

PIN ASSIGNMENT (Top View)

32-Pin DIP (SA-6)



32-Pin SOJ (SD-4, SD-5)



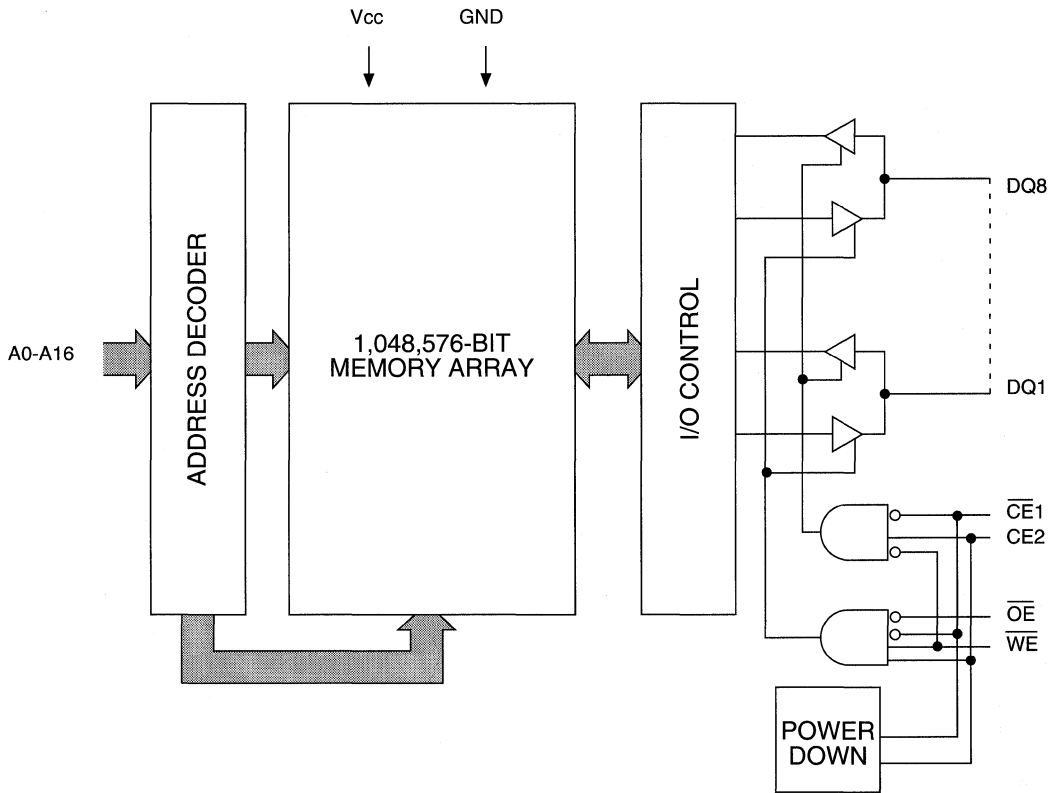
Writing to these devices is accomplished when write enable (\overline{WE}) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when \overline{WE} and CE2 remain HIGH and $\overline{CE1}$ and \overline{OE} go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the \overline{WE} , \overline{OE} and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM

5 VOLT SRAM



TRUTH TABLE

MODE	\overline{OE}	$\overline{CE1}$	$\overline{CE2}$	\overline{WE}	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Storage Temperature (plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA
 Voltage on Any Pin Relative to Vss -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{cc} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{cc} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{cc}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{cc}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{cc}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-12	-15	-17	-20	-25	-35		
Power Supply Current: Operating	CE2 ≥ V _{IH} ; $\overline{CE1} \leq V_{IL}$; V _{cc} = MAX f = MAX = 1/ t _{RC} outputs open	I _{cc}	95	190	165	155	140	125	115	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V _{IH} or $\overline{CE1} \geq V_{IH}$; V _{cc} = MAX f = MAX = 1/ t _{RC} outputs open	I _{SB1}	17	45	40	40	35	30	25	mA	13
	LP version only	I _{SB1}	1.3	3	3	3	3	3	3	mA	13
	CE2 ≤ V _{ss} +0.2V; $\overline{CE1} \geq V_{cc} -0.2V$; V _{cc} = MAX V _{IN} ≤ V _{ss} +0.2V or V _{IN} ≥ V _{cc} -0.2V; f = 0	I _{SB2}	0.4	5	5	5	5	5	5	mA	13
	L and LP versions only	I _{SB2}	0.3	1.5	1.5	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1 MHz V _{cc} = 5V	C _i	8	pF	4
Output Capacitance		C _o	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

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DESCRIPTION	SYM	-12		-15		-17		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	^t RC	12		15		17		20		25		35		ns	
Address access time	^t AA		12		15		17		20		25		35	ns	
Chip Enable access time	^t ACE		12		15		17		20		25		35	ns	
Output hold from address change	^t OH	3		3		3		3		5		5		ns	
Chip Enable to output in Low-Z	^t LZCE	3		5		5		5		5		5		ns	7
Chip disable to output in High-Z	^t HZCE		5		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^t PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^t PD		12		15		17		20		25		35	ns	
Output Enable access time	^t AOE		4		5		5		6		8		12	ns	
Output Enable to output in Low-Z	^t LZOE	0		0		0		0		0		0		ns	
Output disable to output in High-Z	^t HZOE		4		5		5		6		10		12	ns	6
WRITE Cycle															
WRITE cycle time	^t WC	12		15		17		20		25		35		ns	
Chip Enable to end of write	^t CW	8		10		12		12		15		20		ns	
Address valid to end of write	^t AW	8		10		12		12		15		20		ns	
Address setup time	^t AS	0		0		0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		0		0		ns	
WRITE pulse width	^t WP1	8		9		12		12		15		20		ns	
WRITE pulse width	^t WP2	10		12		13		15		15		20		ns	
Data setup time	^t DS	6		7		8		8		10		15		ns	
Data hold time	^t DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^t LZWE	3		3		3		3		3		3		ns	7
Write Enable to output in High-Z	^t HZWE		5		6		7		8		10		15	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1008 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

5 VOLT SRAM

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX				UNITS	NOTES
				-20	-25	-35	-45		
Power Supply Current: Operating	CE2 ≥ V _{IH} ; $\overline{CE1} \leq V_{IL}$; V _{CC} = MAX f = MAX = 1/τ _{RC} outputs open	I _{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V _{IH} or $\overline{CE1} \geq V_{IH}$; V _{CC} = MAX f = MAX = 1/τ _{RC} outputs open	I _{SB1}	17	35	30	25	25	mA	13
	CE2 ≤ V _{SS} + 0.2V; $\overline{CE1} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.4	5	5	5	5	mA	13
L version only	CE2 ≤ V _{SS} + 0.2V; $\overline{CE1} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Data Retention Current	CE1 ≥ (V _{CC} - 0.2V) or CE2 ≤ (V _{SS} + 0.2V) V _{IN} ≥ (V _{CC} - 0.2V) or ≤ 0.2V	V _{CC} = 2V	I _{CCDR}		35	170	μA	14
		V _{CC} = 3V	I _{CCDR}		60	325	μA	14

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1008 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX				UNITS	NOTES
				-20	-25	-35	-45		
Power Supply Current: Operating	CE2 ≥ V _{IH} ; $\overline{CE1} \leq V_{IL}$; V _{CC} = MAX f = MAX = 1/4RC outputs open	I _{CC}	95	150	135	125	120	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V _{IH} or $\overline{CE1} \geq V_{IH}$; V _{CC} = MAX f = MAX = 1/4RC outputs open	I _{SB1}	17	45	40	35	32	mA	13
	CE2 ≤ V _{SS} + 0.2V; $\overline{CE1} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V _{SS} + 0.2V; $\overline{CE1} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
Data Retention Current	$\overline{CE1} \geq (V_{CC} - 0.2V)$ or CE2 ≤ (V _{SS} + 0.2V) V _{IN} ≥ (V _{CC} - 0.2V) or ≤ 0.2V	V _{CC} = 2V	I _{CCDR}		35	1,000	μA	14
		V _{CC} = 3V	I _{CCDR}		60	1,500	μA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.

(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION	SYM	-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
Output hold from address change	t _{OH}	3		3		3		3		ns	
Chip Enable to output in Low-Z	t _{LZCE}	3		3		3		3		ns	7

AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

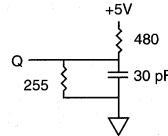


Fig. 1 OUTPUT LOAD EQUIVALENT

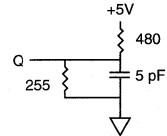


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

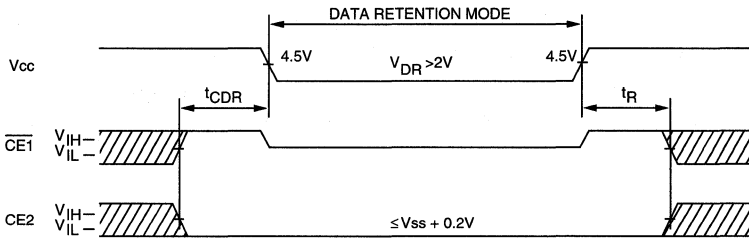
- All voltages referenced to V_{SS} (GND).
- 3V for pulse width < t_{RC}/2.
- I_{CC} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
- \overline{WE} is HIGH for READ cycle.
- Device is continuously selected. All chip enables and output enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC} = Read Cycle Time.
- CE2 timing is the same as $\overline{CE1}$ timing. The waveform is inverted.
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 5V, 25°C and 25ns cycle time.
- Typical currents are measured at 25°C.
- Output enable (\overline{OE}) is inactive (HIGH).
- Output enable (\overline{OE}) is active (LOW).

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

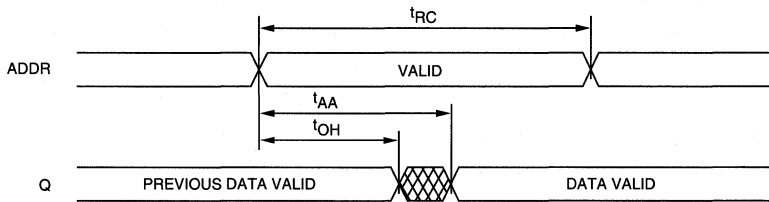
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
V _{CC} for Retention Data		V _{DR}	2			V		
Data Retention Current L version	$\overline{CE1} \geq (V_{CC} - 0.2V)$ or $CE2 \leq (V_{SS} + 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V _{CC} = 2V	I _{CCDR}		35	150	μA	15
		V _{CC} = 3V	I _{CCDR}		60	250	μA	15
		V _{CC} = 3V*	I _{CCDR}		30	100	μA	15
Data Retention Current LP version	$\overline{CE1} \geq (V_{CC} - 0.2V)$ or $CE2 \leq (V_{SS} + 0.2V)$	V _{CC} = 2V	I _{CCDR}		35	150	μA	15
		V _{CC} = 3V	I _{CCDR}		60	250	μA	15
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4	
Operation Recovery Time		t _R	t _{RC}			ns	4, 11	

*Advance

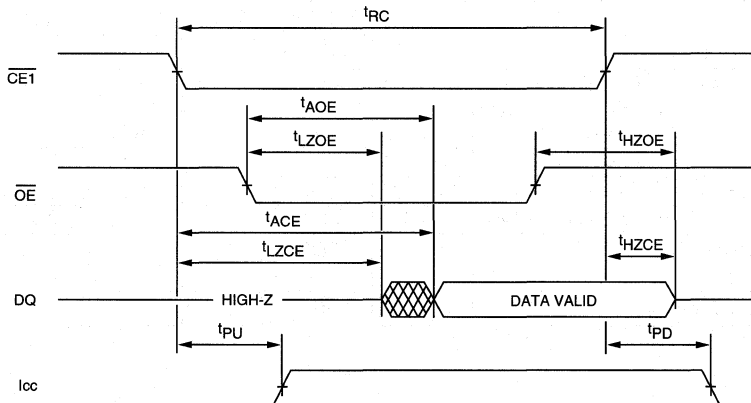
LOW V_{CC} DATA RETENTION WAVEFORM





READ CYCLE NO. 1 8, 9

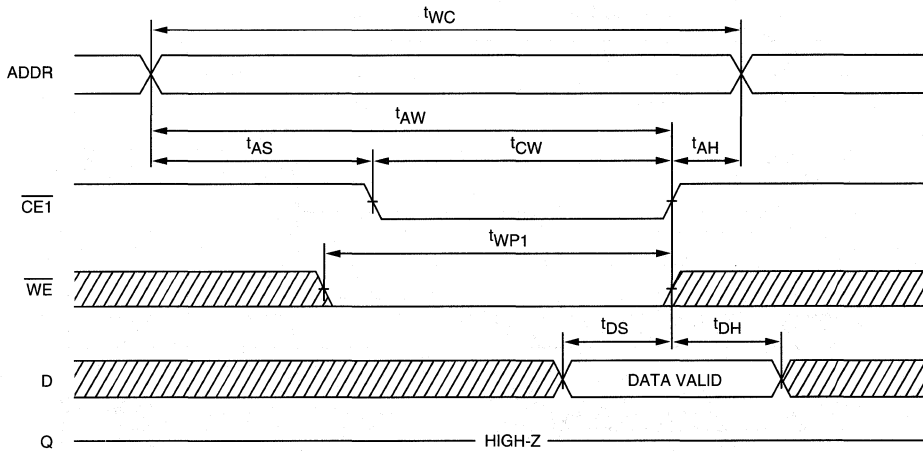


READ CYCLE NO. 2 7, 8, 10, 12

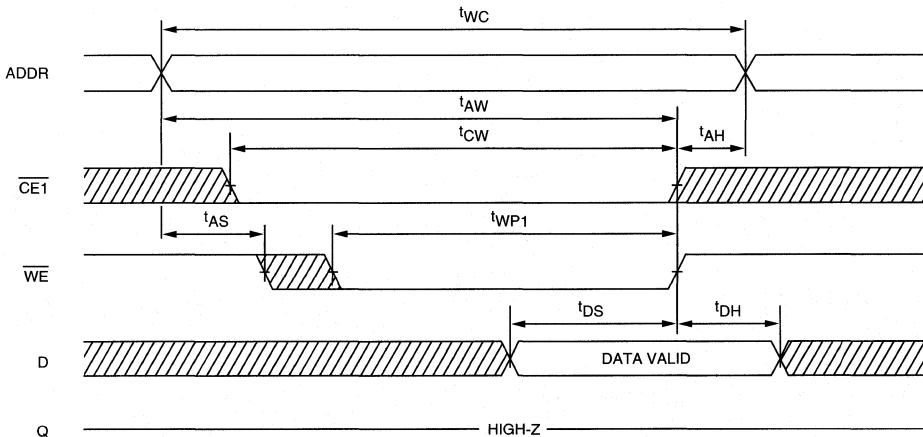




 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 1 ¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2 ^{12, 13, 16}
(Write Enable Controlled)



 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 3 7, 12, 13, 17
(Write Enable Controlled)

