SRAM DIE

1 MEG SRAM

128K x 8, 64K x 16

FEATURES

- Single +3.3V or +5V power supply
- 5V tolerant I/O
- Individual byte controls for both READ and WRITE cycles
- High-performance, low-power, CMOS double-metal process
- All inputs and outputs are TTL-compatible

GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 18.5 mils ±0.5 mils
- Backside wafer surface of polished bare silicon
- Typical metalization thickness 10K angstroms for the top level of metalization
- Typical lower-level metal thickness is 5.5K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over titanium
- Typical topside passivation 6K angstroms phosphorous doped oxide with 6K angstroms of nitride over oxide
- Typical passivation openings: 5.1 x 5.1 mil
  130 x 130 µm

OPTIONS — ORDER NUMBER

• Speed probing*	3.3V	5V
No speed probing	none	none
12ns access	n/a	-12÷
15ns access	-15÷	-15÷
20ns access	-20÷	-20
25ns access	-25	n/a

• Form	
Die	D
Wafer (6" wafer)	W

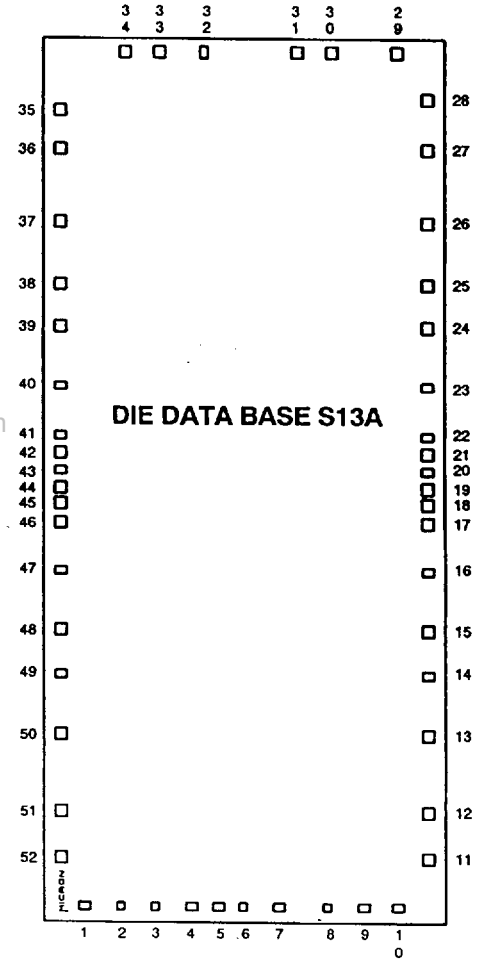
• Testing levels**	
Standard probe	C1
Speed probe	C2

*Refer to "Speed Probing" section of this data sheet. Speed designator should not be included in die part number for C1 level product.
**Refer to "Die Testing Procedures" section of this data sheet.
÷Available as C2 level product only.

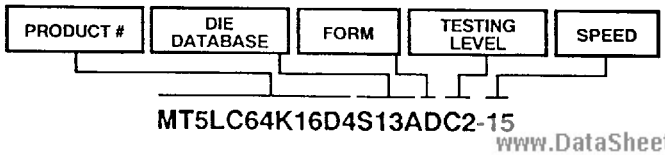
ORDER INFORMATION

• 64K x 16 (+5V)	MT5C64K16A1S13A
• 64K x 16 (+3.3V)	MT5LC64K16D4S13A
• 128K x 8 (+5V)	MT5C128K8A1S13A
• 128K x 8 (+3.3V)	MT5LC128K8D4S13A

DIE OUTLINE (Top View)



Die size: 230 x 501 mil
5,842 x 12,725 µm
See Bond Pad Location and Identification Table.



DIE TESTING PROCEDURES

Micron has established three testing levels for die products. Most Micron products are tested to Standard Probe (C1) level. Selected products are available at Speed Probe (C2) level. Known Good Die (C3) level product is available on selected products as market demand dictates. Level C2 and C3 products are designed to provide customers with improved yields over C1.

STANDARD PROBE (C1)

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C on Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the junction die temperature remains within specified limits. A high voltage functional stress test will be performed at probe to assure minimum junction breakdown integrity. V_{BB} (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield or performance of the product.

SPEED PROBE (C2)

In addition to the testing performed at Standard Probe (C1), Micron also offers Speed Probe (C2). Micron's Hot Chuck Speed Probe assures the speed performance of die products for the fastest speed grades. Although this testing level may increase the yield a customer may see over C1-level, the C2-level die has not received burn-in and therefore is still subject to infant mortality failures.

KNOWN GOOD DIE (C3)

In order to provide the customer with fully warranted die product, Micron has developed a Known Good Die process designed to provide customers with die products of equal quality and reliability to packaged product. Micron's KGD^{Plus}™ process allows Micron to fully test and burn-in die product.

FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets found in the applicable Micron data book, for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2-level product ^{t}AA is guaranteed. C3-level product is warranted to the data sheet.

BONDING INSTRUCTIONS

The S13A SRAM die has 52 bond pads. Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.

The S13A SRAM die has an internal substrate bias generator for normal operation, bond pad 6 is used for manufacturing tests only. Normal bonding leaves bond pad 6 open (not bonded). Micron recommends using a bond wire on each Vcc and Vss bond pad for improved noise immunity. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

The 1 Meg SRAM device operates from a single +5V or 3.3V power supply and all inputs and outputs are fully TTL- compatible.

PACKAGING

For packaging, Micron utilizes Gel-Pak®. We package all die with the top metalization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each package is individually self-locking, or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Ex: 64K16S13A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

STORAGE REQUIREMENTS

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

PRODUCT RELIABILITY MONITORS

Reliability of all products is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations and high temperature steady state (HTSS) tests to monitor electromigration reliability. A summary of these product family evaluations is published on a regular basis.

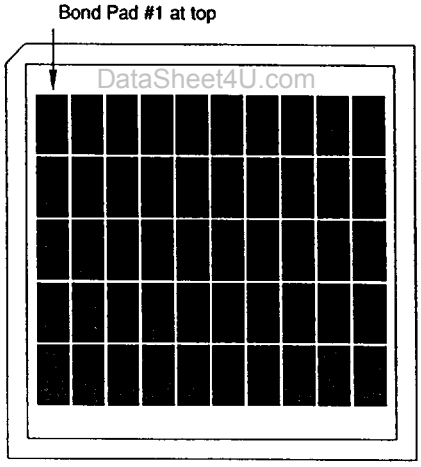


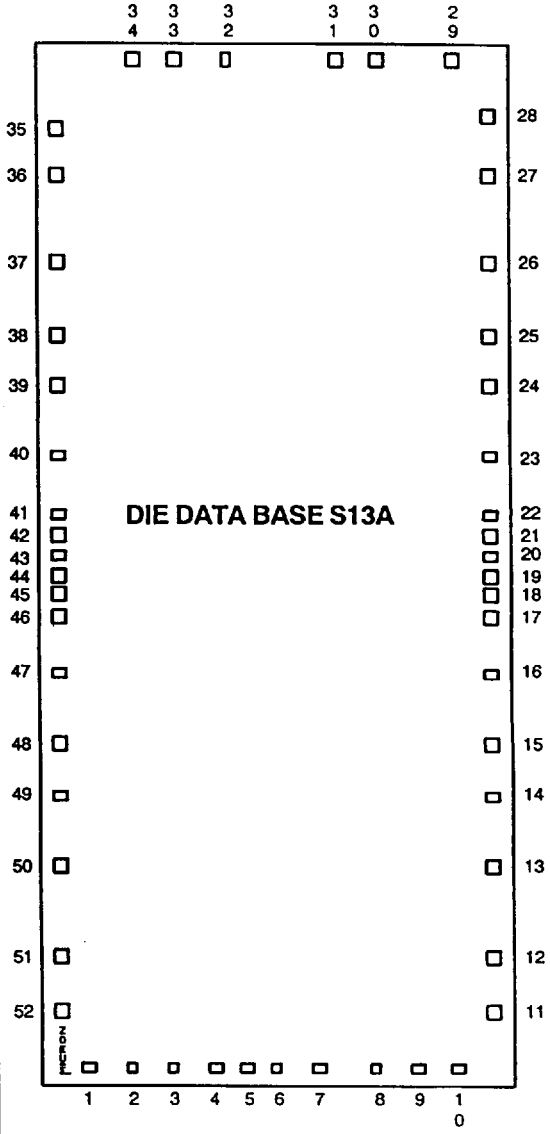
Figure 1
ORIENTATION OF DIE IN GEL-PAK

BOND PAD LOCATION AND IDENTIFICATION TABLE

PAD #	MT5C64K16A1S13A MT5LC64K16D4S13A	MT5C128K8A1S13A MT5LC128K8D4S13A	FROM CENTER OF #1 "X" INCHES	"Y" INCHES	"X" MICRONS	"Y" MICRONS
1	$\overline{OE}$	A7	0.000	0.000	000	000
2	A7	DNU	0.000	-0.020	000	-508
3	A6	A6	0.000	-0.040	000	-1,016
4	A5	A5	0.000	-0.060	000	-1,524
5	DNU*	A4	0.000	-0.075	000	-1,905
6	DNU	DNU	0.000	-0.090	000	-2,286
7	A4	DNU	0.000	-0.110	000	-2,794
8	A3	A3	0.000	-0.138	000	-3,505
9	A2	A2	0.000	-0.158	000	-4,013
10	A1	A1	0.000	-0.178	000	-4,521
11	A0	A0	0.027	-0.196	686	-4,978
12	$\overline{CE}$	$\overline{CE}$	0.054	-0.196	1,372	-4,978
13	DQ1	DNU	0.097	-0.196	2,464	-4,978
14	DQ2	DQ1	0.131	-0.196	3,327	-4,978
15	DQ3	DNU	0.156	-0.196	3,962	-4,978
16	DQ4	DQ2	0.190	-0.196	4,826	-4,978
17	VCC	VCC	0.218	-0.196	5,537	-4,978
18	VCC	VCC	0.228	-0.196	5,791	-4,978
19	VCC	VCC	0.237	-0.196	6,020	-4,978
20	VSS	VSS	0.247	-0.196	6,274	-4,978
21	VSS	VSS	0.257	-0.196	6,528	-4,978
22	VSS	VSS	0.267	-0.196	6,782	-4,978
23	DQ5	DQ3	0.295	-0.196	7,493	-4,978
24	DQ6	DNU	0.329	-0.196	8,357	-4,978
25	DQ7	DQ4	0.354	-0.196	8,992	-4,978
26	DQ8	DNU	0.388	-0.196	9,855	-4,978
27	$\overline{WE}$	$\overline{WE}$	0.430	-0.196	10,922	-4,978
28	DNU	A16	0.458	-0.196	11,633	-4,978
29	A15	A15	0.485	-0.179	12,319	-4,547
30	A14	A14	0.485	-0.142	12,319	-3,607
31	A13	A13	0.485	-0.121	12,319	-3,073
32	A12	A12	0.485	-0.068	12,319	-1,727
33	A11	A11	0.485	-0.043	12,319	-1,092
34	A10	A10	0.485	-0.023	12,319	-584
35	A9	A9	0.458	0.014	11,633	356
36	A8	A8	0.430	0.014	10,922	356
37	DQ9	DNU	0.388	0.014	9,855	356
38	DQ10	DQ5	0.354	0.014	8,992	356
39	DQ11	DNU	0.329	0.014	8,357	356
40	DQ12	DQ6	0.295	0.014	7,493	356
41	VCC	VCC	0.267	0.014	6,782	356
42	VCC	VCC	0.257	0.014	6,528	356
43	VCC	VCC	0.247	0.014	6,274	356
44	VSS	VSS	0.237	0.014	6,020	356
45	VSS	VSS	0.228	0.014	5,791	356
46	VSS	VSS	0.218	0.014	5,537	356
47	DQ13	DQ7	0.190	0.014	4,826	356
48	DQ14	DNU	0.156	0.014	3,962	356
49	DQ15	DQ8	0.131	0.014	3,327	356
50	DQ16	DNU	0.097	0.014	2,464	356
51	$\overline{BLE}$	$\overline{OE}$	0.054	0.014	1,372	356
52	$\overline{BHE}$	DNU	0.027	0.014	686	356

*"DNU" stands for do not use

DIE OUTLINE (Top View)



Wafer diameter: 150mm
Wafer thickness: 18.5 mil ±0.5 mil
Die size: 230 x 501 mil
(stepping interval)
5,842 x 12,725 µm
Bond pad size: 5.8 x 5.8 mil
146 x 146 µm
Passivation Openings (typical): 5.1 x 5.1 mil
130 x 130 µm