SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE,
REVOLUTIONARY PINOUT

FEATURES

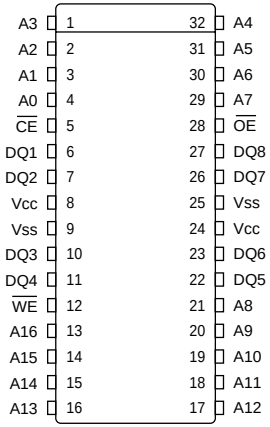
- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Packages
  - 32-pin SOJ (400 mil) — DJ
- Part Number Example: MT5C128K8A1DJ-25 L

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

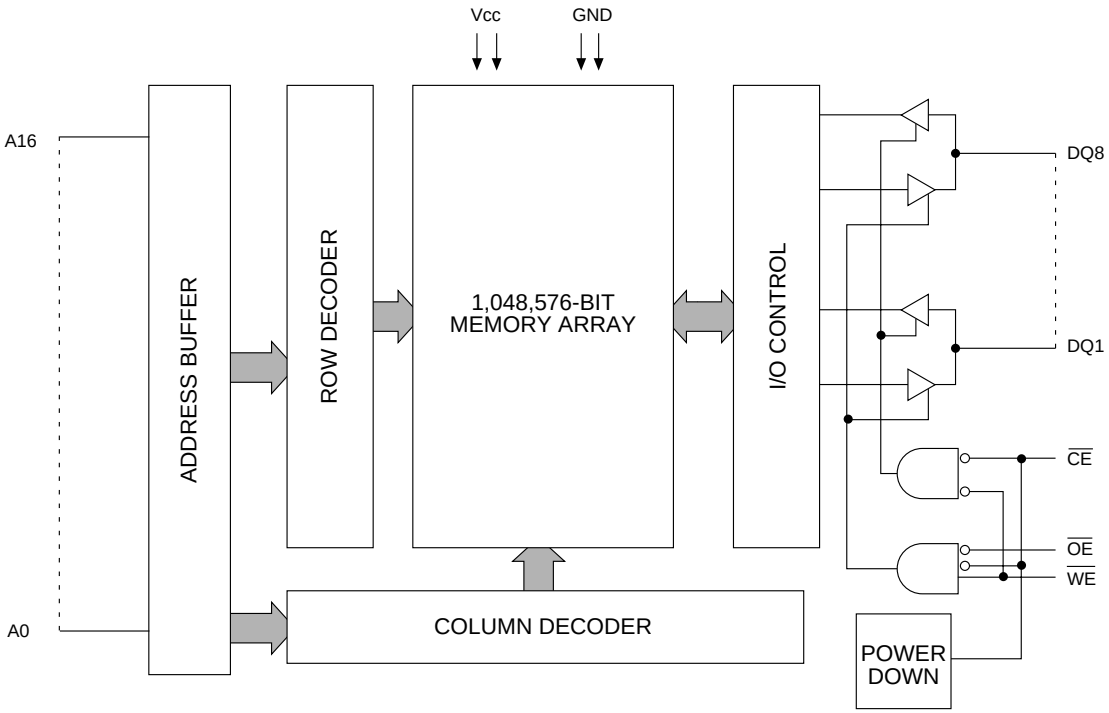
The MT5C128K8A1 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	V_{CC}	Supply	Power Supply: 5V ±10%
9, 25	V_{SS}	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -1V to +7V
Storage Temperature (plastic)..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to Vcc +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	330	280	230	200	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	45	80	70	60	50	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.75	5	5	5	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		14		ns	
WRITE pulse width	$^tWP2$	9		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

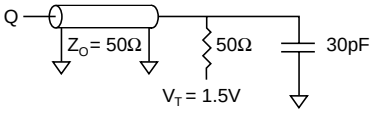


Fig. 1 OUTPUT LOAD EQUIVALENT

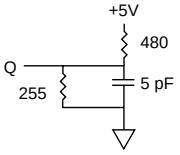


Fig. 2 OUTPUT LOAD EQUIVALENT

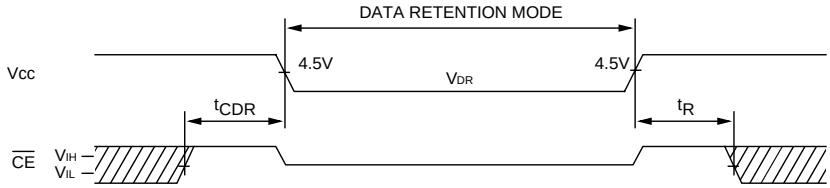
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE, ^tHZOE and ^tHZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical currents are measured at 25°C.
14. Typical values are measured at 25°C, 5V and 15ns cycle time.
15. Contact Micron for extended temperature (IT / AT / XT) timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.

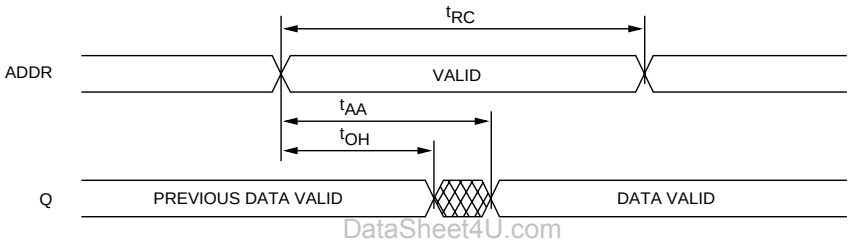
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		70	300	µA	13
		V_{CC} = 3V	I_{CCDR}		175	500	µA	13
Chip Deselect to Data Retention Time			^tCDR	0			ns	4
Operation Recovery Time			^tR	^tRC			ns	4, 11

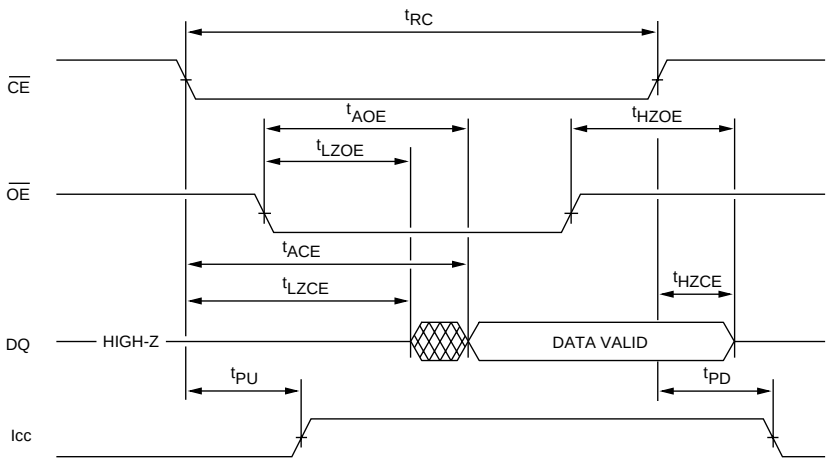
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



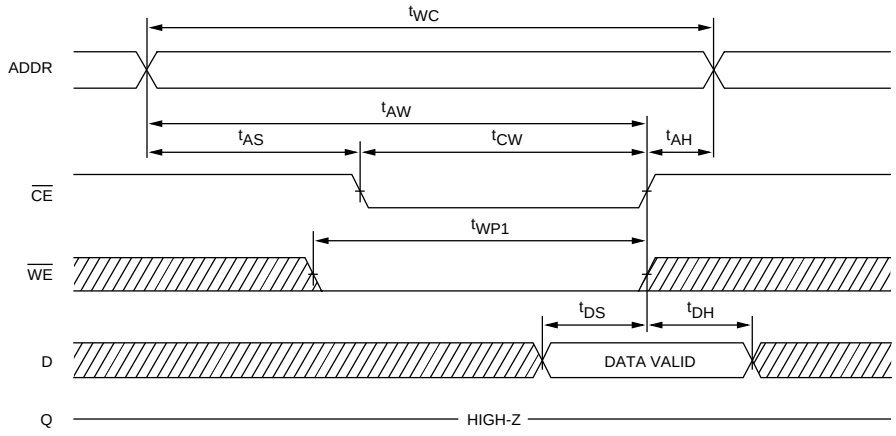
READ CYCLE NO. 2 [7, 8, 10]



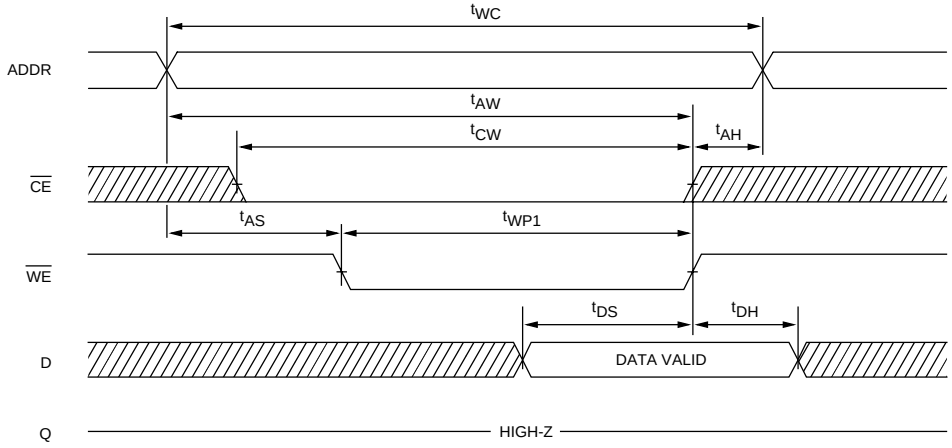
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

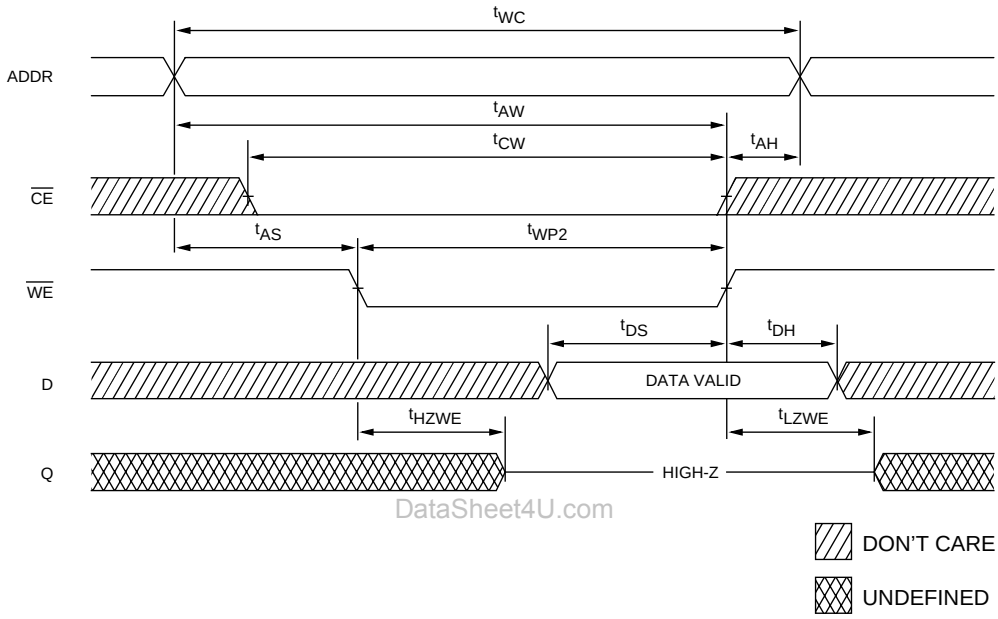


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).