

# SRAM

# 256K x 1 SRAM

**5 VOLT SRAM**

## FEATURES

- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V  $\pm 10\%$  power supply
- Easy memory expansion with  $\overline{CE}$  option
- All inputs and outputs are TTL-compatible

## OPTIONS

- Timing
  - 10ns access
  - 12ns access
  - 15ns access
  - 20ns access
  - 25ns access
  - 35ns access
- Packages
  - Plastic DIP (300 mil)
  - Plastic SOJ (300 mil)
- 2V data retention
- Low power
- Temperature
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)
  - Automotive (-40°C to +125°C)
  - Extended (-55°C to +125°C)

## MARKING

	-10
	-12
	-15
	-20
	-25
	-35
None	
DJ	
L	
P	
None	
IT	
AT	
XT	

- Part Number Example: MT5C2561DJ-15 P

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

## GENERAL DESCRIPTION

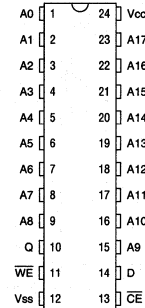
The MT5C2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ( $\overline{CE}$ ) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

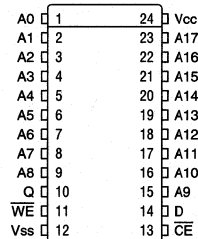
Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes LOW.

## PIN ASSIGNMENT (Top View)

### 24-Pin DIP (SA-3)



### 24-Pin SOJ (SD-1)



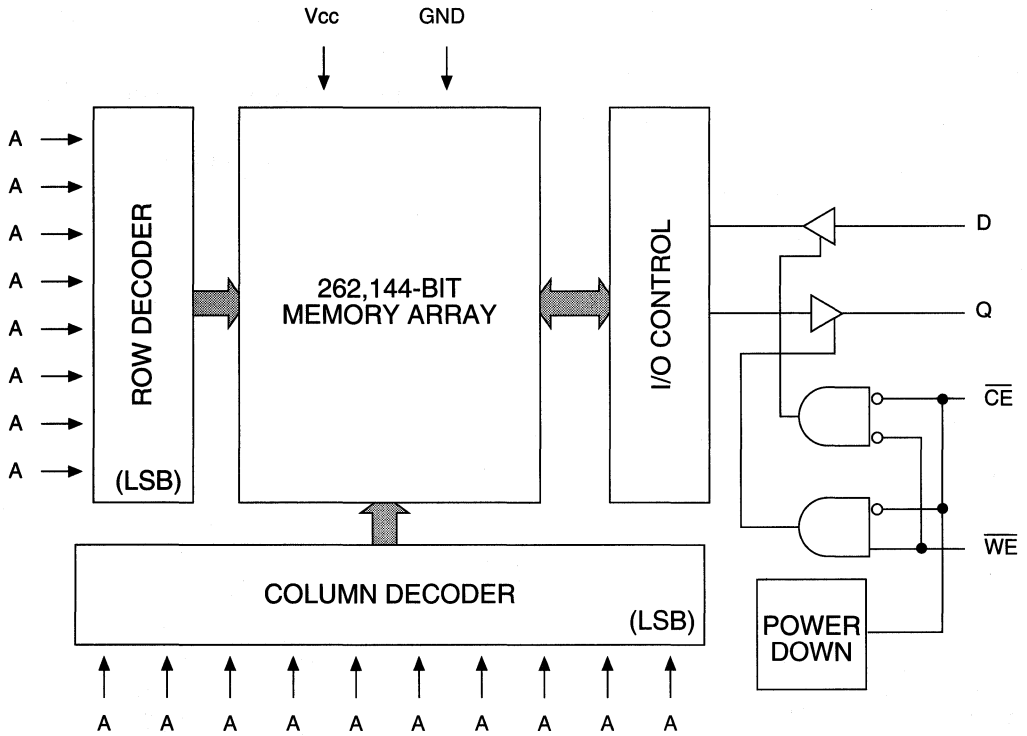
The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current ( $I_{cc}$ ) and TTL standby current ( $I_{SB1}$ ). The latter is achieved through the use of gated inputs on the  $\overline{WE}$  and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

**FUNCTIONAL BLOCK DIAGRAM**

**5 VOLT SRAM**



**TRUTH TABLE**

MODE	CE	WE	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA  
 Voltage on Any Pin Relative to Vss ..... -1V to Vcc +1V

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤ T<sub>A</sub> ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.2	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	I <sub>LI</sub>	-5	5	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	I <sub>LO</sub>	-5	5	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1
Supply Voltage		V <sub>CC</sub>	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-10**	-12**	-15	-20	-25	-35		
Power Supply Current: Operating	CE ≤ V <sub>IL</sub> ; V <sub>CC</sub> = MAX f = MAX = 1/4RC outputs open	I <sub>CC</sub>	103	190	170	150	130	125	120	mA	3, 13
	P version	I <sub>CC</sub>	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	CE ≥ V <sub>IH</sub> ; V <sub>CC</sub> = MAX f = MAX = 1/4RC outputs open	I <sub>SB1</sub>	24	55	50	45	40	35	35	mA	13
	P version	I <sub>SB1</sub>	1.4	-	-	4	4	4	4	mA	13
	CE ≥ V <sub>CC</sub> -0.2V; V <sub>CC</sub> = MAX V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V; f = 0	I <sub>SB2</sub>	0.6	5	5	5	5	5	7	mA	13
	P version	I <sub>SB2</sub>	0.4	-	-	3	3	3	3	mA	13

\*\*P version not available with this speed.

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C; f = 1 MHz V <sub>CC</sub> = 5V	C <sub>I</sub>	6	pF	4
Output Capacitance		C <sub>O</sub>	6	pF	4

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Note 5) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>CC</sub> = 5V ±10%)

DESCRIPTION	SYM	-10		-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>															
READ cycle time	<sup>t</sup> RC	10		12		15		20		25		35		ns	
Address access time	<sup>t</sup> AA		10		12		15		20		25		35	ns	
Chip Enable access time	<sup>t</sup> ACE		10		12		15		20		25		35	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	<sup>t</sup> LZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	<sup>t</sup> HZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	<sup>t</sup> PD		10		12		15		20		25		35	ns	
<b>WRITE Cycle</b>															
WRITE cycle time	<sup>t</sup> WC	10		12		15		20		25		35		ns	
Chip Enable to end of write	<sup>t</sup> CW	7		8		10		12		15		20		ns	
Address valid to end of write	<sup>t</sup> AW	7		8		10		12		15		20		ns	
Address setup time	<sup>t</sup> AS	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	1		1		1		1		1		1		ns	
WRITE pulse width	<sup>t</sup> WP	7		8		10		12		15		20		ns	
Data setup time	<sup>t</sup> DS	6		7		7		10		10		15		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	<sup>t</sup> LZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	<sup>t</sup> HZWE		5		6		7		8		10		12	ns	6, 7

\*Preliminary

**INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)**

The following specifications are to be used for Industrial Temperature (IT) MT5C2561 SRAMs.  
(-40°C ≤ T<sub>A</sub> ≤ 85°C)

DESCRIPTION	CONDITIONS	SYM	MAX						UNITS	NOTES
			-10	-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$ ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sup>1</sup> RC outputs open	I <sub>CC</sub>	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$ ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sup>1</sup> RC outputs open	I <sub>SB1</sub>	65	60	50	45	40	40	mA	13
	$\overline{CE} \geq V_{CC} - 0.2V$ ; V <sub>CC</sub> = MAX V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V; f = 0	I <sub>SB2</sub>	6	6	6	6	6	7	mA	13

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ V <sub>IN</sub> ≥ (V <sub>CC</sub> - 0.2V) or ≤ 0.2V	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>	400	μA	
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>	600	μA	
Data Retention Current LP version	$\overline{CE} \geq (V_{CC} - 0.2V)$	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>	400	μA	
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>	600	μA	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.  
(Notes 5, 13) (-40°C ≤ T<sub>A</sub> ≤ 85°C)

DESCRIPTION	SYM	-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>													
Output hold from address change	t <sup>1</sup> OH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	t <sup>1</sup> LZCE	2		2		2		2		2		ns	7

**AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)**

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2561 SRAMs.

( $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  - AT) ( $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  - XT)

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{\text{CE}} \leq V_{IL}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/4\text{RC}$ outputs open	I <sub>CC</sub>	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{\text{CE}} \geq V_{IH}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/4\text{RC}$ outputs open	I <sub>SB1</sub>	60	50	45	40	40	mA	13
	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}; V_{CC} = \text{MAX}$ $V_{IN} \leq V_{SS} + 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}; f = 0$	I <sub>SB2</sub>	7	7	7	7	7	mA	13

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Data Retention Current	$\overline{\text{CE}} \geq (V_{CC} - 0.2\text{V})$ $V_{IN} \geq (V_{CC} - 0.2\text{V})$ or $\leq 0.2\text{V}$	$V_{CC} = 2\text{V}$	I <sub>CCDR</sub>	500	$\mu\text{A}$
		$V_{CC} = 3\text{V}$	I <sub>CCDR</sub>	800	$\mu\text{A}$
Data Retention Current LP version	$\overline{\text{CE}} \geq (V_{CC} - 0.2\text{V})$	$V_{CC} = 2\text{V}$	I <sub>CCDR</sub>	500	$\mu\text{A}$
		$V_{CC} = 3\text{V}$	I <sub>CCDR</sub>	800	$\mu\text{A}$

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.

(Notes 5, 13) ( $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

DESCRIPTION	SYM	-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>													
Output hold from address change	t <sub>OH</sub>	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	t <sub>LZCE</sub>	2		2		2		2		2		ns	7

**AC TEST CONDITIONS**

Input pulse levels .....	V <sub>SS</sub> to 3.0V
Input rise and fall times .....	3ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2

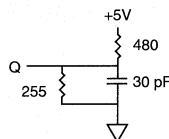


Fig. 1 OUTPUT LOAD EQUIVALENT

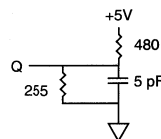


Fig. 2 OUTPUT LOAD EQUIVALENT

**NOTES**

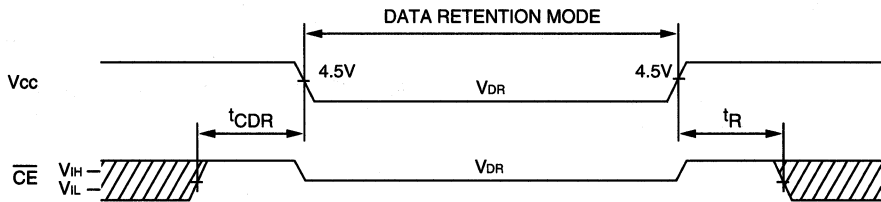
1. All voltages referenced to V<sub>SS</sub> (GND).
2. -3V for pulse width < t<sub>RC</sub>/2.
3. I<sub>CC</sub> is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub>.
8.  $\overline{WE}$  is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t<sub>RC</sub> = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

**5 VOLT SRAM**

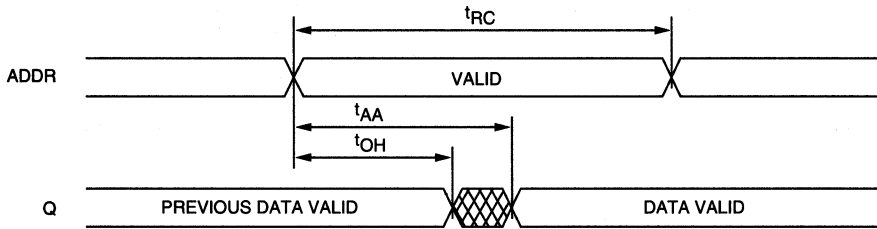
**DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)**

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> for Retention Data			V <sub>DR</sub>	2			V	
Data Retention Current L version	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>		175	300	μA	14
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>		250	500	μA	14
Data Retention Current LP version	$\overline{CE} \geq (V_{CC} - 0.2V)$	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>		175	300	μA	14
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>		250	500	μA	14
Chip Deselect to Data Retention Time			t <sub>CDR</sub>	0			ns	4
Operation Recovery Time			t <sub>R</sub>	t <sub>RC</sub>			ns	4, 11

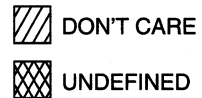
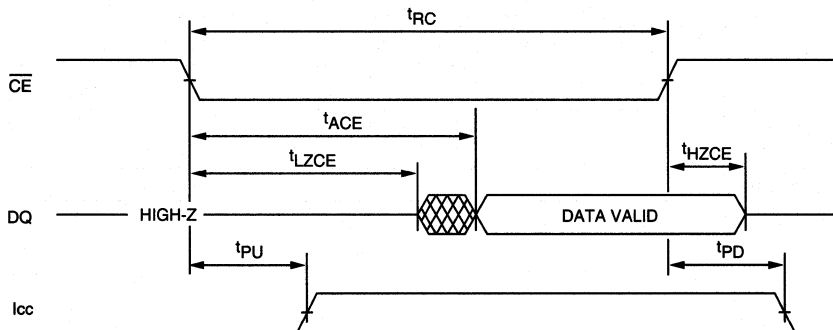
**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM**



**READ CYCLE NO. 1 8, 9**

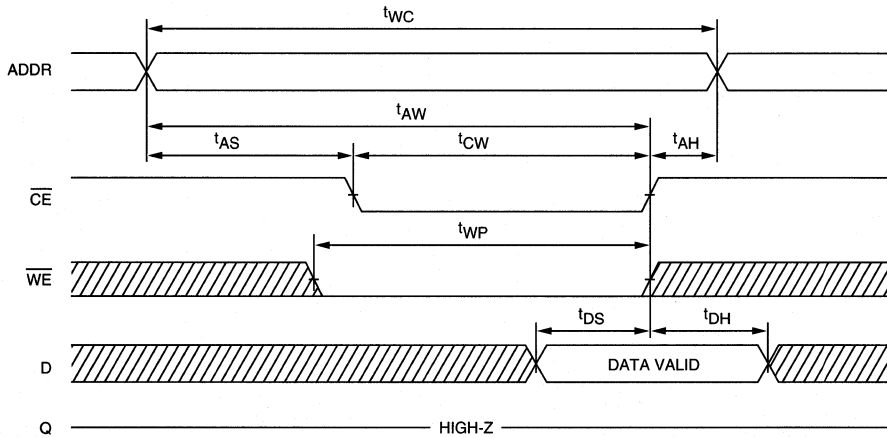


**READ CYCLE NO. 2 7, 8, 10**

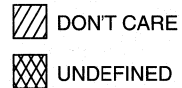
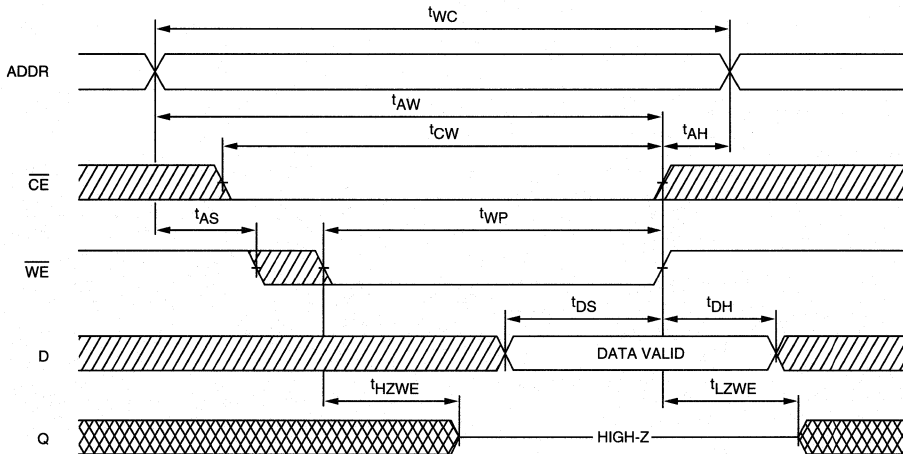




**WRITE CYCLE NO. 1**<sup>12</sup>  
(Chip Enable Controlled)



**WRITE CYCLE NO. 2**<sup>7, 12</sup>  
(Write Enable Controlled)



**5 VOLT SRAM**