SRAM

32K x 8 SRAM

FEATURES

- High speed: 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

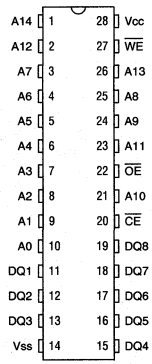
OPTIONS — MARKING

- Timing
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C2568DJ-20 IT

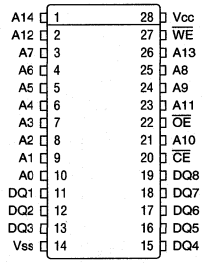
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The MT5C2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

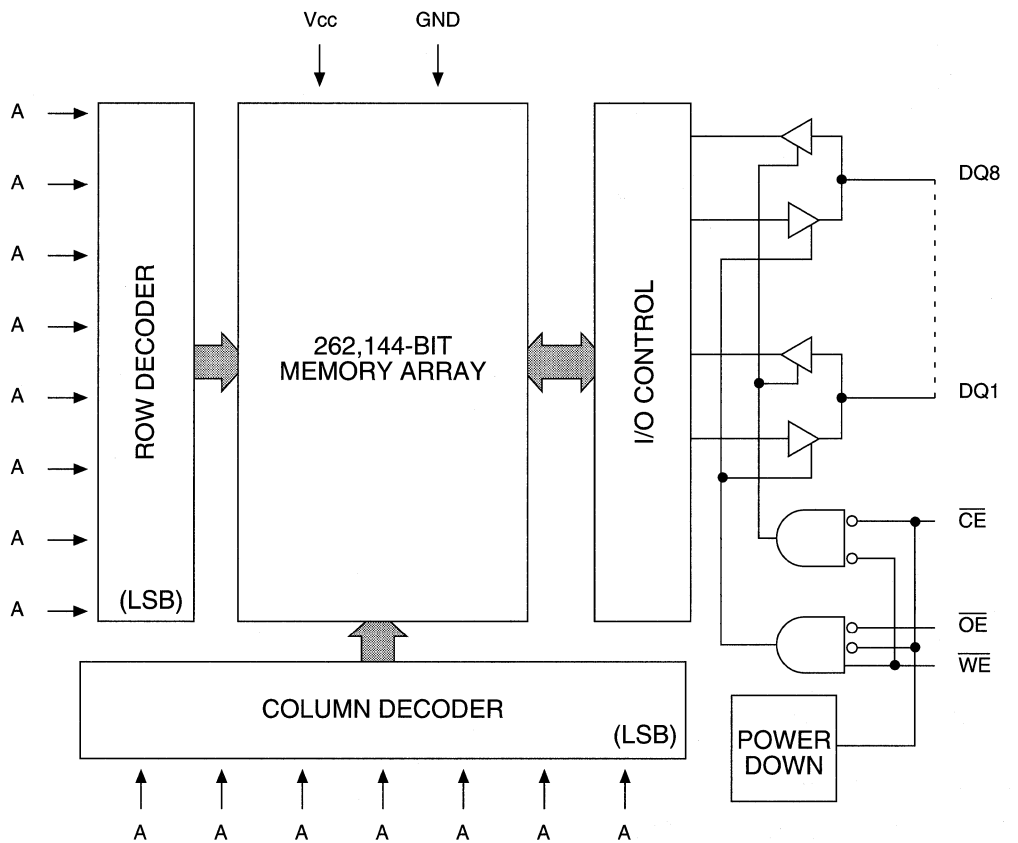
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

					MAX							
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10**	-12**	-15**	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	103	190	170	150	130	125	120	mA	3, 13
	P version	I_{CC}	96	-	-	135	125	120	115	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	4	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	3	mA	13

**P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	10		12		15		20		25		35		ns	
Address access time	^tAA		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		10		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		5		6		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		5		6		6		7		7		12	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		20		ns	
Address valid to end of write	^tAW	7		8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		20		ns	
Data setup time	^tDS	6		7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10		12	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2568 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX							
DESCRIPTION	**CONDITIONS**	**SYM**	**-10**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2568 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**-35**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	180	155	140	135	135	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
Output hold from address change	^tOH	2		2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		2		ns	7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

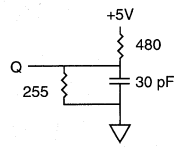


Fig. 1 OUTPUT LOAD EQUIVALENT

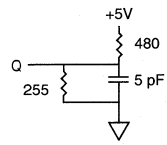


Fig. 2 OUTPUT LOAD EQUIVALENT

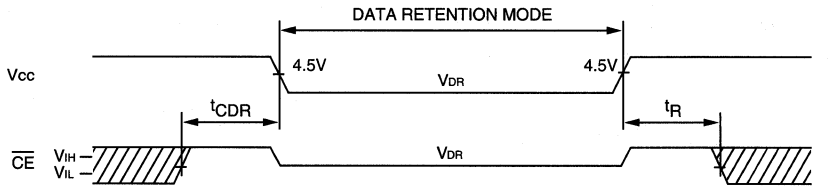
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

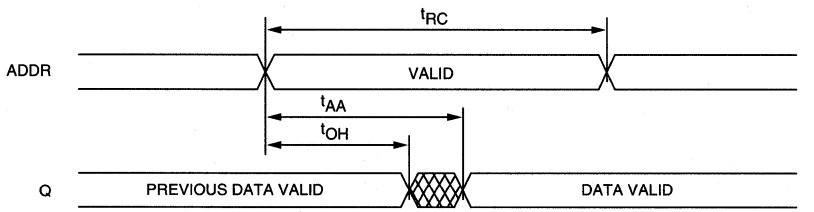
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		175	300	µA	14
		Vcc = 3V	ICCDR		250	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

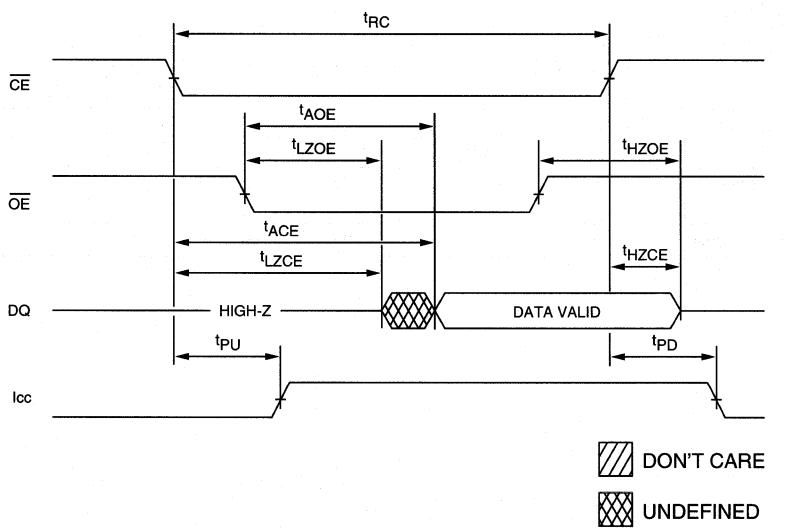
LOW Vcc DATA RETENTION WAVEFORM



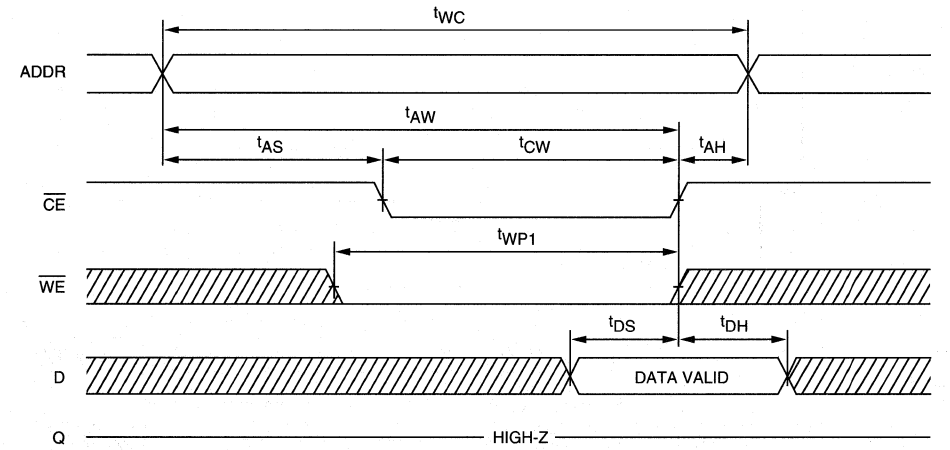
READ CYCLE NO. 1 [8, 9]



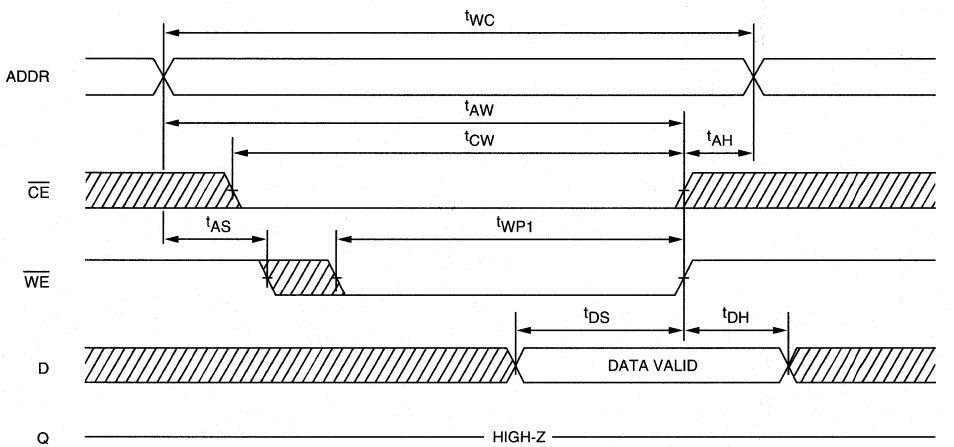
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 15]
(Write Enable Controlled)



DON'T CARE

UNDEFINED

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)