SRAM

1 MEG x 4 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5LC1M4D4DJ-20

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)

A0	1	32	A19
A1	2	31	A18
A2	3	30	A17
A3	4	29	A16
A4	5	28	A15
$\overline{CE}$	6	27	$\overline{OE}$
DQ1	7	26	DQ4
Vcc	8	25	Vss
Vss	9	24	Vcc
DQ2	10	23	DQ3
$\overline{WE}$	11	22	A14
A5	12	21	A13
A6	13	20	A12
A7	14	19	A11
A8	15	18	A10
A9	16	17	NC

32-Pin TSOP (SE-1)

A0	1	32	A19
A1	2	31	A18
A2	3	30	A17
A3	4	29	A16
A4	5	28	A15
$\overline{CE}$	6	27	$\overline{OE}$
DQ1	7	26	DQ4
Vcc	8	25	Vss
Vss	9	24	Vcc
DQ2	10	23	DQ3
$\overline{WE}$	11	22	A14
A5	12	21	A13
A6	13	20	A12
A7	14	19	A11
A8	15	18	A10
A9	16	17	NC

GENERAL DESCRIPTION

The MT5LC1M4D4 is organized as a 1,048,576 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

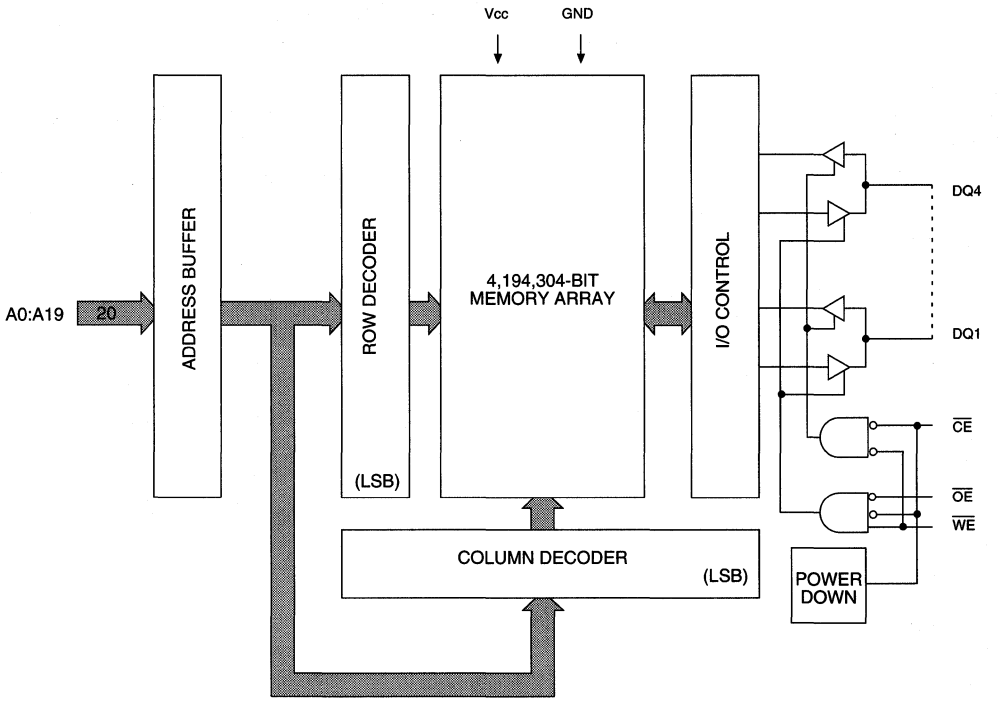
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDENCE (EST)[16]

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	32	1.0	15	60
TSOP	32	1.0	5	70

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC; outputs open	I_{CC}	ALL	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX; f = 0 VIN ≥ Vcc -0.2V or VIN ≤ VSS +0.2	I_{SB2}	STD	1.0	1.0	1.0	1.0	1.0	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	Vcc = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		20		ns	
WRITE pulse width	$^tWP2$	9		11		14		17		22		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

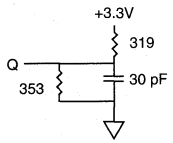


Fig. 1 OUTPUT LOAD EQUIVALENT

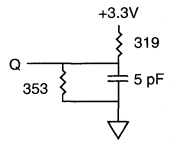


Fig. 2 OUTPUT LOAD EQUIVALENT

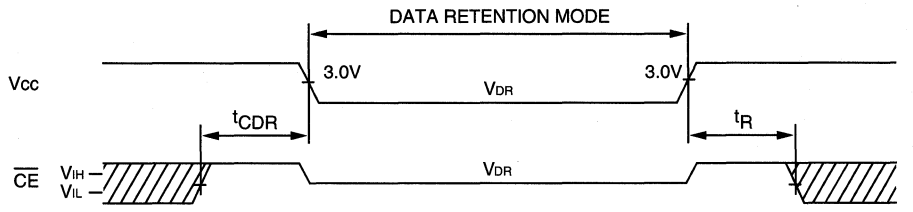
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable ($\overline{OE}$) is inactive (HIGH).
15. Output enable ($\overline{OE}$) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

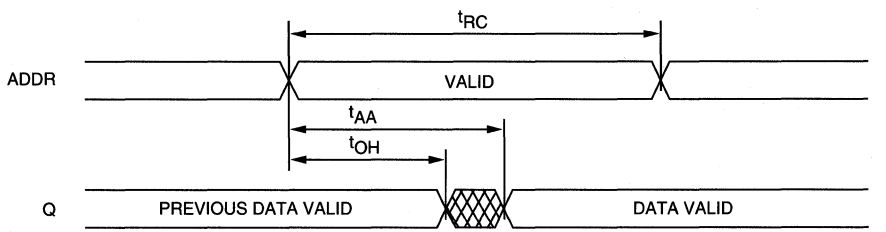
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current L version	$\overline{CE} \geq (Vcc -0.2V)$ $V_{IN} \geq (Vcc -0.2V)$ or $\leq 0.2V$ Vcc = 2.0V	I_{CCDR}		700	µA	
Data Retention Current LP version	$\overline{CE} \geq (Vcc -0.2V)$ Vcc = 2.0V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

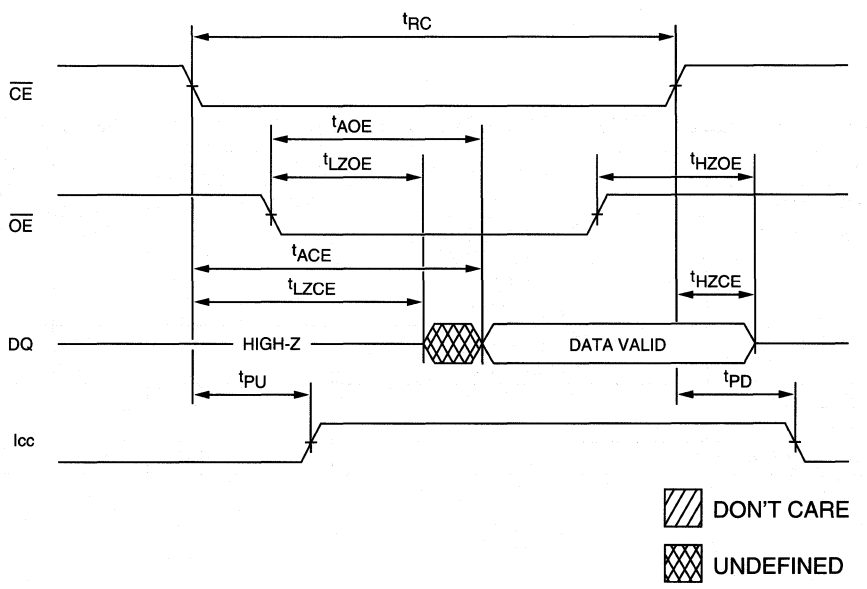
LOW Vcc DATA RETENTION WAVEFORM



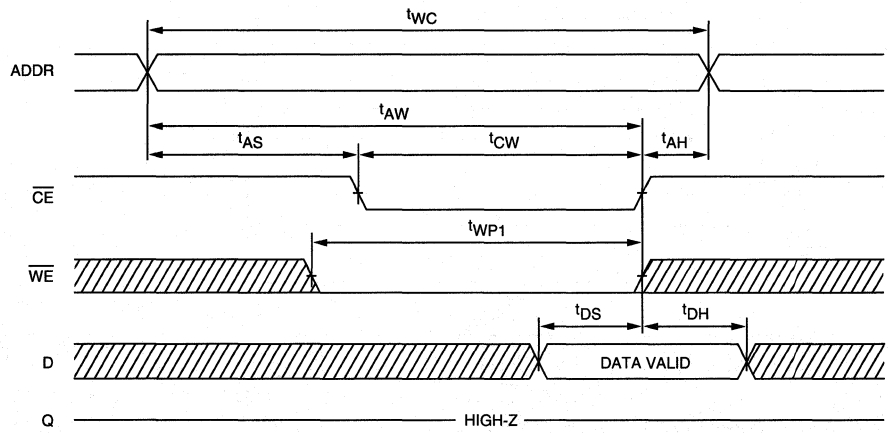
READ CYCLE NO. 1 [8, 9]



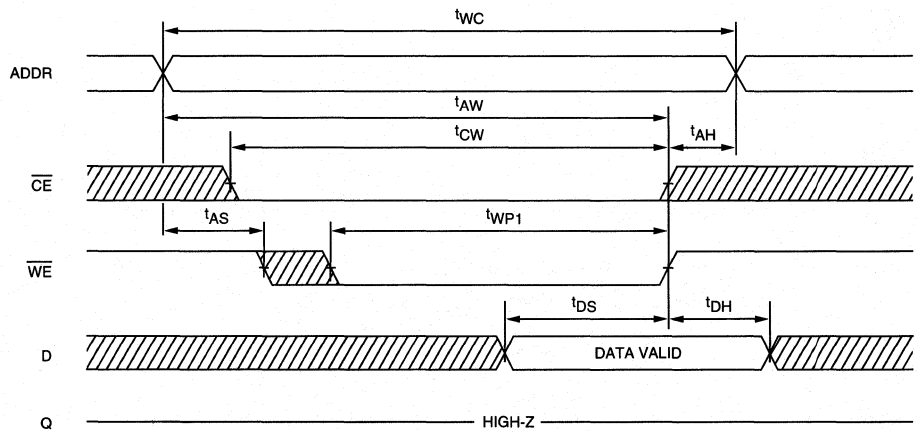
READ CYCLE NO. 2 [7, 8, 10]

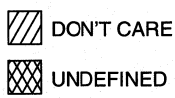


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 14]
(Write Enable Controlled)





WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)