SRAM

256K x 1 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC LVTTL voltage standards

OPTIONS

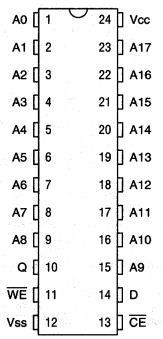
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
• 2V data retention	L
• Low power	P
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5LC2561DJ-20 P

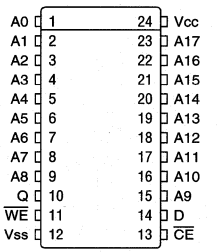
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)



24-Pin SOJ
(SD-1)



GENERAL DESCRIPTION

The MT5LC2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

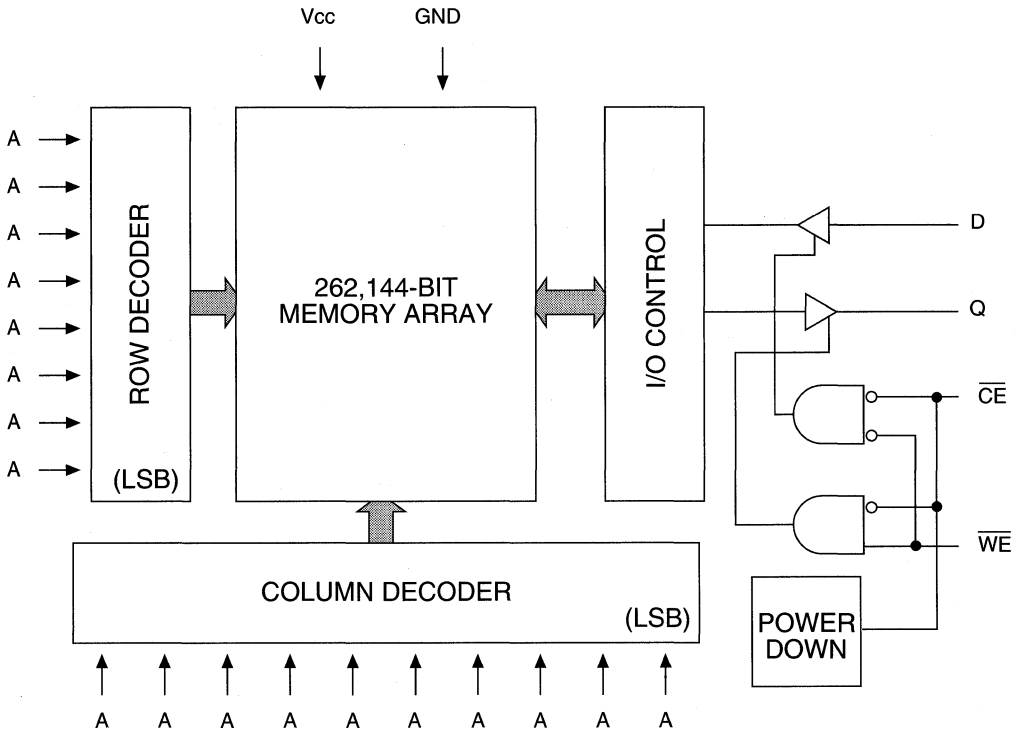
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed-systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD	73	125	110	95	90	85	mA	3, 14
			P	39	–	65	55	50	50	mA	
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD	17	35	30	25	25	25	mA	14
			P	8	–	18	15	12	12	mA	14
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD	1.0	3	3	3	3	5	mA	14
			P	300	–	750	750	750	1,500	µA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES		
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Output hold from address change	^tOH	–	–	4		4		4		4		ns	16
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in Low-Z	^tLZCE	–	–	4		4		4		4		ns	16
Chip disable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
Address hold from end of write	^tAH	–	–	0		0		0		0		ns	16
WRITE pulse width	^tWP	8		10		12		15		20		ns	
Data setup time	^tDS	7		8		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10		12	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

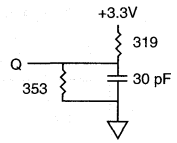


Fig. 1 OUTPUT LOAD EQUIVALENT

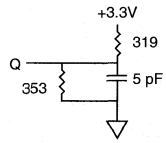


Fig. 2 OUTPUT LOAD EQUIVALENT

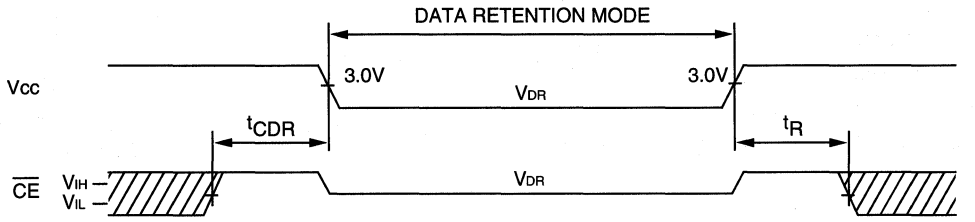
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Typical values are measured at 3.3V, 25°C and 15ns cycle time for STD and 20ns for P.
15. Typical currents are measured at 25°C.
16. These timing specifications are only valid for P (low power) parts.

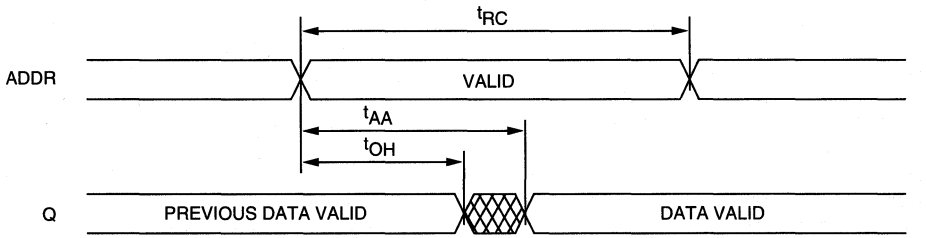
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other Inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	15
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		195	350	µA	15
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

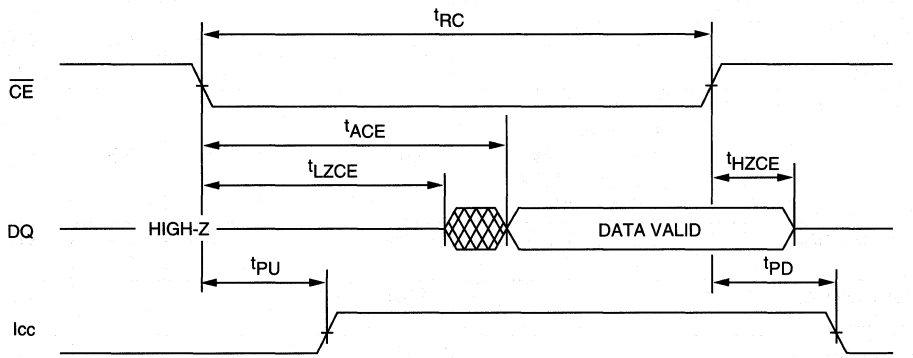
LOW Vcc DATA RETENTION WAVEFORM

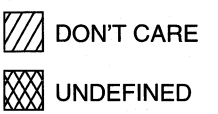


READ CYCLE NO. 1 [8, 9]

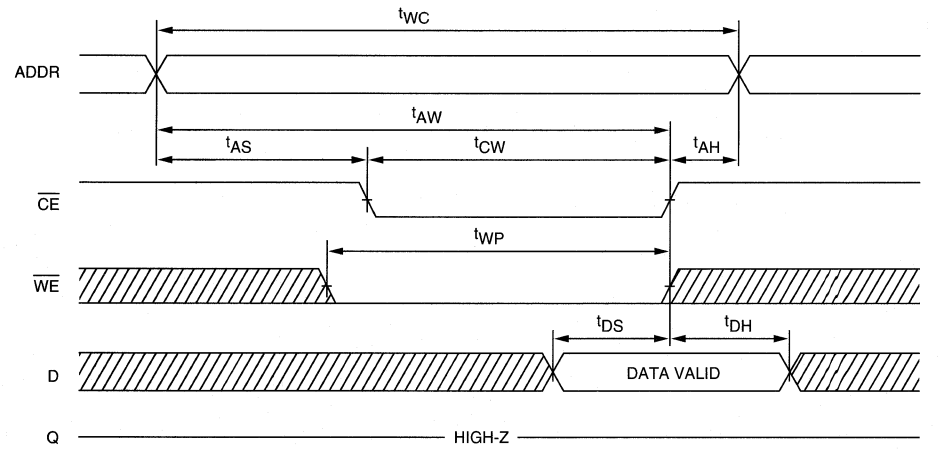


READ CYCLE NO. 2 [7, 8, 10]





WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)