Mosway Technologies Ltd.

MT6136

3-Phase High Voltage Gate Driver IC

General Description

The MT6136 is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels for 3-phase applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600V. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current or under-voltage shutdown has occurred. Over-current fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

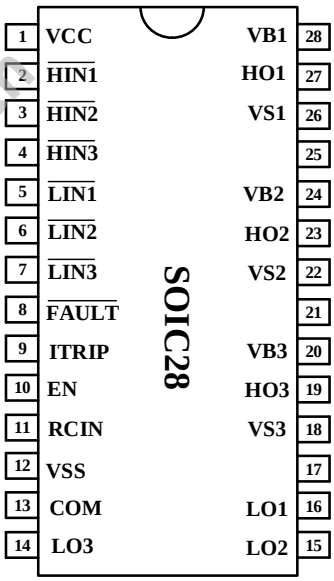
Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for all channels
- Cross-conduction prevention logic
- Over-current shutdown turns off all six drivers
- Externally programmable delay for automatic fault clear
- Independent 3 half-bridge drivers
- -5V negative Vs ability
- Matched propagation delay for all channels

Applications

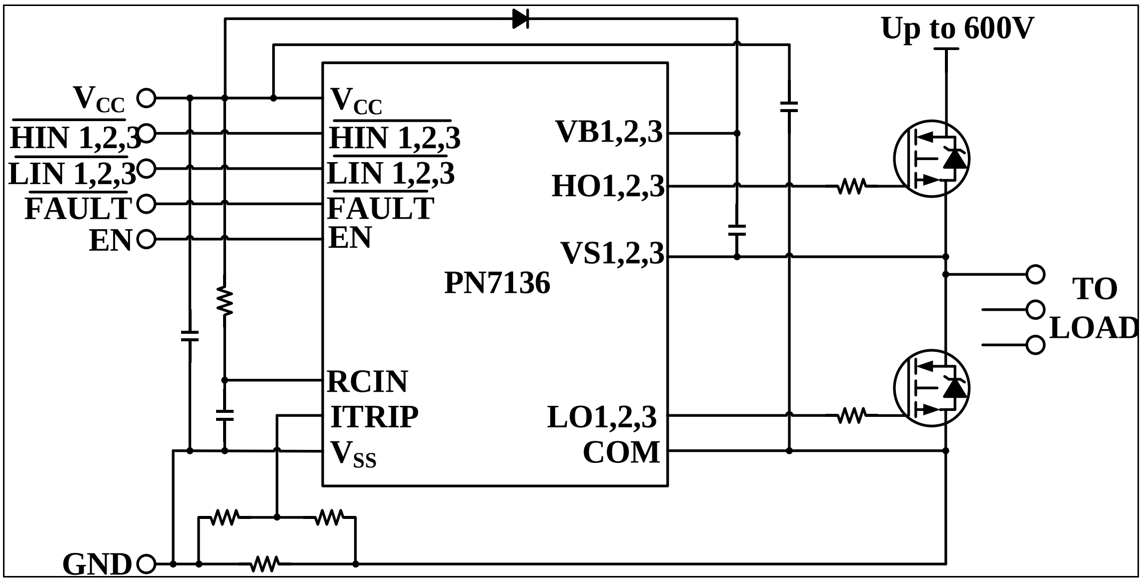
- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Packages/Order information



Part number	Order Code	Package
MT6136	**MT6136SAC-R1**	**SOIC28**

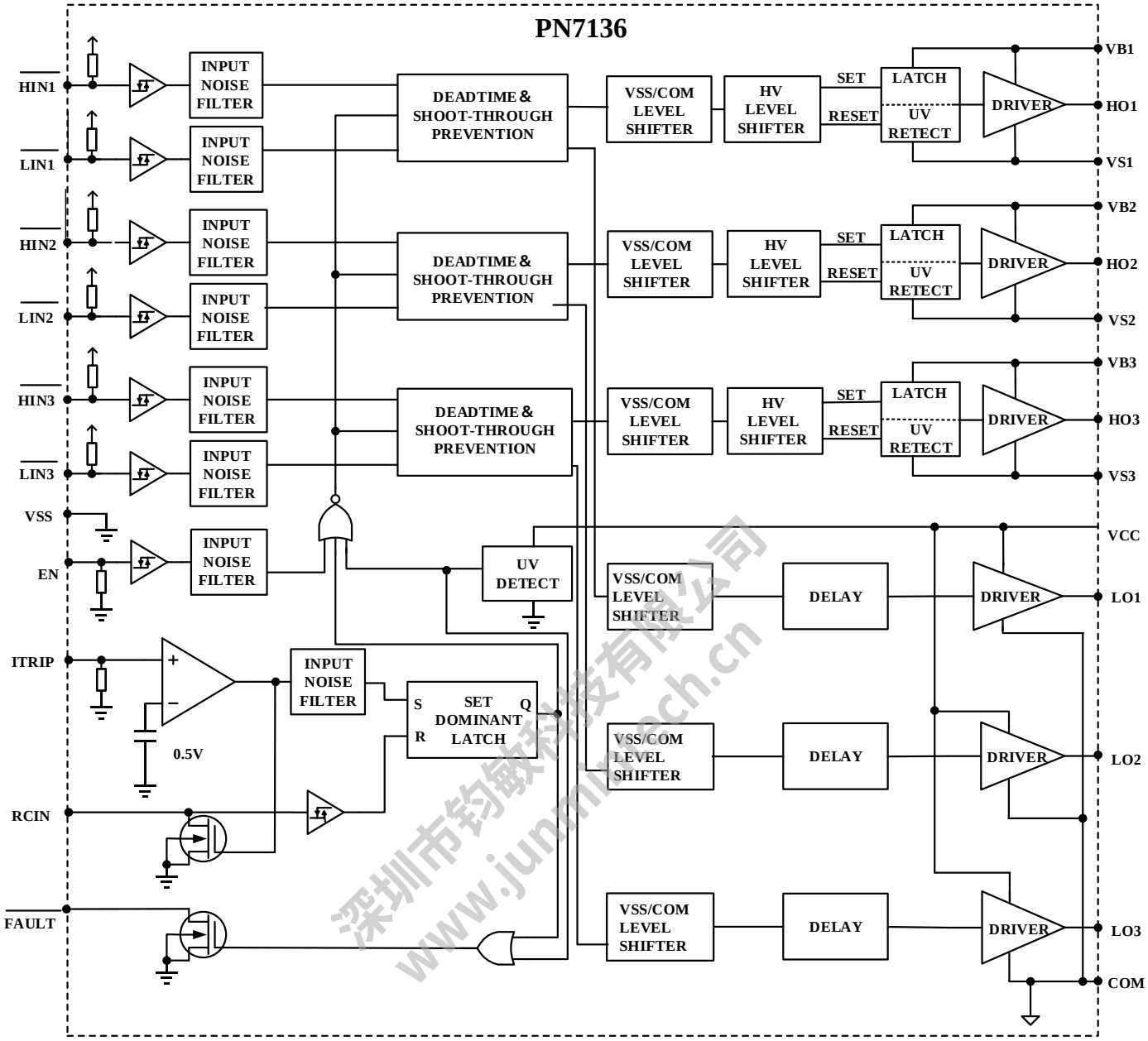
Typical Application Circuit



Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	VCC	Low side and logic fixed supply voltage
2	HIN1	Signal Input for 1^{st} Phase High-side
3	HIN2	Signal Input for 2^{nd} Phase High-side
4	HIN3	Signal Input for 3^{rd} Phase High-side
5	LIN1	Signal Input for 1^{st} Phase Low-side
6	LIN2	Signal Input for 2^{nd} Phase Low-side
7	LIN3	Signal Input for 3^{rd} Phase Low-side
8	FAULT	Indicates over-current (ITRIP)or low-side under-voltage lockout
9	ITRIP	Analog input for overcurrent shutdown.
10	EN	Logic input to enable I/O functionality
11	RCIN	External RC network input used to define FAULT CLEAR delay
12	VSS	Logic ground
13	COM	Low side gate drivers return
14	LO3	Low side gate driver outputs for 3^{rd} Phase
15	LO2	Low side gate driver outputs for 2^{nd} Phase
16	LO1	Low side gate driver outputs for 1^{st} Phase
18	VS3	High voltage floating supply return for 3^{rd} Phase
19	HO3	High side gate driver outputs for 3^{rd} Phase
20	VB3	High side floating supply for 3^{rd} Phase
22	VS2	High voltage floating supply return for 2^{nd} Phase
23	HO2	High side gate driver outputs for 2^{nd} Phase
24	VB2	High side floating supply for 2^{nd} Phase
26	VS1	High voltage floating supply return for 1^{st} Phase
27	HO1	High side gate driver outputs for 1^{st} Phase
28	VB1	High side floating supply for 1^{st} Phase

Functional Block Diagram



Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
$V_{B1,2,3}$	High side floating supply		-0.3	622	
$V_{S1,2,3}$	High side floating supply return		V_B - 22	V_B + 0.3	
$V_{HO,1,2,3}$	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	22	
$V_{LO1,2，3}$	Low side gate drive output		-0.3	V_{CC} + 0.3	V
V_{IN}	Logic input of $\overline{HIN}$ & $\overline{LIN}$		-0.3	V_{CC} + 0.3	
VSS	Logic ground		V_{CC}-22	V_{CC}+0.3	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	
V_{FLT}	$\overline{FAULT}$ output voltage		V_{SS}-0.3	V_{CC}+0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
P_D	Package Power Dissipation @ TA ≤25°C	28 Lead SOIC	—	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	28 Lead SOIC	—	200	°C /W
T_J	Junction Temperature		—	150	
T_S	Storage Temperature		-55	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
$V_{B1,2,3}$	High side floating supply	V_S +10	V_S +20	
$V_{S1,2,3}$	High side floating supply return	-5	600	
$V_{HO1,2,3}$	High side gate drive output voltage	$V_{S1,2,3}$	$V_{B,1,2,3}$	
V_{CC}	Low side supply	10	20	
$V_{LO1,2,3}$	Low side gate drive output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage($\overline{HIN}$ & $\overline{LIN}$)	0	V_{CC}	
V_{SS}	Logic ground	-5	5	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

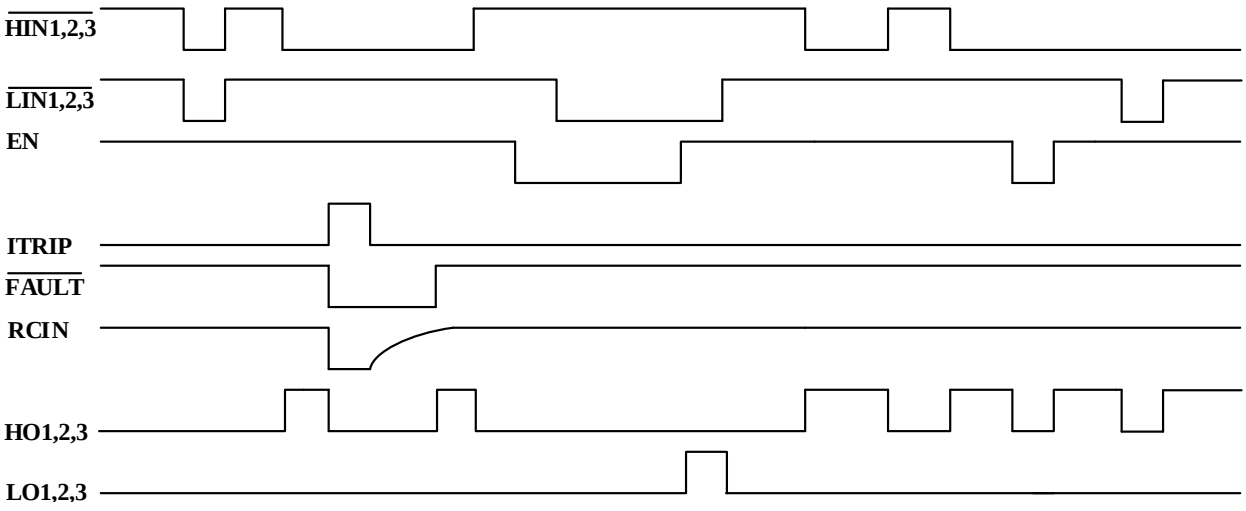
Symbol	Definition	MIN.	TYP.	MAX.	Units
t_{on}	Turn-on propagation delay	500	630	850	ns
t_{off}	Turn-off propagation delay	500	630	850	
t_r	Turn-on rise time	—	90	170	
t_f	Turn-off fall time	—	40	90	
t_{EN}	ENABLE low to output shutdown propagation delay	320	430	620	
t_{ITRIP}	ITRIP to output shutdown propagation delay	400	600	1000	
t_{bl}	ITRIP blanking time	—	260	—	
t_{FLT}	ITRIP to $\overline{FAULT}$ propagation delay	350	550	900	
t_{FLTIN}	Input filter time ($\overline{HIN}$, $\overline{LIN}$)	250	400	560	
$t_{filterEN}$	Input filter time (EN)	100	200	—	
DT	Deadtime	300	400	530	ns
MT	Matching delay ON and OFF	—	—	50	
MDT	Matching delay, max (t_{on}, t_{off}) – min (t_{on}, t_{off}), (t_{on}, t_{off} are applicable to all 3 channels)	—	—	60	
PM	Output pulse width matching	—	—	75	
t_{FLTCLR}	$\overline{FAULT}$ clear time RCIN: R = 2 MΩ, C = 1nF	1.3	1.65	2	**ms**

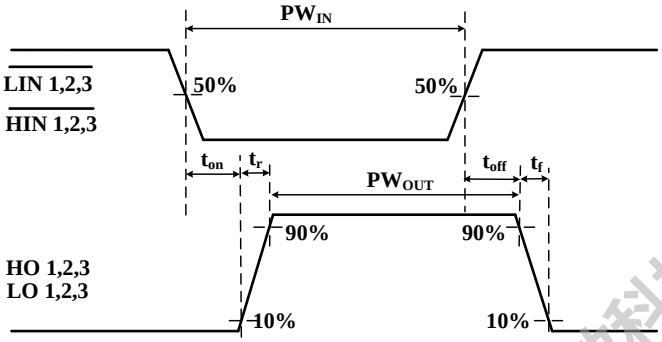
Static Electrical Characteristics

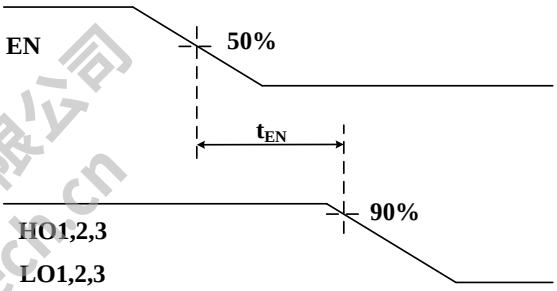
V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

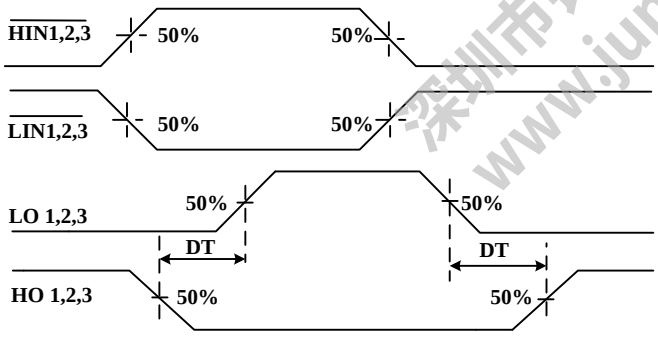
Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic "1"($\overline{HIN}$ & $\overline{LIN}$) input voltage	2.5	—	—	V
V_{IL}	Logic "0" ($\overline{HIN}$ & $\overline{LIN}$) input voltage	-	-	0.8	
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5	
$V_{EN,TH}$	Enable negative going threshold	0.8	—	—	
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55	
$V_{IT,HYS}$	ITRIP input hysteresis	—	0.07	—	
$V_{RCIN,TH+}$	RCIN positive going threshold	—	6.5	—	
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—	
V_{OH}	High level output voltage, VBIAS - VO	-	-	0.3	
V_{OL}	Low level output voltage, VO	-	-	0.3	
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	
V_{CCUV-}		7.4	8.2	9.0	
V_{CCUVHY}	VCC supply under-voltage hysteresis	0.3	0.7	—	
V_{BSUV+}	VBS supply UVLO threshold	8	8.9	9.8	
V_{BSUV-}		7.4	8.2	9	
V_{BSUVHY}	VBS supply under-voltage hysteresis	0.3	0.7	—	
I_{LK}	Leakage current from VS(600V) to GND	—	—	50	μA
I_{QBS}	Quiescent VB supply current	—	45	120	
I_{QCC}	Quiescent VCC supply current	—	1	3	mA
$V_{IN,CLAMP}$	Input clamp voltage($\overline{HIN}$, $\overline{LIN}$,ITRIP and EN)	5.7	6.0	6.55	V
I_{LIN+}	Input bias current(LOUT=HI)	—	120	160	μA
I_{LIN-}	Input bias current(LOUT=LO)	—	160	210	
I_{HIN+}	Input bias current(HOUT=HI)	—	120	160	
I_{HIN-}	Input bias current(HOUT=LO)	—	160	210	
I_{ITRIP+}	"High" ITRIP input bias current	—	5	40	
I_{ITRIP-}	"Low" ITRIP input bias current	—	—	1	
I_{EN+}	"High" ENABLE input bias current	—	5	40	
I_{EN--}	"Low" ENABLE input bias current	—	—	1	
I_{RCIN}	RCIN input bias current	—	—	1	
I_{O+}	Output high short circuit pulsed current	370	450	—	mA
I_{O-}	Output low short circuit pulsed current	600	700	—	
R_{on_RCIN}	RCIN low on resistance	—	30	80	Ω
R_{on_FAULT}	$\overline{FAULT}$ low on resistance	—	30	80	

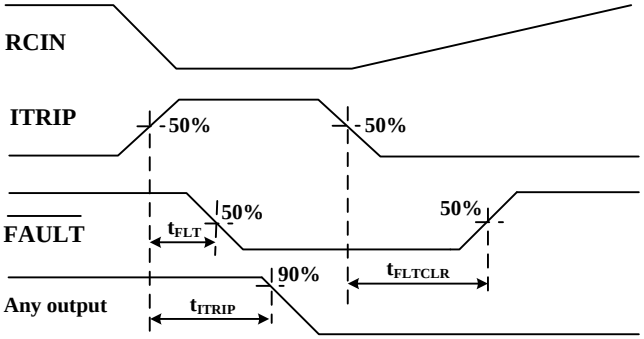
Logic Function & Timing Spec

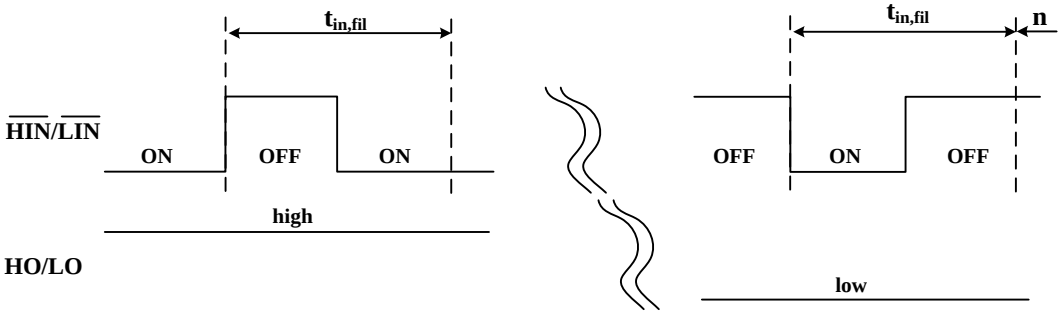










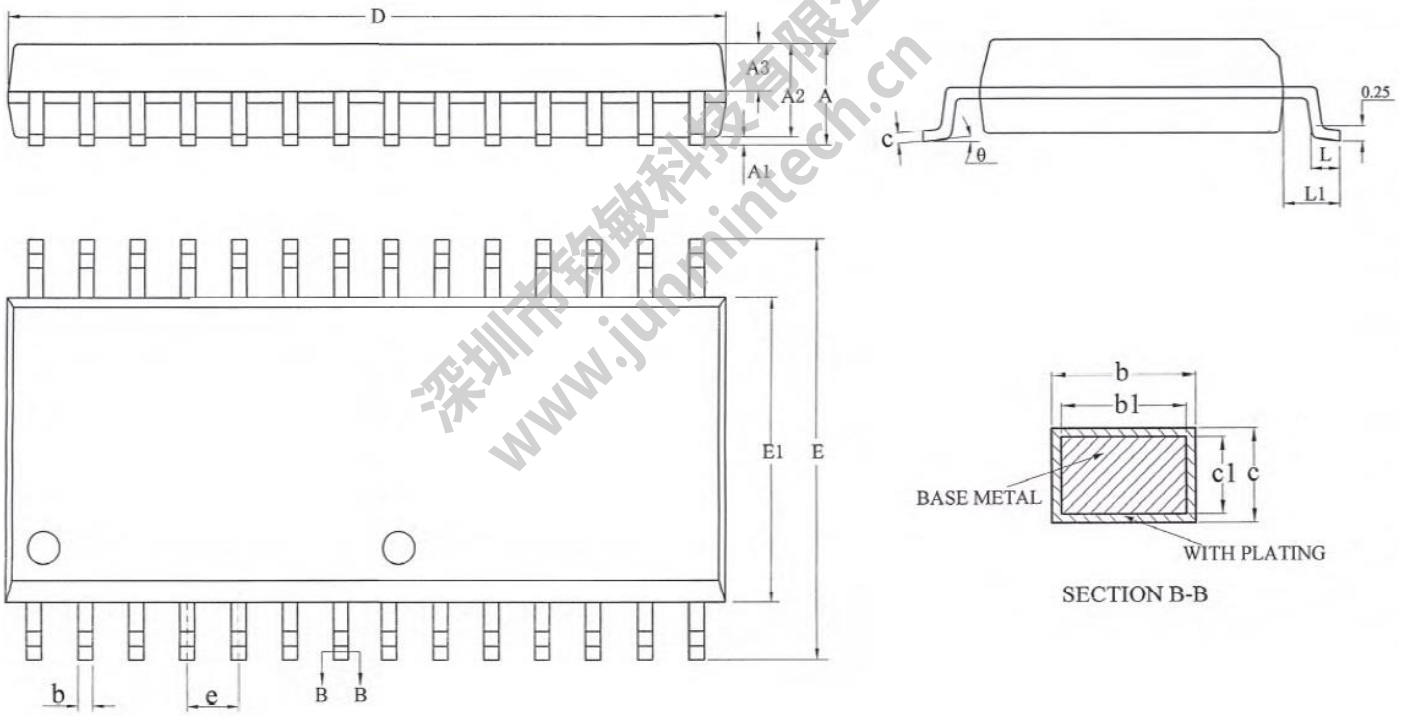


Package Information

SOIC28 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	2.65	D	17.89	18.09	18.29
A1	0.10	-	0.30	E	10.10	10.30	10.50
A2	2.25	2.30	2.35	E1	7.30	7.50	7.70
A3	0.97	1.02	1.07	e	1.27BSC		
b	0.39	-	0.48	L	0.70	-	1.00
b1	0.38	0.41	0.43	L1	1.40BSC		
c	0.25	-	0.31	θ	0	-	8°
c1	0.24	0.25	0.26				

SOIC28 Package Outlines



Mark	Package
MT6136 ABYWX	SOIC28

Note：AB：Product code，Y：Year code； W：Week code； X：Package code

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Product status definition

Datasheet status	Product status	Definition
Advance information	In definition and Design Stage	Target specification for design and development of the described product. Mosway Technologies reserves the right to change specification in any manner without prior notice.
Preliminary	In engineering sample and pre-qualification stage	Datasheet contains preliminary data which are supported by results from initial silicon and preliminary evaluation. Mosway Technologies reserves the right to change specification in any manner without prior notice.
No identification needed / Specified	In full production Stage	Datasheet contains final specifications supported by result in qualification and pilot-production. Mosway Technologies shall notify affected customers for any major changes in form, fit, function and quality / reliability.