MT6139 Data Sheet

Revision History

Revision	Date	Author	Comments
0.1	2006/04/05	MH Tsai	First draft release for MT6139
2.0	2006/09/29	Charles Chiu	First release for MT6139

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1 Introduction

1.1 Features

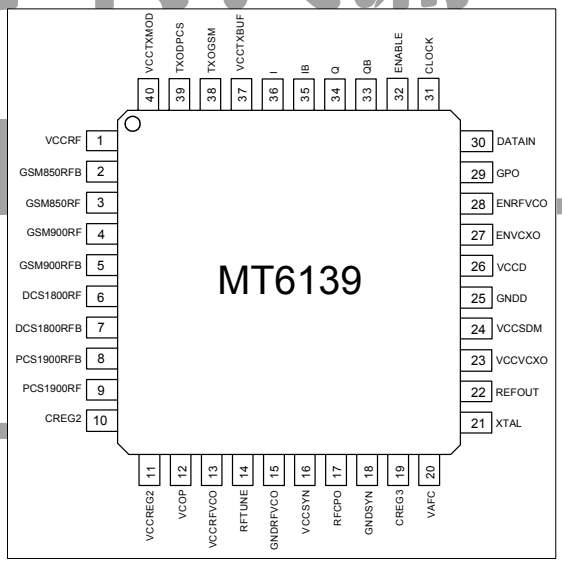
- **Receiver**
  - Direct-conversion architecture with automatic DC-Offset Correction (DCOC) loops
  - Quad-band differential-input LNAs
  - Fully-integrated 135 kHz channel filter
  - 93 dB gain with 60 dB gain control range
  - No IIP2 calibration needed
- **Transmitter**
  - High-precision I/Q modulator
  - Direct-conversion architecture
- **Frequency Synthesizer**
  - Fractional-N architecture with a built-in automatic frequency calibration loop
  - Fully-integrated wide-range VCO
  - Semi-integrated loop filter
- **Voltage-Controlled Crystal Oscillator (VCXO)**
  - One-pin 26 MHz crystal oscillator
  - On-chip programmable capacitor array
  - On-chip varactor
- **Regulators**
  - Built-in low-noise, Low-DropOut (LDO) regulators for Sigma-Delta Modulator (SDM), VCO, and VCXO.
- **3-wire serial interface**
- **0.35µm BiCMOS process**
- **6x6 mm^2 40-pin Quad Flat No-lead (QFN) package**
- **Lead-free/RoHS-compliant**

1.2 Applications

GSM900 / DCS1800 dual-band handsets
GSM850 / PCS1900 dual-band handsets
GSM900 / DCS1800 / PCS1900 tri-band handsets
GSM850 / DCS1800 / PCS1900 tri-band handsets

1.3 General Descriptions

MT6139 is a highly-integrated RF transceiver IC for the Global Systems for Mobile Communication (GSM850/GSM900), Digital Cellular Communication Systems (DCS1800), and Personal Communication Services (PCS1900) cellular systems. It includes four LNAs, two RF quadrature mixers, a channel filter, a programmable-gain amplifier for the receiver, a high-precision I/Q modulator for the transmitter, a 26 MHz VCXO reference, a fractional-N frequency synthesizer with a fully-integrated LC-tank VCO and three built-in LDO regulators for VCO, VCXO and SDM. It is housed in a 40-pin QFN package with a downset paddle for additional grounding. Figure 1 shows the MT6139 functional block diagram.



MT6139 Pin Assignment (Top View)

1.4 Functional Block Diagram

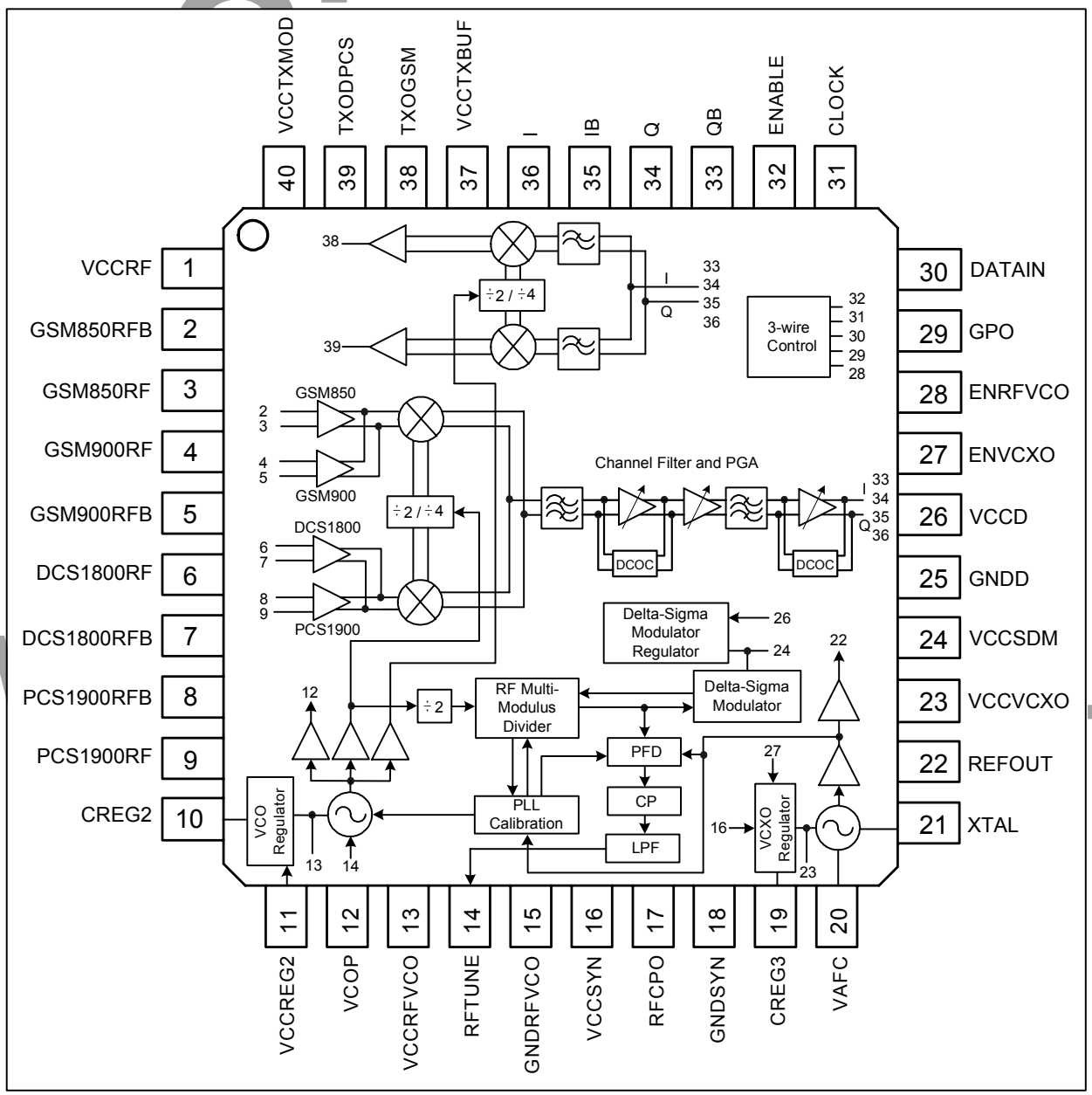


Figure 1 MT6139 Functional Block Diagram

1.5 Pin Assignment and Description

Pin No.	Pin Name	Description
1	VCCRF	RX RF block supply voltage / TX DIV block supply voltage
2	GSM850RFB	Receiver GSM850 RF differential negative input
3	GSM850RF	Receiver GSM850 RF differential positive input
4	GSM900RF	Receiver GSM900 RF differential positive input
5	GSM900RFB	Receiver GSM900 RF differential negative input
6	DCS1800RF	Receiver DCS1800 RF differential positive input
7	DCS1800RFB	Receiver DCS1800 RF differential negative input
8	PCS1900RFB	Receiver PCS1900 RF differential negative input
9	PCS1900RF	Receiver PCS1900 RF differential positive input
10	CREG2	Regulator 2 (VCO) external noise bypass
11	VCCREG2	Regulator 2 (VCO), RX DIV block, VCO buffer supply voltage
12	VCOP	VCO test differential positive output
13	VCCVCO	VCO supply voltage
14	RFTUNE	VCO tune input
15	GNDVCO	VCO ground
16	VCCSYN	RF synthesizer, PFD, charge pump, VCXO regulator supply voltage
17	RFCPO	RF synthesizer charge pump output
18	GNDSYN	RF synthesizer, PFD and charge pump ground
19	CREG3	Regulator 3 (VCXO) external noise bypass
20	VAFC	VCXO tuning
21	XTAL	26 MHz crystal reference input
22	REFOUT	26 MHz reference output
23	VCCVCXO	VCXO supply voltage and Regulator 3 (VCXO) output
24	VCCSDM	RF synthesizer Sigma-Delta modulator supply voltage and Regulator 1 (SDM) output
25	GNDD	3-wire digital circuit and RF synthesizer Sigma-Delta modulator ground
26	VCCD	Supply voltage for 3-wire digital circuit and supply voltage for Regulator 1 (SDM)
27	ENVCXO	Regulator 3 enable input for VCXO
28	ENRFVCO	Regulator 2 enable input for VCO
29	GPO	General-purpose output. Auxiliary test output
30	DATAIN	3-wire serial bus data input
31	CLOCK	3-wire serial bus clock input
32	ENABLE	3-wire serial bus enable input
33	QB	Q path negative baseband input / output
34	Q	Q path positive baseband input / output
35	IB	I path negative baseband input / output
36	I	I path positive baseband input / output
37	VCCTXBUF	TX buffer block supply voltage
38	TXOGSM	TX buffer output for GSM850 / GSM900
39	TXODPCS	TX buffer output for DCS1800 / PCS1900
40	VCCTXMOD	TX modulator supply voltage

Table 1 MT6139 Pin Assignment and Description

2 Functional Description

2.1 Receiver

The receiver section of MT6139 includes Quad-band Low-Noise Amplifiers (LNAs), RF quadrature mixers, channel filters, Programmable-Gain Amplifiers (PGAs), and on-chip automatic DC-offset correction loops. The fully-integrated channel filters reject interference and blocking signals without any external components. The MT6139 includes four differential LNAs for GSM850 (869-894 MHz), GSM900 (925-960 MHz), DCS1800 (1805-1880 MHz) and PCS1900 (1930–1990 MHz) applications. The differential inputs are matched to external SAW filters using LC networks and the H/L gain step is 36 dB. Following the LNAs are two quadrature RF mixers that down-convert the RF signal to IF I/Q signals. The LO signals for mixers are generated by VCO divided-by-2 (for DCS1800/PCS1900) and divided-by-4 (GSM850/GSM900). No external components are needed at the output of the RF mixers.

The IF I/Q signals are then filtered and amplified through a low-pass filter and a PGA. The overall channel reponse composes of an anti-blocking low-pass filter with f_{3dB} = 1.5 MHz at mixer differential load and a 5th-order Butterworth low-pass filter with f_{3dB} = 135 kHz.The multi-stage PGA is implemented between filtering stages to control the gain of the receiver. With a 2 dB gain step, a 60 dB dynamic range of the PGA ensures a proper signal level for baseband setting requirement.

Two DC-Offset Correction (DCOC) loops ensure that the residual static DC-offset voltage held digitally is less than 200mV at maximum gain case. DC-offset correction is performed every time the receiver gain is programmed even in the multislot mode.

By careful control of the chip isolation and mismatch condition, 2nd-order intercept point (IP2) performance (which is correlated to Amplitude-Modulation (AM) suppression performance) is guaranteed by design and no calibration procedure is needed.

2.2 Transmitter

MT6139 transmitter adopts the direct-conversion architecture with higher integration level and simpler frequency plan. It consists of BaseBand (BB) I/Q filters, I/Q modulators, frequency dividers, output buffers and a bias-core circuit. BB I/Q differential signals from the BB chip are fed into the one-pole RC low-pass filter first for better out-of-the-band noise performance. The 3-dB frequency corner is allocated at 700 kHz. Two double balanced mixers (modulators), one for I+/I- and another for Q+/Q- signals, are responsible for translating the filtered BB I/Q signals to the transmitting frequencies. LO signals are provided by the divided-by-2 (for DCS1800/PCS1900) and divided-by-4 (for GSM850/GSM900) dividers. Such kind of the frequency plan will minimize VCO pulling effect and also achieve the better in-band phase noise. The output buffers amplify the modulator output signals to an adequate level to fulfill P_{in} requirement of Power Amplifiers (PA). A Proportional-To-Absolute-Temperature (PTAT) bias-core circuit is used to minimize output power variations under temperature extremes. At last, the on-chip balun is used to convert the differential signals to single-ended output signal.

2.3 RF Frequency Synthesizer

2.3.1 Synthesizer System Description

The MT6139 includes a Phase-Locked Loop (PLL)-based fractional-N frequency synthesizer with a fully-integrated LC-tank VCO. It provides the Local Oscillator (LO) signals for both receiver and transmitter. In order to reduce the inherent spurs caused by the fractional-N synthesizer, a 3rd-order sigma-delta modulator with a dithering function is

used to generate the division number N for the prescaler. The prescaler is composed of a high-frequency divided-by-2 circuit and a multi-modulus frequency divider with the programmable division number ranging from 32 to 127. A conventional digital-type Phase-Frequency Detector (PFD) with a charge pump is used for phase comparison. By changing the output current of the charge pump, the phase detector gain can be programmed from $50/2\pi$ μA/rad to $400/2\pi$ μA/rad.

To reduce the acquisition time or to enable fast settling time for multi-slot data services such as GPRS, a digital frequency calibration loop along with a fast-acquisition system are implemented in the RF synthesizer. During the synthesizer programming, the VCO is pre-set to the vicinity of the desired frequency by the digital frequency calibration loop. After the frequency calibration is finished, a fast-acquisition option is utilized for a period of time to facilitate fast locking. Once the acquisition is done, the PLL reverts back to the normal operation mode.

2.3.2 Synthesizer Frequency Programming

The frequency range of the RF synthesizer is as following.

Rx mode	GSM850	3476 MHz ~ 3576 MHz
	GSM900	3700 MHz ~ 3840 MHz
	DCS1800	3610 MHz ~ 3760 MHz
	PCS1900	3860 MHz ~ 3980 MHz
Tx mode	GSM850	3296 MHz ~ 3396 MHz
	GSM900	3520 MHz ~ 3660 MHz
	DCS1800	3420 MHz ~ 3570 MHz
	PCS1900	3700 MHz ~ 3820 MHz

And the division number N can be decided by the following procedure.

1. Calculate LO frequency f_{VCO} from Rx channel frequency f_{CH}
   $f_{VCO} = 4 * f_{CH}$ for GSM850 and GSM900
   $f_{VCO} = 2 * f_{CH}$ for DCS1800 and PCS1900
2. Calculate the division number N, N_{int} and N_{frac}
   $N = (f_{VCO}/2) / 26\ MHz = N_{int} + N_{frac}/130$ N_{int} and N_{frac} are integers
   $0 \le N_{frac} < 130$
3. Use the binary equivalents of N_{int} and N_{frac} to program registers CW1-N_INTEGER[1] and CW1-N_FRACTION[1].

2.3.3 Digital Frequency Calibration Loop

The MT6139 adopts a digital calibration technique to shorten the synthesizer locking time. Once the frequency synthesizer is programmed through a 3-wire serial interface, a calibration loop is activated. The main function of the calibration loop is to preset the VCO to the vicinity of the desired frequncy quickly and correctly, thus aiding the PLL to settle faster. On the other hand, since a large portion of initial frequency error is dealt with by the integrated calibration loop, the overall locking time can be drastically confined within a small range, irrespective of the desired frequency.

[1] Please refer to MT6139 3-wire setting programming guide.

2.3.4 Fast-Acquisition Option

After the digital calibration loop presets the VCO, the RF synthesizer reverts to the PLL operation and a fast-acquisition option is activated. For faster settling, the charge pump current is set to a higher current than normal setting for a period of time. In MT6139, 20 μs or 60 μs is allowed.

2.4 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO consists of an amplifier, an output buffer, a programmable capacitor array and on-chip varactors. It is an one-pin, parallel-resonance design where a grounded 26 MHz crystal can be used. The output buffer provides a typical 600 mV_{pp} voltage swing at 26 MHz to the BB processor. The programmable capacitor array is used to compensate initial crystal tolerance and aging while the on-chip varactors are used for Automatic Frequency Control (AFC) function.

2.5 Regulator

In MT6139, there are three built-in LDO regulators to provide low-noise, stable, temperature and process independent supply voltages to critical blocks, including VCO, VCXO and sigma-delta modulator. The regulated voltages for these three critical blocks are 1.2 V, 2.5 V and 2 V, respectively. In this way, the pushing figures of VCO and VCXO can be enhanced and the fractional-N spurs caused by SDM can be minimized as well.

3 MT6139 Hardware Control Pin Descriptions

A description of MT6139 hardware control pins and their functionality are shown in the table below.

Pin Name	Setting	Description
ENVCXO	0	Power off VCXO
	1	Power on VCXO
ENRFVCO	0	Power off VCO
	1	Power on VCO

Table 2 Hardware Control Pin Descriptions

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	Symbol	Min	Max	Unit
Power supply voltage	VCCRF	TBD	TBD	V
	VCCREG2	TBD	TBD	V
	VCCSYN	TBD	TBD	V
	VCCD	TBD	TBD	V
	VCCTXBUF	TBD	TBD	V
	VCCTXMOD	TBD	TBD	V
Pin voltage	V_T	TBD	TBD	V
Maximum power dissipation	P_T	TBD	TBD	mW
Operating temperature	T_{opr}	-20	80	°C
Storage temperature	T_{stg}	-55	125	°C

Table 3 Absolute Maximum Ratings

4.2 Recommended Operating Range

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	VCCRF	2.7	2.8	2.9	V
	VCCREG2	2.7	2.8	2.9	V
	VCCSYN	2.7	2.8	2.9	V
	VCCD	2.7	2.8	2.9	V
	VCCTXBUF	2.7	2.8	2.9	V
	VCCTXMOD	2.7	2.8	2.9	V
Operating ambient temperature	T_{opr}	-20	25	65	°C

Table 4 Recommended Operating Range

4.3 DC Specifications

(T_A = 25°C, V_{CC} = 2.8 V unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Power supply current (Rx)	I_{Rx}	ALL[2]			85		mA
Power supply current (Tx)	I_{Tx}	GSM850			152		mA
		GSM900			152		mA
		DCS1800			140		mA
		PCS1900			140		mA
Power supply current (Warm-up)	I_{wp}	ALL	Including VCXO		40		mA
Power supply current (Standby)	I_{sb}	ALL	Regulators + VCO + VCXO		25		mA
Power supply current (VCXO)	I_{vcxo}	ALL	Regulator 3 + VCXO		3.1		mA
Power saving mode supply current (Sleep)	I_{sleep}	ALL	ENVCXO = 0 V, SDATA = 0 V, CLOCK = 0 V, ENABLE = 0 V		1.0		μA
Serial data VH (CLOCK, SDATA, ENABLE)		ALL	VCCD = 2.8 V	2.5			V
Serial data VL (CLOCK, SDATA, ENABLE)		ALL	VCCD = 2.8 V			0.3	V
Control pin VH (ENVCXO)		ALL		2.5			V
Control pin VL (ENVCXO)		ALL				0.3	V
Control pin VH (ENRFVCO)		ALL		2.5			V
Control pin VL (ENRFVCO)		ALL				0.3	V
I/Q common-mode DC output voltage		ALL	Receiver output DC		1.35		V
I/Q common-mode DC input voltage		ALL	Transmitter input DC		1.3		V

Table 5 DC Specifications

[2] ALL mode refers to GSM850 / GSM900 / DCS1800 / PCS1900 bands.

5 Receiver Specifications

(T_A = 25 °C, V_{CC} = 2.8 V unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	GSM850		869		894	MHz
		GSM900		925		960	MHz
		DCS1800		1805		1880	MHz
		PCS1900		1930		1990	MHz
Differential max voltage gain	G_{max}	GSM850	LNA = high gain. PGA = 60 dB	91	93		dB
		GSM900		91	93		dB
		DCS1800		91	93		dB
		PCS1900		91	93		dB
Front-end LNA gain step	$G_{step,LNA}$	GSM850	LNA = high gain to low gain		36		dB
		GSM900			36		dB
		DCS1800			36		dB
		PCS1900			36		dB
Noise figure	NF	GSM850	LNA = high gain. PGA = 60 dB		2.5	3.5	dB
		GSM900			2.5	3.5	dB
		DCS1800			3.5	5	dB
		PCS1900			3.5	5	dB
		GSM850	LNA = low gain. PGA = 60 dB		32	34	dB
		GSM900			32	34	dB
		DCS1800			34	36	dB
		PCS1900			34	36	dB
Noise figure @ 65 °C	NF_{65}	GSM850	LNA = high gain. PGA = 60 dB			4	dB
		GSM900				4	dB
		DCS1800				5.5	dB
		PCS1900				5.5	dB
2nd-order input intercept point	IIP2	GSM850			38		dBm
		GSM900			38		dBm
		DCS1800			33		dBm
		PCS1900			32		dBm
3rd-order input intercept point	IIP3	GSM850	LNA = high gain. PGA = 0 dB		-13		dBm
		GSM900			-13		dBm
		DCS1800			-13		dBm
		PCS1900			-13		dBm

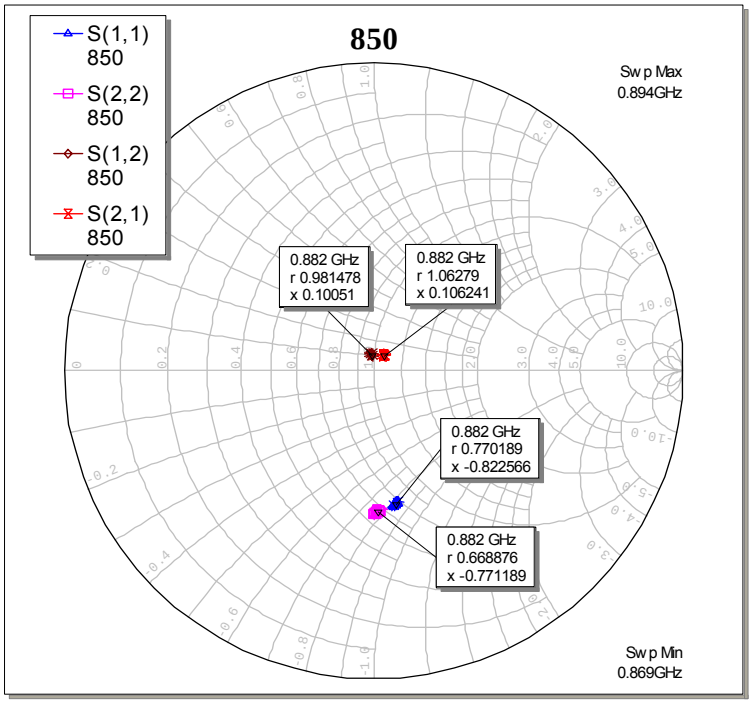
Table 6 AC Specifications of Receiver[3]

[3] Please refer to MT6139 test procedure document.

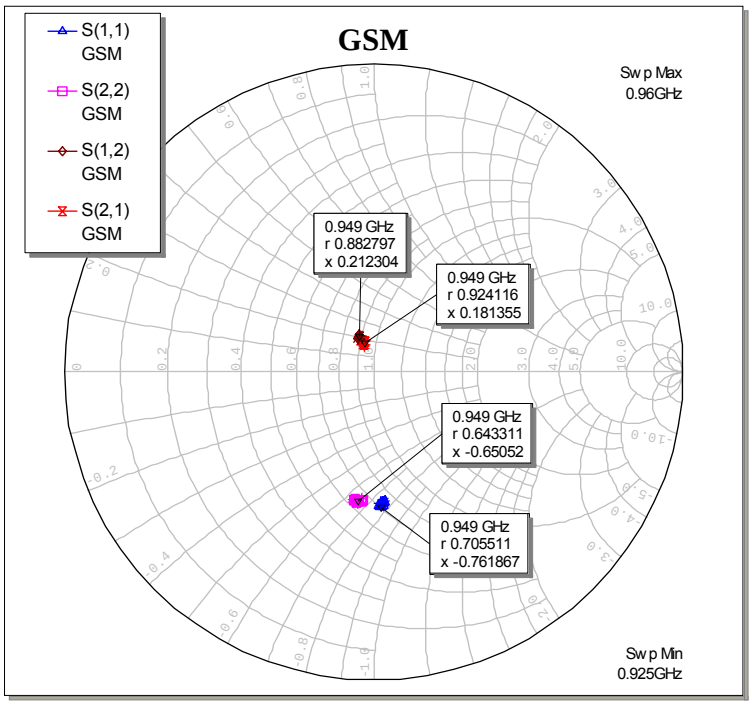
(T_A = 25 °C, V_{CC} = 2.8 V unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
3rd-order input intercept point @ -20 °C	$IIP3_{-20}$	GSM850	LNA = high gain. PGA = 0 dB	-14.5			dBm
		GSM900		-14.5			dBm
		DCS1800		-15			dBm
		PCS1900		-15			dBm
Input 1 dB compression point	IP1dB	GSM850	LNA = high gain. PGA = 0dB		-22		dBm
		GSM900			-22		dBm
		DCS1800			-23		dBm
		PCS1900			-23		dBm
Receiver S/N with 3 MHz blocker		GSM850	Blocker = –23 dBm. Noise power is calculated within 130 kHz bandwidth		10		dB
		GSM900			10		dB
		DCS1800	Blocker = –26 dBm. Noise power is calculated within 130 kHz bandwidth		10.5		dB
		PCS1900			11		dB
I/Q gain error		GSM850			0.5		dB
		GSM900			0.5		dB
		DCS1800			0.5		dB
		PCS1900			0.5		dB
I/Q phase error		GSM850			1		degrees
		GSM900			1		degrees
		DCS1800			5		degrees
		PCS1900			5		degrees
Receiver channel response attenuation		ALL	@ 200 kHz offset		17		dB
			@ 400 kHz offset		47		dB
			@ 600 kHz offset		65		dB
			@ 1.6 MHz offset		110		dB
Group delay variation		ALL	For all gain settings. 0 ~ 100 kHz		1.8		µs
Receiver filtering 3-dB bandwidth		ALL	For all gain settings		135		kHz
PGA gain linearity		ALL	In any 20 dB setting		0.5	1	dB
			For all gain settings		0.8	1.5	dB
PGA gain step		ALL		1.75	2	2.25	dB
PGA dynamic range		ALL	PGA = 0 dB to 60 dB	59	60		dB
I/Q maximum output swing		ALL	For all gain settings	2.0	2.2		V_{p-p}
I/Q common-mode output voltage		ALL	For all gain settings	1.25	1.35	1.45	V
Output static dc offset (after DC-offset calibration)		ALL	For all gain settings			200	mV

Table 6 AC Specifications of Receiver (Continued)

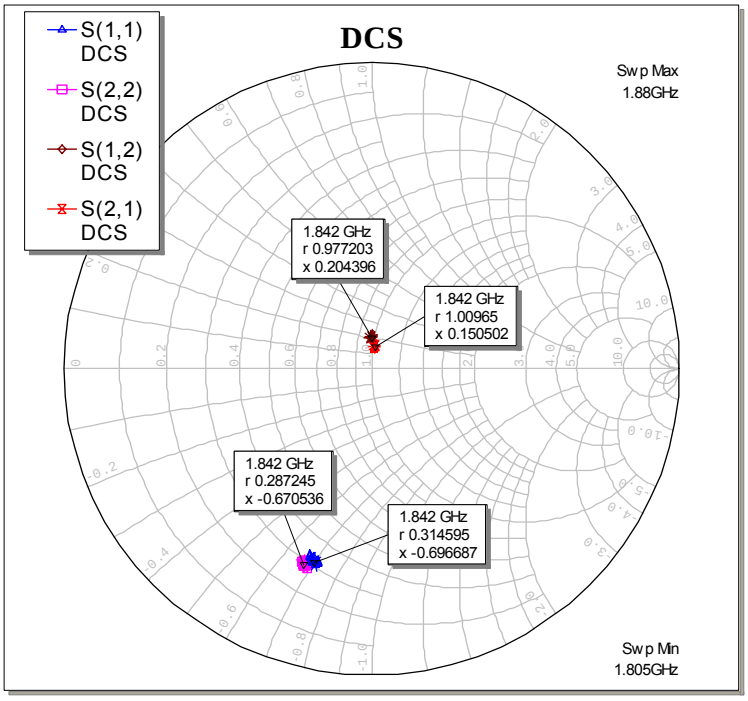


(a) GSM850 Band

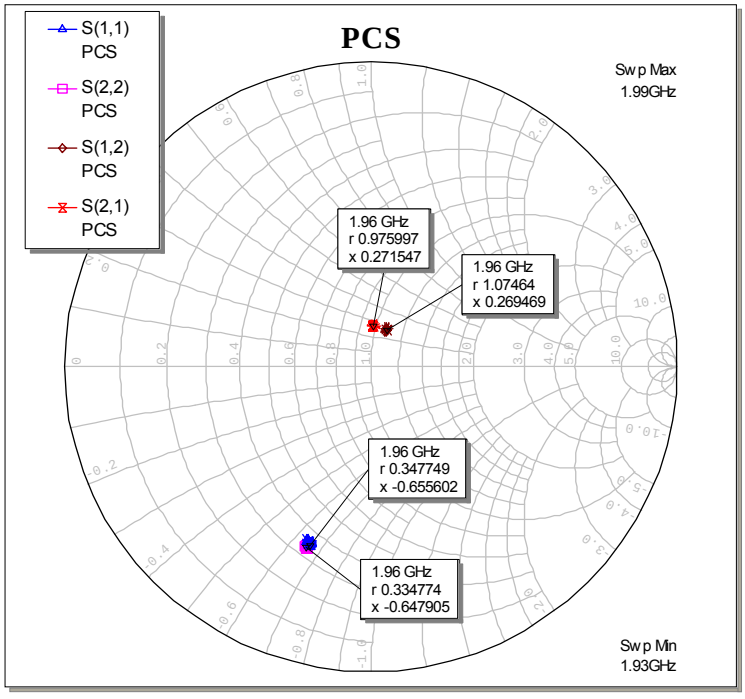


(b) GSM900 Band

Figure 2 Receiver Input S-Parameters (LNA Differential Inputs are Port 1 and Port 2, respectively)



(c) DCS1800 Band



(d) PCS1900 Band

Figure 2 Receiver Input S-Parameters (LNA Differential Inputs are Port 1 and Port 2, respectively) (Continued)

6 Transmitter Specifications

(T_A = 25 °C, V_{CC} = 2.8 V, I/Q common-mode voltage = 1.3 V, I/Q differential input signal = 0.45 V_{p-p} unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Frequency		GSM850		824		849	MHz
		GSM900		880		915	MHz
		DCS1800		1710		1785	MHz
		PCS1900		1850		1910	MHz
RMS phase error	PE_{rms}	GSM850 GSM900			1		degrees
		DCS1800 PCS1900			2		degrees
Carrier suppression	CS	GSM850 GSM900	67.7 kHz sinusoid		-35		dBc
Side-band suppression	SS				-40		dBc
IM3 suppression	IM3				-50		dBc
Carrier suppression	CS	DCS1800 PCS1900			-40		dBc
Side-band suppression	SS				-33		dBc
IM3 suppression	IM3				-55		dBc
Output modulation spectrum	ORFS	ALL	200 kHz offset (RBW = 30 kHz bandwidth)		-36		dBc
		GSM850 GSM900	400 kHz offset (RBW = 30 kHz bandwidth)		-67		dBc
		DCS1800 PCS1900			-65		dBc
		ALL	600 kHz offset (RBW = 30 kHz bandwidth)		-73		dBc
		ALL	1.2 MHz to 1.8 MHz offset (RBW = 30 kHz bandwidth)		-80		dBc

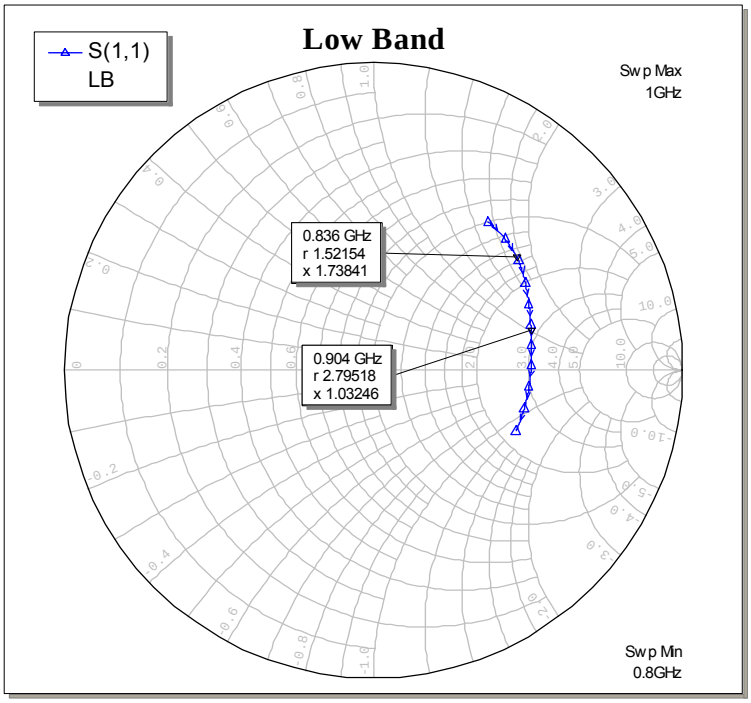
Table 7 AC Specifications of Transmitter[4]

[4] Please refer to MT6139 test procedure document.

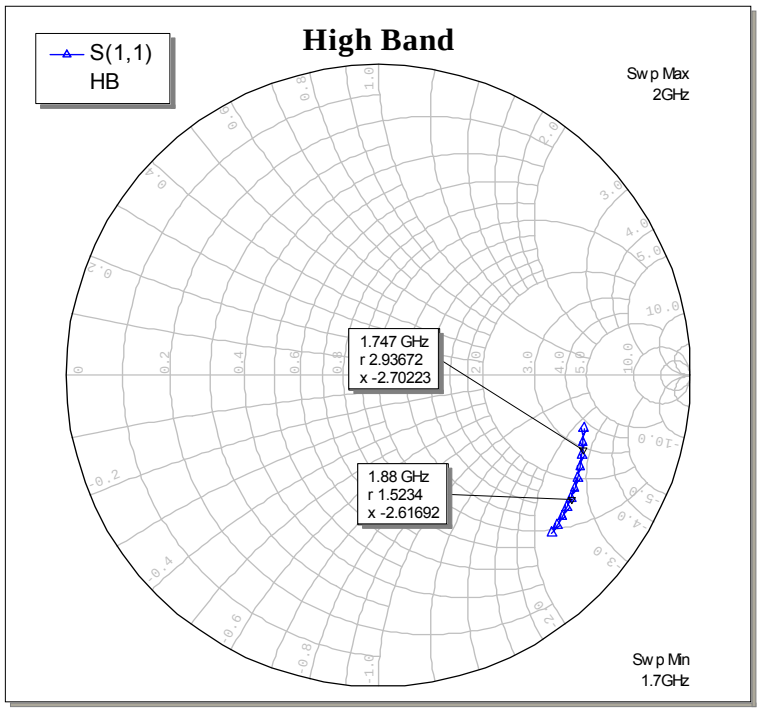
(T_A = 25 °C, V_{CC} = 2.8 V, I/Q common-mode voltage = 1.3 V, I/Q differential input signal = 0.45 V_{p-p} unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Tx noise in Rx band		GSM850	869 MHz to 894 MHz. 20 MHz up from Tx band		-158		dBc/Hz
		GSM900	935 MHz to 960 MHz. 20 MHz up from Tx band		-160		dBc/Hz
		DCS1800	1805 MHz to 1880 MHz. 20 MHz up from Tx band		-154		dBc/Hz
		PCS1900	1930 MHz to 1990 MHz. 20 MHz up from Tx band		-154		dBc/Hz
I/Q differential input swing		ALL		0.4	0.45	0.5	V_{p-p}
I/Q common-mode input voltage		ALL		1.25	1.3	1.35	V
Output power level	P_{out}	GSM850 GSM900	PA driver amplifier. R_{load} = 50 Ω	3	5	7	dBm
		DCS1800 PCS1900		1.5	4	6	dBm
Power level temperature coefficient		GSM850 GSM900	PA driver amplifier. R_{load} = 50 Ω		-4.4		dB/100°C
		DCS1800 PCS1900			-2.6		dB/100°C
Output harmonics		ALL	PA driver amplifier.			-30	dBc

Table 7 AC Specifications of Transmitter (Continued)



(a) GSM850 / GSM900 Bands



(b) DCS1800 / PCS1900 Bands

Figure 3 Transmitter Output S-Parameters (Single-ended)

7 Frequency Synthesizer Specifications

(T_A = 25 °C, V_{CC} = 2.8 V unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Frequency range	$F_{range,25}$	ALL	@ 25 °C	3100		4060	MHz
	$F_{range,-20}$		@ -20 °C	3110		4080	MHz
	$F_{range,65}$		@ 65 °C	3090		4040	MHz
Reference frequency	F_{ref}	ALL			26		MHz
Frequency step resolution	F_{res}	ALL			400		kHz
Phase detector sink versus source mismatch		ALL	V_{CPO} = VCCRFCP/2		4		%
Phase detector gain versus voltage		ALL	0.4 V < V_{CPO} < VCCRFCP – 0.4 V		10		%
Phase noise	PN_{10k}	ALL	@ 10 kHz offset		-80		dBc/Hz
	PN_{400k}		@ 400 kHz offset		-113		dBc/Hz
	PN_{3M}		@ 3 MHz offset		-138		dBc/Hz
Spurious performance		ALL	@ 200 kHz offset		-65		dBc
			@ 400 kHz offset		-75		dBc
			@ 600 kHz offset		-80		dBc
			@ 800 kHz offset		-85		dBc
			@ 1 MHz offset		-90		dBc
			@ ≧1.2 MHz offset		-95		dBc
Lock time	T_{lock}	ALL	Frequency error < ± 2 kHz		140		µs
PLL bandwidth	BW_{PLL}	ALL		35		65	kHz

Table 8 AC Specifications of Frequency Synthesizer[5]

[5] Please refer to MT6139 test procedure document.

8 VCXO Specifications

(T_A = 25 °C, V_{CC} = 2.8 V unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Supply current			VCCVCXO = 2.5 V		3.1		mA
Operating frequency					26		MHz
Output frequency			Baseband clock		26		MHz
Static range			VAFC = 1.4 V, CW0_AFC from 0 to 63 (Crystal C_{load} = 8.5 pF, tuning sensitivity = 27 ppm/pF)		± 22		ppm
Dynamic range			CW0_AFC = 32, VAFC from 0 to 2.8 V (Crystal C_{load} = 8.5 pF, tuning sensitivity = 27 ppm/pF)		± 23		ppm
Negative resistance					171		Ω
Buffer output level			26 MHz baseband clock (Load = 10 kΩ// 10 pF)	400	600		mV_{p-p}
Duty cycle			26 MHz baseband clock	45		55	%
Buffer output 2nd harmonic			Load = 20 pF		TBD		dBc
Buffer output 3rd harmonic			Load = 20 pF		TBD		dBc
Start-up time			Including regulator 3 power-on time by ENVCXO pull high			5	ms

Table 9 AC Specifications of VCXO[6]

[6] Please refer to MT6139 test procedure document.

9 Regulator Specifications

9.1 Regulator 1 (SDM) Specifications

(T_A = 25 °C, V_{CC} = 2.8 V, C_{out} = 1 µF unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Input voltage	V_{in}			2.7	2.8	2.9	V
Output voltage	V_{out}			1.9	2	2.1	V
Maximum output current	$I_{out,max}$				10		mA
Ground pin current	I_{gnd}				218		µA
Dropout voltage	V_{drop}		V_{in} - V_{out} when V_{out} = ($V_{out, nominal}$ - 100 mV), I_{out} = 10 mA			300	mV
Line regulation	V_{line}		V_{in} = 2.7 V to 2.9 V, I_{out} = 10 mA			10	mV
Load regulation	V_{load}		I_{out} = 1 mA to 10 mA			10	mV
Power supply ripple rejection	PSRR		f = 216.7 Hz, I_{out} = 10 mA	40	50		dB
Temperature coefficient			V_{in} = 2.8 V, I_{out} = 10 mA, TC = ΔV_{OUT} / [$V_{out, nominal}$*ΔT], ΔT = 65 - (-20) = 85 °C		80		ppm/°C
Output disable voltage			When circuit is disabled	2.6		2.9	V

Table 10 AC Specifications of Regulator 1 (SDM)

9.2 Regulator 2 (VCO) Specifications

(T_A = 25 °C, V_{CC} = 2.8 V, C_{out} = 4.7 µF, C_{bp} = 10 nF unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Input voltage (VCCREG2)	V_{in}			2.7	2.8	2.9	V
Output voltage	V_{out}			1.18	1.22	1.27	V
Maximum output current	$I_{out,max}$				30		mA
Ground pin current	I_{gnd}		I_{out} = 30 mA		325		µA
Dropout voltage	V_{drop}		V_{in} - V_{out} when V_{out} = ($V_{out, nominal}$ - 100 mV), I_{out} = 30 mA			900	mV
Line regulation	V_{line}		V_{in} = 2.7 V to 2.9 V, I_{out} = 30 mA			10	mV
Load regulation	V_{load}		I_{out} = 1 mA to 30 mA			10	mV
Output voltage noise			f = 10 Hz to 100 kHz		20	60	μV_{rms}
Power supply ripple rejection	PSRR		f = 216.7 Hz, I_{out} = 30 mA	50	60		dB
Temperature coefficient			V_{in} = 2.8 V, I_{out} = 30 mA, TC = ΔV_{OUT} / [$V_{out, nominal}$*ΔT], ΔT = 65 - (-20) = 85 °C		85		ppm/°C
Turn-on time	T_{on}		V_{out} step from 0 V to $V_{out\ nominal}$ ± 4 %		30	40	µs

Table 11 AC Specifications of Regulator 2 (VCO)

9.3 Regulator 3 (VCXO) Specifications

(T_A = 25 °C, V_{CC} = 2.8 V, C_{out} = 1 µF, C_{bp} = 0.1 µF unless otherwise stated)

Item	Symbol	Mode	Test Condition	Min	Typ	Max	Unit
Input voltage	V_{in}			2.7	2.8	2.9	V
Output voltage of	V_{out}			2.35	2.45	2.55	V
Maximum output current	$I_{out,max}$				5		mA
Ground pin current	I_{gnd}		I_{out} = 5 mA		325		µA
Dropout voltage	V_{drop}		V_{in} - V_{out} when V_{out} = ($V_{out,\ nominal}$ - 100 mV), I_{out} = 3 mA			100	mV
Line regulation	V_{line}		V_{in} = 2.7 V to 2.9 V, I_{out} = 5 mA			10	mV
Load regulation	V_{load}		I_{out} = 1 mA to 5 mA			10	mV
Output voltage noise			f = 10 Hz to 100 kHz		20	60	μV_{rms}
Power supply ripple rejection	PSRR		f = 216.7 Hz, I_{out} = 5 mA	50	60		dB
Temperature coefficient			V_{in} = 2.8 V, I_{out} = 5 mA, TC = ΔV_{OUT} / [$V_{out,nominal}$*ΔT], ΔT = 65 - (-20) = 85 °C		85		ppm/°C
Turn-on time	T_{on}		V_{out} step from 0 V to $V_{out\ nominal}$ ± 4 %		20	40	µs

Table 12 AC Specifications of Regulator 3 (VCXO)

10 Package Dimensions

Figure 4 illustrates the package details for MT6139. The package is 40-pin QFN and lead-free/RoHS compliant.

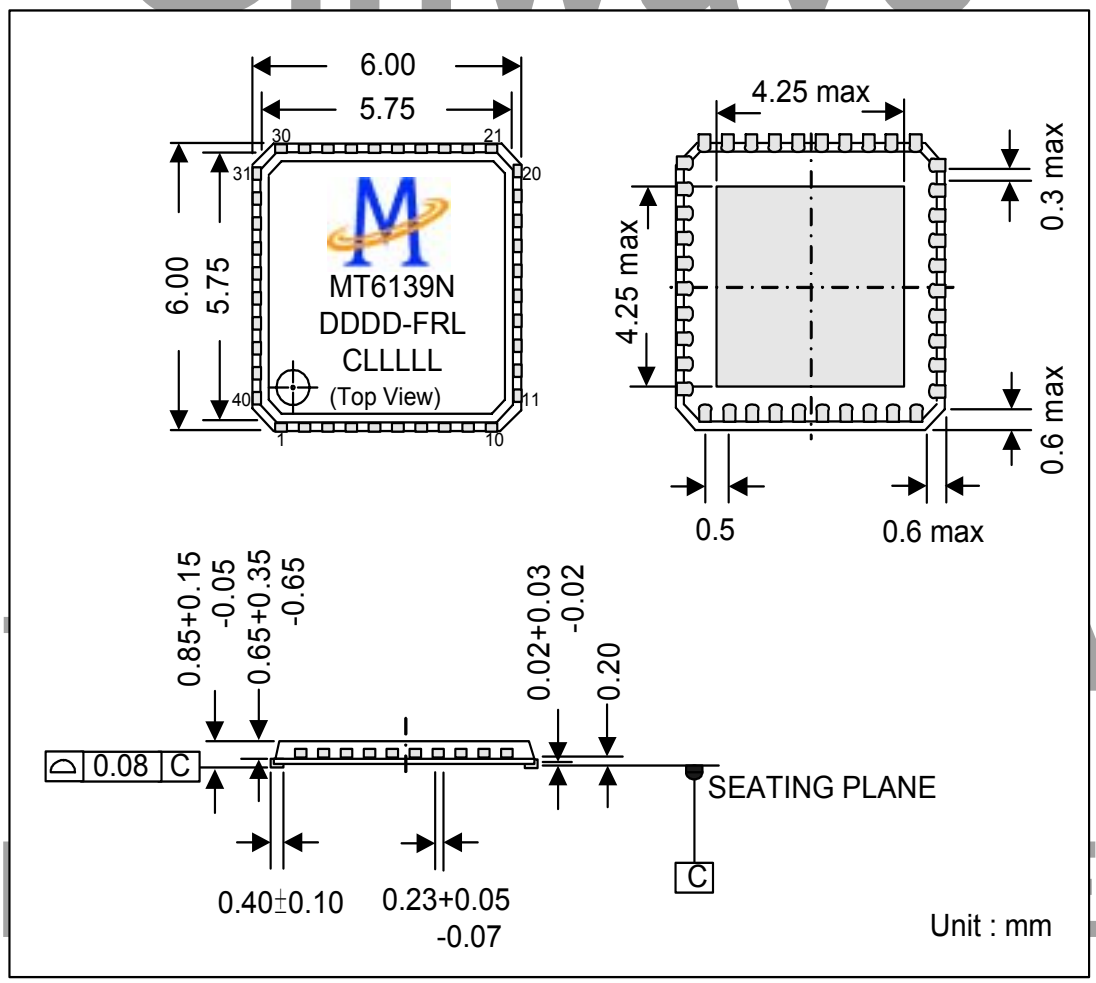


Figure 4 Package Dimensions

11 Application Circuit

Figure 5 shows the typical MT6139 GSM900 / DCS1800 / PCS1900 application circuit diagrams.

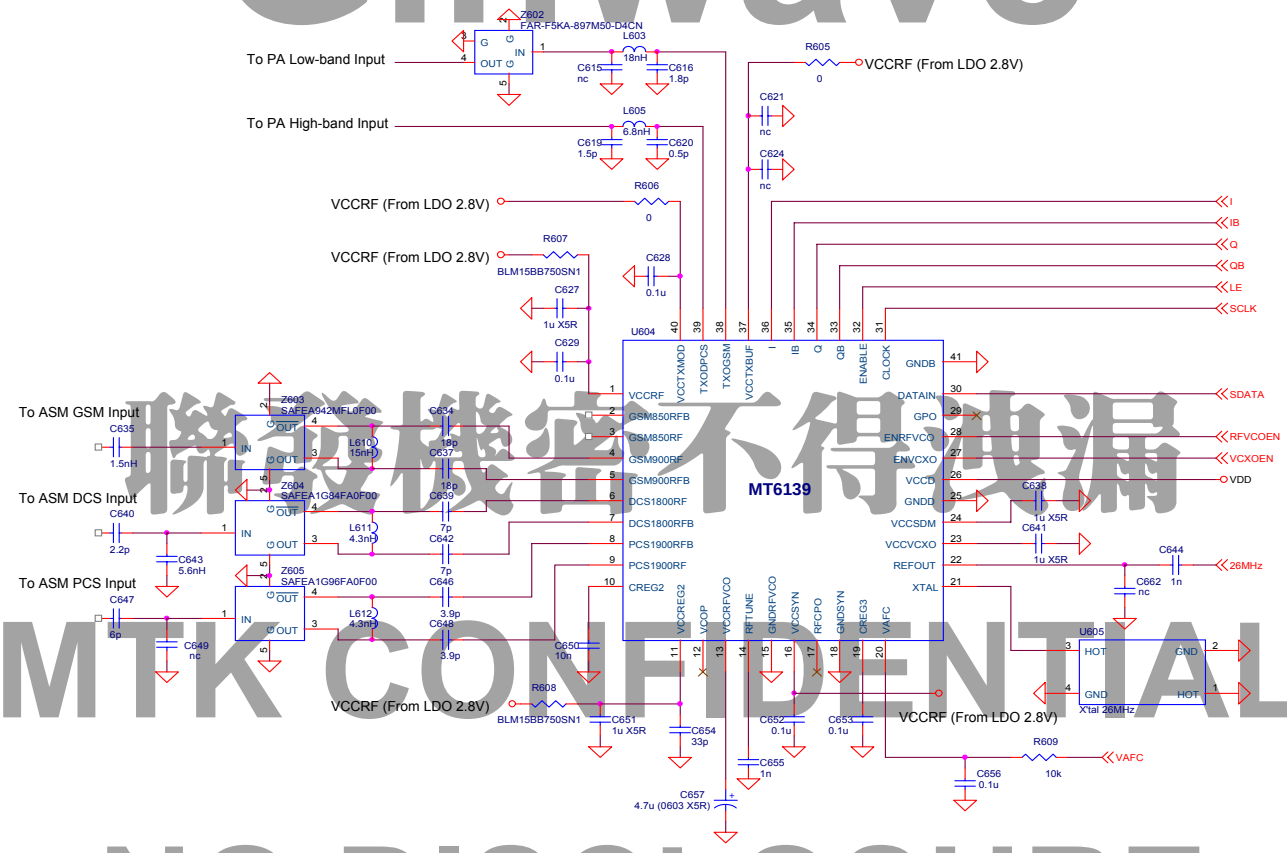


Figure 5 Typical GSM900 / DCS1800 / PCS1900 Application Circuit

Notes:

1. 10 nF C650 (pin 10, external noise bypass capacitor) is recommended.
2. 0.1 µF C652 (pin 16, external bypass capacitor) or value above is recommended.

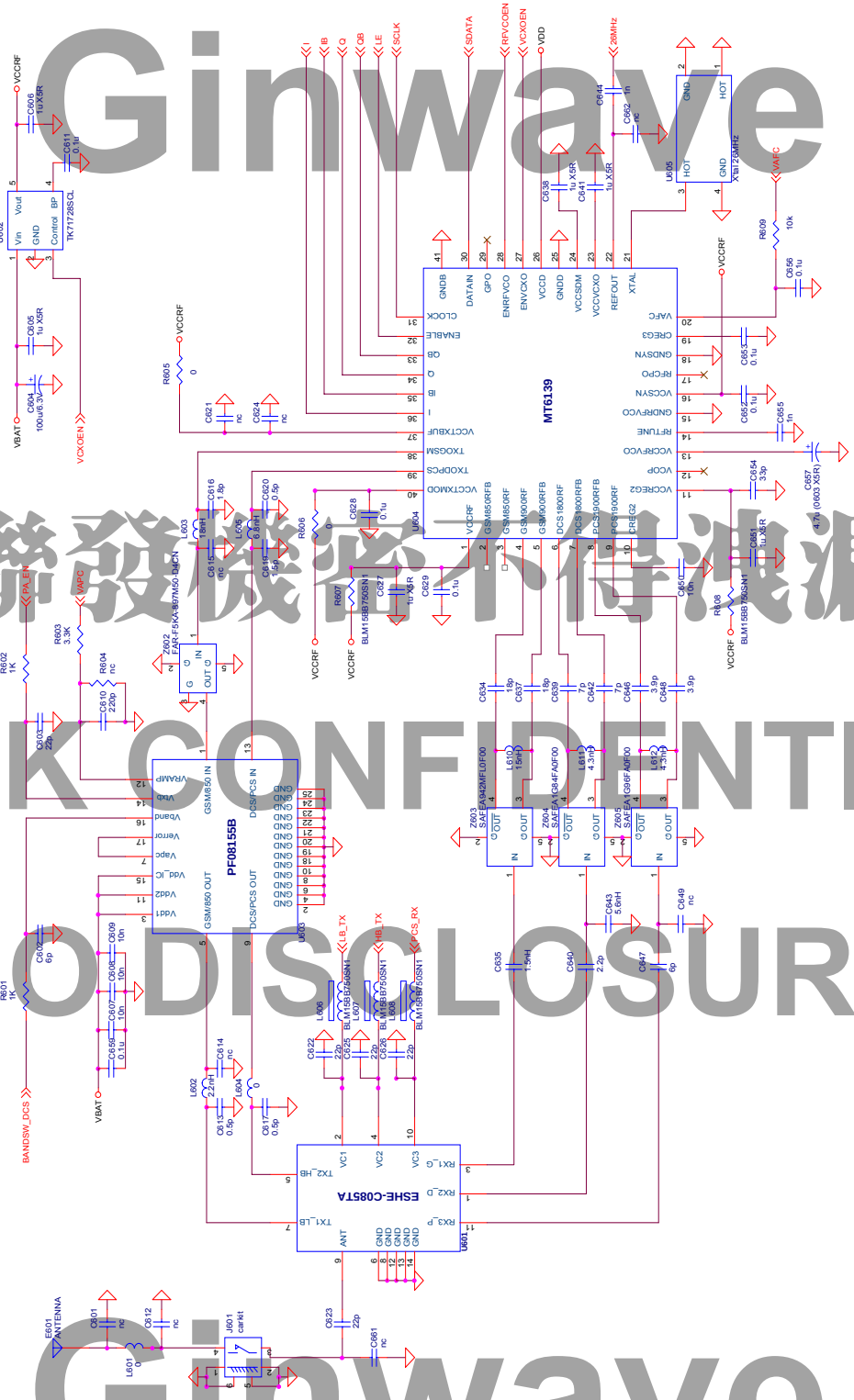


Figure 5 Typical GSM900 / DCS1800 / PCS1900 Application Circuit (Continued)

Bibliography References

1. MT6139 3-wire setting programming guide.
2. MT6139 test procedure.